LPDDR4 Memory Controller IP Core for Nexus Devices

IP Version: v2.6.3

Release Notes

FPGA-RN-02057-1.3

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Contents

1. Introduction

This document contains the Release Notes for the LPDDR4 Memory Controller IP and LPDDR4 Memory Controller Driver. For specific details about the IP and driver, refer to the following:

- LPDDR4 Memory Controller IP Core for Nexus Devices - User Guide (FPGA-IPUG-02127)
- CertusPro-NX LPDDR4 Memory Controller Driver User Guide (FPGA-TN-02378)

LPDDR4 Memory Controller IP v2.6.3

Software	Software Version	Summary of Changes
Lattice Radiant	2025.2	• Fixed a corner-case arbitration issue related to self-refresh when dual rank is enabled. • Fixed a corner-case issue affecting read operations. • Configured the internal PLL clock to 50 MHz instead of sourcing it from the APB clock. • Reduced simulation time. Added an option to enable simulation with DATA MASK toggling, which may increase simulation time from a maximum of 10 minutes to up to 1 hour and 30 minutes.

LPDDR4 Memory Controller IP v2.6.2

Software	Software Version	Summary of Changes

Lattice Radiant	2025.1.1	• Updated the following default settings in the GUI to align with the Radiant software timing model fix. These settings are automatically adjusted based on the Radiant version:
		  • Trained Write Latency: 7 or 4
		  • Trained Read Latency: [12, 11] or [9, 8] — automatically adjusted based on the DDR command frequency.
		• Improved centering of CA to CK rising edge in CBT.
		• Improved automatic CK adjustment in Write Leveling.
		• Fixed possible data glitch in dual rank when the data access is too near to the other rank's refresh command.
		• Fixed an incorrect arbitration issue with dual rank and power down enabled.
		• Updated the SIM_FLOAT_PRECISION parameter for the internal PLL to 0.625.
		• Added automated pin assignment based on selected example design board.

LPDDR4 Memory Controller IP v2.6.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1	• Updated the I/O settings based on electrical compliance test • Added 128 and 256 options to the MAX_BURST_LEN parameter when AXI_DATA_WIDTH is 128, 64 or 32 bits. • Improved internal timing path for better timing closure. • Updated the example design to support both 128 and 256 burst lengths. • Added cacheable tag to enable caching of the memory address range in Propel.

LPDDR4 Memory Controller IP v2.5.0

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2.1	• Enhanced the random deassertion of data strobes to cover any condition, rather than on the first and last beat only. • Updated driver

LPDDR4 Memory Controller IP v2.4.0

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2	• Removed support for Dual Rank 533 MHz. • Removed support for 64-bit DDR width. • Fixed ECO Editor error caused by invalid IP parameter format. • Added 1000 iteration test in the Example Design.

LPDDR4 Memory Controller IP Earlier Versions

IP Version	Summary of Changes
2.3.1	• Updated driver to add NOP delay when polling for training done. • Disable dual rank option for 533 MHz.
2.3.0	Added driver support.
2.2.0	• Reduce AXI4 Read Latency. • Added Dual Rank support. Added ODT programming support. • Added Automatic Vref Training support. • Fix write-read ordering issue when write queue is full. • Added support for LFCPNX-100AUTODIE device.
2.1.0	• Added support for random AXI4 strobe. • Added support for AXI4 data width less than DDR data width * 8. • Only Synplify Pro is supported for this version. The IP fails on the board using LSE.
2.0.2	• Supported random AXI4 burst length from 1 to 64 beats. • Supported any combination of burst length and burst size.
2.0.1	• Fixed Single access issues. • Added Enable APB I/F option in the GUI. • Enabled the No. of Outstanding Refresh Option and set the default value to 8. • Only Synplify Pro is supported for this version. The IP fails on the board using LSE.
2.0.0	• Replace AHB-Lite and Native I/F with AXI4. • Improve performance up to >80% DDR bus efficiency. • Implemented Partial encryption to enable constraint propagation. • Added 300 MHz and 350 MHz support. • Validated all supported DDR clock frequencies on the board. • Only Synplify Pro is supported for this version. The IP fails on the board using LSE.
1.3.0	• Added Vref training support for CA Vref, Controller's DQ Vref, and Memory DQ Vref. • Improved Read performance for Native I/F. • Added testbench for running simulation. • Removed DDR3 support for this Memory Controller IP. • Updated GUI options: ECC is fixed to Disabled, Internal RISC-V CPU is fixed to Enabled.
1.2.1	• Added limitation for DDR3. • The DDR Interface Type GUI option has been fixed to LPDDR4.

IP Version	Summary of Changes
1.2.0	• Updated for Radiant 3.1. • Updated eval files to add the design for testing the IP on the board. • Updated training logic to work on the board. • Added Native I/F local data bus.
1.1.0	• Updated for Radiant 3.0. • Added support for Micron WDQS Control Mode 2.
1.0.0	Initial release.

References

- LPDDR4 Memory Controller IP Core for Nexus Devices - User Guide (FPGA-IPUG-02127)
- CertusPro-NX LPDDR4 Memory Controller Driver User Guide (FPGA-TN-02378)
- Lattice Nexus Platform web page
- CertusPro-NX web page
- Certus-NX web page
- CrossLink-NX web page
- IP Core for Nexus devices
- Lattice Propel Builder software
- Lattice Radiant FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

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