ispLEVER Release Notes

Version 2.01

Service Pack 6

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Table of Contents

ispLEVER 2.01 Service Pack 6

Enhancements

The ispLEVER™ 2.01 Service Pack 6 includes the following enhancements for PC and UNIX operating systems:

Performance Analyst Enhancement

This enhancement affects all CPLD devices.

The default fMAX Clock Enable setting in the Performance Analyst fMax Options dialog box is changed to ON. This setting may be changed for each project.

To turn off this setting, double-click the **Timing Analysis** process in the Project Navigator to open the Performance Analyst. Under Analysis, make sure that **fMAX** is selected, and then click **Options** to open the dialog box. Under fMAX for, clear the **Clock Enable** check box.

Constraint Editor Enhancements

The following enhancements have been added to the Constraint Editor:

Input Register Enhancement

This enhancement affects the ispMACH4000 device families.

The Input Register default value in the Constraint Editor's Default Settings dialog box is changed to NONE to improve implementation. Logic functions that are placed and routed as inreg functions can only be placed on macrocells that go out to an I/O pin. With the NONE setting, logic functions that are placed and routed as non-inreg functions can be placed on any macrocell.

Dual Function Macrocell Support

This enhancement affects the following devices: MACH 5000VG, ispXPLD 5000MX, and ispLSI 5000VE.

A new pin attribute, Dual_Function_Macrocell, has been added to the Constraint Editor. Its dual function allows the placement of two logic functions on the same macrocell, which means you can pack more functions into the device.

You can turn the dual function on or off by using the Global Constraints tab in the Constraint Editor. You can override the global setting by using the Pin Attributes tab of the Constraint Editor. You can then turn the attribute on or off for each signal.

Global Constraints

All the global constraints supported for CPLD and ispXPGA devices in this release are listed in the following Table 1 and Table 2.

Table 1. Global Constraints for CPLD Devices

Constraint Name	Value Description
Security	Defaults to Off. On - Programs the security bit of the device. Off - Disables this constraint.
Toe_as_io (ispLSI1000/2000/5000B/ 5000VE only)	Defaults to Off. On - Configures the TOE pin as Test Output Enable or IO. Off - Disables this constraint.
Usercode	Enter Hex, Bin, or ASCII values to program the Usercode bits.
Usercode_format	Hex, Bin, ASCII, Checksum - Sets the format of the Usercode. (Note: To an ispGDX device, there is no checksum.)
Setcomb (ispGDX only)	Defaults to Off. On - Controls the registers/latches in bidirectional paths to globally function as input registers/latches. Off - Disables this constraint.
Isp (ispLSI1000/2000 only)	Defaults to On. On - Prevents the use of all ISP pins. Off - Disables this constraint.

Table 1. Global Constraints for CPLD Devices (Continued)

Constraint Name	Value Description
Isp_except_y2 (ispLSI1000/2000 only)	Defaults to Off. On - Prevents the use of all ISP pins except the Y2 pin. Off - Disables this constraint.
Y1_as_reset (ispLSI1000/2000 only)	Defaults to On. On - Uses Y1/RESET as Y1 or RESET. Off - Disables this constraint.
Pullup (ispLSI1000/2000/8000 only)	Defaults to Up. Up - Specifies pull up feature. Off - Disables this constraint.
Slewrate (ispLSI1000EA/2000/8000 only)	Defaults to Fast. Fast, Slow - Specifies slew rate feature.
Isplsi_strategy (ispLSI1000/2000/8000 only)	Defaults to Delay. Area - When applied, the Fit Design process can use the device resources to the best. Delay - When applied, the Fit Design process can bring up the best timing delay result.
Isplsi_max_glb_inputs (ispLSI1000/2000/8000 only)	Specifies maximum GLB input range. ispLSI1000/2000: 2-18 (defaults to 16) ispLSI8000: 2-44 (defaults to 42)
Isplsi_max_glb_outputs (ispLSI1000/2000/8000 only)	Specifies maximum GLB output range. ispLSI1000/2000: 1-4 (defaults to 4) ispLSI8000: 1-20 (defaults to 20)
Isplsi_carry_pin_direction (ispLSI1000/2000/8000 only)	Defaults to Off. On - Specifies Carry Pin direction. Off - Disables this constraint.

Table 1. Global Constraints for CPLD Devices (Continued)

Constraint Name	Value Description
Isplsi_ignore_fixed_pin (ispLSI1000/2000/8000 only)	Defaults to Off. On - Ignores reserved pins. Off - Disables this constraint.
Fitter_effort_level (ispLSI1000/2000/8000 only)	Defaults to Medium. Low, Medium, High - Specifies the Fitter effort level.
Isplsi_case_sensitive (ispLSI1000/2000 only)	Defaults to Off. On - Enables case sensitive in the Fit Design process. Off - Disables this constraint in the Fit Design process.
Isplsi_use_global_reset (ispLSI1000/2000/8000 only)	ispLSI1000/2000: defaults to On ispLSI8000: always Off On - Uses Global Reset. Off - Disables this constraint.
Isplsi_min_glb_levels (ispLSI1000/2000/8000 only)	ispLSI1000/2000: defaults to Low ispLSI8000: defaults to High Low, High - Minimizes GLB levels for all paths.
Isplsi_clock_enable (ispLSI8000 only)	Defaults to On. On - Specifies Clock_enable. Off - Disables this constraint.
Zero_hold_time (ispMACH4A3/4A5, MACH4, MACH4 Low Voltage only)	Defaults to On. On - Sets the Zero Hold Time fuse for input registers. Off - Disables this constraint.
Svf_erase_program_verify	Defaults to Off. On - Specifies erase, program, and verify operations for the SVF file. Off - Disables this constraint.

Table 1. Global Constraints for CPLD Devices (Continued)

Constraint Name	Value Description
Svf_erase_program_verify_secure	Defaults to Off. On - Specifies erase, program, verify, and secure operations for the SVF file. Off - Disables this constraint.
Svf_verify_only	Defaults to Off. On - Specifies verify-only operation for the SVF file. Off - Disables this constraint.
Balanced_partitioning (ispLSI1000/2000/5000/8000, ispMACH4000, MACH4, MACH5 only)	Default varies from different device families. Yes - Specifies balanced partitioning in the partition score calculation. No - Disables this constraint.
Dual_function_macrocell (ispLSI5000 only)	Defaults to On. On - Allows the placement of two logic functions on the same macrocell. Off - Disables the constraint.
IspLSI_timing_analysis (ispLSI1000/2000/8000 only)	Defaults to On. On - When applied, the timing report file can be generated automatically. Off - When applied, no timing report file will be generated. If you need a timing report file, run the Timing Analysis process from the Project Navigator.

Table 1. Global Constraints for CPLD Devices (Continued)

Constraint Name	Value Description
Logic_optimization_effort (ispLSI1000/2000/5000/8000, ispMACH4000 only)	The limit for collapsing if equations exceed the specific level of complexity based on the number of inputs and P-Terms in each equation. Greater equation complexity lowers the probability that equations will collapse within the specified P-Term/Input limit and requires more computation time. A greater logic optimization effort lets the optimizer try more complex equations for collapsing. The effort might or might not be successful. In most cases, an increase in the logic effort level leads to an increase in run time. Used by the Optimizer. Defaults to 2. The value range for ispLSI1000/2000/8000 is 1 to 4. The value range for ispLSI5000 is 1 to 7.
Max_area (ispLSI5000, ispMACH4000 only)	The maximum number of macrocells used by the Optimizer to limit equation collapsing. Collapsing tends to minimize the number of equations, but it may cause higher macrocell/P-Term utilization. Normally, the Max_Area should not exceed the maximum number of macrocells in a device. However, during the optimization process, the number of P-Terms in the middle of the optimization can exceed the device limit temporarily but finally come within the device resource limit. That is why sometimes assigning Max_Area over the device limit might produce the better optimization result. Increasing this option over the device limit creates the risk of fitter failure due to the lack of resources. Default varies for different device families. The value range varies for different device families.

Table 1. Global Constraints for CPLD Devices (Continued)

Constraint Name	Value Description
Max_fanin_limit (ispLSI1000/2000/5000/8000, ispMACH4000 only)	The maximum number of inputs for each equation. Max_fanin_limit controls the number of inputs in an equation during collapsing. Usually this number should not exceed the device limit in order to guarantee the fitting capability. If a Max_fanin is assigned that exceeds the device limit, the equations might not fit. A Max_fanin that goes beyond the device input limit is not recommended. A Max_fanin increase allows more collapsing. The Max_fanin option controls collapsing in the Area and Speed mode. The Max_fanin_limit controls collapsing for the critical FF-to-FF paths in the Fmax mode. Used by the Optimizer. Default varies for different device families. The value range varies for different device families.
Max_glb_input_percent (ispLSI1000/2000/5000/8000, ispMACH4000 only)	The maximum number of GLB inputs that the fitter uses to fit equations in a block. A Max_glb input increase allows fitting more equations in a block but may cause the Router to fail. Max_GLB_Input_Percent parameter is global for all GLBs. Used by the Partitioner. Defaults to 100. The value range is 94 to 100.

Table 1. Global Constraints for CPLD Devices (Continued)

Constraint Name	Value Description
Max_PTerm_limit (ispLSI1000/2000/5000/8000, ispMACH4000 only)	The maximum number of P-Terms for each equation. Max_PTerm_limit controls the number of P-Terms in an equation during collapsing. A Max_PTerm increase allows more collapsing. Usually this number does not exceed the device limit. However, if the assigned Max_PTerm exceeds the device limit, the collapsed equations might finally be within the device limit. That is why sometimes assigning a Max_PTerm that exceeds the device limit might produce a better optimization result. A Max_PTerm increase will never create equations that exceed Max_PTerm_Split. That is why Max_PTerm_Split should never be more than the device limit. The Max_PTerm_collapse option controls collapsing in the Area and Speed mode. Max_Pterm_limit controls collapsing for the critical FF-to-FF paths in the Fmax mode. ispMACH4000: the value range is 60 to 80 (defaults to 80) ispMACH5000VG: the value range is 40 to 160 (defaults to 160) ispXPLD: the value range is 40 to 160 (defaults to 160) Other device families: the value range is 20 to 35 (the default varies for different device families)
Opendrain (ispLSI2000E/2000VE/2000VL only)	Default to Off. On - Controls the external output or bidirectional pins use the opendrain feature. Off - Disables the opendrain feature.
Speed (ispLSI1000/2000/5000/8000, MACH4, MACH5 only)	Defaults to Yes. Fmax - Sets target logic optimization between registers. Yes - Speed

Table 2. Global Constraints for ispXPGA

Constraint Name	Value Description
Design_type	Defaults to Normal. Normal, Firm_macro, Ip - Specifies the design type.
Lpm_hint_default	Defaults to Speed. Speed - When applied, the LPM will be optimized for speed. Area - When applied, the LPM will be optimized for area.
Fmax_ce	Defaults to On. On - Specifies the clock-enable path is included in the Fmax calculation when timing calculation is being performed (during timing-driven place and route and timing analysis processes). Off - Disables this feature.
Packing_density	Defaults to Low. Low, Medium, High - Specifies the packing density in the PFU.
Packing_effort	Defaults to High. Low, Medium, High - Specifies the packing effort.
Pio_pff_merge	Defaults to None. None - When applied, the Packer packs all DFF's into PIOs. All - When applied, the Packer tries to pack DFF's into I/O cells.
Packing_datapath	Defaults to 0. 0 - Disables the datapath algorithm. 1 - Enables the datapath algorithm, which could improve Fmax.

Table 2. Global Constraints for ispXPGA (Continued)

Constraint Name	Value Description
Packing_algorithm	Defaults to 1. 0 - Disables alternate packing algorithm. 1 - Enables alternate packing algorithm, which can improve Fmax.
Placement_effort	Defaults to Low. Low, Medium, High - Specifies the placement effort.
Placement_spread	Defaults to On. Off - PFUs will be placed close together. On - The software will spread PFU placement to relieve routing congestion.
Buffer_insertion_fanout_limit	Defaults to 8. The value range is 1 to 9999. A buffer is added when the fanout exceeds the number you set. This may help to improve design performance. Normally, this constraint is used in conjunction with Tdp_effort setting to Low, Medium or High.
Tdp_effort	Defaults to High. None, Low, Medium, High - Specifies the timing-driven placement effort, which may improve design performance.
Routing_effort	Defaults to High. Low, High - Specifies the routing effort. If you run into unrouted nets, change this to High.
Routing_option	0, 1, 4 - This allows the use of a different algortihm for Routing the design. Option available from 0, 1, 4.
Tdr_effort	Defaults to High. None, Low, Medium, High - Specifies the timing-driven routing effort. If you run into unrouted nets, change this to None.

Table 2. Global Constraints for ispXPGA (Continued)

Constraint Name	Value Description
Maxdb	Defaults to 8. The value range is 1 to 16. Specifies the number of double routing nets per node. This may improve design performance. The higher the number, the better routability you may achieve, but at the expense of timing. The normal usage range for this constraint is 4 to 15.
Fmax_ram	Defaults to Off. Off - Turns OFF the RAM signal delay paths to be included in the FMAX calculation. On - Turns ON the RAM signal delay paths to be included in the FMAX calculation.
Max_number_clocks	Defaults to 6. The value range is 1 to 8. Tells the placer software the number of global clocks to use for the design.
Design_Optimization	Defaults to 3. The value range is 0 to 4. Sets the different optimization algorithms to be used for the Placer software.
Placement_Algorithm	Defaults to 0. The value range is 0 to 3. Enables different placement algorithms. A setting of 0 provides the best Fmax result for most designs; for some designs, algorithm 1 yields better results.

ispGDX2 Device Enhancements

These enhancements affect all ispGDX2 devices.

Automatic Pin Locking Support

This software release can do automatic pin locking for designs containing LVDS macros.

Bit Assignment in Bus

This software release allows you to do bit assignment in bus using the tabular pin assignment window.

Output Switch Matrix (OSM) Bypass Assignment Enhancement

This enhancement affects the ispMACH4000 device families.

The OSM BYPASS attribute instructs the fitter to take the output of a macrocell directly out to its corresponding bonded I/O. Using the OSM BYPASS attribute eliminates the use of the OSM and causes less delay. Before this enhancement, the OSM BYPASS attribute was available only from the Pin Attributes pop-up menu in the Constraint Editor. The enhancement makes it available within the ABEL, VHDL and Verilog source as well.

The following examples show the use of the OSM BYPASS attribute for ABEL, VHDL, Verilog (Exemplar), and Verilog (Synplicity).

ABEL Source Constraint Example

```
SYNTAX

LAT_OSM_BYPASS ([TYPE],[PinList]);
Type: OSM type. This can be either BYPASS or NONE.
PinList: Pin names separated by colons, i.e., pin1:pin2:pin3...

EXAMPLE

MODULE osm

library ‘lattice’;

inA,inB   pin;

osm0 pin istype ‘com’;

//--- Constraining OSM BYPASS in ABEL ---

LAT_OSM_BYPASS (BYPASS, osm0);
```

```
equations

osm0 = !inA & inB;

END
```

VHDL Source Constraint Example

```
SYNTAX

ATTRIBUTE OSM: STRING;
--  ATTRIBUTE OSM OF [SigName]: SIGNAL IS "TYPE";
TYPE can be either BYPASS or NONE.

EXAMPLE

LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY osmbypass IS
PORT (      inA :in STD_LOGIC;
            inB :in STD_LOGIC;
      osmbypassO:out STD_LOGIC);

---------- OSM Bypass Assignments ----------

ATTRIBUTE OSM : string;
ATTRIBUTE OSM OF osmbypassO: SIGNAL IS "BYPASS";

END osmbypass;

ARCHITECTURE rtl OF osmbypass IS

BEGIN

osmbypassO <= inA OR inB;

END rtl;
```

Verilog Source Constraint Example for Exemplar

```
SYNTAX

//exemplar attribute [NodeName] OSM [TYPE]
/* TYPE can be either BYPASS or NONE. If not specified, do not
bypasss. */

module osmbypassvlog(inA,inB,osmbypassO);

//declarations
input inA,inB;

//---------- Constraining OSM -------------------

output osmbypassO; //exemplar attribute osmbypassO OSM BYPASS

//equations

assign osmbypassO = !inA & inB;

endmodule
```

Verilog Source Constraint Example for Synplicity

```
SYNTAX

// output [PinName] /* synthesis OSM="TYPE" */;
// TYPE can be either BYPASS or NONE. If not specified, then do not
bypass.

module osmbypassvlog(inA,inB,osmbypassO);

//declarations
input inA,inB;

//---------- Constraining OEM -------------------

output osmbypassO /* synthesis OSM="BYPASS" */;

//equations
assign osmbypassO = !inA & inB;

endmodule
```

Clock Enable Control Enhancement for MACH 4000 Devices

This enhancement affects the ispMACH 4000 device families.

In the MACH 4000 architecture, the clock enable of each macrocell can come from several sources: PT initialization/CE, PT initialization/CE inverted, shared PT clock, and Logic high. When the clock enable control is turned on, the synthesis tool can choose the best solution for the clock enable.

You can turn the clock enable control on or off during synthesis by using the Properties dialog box.

To change the setting, select the Verilog or VHDL source file in the Sources Window of Project Navigator. In the Processes window, right-click the **Synthesize** process to open the Properties dialog box. Double click **Utilize Clock Enable** to select Yes or No. The default is No, which provides better fitting results.

ispVM System Enhancements

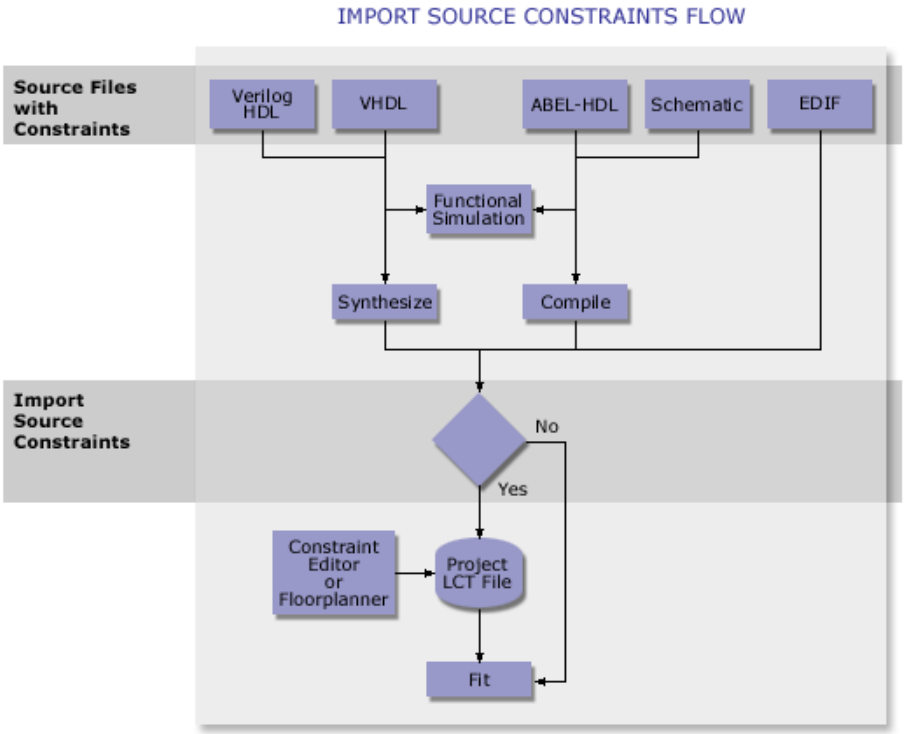
The following devices are supported:

- ispMACH 5128B
- ispMACH 5384B
- ispMACH 4000V-XXXXE (Automotive Temperature)

Import Source Constraints Explanation

If you import constraints from source files into your project, these constraints are written into your Lattice Constraint File (`<project>.lct`). The source file constraints will overwrite any similar constraints you may have set in the Constraint Editor or Floorplanner.

For example, if you set pin assignment constraints in your source code file, and you import the source constraints into your project, then all pin assignments currently set in the LCT file are removed and replaced with the source constraints. Even if only one pin assignment was defined in the source file, all pin assignments will be deleted and replaced with the new constraints. Other constraints in the project LCT file, such as SLEW, Pull, etc., are not changed unless you have these constraints in the source file. Note that if you do not have any source constraints, the constraints in the Project LCT file will not be changed.



This constraint flow allows you to modify constraints without having to resynthesize or recompile your source file. By definition, all tools such as the fitter, optimizer, Constraint Editor, and Floorplanner, read/write constraints to the Project LCT file only.

If you import constraints using the Import Source Constraints Option dialog box set to Always Import Source Constraints and decide to change them using the Constraint Editor or Floorplanner, remember to go back to the dialog box and select **Do Not Import Source Constraints**. Otherwise, any changes you make will be overwritten with the constraints in the source files the next time you fit the design.

Also, if you use the Always Import Source Constraints setting and refit the design, only the compiler will be run. In this case ispLEVER is still reading the edited constraint file and does not go back and import the source code constraints. Therefore, in this case, if you want ispLEVER to read the source constraints, always force the design to run from Synthesis (Generate Database process).

Known Issues and Solutions - ispXPGA

The following known ispXPGA issues have been identified and their solutions are determined.

Issue:	When opening the Constraint Editor targeting an ispXPGA device, you will receive a an error message such as "can't open.vci file" unless you have the appropriate permission to the design files
Workaround:	Make sure that you have Read/Write permission to the design files and directory.
Devices Affected:	ispXPGA

Issue:	The Group function in the Constraint Editor does not support PIO (IOB) instances.
Workaround:	None. Only internal cells for PFUs are supported.
Devices Affected:	ispXPGA

Place and Route Issues

Issue:	Some designs do not route with the default Place & Route settings in Project Navigator.
Workaround:	Change TDR_effort from Low to None in the Global Constraint sheet of the Constraint Editor; *or* Use ispEXPLORER to set a variety of properties in multiple runs through the software to get the design to route successfully.
Devices Affected:	ispXPGA

Issue:	The following message is generated by the Pack & Place Design process: `<Error> 54013 PFU blocks insufficient` The possible cause of this error is insufficient device resources due to the optimization and Place & Pack properties used by the software.
Workaround:	Use ispEXPLORER to set a variety of properties in multiple runs through the software to get the design to pack and place successfully.
Devices Affected:	ispXPGA

Issue:	The report file does not reflect the setting for Timing-Driven Placement Effort level (also referred to as TDP_effort).
Workaround:	Refer to the `Automake.log` file, which will contain the proper setting for Timing-Driven Placer Effort level.
Devices Affected:	ispXPGA

Issue:	Reserved pins specified in Constraint Editor are not specified in the following reports: a. Pack/Place Report's Device_Pinout Listing section (enable with Verbose mode under Pack/Place Design Properties dialog box) b. Post-Place Pinouts c. Post-Place or Post-Route Floorplan Design
Workaround:	a. Note that the placer did reserve the pins, which means that the placer will not assign any design pins to the reserved pins. The number of Reserved Pins is indicated in the Design Summary section of the Pack/Place Report file. b. ***PC Only*** – For Exemplar Synthesis, you can specify floating pins in the design source, and these pins will not be removed. Placer will assign these floating pins (treated as reserved pins).
Devices Affected:	ispXPGA

Issue:	Place and Route do not support sysIO Type on the GSR (Reset Signal) pin.
Workaround:	None
Devices Affected:	ispXPGA

Issue:	***UNIX only*** – When running the ispXPGA Route Design process, you might see the following warning: `<Warning> W64001: while exporting data to Hood database`
Workaround:	Ignore this warning message. The design files created are correct.
Devices Affected:	ispXPGA

Issue:	***UNIX only –*** When using LPM_MULT Area mode in the VHDL source, you might encounter Pack & Place Design process failure.
Workaround:	In the LPM_Mult dialog box of the Module/IP Manager, select Speed mode to generate a fast multiplier. If an area efficient multiplier is required, contact Lattice Technical Support.
Devices Affected:	ispXPGA

Floorplanner Issues

Issue: Floorplanner prevents you from accidentally moving and saving individual PFU packing/placement constraints in an IP, LPM or macro. However, Floorplanner does not have such safeguard control over carry-chain cells and PFUs connected to carry-chains. When you save such PFUs individually, an error can result in Place and Route.

Therefore, it is recommended that you do not choose **File > Save Constraint** to move and save the PFU packing/placement for the following PFUs:

a. Carry-chains cells (`CCU_*`), which must be placed vertically
b. PFUs connected to Carry-chains
c. PFUs used in LPMs, macros, or IPs

Workaround: None.

Devices Affected: ispXPGA

Issue: Moving EBR (Embedded Block RAM) cells is not supported.

Workaround: None

Devices Affected: ispXPGA

Timing Analysis Issues

Issue: In the Performance Analyst Expanded Path window, if the signal name is very long, the Destination signal label at the top of the window might not display properly.

Workaround: None

Devices Affected: ispXPGA

CAE Synthesis Issues

Issue: RAM primitive instantiation in VHDL / Verilog source is not supported. You must use LPM for RAM applications.

Workaround: Refer to the online Help topic *Design Entry > Macro and IP Design > Macro Design Flow.*

Devices Affected: ispXPGA

Issue: ***PC only*** – Spectrum and Synplify synthesis tools use different signal labels for Verilog bus signal names. Synplify uses square brackets, whereas Spectrum uses parentheses.

For example:

```
Bus pin
Verilog source: count[3:0];
Synplify edif:     count[3], count[2], count[1], count[0]
Spectrum edif: count(3), count(2), count(1), count(0)
```

If you make pin assignments or backannotate pins, and then change the synthesis tool from Spectrum to Synplify (or vice versa), you will encounter the following error:

```
<Error> F51054: Pin c(0) specified in [LOCATION
ASSIGNMENTS] of lci file not found in the design
```

.

Workaround: Stay with one synthesis tool if you have pin assignments.

Devices Affected: ispXPGA

Issue:	***PC only –*** When you Exemplar synthesis, floating pins in the design are kept and will be assigned by the ispXPGA placer. Warning messages are specified in the `Automake.log` file. Note that Synplify Synthesis removes floating pins.
Workaround:	None
Devices Affected:	ispXPGA

Issue:	***PC only*** – Synplify synthesis does not support 1-bit wide array (for example, input [0:0] EDI). The array will be written out as a scalar signal (EDI), which might cause a connect error if LPM is used. Below is an example of an error message: `ERROR: Unable to find pin 'EDI(0)' (renamed as 'EDI_0') on instance 'U0' in join section near line 349`
Workaround:	Use Exemplar synthesis, or change the 1-bit array to an individual signal.
Devices Affected:	ispXPGA

Issue:	***PC only –*** VHDL/Verilog designs may not achieve good performance (Fmax, etc.) when the Exemplar synthesis tool is automatically invoked as part of the process flow within the Project Navigator.
Workaround:	Compile your designs in the Exemplar design environment, and then import your EDIF file into the Project Navigator. You can access the Exemplar design environment from the Project Navigator by choosing choose **Tools > LeonardoSpectrum Synthesis**.
Devices Affected:	ispXPGA

Issue: ***PC only –*** When you use PLL macros (SPLL, STDPLL and STDPLLX) with Exemplar synthesis, you get the following warning message:

```
"C:/isptools/ispcpld/examples/ispxpga/Constraints/PL
L/Verilog/VlogExem/StandardPLL/std_pll.v",line 17:
Warning, module STDPLL is empty.
```

Workaround: Ignore this warning message. The PLL macro is instantiated as a black-box. The EDIF netlist created is correct.

Devices Affected: ispXPGA

Issue: Included in the ispLEVER 2.0 are the Verilog and VHDL simulation libraries for ispXPGA. For standalone CAE Simulators, you must compile these libraries before doing timing simulation for ispXPGA. The following ispXPGA libraries are included:

Verilog library directory

```
\installed_dir\kits\ispxpga\verilog\
```

Verilog library file:
`lava1.v`

VHDL library directory

```
\installed_dir\kits\ispxpga\vhdl\
```

VHDL library files:
`lava1_components.vhd`
`lava1.vhd`

NOTE: The VHDL library files must be compiled in the order specified.

NOTE: During the ispLEVER installation, you must select the option **Interface Kits** and click **Change** to enable the ispXPGA option. By default, this option is disabled. If you have already installed ispLEVER, you can rerun the installation program to install the Interface Kits components.

Workaround: None

Devices Affected: ispXPGA

Issue:	***PC only –*** Different synthesis tools can generate different bus signal names in EDIF for Verilog designs. Therefore, locking the signal to I/O pin in one synthesis tool might not be valid for the other synthesis tool.
Workaround:	Stay with one synthesis tool if you have pin assignments.
Devices Affected:	ispXPGA

Known Issues and Solutions - CPLD

The following known CPLD issues have been identified and their solutions are determined:

Issue:	***PC only –*** You cannot mix Exemplar and Synplicity `.ppn` conversions. For Synplicity PPN files, square brackets are used [ ] to enclose the components of the bus. For example, `a[10]`. The Exemplar PPN files, however, use parentheses ( ) to enclose the components of the bus. For example, `a(10)`.
Workaround:	Don't mix constraint files (`.lci`) that were created with different synthesis tools.
Devices Affected:	ispLSI 1K, 2K, and 8K

Issue:	When you use the Preserve attribute for MACH devices, the report file does not show that the signals are preserved.
Workaround:	The property is working correctly, but it is not reported in the report file.
Devices Affected:	All MACH devices

Issue:	The first line of VHDL code cannot be a commented line.
Workaround:	Use the library declaration for the first line of VHDL code.
Devices Affected:	All

Issue:	The following constraints specified in the Schematic Editor will not work: PULL, SLEWRATE, OPENDRAIN, VOLTAGE, GROUP, RESERVE, CRIT, OUTDELAY.
Workaround:	Use the Constraint Editor to specify the constraints.
Devices Affected:	ispLSI 1K/2K/8K

Issue:	***UNIX only –*** If you have only one attribute when specifying the LAT_OSM_BYPASS attribute for ABEL, the fitter will issue a warning that the attribute is not implemented. In the Constraint Editor, this Bypass attribute is displayed in red. Note that this problem only arises when there is a space in the signal name, as in the following example: `LAT_OSM_BYPASS (BYPASS, pullup); //there is a space before the signal name pullup`
Workaround:	Remove the space in the LAT_OSM_BYPASS signal name. Example: `LAT_OSM_BYPASS (BYPASS,pullup);`
Devices Affected:	ispMACH 4K

Issue:	You cannot use the OSM_BYPASS attribute to select bits of a bus. The OSM_BYPASS can only be assigned to a bus or to a specific signal; it cannot be assigned to specific bits.
Workaround:	To assign an attribute to a specific bit, use the Constraint Editor.
Devices Affected:	ispMACH 4K

Issue:	Reserved pin assignments are not reported in the design summary section of the report file.
Workaround:	None
Devices Affected:	ispMACH 5K

Issue:	***PC only –*** When you use PLLs in your design, `prefit.exe` generates a warning regarding the removal of intermediate nodes that are inserted by the synthesis tools.
Workaround:	Ignore the warnings.
Devices Affected:	ispMACH 5KVG

Issue:	You cannot set both the GLB clock (CLK1, CLK2) and the IOC clock (IOCLK0, IOCLK1) in the Constraint Editor, for all the ispLSI 1000 devices. For example, to use one clock GLB_IOC to clock a register in both the GLB and IOC, the setting would be GLB_IOC=CLK1,IOCLK0. See page 10 of the *1000EA Data Sheet* to understand the clock matrix and this limitation.
Workaround:	You can set the clock in the ABEL source by using the legacy ABEL attributes plsi PROPERTY 'CLK glb_io_clk clk1 ioclk0'; There is no solution for the Verilog and VHDL, because the attributes are not supported in the source.
Devices Affected:	ispLSI 1K/1KE/1KEA

Known Issues and Solutions - ispXPLD

The ispXPLD devices support VHDL and Verilog design entry only. The following known ispXPLD issues have been identified and their solutions are determined:

Issue:	SYSIO LVDS IO types can be specified in the Constraint Editor. LVDS Macros—LVDSIN, LVDSOUT, LVDSIO, LVDSTRI—are not implemented.
Workaround:	Use LCI constraint to specify LVDS type.
Devices Affected:	ispXPLD

Issue:	The fitter may fail to satisfy the Group and Pin Assignment request if PT Input Cascading is used.
Workaround:	None.
Devices Affected:	ispXPLD

Issue:	Arithmetic function implemented with the carry chain may have higher utilization and worse performance than the logic implementation. There is no switch in the software that allows you to get the logic implementation.
Workaround:	None.
Device Affected:	ispXPLD

Issue:	When you import an EDIF file that contains a module such as memory or carry-chain, a question mark (?) appears in the lower module of the EDIF under the Source column. This error occurs in VHDL designs when you're using the PMI template. It is caused by missing attributes in the .vhd file.

Workaround:	Open the .vhd file with a text editor and add the following attributes for the specific component after it is specified:
	
	`attribute syn_black_box: boolean;`
	`attribute syn_black_box of <component_name>: component is true;`

Devices Affected:	ispXPLD

Issue:	The edif2blif does not guarantee the correct flag generation for FIFO 512x32 flags.
Workaround:	Use ALL FIFO flags in the design (to connect to IO or logic). This limitation will be removed with the next build opportunity.
Devices Affected:	ispXPLD

Issue:	The fitter complains of a missing macro instance for PLL. When a design that was last fit with a constraint, such as a PLL, is being recompiled without that constraint, the fitter generates a message regarding the missing constraint. The ispLEVER software uses data contained in the `.lct` (constraints file) to "remember" the PLL attributes. When you remove the PLL from your source, the ispLEVER software does not remove the PLL attributes from the LCT file. When the source and `LCT` files mismatch in this fashion, the fitter aborts because of the mismatch. This can happen when you import a new EDIF file to the existing project without clearing the constraints of the existing constraint file. When you replace or import a new EDIF file into the project workspace, the existing LCT file is not overwritten or cleared. If you do not clear the existing LCT file, all previous constraints, such as PLL descriptions, are still valid.
Workaround:	Use a TEXT EDITOR to remove the PLL attributes from the .lct file. To specify constraints from scratch, clear the constraints by choosing **Tools > Clear Constraints** in the Project Navigator.
Devices Affected:	ispXPLD

Known Issues and Solutions - ispGDX2

The following known ispGDX2 issues have been identified and their solutions are determined:

Issue:	When you use the Constraint Editor process for ispGDX2 designs, the ispLEVER runs the Fit Design process first. The Constraint Editor will not come up if Fit Design fails.
Workaround:	Edit the LCT file directly or specify constraints in the VHDL or Verilog HDL design source file.
Devices Affected:	ispGDX2

Issue:	If a sysIO such as GTL+ is specified, the Vref/Vcco pin should be reserved; however, the software might still assign a signal to Vref/Vcco.
Workaround:	Avoid using Vref/Vcco and ensure that a signal is not assigned to Vref/Vcco after fitting if sysIO is used.
Devices Affected:	ispGDX2

Issue:	When you select the Bus Assignment check box in the Constraint Editor Location Assignment dialog box, the dialog box changes to display a Bus Assignment window, which shows the signals that have been grouped as part of your bus design. This helps in assigning pins. However, not all signals are displayed in the Bus Assignment Bus List, so you might not see the particular signal you are looking for.
Workaround:	Signals that are not considered part of a bus are shown in the Constraint Editor Location Assignment dialog box under Signals List.
Devices Affected:	ispGDX2

Issue:	After invoking the Bus Assignment dialog from the Constraint Editor, no input signals can be seen on a bus.
Workaround:	None. In this release, pure input signals are regarded as bit signals.
Devices Affected:	ispGDX2

Issue:	The output and/or bidirectional signal may not be grouped into a bus.
Workaround:	None. The input data of the output and/or bidirectional signal is fanout to multiple destination Muxes.
Devices Affected:	ispGDX2

Issue:	In the Bus Assignment dialog of the Constraint Editor, no sufficient candidate pins are listed for doing the bus assignment.
Workaround:	Try to lock bus from the very first IO of each block. If you cannot find such an IO, try lock from the very first IO of each nibble.
Devices Affected:	ispGDX2

Issue:	After doing bus assignment, the fitting process fails.
Workaround:	None
Devices Affected:	ispGDX2

Known Issues and Solutions - ORCA

The following known ORCA issues have been identified and their solutions are determined.

Issue: ***UNIX only –*** A missing command line problem occurs in the Module/IP Manager when you generate an FPSC core.

This problem has been fixed in Service Pack 6. However, the problem will still occur if you install an FPSC design kit after you've installed the ispLEVER Service Pack 6. The FPSC design kit overwrites the service pack fixes that pertain to FPSCs.

Workaround: a. Install the FPSC kit *before* installing the Service Pack 6.
b. If you've already installed the FPSC kit after installing the Service Pack 6, reinstall the Service Pack 6.

Devices Affected: FPSC

Issue: FPSC environment variables are not set for the ispgui and setup_lv.csh. This can cause the Module/IP Manager to fail to generate a proper netlist. For example, no netlist is generated for the ORLI10G Core.

Workaround: Set the environment variables manually, as shown in the following examples.

ksh example:

```
export FPSC=.../isptools/ispFPSC
export PATH=$FPSC/fpscbin/sol:$PATH
export
LD_LIBRARY_PATH=$LD_LIBRARY_PATH:$FPSC/fpscbin/sol
```

csh example:

```
setenv FPSC .../isptools/ispFPSC
setenv PATH ${FPSC}/fpscbin/sol:${PATH}
setenv LD_LIBRARY_PATH
${LD_LIBRARY_PATH}:${FPSC}/fpscbin/sol
```

You may wish to add these to your login scripts for the ispLEVER tools, in addition to the normal setting of the FOUNDRY and PATH variables.

Devices: FPSC

Issue: Running the ORCA Floorplanner does not update the design flow for reports. If you change the logical groups using the ORCA Floorplanner, the `.ngd` file will change and you will need to run map again. However, upon return to the Project Navigator, right clicking **Map Trace Report** and selecting **View** does not force the rerunning of map.

Workaround: Right-click **Map Design** and run **Force One Level** to rerun map.

Devices Affected: ORCA

Issue: Project Navigator allows you to run the Floorplanner with an ORCA Series 2 design. This is not legal. Any logical floorplanning you do with an ORCA Series 2 design will be ignored. Attempts to do physical floorplanning with an ORCA Series 2 design will result in an error.

Workaround: None

Devices Affected: ORCA

Issue: The Module/IP Manager bus expression is not valid for Verilog/VHDL. From Module/IP Manager, the Expression Style is only applicable to EDIF. It does not affect the output for Verilog/VHDL.

Workaround: None

Devices Affected: ORCA

Issue: When running Timing Checkpoint Options and the TRACE Options command under the Tools menu, the following message is displayed:

```
Font specified in font.properties not found [urw-itc
zapfdingbats-medium-rnormal . . .]
```

Workaround: Ignore the message. The tools are fully functional.

Devices Affected: ORCA 2, 3, 4

Issue:	The values for the Timing Checkpoint Options and Trace Options are saved when the project navigator is exited. However, the default logic percent for the timing checkpoint is not updated when a new device is selected. The user will need to update this value when a new device is selected.
Workaround:	None
Devices Affected:	ORCA

Issue:	Installation that overflows disc quota produces only the Java Error: "`The message is one or more errors that occurred during the copying of files (bean14). Please refer to the install log for additional information`."
Workaround:	Make sure you have adequate disk space and reinstall.
Devices Affected:	ORCA

Issue:	The `ispflow.exe` batch mode command does not support ispXPGA or ORCA devices.
Workaround:	None
Devices Affected:	ORCA

Known Issues – Miscellaneous

The following known miscellaneous issues have been identified and their solutions are determined.

ispVM Programming System Issues

Issue:	When a JTAG-ISC device is in the chain description file (`.xdf`), selecting **Edit > Set Chain Operations** does not change the operation for the JTAG-ISC device.
Workaround:	To change the operation for the JTAG-ISC device, double click the JTAG-ISC device in the GUI, or select **Edit > Edit Device** to open the Device Information dialog box. Click the down arrow to the right of the Action List combo box, select the operation, click the down arrow to the right of the Action List combo box again, and click **OK**.
Devices Affected:	All

Issue:	When performing a Read and Save Action (operation) on a JTAG-ISC device in a chain with non-JTAG-ISC devices, the ISC data file might not be written if a non-JTAG-ISC device is in front of the JTAG-ISC device (TDI side).
Workaround:	a. Move the JTAG-ISC device in front of the non-JTAG-ISC devices. *or* b. Create a new chain file and select **JTAG-ISC** for all non-JTAG-ISC devices in front of the JTAG-ISC device.
Devices Affected:	All

Issue:	For JTAG-ISC and JTAG-SVF devices, when manually editing the file or path of the Data File, BSDL File, Input ISC Data File, or Read and Save Output ISC Data File, start on the right end of the edit box and use the Back Space key.
Workaround:	Use the Browse button and select the file.
Devices Affected:	All

Issue: In the Device Information dialog box, when a Read & Save operation is selected and you are entering the Data File path and name manually, make sure that you type the correct data file extension. For example, when typing a JEDEC file name, type the `.jed` extension. When typing an ISC data file name, type the `.isc` extension.

Workaround: None

Devices Affected: All

Issue: MACH111SP Model 300 support might report a false verify failure. This false failure could be due to the speed improvements made to JTAG pins for our faster devices.

Workaround: Change the TCK Low Pulse Width Delay in **Project > Project Settings > Advanced** to a value of 2 or greater.

Devices Affected: All

ispEXPLORER Issues

Issue: When running ispEXPLORER, you might see the following message in the console window:

```
Font specified in font properties not found [-urw-itc
zapfdingbats-medium-r-normal . . .]
```

Workaround: None. Ignore the message. The ispEXPLORER is fully functional.

Devices Affected: CPLD, ispXPGA, ispXPLD

Online Help/Documentation Issues

Issue: In the online Help, black box attributes for LPMs are missing from the VHDL design examples that use the PMI template. See **Macro and IP Design > The PMI Template > References > VHDL LPM Examples**.

Solution: For each of the VHDL LPM design examples that you want to use with the PMI template, add the black box attribute for the specified component:

```
attribute syn_black_box: boolean;
attribute syn_black_box of <component_name>: component is
true;
```

These attributes must be added after the component is specified.

Example:

```
library IEEE;
use IEEE.std_logic_1164.all;

entity test_fifo is

port (
     Data           :in std_logic_vector(18 downto 0);
     WrClock      : in std_logic;
     WrEn         : in std_logic;
     RdClock      : in std_logic;
     RdEn         : in std_logic;
     Reset        : in std_logic;
     RPReset      : in std_logic;
     Q             : out std_logic_vector(18 downto 0);
     Full         : Out std_logic;
     Empty        : Out std_logic;
     AlmostFull   : Out std_logic;
     AlmostEmpty  : Out std_logic);
end test_fifo ;


architecture behave of  test_fifo  is

component fifo1kx19
generic (
     LPM_TYPE     : string := "LPM_FIFO_DC";
     LPM_WIDTH    : positive;
     LPM_WIDTHU   : positive;
     LPM_NUMWORDS : positive;
     LPM_HINT     : string :="UNUSED");
port (  Data       : in std_logic_vector(LPM_WIDTH-1
  downto 0);
```

```
WrClock        : in std_logic := '0';
WrEn           : in std_logic;
RdClock        : in std_logic := '0';
       RdEn            : in std_logic;
       Reset           : in std_logic;
       RPReset         : in std_logic;
       Q               : out
         std_logic_vector(LPM_WIDTH-1 downto 0);
       Full           : out std_logic;
       Empty          : out std_logic;
       AlmostFull     : out std_logic;
       AlmostEmpty    : out std_logic );
end component ;

attribute syn_black_box: boolean;
attribute syn_black_box of fifo1kx19: component is
  true;

begin
lpm_gen: fifo1kx19
generic map (LPM_WIDTH => 19,
       LPM_WIDTHU   => 10,
       LPM_NUMWORDS => 1024,
       LPM_TYPE     => "LPM_FIFO_DC")
port map (   Data => Data,
       WrClock     => WrClock,
       WrEn        => WrEn,
       RdClock     => RdClock,
       RdEn        => RdEn,
       Reset         => Reset,
       RPReset     => RPReset,
       Q           => Q,
       Full        => Full,
       Empty       => Empty,
       AlmostFull  => AlmostFull,
       AlmostEmpty => AlmostEmpty );
end behave;
```

Devices Affected: ispXPGA, ispXPLD

Issue:	***PC only –*** If you install, uninstall, and reinstall the ispLEVER software to a different location on your PC hard drive, you might receive an error message when you attempt to start Help. This can be caused by conflicts between the new location of Help and its old `.gid` file. GID files (`<help_file_name>.gid`) are configuration files that are dynamically created by Windows when starting Help. They contain the last location of the Help file. If the GID file is out of sync with the Help file (for example the GID file was not deleted during the uninstall process), you will receive a message saying that the Help file cannot be found
Solution:	Search for and delete all files with the extension `.gid` on your hard drive. Windows will automatically create a new GID file for each help system on your computer when you start the help system.
Devices Affected:	All