DDR3 SDRAM Controller IP

IP Version: v2.4.1

Release Notes

FPGA-RN-02032-1.7

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1. Introduction

This document contains the Release Notes for the DDR3 SDRAM Controller IP and the DDR3 Memory Controller Driver. For specific details about the IP and driver, refer to the following:

- DDR3 SDRAM Controller IP Core for Nexus Devices (FPGA-IPUG-02086)
- Nexus DDR3 Memory Controller Driver User Guide (FPGA-TN-02401)

DDR3 SDRAM IP v2.4.1

Software	Software Version	Summary of Changes
Lattice Radiant	2026.1.1	Fixed the IP Block Wizard GUI displaying a blank window in Radiant patch releases.

DDR3 SDRAM IP v2.4.0

Software	Software Version	Summary of Changes

Lattice Radiant	2026.1	• Tri-stated the DM signals on the memory interface when there are no active transactions.
		• Split the AXI reset from the memory controller reset so that resetting the AXI interface does not reset the memory controller, and resetting the memory controller does not reset the AXI interface.
		• Added device support for LFMXO5-55TDQ and LFMXO5-65TDQ.
		• Added device support for LFD2NX-15P, LFD2NX-25P, and LFMXO5-25P, including PLL primitive (PLLD) changes for these devices.
		• Set the maximum supported memory clock frequency to 300 MHz for the following devices: LFD2NX-15, LFD2NX-15P, LFD2NX-25, LFD2NX-25P, LFMXO5-15D, LFMXO5-25, and LFMXO5-25P.
		• Added training data generation within the IP to support running extended calibration using the IP driver, and extended the status register to capture additional flags related to extended training.
		• Limited memory data bus width of x32 with AXI enabled in Gear 2 to configurations where the memory clock is set to less than 400 MHz.
		• Driver updates:
		  • Separated ddr3_init (controller base setup) from ddr3_do_training (PLL wait, basic training, and data mode).
		  • Replaced the global instance and read/write helper functions with DDR3_READ32 and DDR3_WRITE32 macros.
		  • Removed printf logging from the basic training sequence.
		  • Expanded ddr3_nexus.h to include the extended-training register map, additional status bitfields, and dqdm_sweep_info structure.
		  • Added driver functions for coarse DQDM calibration, followed by write DQDM calibration and read DQ calibration.

DDR3 SDRAM IP v2.3.1

Software	Software Version	Summary of Changes

Lattice Radiant	2025.2.1	• Enhanced the write centering of the extended training in the example design.
		• Added support for periodic voltage/temperature compensation of I/O delay.
		• Updated the default values of the following IP parameters based on the Certus-NX Versa board:
		  • Write DQ/DM delay value
		  • Read DQ delay value
		  • Read DQ phase adjustment value

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DDR3 SDRAM IP v2.3.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.2	• Increased the auto refresh period from 5.7 µs to 7.8 µs to match the JEDEC specification. • Fixed an incorrect, intermittent AXI reset behavior. • Fixed the internal arbitration handling between the issuing of auto-refresh and power-down. • Updated the SIM_FLOAT_PRECISION parameter for the internal PLL to a value of 0.625. • Added a 2 – 4 SCLK margin to the auto-refresh period to account for clock inaccuracies. • Added options to select the type of board used with the example design and automatically assign pins according to the selected board. • Added support for extended calibration, which includes write training and read data-eye training. • Added automatic CK delay adjustments during write leveling. • Added Lattice Reveal debug ports to support debugging of the extended calibration.

DDR3 SDRAM IP v2.2.1

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1.1	Fixed timing model and disabled the simulation workaround. In earlier versions of the software, the simulation workaround remains enabled.

DDR3 SDRAM IP v2.2.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1	• Added AXI upsizing capability. • Updated the PLL for better jitter. • Added IP constraints to the Radiant Constraints Propagation Engine. • Added additional debug ports for use with Reveal. • Enabled support for AXI burst length up to 64 bits. • Added cacheable tag to enable caching of the memory address range in Propel.

Corrections to Previous Release Notes

- In version 2.0.1, the DDR reset initialization timing fix was omitted in the release notes.
- In version 2.0.1, the release notes incorrectly stated that em_ddr_clk_t and em_ddr_clk_c alignment was fixed for gearing ratio 4:1. The alignment fix applies to all gearing ratios.

DDR3 SDRAM IP v2.1.0

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2	Added driver support

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DDR3 SDRAM IP v2.0.1

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2	• Added support for AXI4 Interface as data bus and APB Interface as control bus. • Added example design. Updated testbench to make use of the example design in simulation. • Disabled obfuscation to enable the constraints in Radiant flow. • Added GUI options: MC CK/Command Delay value and MC DQS/DQ ODT Value. • Fix em_ddr_clk_t and em_ddr_clk_c alignment for Gearing ratio 4:1

DDR3 SDRAM Controller IP Earlier Versions

IP Version	Summary of Changes
1.4.2	• Fixed timing parameters for gearing ratio 8:1. • Removed tRFC wait time when issuing a precharge during auto-refresh. • Removed set_max_delay of synchronizers for the de-assertion of reset in top_constraint.pdc.
1.4.1	• Fixed the missing activate issue when cmd_rdy_o are cmd_valid_i are changed from invalid to valid at the same time. • Added cmd_burst_cnt_i sweep in the testbench/testcase.vh. • Removed global clock constraint in the top_constraint.pdc and improve the constraints. • Synchronized the reset de-assertion inside the IP. • Added Enable External PLL Reset attribute. • Added external ports for write leveling start and done. • Added support for both internal and external refresh when Enable External PLL Reset and External Auto Refresh Port are selected. • Fixed precharge all command during internal auto refresh.
1.4.0	• Updated read training logic based on validation in the board. • Added option to disable the internal PLL • Updated the selectable values for Select Memory and RefClock attributes. • Changed the default value of Controller Reset to Memory attributes. • Updated the testbench to add write delay that would match with the PHY delay settings that worked on the board. Fixed the cmd_burst_cnt_i=2 issue when 8:1 gearing ratio.
1.3.0	Updated for Radiant 3.0.
1.2.1	Updated PLL instance.
1.2.0	Added LFCPNX support.
1.1.1	Improved performance for 8:1 gearing ratio.
1.1.0	• Updated for Radiant 2.1. • Added 8:1 gearing ratio support. • Added eval folder. Added Certus-NX support. • Updated clock signal names: clk_i, sclk_o. • Updated PLL instance.
1.0.1	Updated for Radiant 2.0 Service Pack 1.
1.0.0	Preliminary release.

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References

- DDR3 SDRAM-Controller IP Core for Nexus Devices (FPGA-IPUG-02086)
- Nexus DDR3 Memory Controller Driver User Guide (FPGA-TN-02401)
- Lattice Nexus Platform web page
- IP Core for Lattice Nexus devices
- Lattice Propel Builder software
- Lattice Radiant FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

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