



PCIe x4 IP

IP Version: v4.0.0

Release Notes

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This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language [FAQ 6878](#) for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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1. Introduction

This document contains the Release Notes for the PCIe x4 IP and PCIe x4 Driver. For specific details about the IP and the driver, refer to the following:

- [PCIe x4 IP Core User Guide \(FPGA-IPUG-02126\)](#)
- [Lattice Avant and Nexus PCIe Host DMA Driver Software User Guide \(FPGA-TN-02386\)](#)
- [Lattice Avant and Nexus PCIe Basic Memory-Mapped Host Driver \(Non-DMA\) User Guide \(FPGA-TN-02387\)](#)
- [PCI Express for Nexus FPGAs](#) web page

PCIe x4 IP v4.0.0

Software	Software Version	Summary of Changes
Lattice Radiant™	2025.2	<ul style="list-style-type: none"> • IP Update <ul style="list-style-type: none"> • Made enhancements to the IP user interface. • Feature Updates <ul style="list-style-type: none"> • Enabled MSI-X feature in the AXI Bridge mode. • Example Design Update <ul style="list-style-type: none"> • Enabled QuestaSim Lattice-Edition simulation. • Driver Update <ul style="list-style-type: none"> • Refreshed non-DMA driver.

PCIe x4 IP v3.6.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1.1	<ul style="list-style-type: none"> • Feature Updates <ul style="list-style-type: none"> • Added LFMX05-55TDQ device support. • Enabled PCIe Legacy Interrupt Capability.

PCIe x4 IP v3.5.1

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1	<ul style="list-style-type: none"> • Updated the PCIe IP License string. • Enabled the clock user out signal.

PCIe x4 IP v3.5.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1	<ul style="list-style-type: none"> • Feature Updates <ul style="list-style-type: none"> • AXI Bridge Mode enablement. • Example Design Update <ul style="list-style-type: none"> • Example Design for NON-DMA configuration is now updated to be compatible with both simulation and hardware implementation.

PCIe x4 IP v3.4.0

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2.1	<ul style="list-style-type: none"> • Feature Updates <ul style="list-style-type: none"> • Bug Fixes on AXI-S DMA • Driver Updates <ul style="list-style-type: none"> • Added Official Driver support for AXI-S DMA.

PCIe x4 IP v3.3.0

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2	<ul style="list-style-type: none"> Feature Updates <ul style="list-style-type: none"> Bug Fixes. Driver Updates <ul style="list-style-type: none"> Added support for Bi-Directional concurrent DMA transfer in DMA Performance Measurements for AXI-MM DMA Official Driver. Added Official Driver support for Non-DMA Endpoint. Removed AXI-MM DMA Demo drivers.

PCIe x4 IP v3.2.0

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2	<ul style="list-style-type: none"> Feature Updates <ul style="list-style-type: none"> Added AXI-Stream DMA for FPGA-to-Host DMA data transfer. Added DMA Bypass Mode for both AXI-MM DMA and AXI-Stream DMA. Added Error and Status logging and interrupt triggering for both AXI-MM DMA and AXI-Stream DMA. Added User Interrupt pins for both AXI-MM DMA and AXI-Stream DMA. Re-architected Non-DMA AXI-Stream for timing fix for PCIe Gen3. Bug fixes. Example Design Updates <ul style="list-style-type: none"> Added Example Design for AXI-Stream DMA. Driver Updates <ul style="list-style-type: none"> Added Official Driver support for AXI-MM DMA (AXI-S DMA driver support is available in 2024.2 SP1).

PCIe x4 IP Earlier Versions

IP Version	Summary of Changes
3.1.0	<ul style="list-style-type: none"> Update on High Performance PCIe DMA for PCIe Gen3x4 <ul style="list-style-type: none"> Example Design simulation and hardware are supported. Hardware tested using CertusPro™-NX Bridge Board. Performance data based on simulation and hardware are published in the IPUG. Application driver with Demo user interface running on the host PC supported. Refer to the IPUG on the compile instructions.
3.0.0	<ul style="list-style-type: none"> High Performance PCIe DMA for PCIe Gen3x4 <ul style="list-style-type: none"> Supports AXI-MM interface on user application. Supports Descriptor Prefetching for performance improvement. Supports MSI interrupt when DMA transfer is completed. Example Design simulation supported.
2.4.0	<ul style="list-style-type: none"> Enable Propel support. Fixed issue where gen3x1 simulation time is slower than gen3x4. Fixed timing constraint issues not read in properly in encrypted RTL. Fixed Link1 PF config issue. Fixed sd_ext_1_refclk_i issue. Warnings fix.
2.3.1	Reduced simulation time for Modelsim OEM simulator

IP Version	Summary of Changes
2.2.0	<ul style="list-style-type: none">Updated for Gen1/2/3 Endpoint with DMA x1, x2 and x4 support.Updated user data interface to 64, 128 and 256 bits but clock frequency is half of sys_clk.Updated maximum descriptor block size supported to 4KB.Supported 125 MHz PHY refclk.Added mixed mode support.Added example design for simulation.
2.1.0	Updated for Gen3 Endpoint with DMA 1x1 support.
2.0.0	Optimized for Gen3 Endpoint with DMA 1x4 support
1.1.0	Added Endpoint DMA 1x4 function and Root Port Mode.
1.0.1	Initial release.

References

- [PCIe x4 IP Core User Guide \(FPGA-IPUG-02126\)](#)
- [Lattice Avant and Nexus PCIe Host DMA Driver Software User Guide \(FPGA-TN-02386\)](#)
- [Lattice Avant and Nexus PCIe Basic Memory-Mapped Host Driver \(Non-DMA\) User Guide \(FPGA-TN-02387\)](#)
- [CertusPro-NX](#) web page
- [PCI Express for Nexus FPGAs](#) web page
- [Lattice Propel Builder](#) software
- [Lattice Radiant](#) FPGA design software
- [Lattice Insights](#) for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase



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