PCIe x8 IP

IP Version: v3.1.1

Release Notes

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1. Introduction

This document contains the Release Notes for the PCIe x8 IP and PCIe x8 Driver. For specific details about the IP and the driver, refer to the following:

- PCIe x8 IP Core User Guide (FPGA-IPUG-02243)
- Lattice Avant and Nexus Linux PCIe Host DMA Driver User Guide (FPGA-TN-02433)
- Lattice Avant and Nexus Linux PCIe Host Non-DMA Driver User Guide (FPGA-TN-02424)
- PCI Express for Avant FPGAs web page

PCIE x8 IP v3.1.1

Software	Software Version	Summary of Changes
Lattice Radiant™	2026.1.1	• Corrected the supported legacy INTx interrupt pin range from INTA up to INTD based on the configured number of Physical Functions, in compliance with the PCIe specification. • Corrected the default mgmt_ftl_decode_ignore_poison bit register value from 1'b1 to 1'b0 for endpoint applications.

PCIE x8 IP v3.1.0

Software	Software Version	Summary of Changes

Lattice Radiant	2026.1	• Corrected Function 0 BAR 0 to disable 64-bit address and prefetchable options when I/O is selected as the memory type of Function 0 BAR 0.
		• Removed the unused m0_aximm_awuser_o interface for Bridge Mode configuration.
		• Corrected the interface width for m0_aximm_aruser_o for Bridge Mode from 48 bits to 8 bits.
		• Added the link0_reset_done_o signal.
		• Added ucfg_chg_sync_lmmi_o for TLP Mode (TLP Data Interface).
		• Updated the width for link0_flr_ack_i and link0_flr_o to 32 bits when FLR is enabled for TLP Mode (TLP Data Interface) variant.
		• Enabled the Active State Power Management (ASPM) L1 capability for TLP Mode (TLP Data Interface).
		• Enabled the Latency Tolerance Reporting (LTR) capability for TLP Mode (TLP Data Interface).
		• Enabled Virtual Function Support for TLP Mode (TLP Data Interface).
		• Enabled Reference Clock Modes Selection.
		• Driver Update
		  • Replaced DMA official driver support with open-source Linux driver.
		  • Removed non-DMA official driver support.
		  • Removed hardened DMA official driver support.

Corrections to Previous Release Notes

In v3.0.0, an open-source Linux driver is added for non-DMA configuration.

PCIE x8 IP v3.0.1

Software	Software Version	Summary of Changes
Lattice Radiant	2025.2.1	Fixed issues observed in the Propel software.

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PCIE x8 IP v3.0.0

Software	Software Version	Summary of Changes

Lattice Radiant	2025.2	• IP Update
		  • Made enhancements to the IP user interface.
		  • Added device support for Certus-N2 (except LN2-CT-20ES).
		• Feature Update
		  • Enabled DMA.
		  • Enabled MSI-X feature in AXI Bridge mode.
		• Example Design Update
		  • Added DMA Example Design simulation and hardware support.
		• Driver Update
		  • Added the official driver support for DMA.

PCIE x8 IP v2.4.0

Software	Software Version	Summary of Changes

Lattice Radiant	2025.1.1	• Driver Update
		  • Added the official driver support for the AXI Bridge mode.
		• IP Update
		  • Restored link0_clk_usr_o.
		  • Updated the default values for Device ID and Vendor ID.
		  • Updated width for link0_flr_ack_i and link0_flr_o to 32 bits when FLR is enabled for hard DMA variant.
		• Feature Update
		  • Restored Advance Error Reporting (AER) capability.
		  • Removed Surprise Down Error and TLP Prefix Blocked reporting.

Corrections to Previous Release Notes

In v2.3.0, the Active State Power Management (ASPM) capability and Latency Tolerance Reporting (LTR) capability are disabled as these were unintentionally made available in the v2.2.0 release. Any use during the v2.2.0 release is unsupported and may carry risks due to incomplete validation.

PCIE x8 IP v2.3.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1	• Feature Updates • AXI Bridge Mode enablement.

PCIE x8 IP v2.2.0

Software	Software Version	Summary of Changes

Lattice Radiant	2024.2.1	• Feature Updates
		  • Active State Power Management (ASPM) capability enablement
		• Example Design Updates
		  • Added Harden DMA Gen4x8 Example Design hardware support.
		  • Added non-DMA Gen4x8 Example Design hardware support.
		• Driver Updates
		  • Added official driver support for Harden DMA and non-DMA

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PCIE x8 IP v2.1.0

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2	• Enabled Harden DMA Gen4x8 support for Synthesis/Timing/Simulation. • Enabled Harden DMA Gen4x8 Example Design simulation. • Updated the PCIe PCS/PHY parameters for hardware support (official hardware support in Radiant 2025.1). • Fixed bugs related to PCIe BAR, PF, VF, MSI and MSI-X.

PCIE x8 IP Earlier Versions

IP Version	Summary of Changes

2.0.0	• PHY Configuration
	  • Increased aggregation and bifurcation up to x8 lanes
	  • Increased data rates of 8.0 Gbps and 16.0 Gbps
	  • Added 128b/130b encoding at 8 Gbps and 16 Gbps
	  • Added support for PCIe L1-substate power management and Separate RefClk Independent SSC Architecture (SRIS)
	• Hard IP Link Layer Features
	  • PCI Express Base Specification Revision 4.0 compliant including compliance with earlier PCI Express Specifications
	  • Backward compatible with PCI Express 3.x, 2.x, 1.x
	  • x8 PCI Express Lanes with support for bifurcation
	  • Supported lane configurations: 1 × 8, 1 × 4, 1 × 2, 1 × 1

1.1.0	• PHY Configuration
	  • Aggregation and bifurcation up to x4 lanes
	  • Data rates of 2.5 Gbps and 5.0 Gbps
	  • Selectable parallel data widths such as 8, 16, 32, and 64
	  • 8b/10b encoding at 2.5 Gbps and 5 Gbps
	  • Adaptive and configurable RX Continuous Time Linear Equalizer (CTLE) and Decision Feedback Equalizer (DFE)
	  • Adaptive and programmable TX equalization
	  • Extensive PMA debug capability through read/write and read-only registers in PCS
	  • Register-based control of all PCS-to-PMA signals
	  • A wide range of reference clock frequencies with optional fractional frequency correction capability
	  • A wide range of divided clock frequencies for external-to-PHY usage with optional spread-spectrum clock (SSC) capability
	  • Built-in, on-chip SSC generation and full configuration from –5000 to +5000 ppm
	  • Test support features such as near-end loopback, PLL bypass modes, and others
	  • Protocol-compatible features such as LOS, squelch, power modes, and others
	• Hard IP Link Layer Features
	  • PCI Express Base Specification Revision 2.0 compliant including compliance with earlier PCI Express Specifications
	  • Backward compatible with PCI Express 1.x
	  • x4 PCI Express Lanes with support for bifurcation
	  • Supported lane configurations: 1 × 4, 1 × 2, 1 × 1

1.0.1	• Supports Synthesis/Timing/Simulation • Supports Gen1/2 x1/x2/x4 Endpoint • Supports AXI-L/LMMI for config bus • Supports AXI-S/TLP interface for data bus • Supports Example Design simulation using QuestaSim (refer to IPUG for details) • Supports up to 8 PF with workaround (refer to IPUG or ED. To be addressed in 2023.2 SP1)

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- Lattice Avant and Nexus Linux PCIe Host DMA Driver User Guide (FPGA-TN-02433)
- Lattice Avant and Nexus Linux PCIe Host Non-DMA Driver User Guide (FPGA-TN-02424)
- Avant-G web page
- Avant-X web page
- PCI Express for Avant FPGAs web page
- Lattice Propel Builder software
- Lattice Radiant FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

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