



AXI Register Slice IP

IP Version: v1.3.0

Release Notes

FPGA-RN-02049-1.2

June 2026

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language [FAQ 6878](#) for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

Contents 3

1. Introduction 4

 AXI Register Slice IP v1.3.0 4

 AXI Register Slice IP v1.2.0 4

 AXI Register Slice IP v1.1.0 4

 AXI Register Slice IP Earlier Versions 4

References 5

Technical Support Assistance 6

1. Introduction

This document contains the Release Notes for the AXI Register Slice IP. For specific details about the IP, refer to the following:

- [AXI Register Slice IP User Guide \(FPGA-IPUG-02235\)](#)

AXI Register Slice IP v1.3.0

Software	Software Version	Summary of Changes
Lattice Propel™ Builder	2026.1	- Added support for LN2-CT-20 and LN2-CT-20ES1 devices. - Added support for LFD2NX-15P and LFD2NX-25P devices. - Added support for LFMXO5-25P device. Note: There are no updates to the IP user guide for this release. Refer to the AXI Register Slice IP User Guide (FPGA-IPUG-02235, v1.1) for the applicable documentation.

AXI Register Slice IP v1.2.0

Software	Software Version	Summary of Changes
Lattice Propel Builder	2025.1	- Updated the minimum supported values of <i>Address ID Width</i> and <i>User Width</i>. - Added support for LFD2NX-15, LFD2NX-25, LFD2NX-35, and LFD2NX-65 devices. - Added support for LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T devices. - Documented the changes for earlier IP versions in the IP Release Notes.

AXI Register Slice IP v1.1.0

Software	Software Version	Summary of Changes
Lattice Propel Builder	2024.2	Added support for Certus-N2, LatticeECP3, and ECP5 devices.

AXI Register Slice IP Earlier Versions

IP Version	Summary of Changes
1.0.0	Initial release.

References

- [AXI Register Slice IP User Guide \(FPGA-IPUG-02235\)](#)
- [LatticeECP3](#) web page
- [ECP5](#) web page
- [CertusPro-NX](#) web page
- [Certus-N2](#) web page
- [Certus-NX](#) web page
- [CrossLink-NX](#) web page
- [MachXO5-NX](#) web page
- [Avant-E](#) web page
- [Avant-G](#) web page
- [Avant-X](#) web page
- [AXI Register Slice IP Core](#) web page
- [Lattice Propel Builder](#) software
- [Lattice Radiant](#) FPGA design software
- [Lattice Diamond Software](#) web page
- [Lattice Insights](#) for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.



www.latticesemi.com