DDR Memory Controller IP

IP Version: v2.7.0

Release Notes

FPGA-RN-02033-1.4

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Contents

1. Introduction

This document contains the Release Notes for the DDR Memory Controller IP and DDR Memory Controller Driver. For specific details about the IP and driver, refer to the following:

- DDR Memory Controller IP Core (FPGA-IPUG-02208)
- DDR Memory Controller Driver (FPGA-TN-02379)

DDR Memory Controller IP v2.7.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.2	Added support for DQ-bit swapping in LPDDR4.

DDR Memory Controller IP v2.6.1

Software	Software Version	Summary of Changes

Lattice Radiant	2025.1.1	• Updated constraints for the PLL instance.
		• Updated sequence for changing CK delay during auto-CBT to avoid glitch.
		• Updated CK Delay default value in IP GUI.
		• Enabled Bit-Level Trim Sweep for 1,600 Mbps and 1,866 Mbps.
		• Driver changes:
		  • Added LPDDR4 support to training logic (previously DDR4-only).
		  • Enabled additional training bits for LPDDR4 based on DDR frequencies.
		  • Introduced a new error type for clearer issue reporting.
		  • Removed printf() and commented-out lines.

DDR Memory Controller IP v2.6.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1	• Added support for LAV-AT-G30 and LAV-AT-X30 devices. • Added *Configuration* attribute in the IP GUI. • Added DRAM and MC Vref settings in the IP GUI. • Updated the I/O slew rate default values in the IP GUI. • Updated the ODT default values and remove unused settings in the IP GUI for DDR4. • Added the CS delay attribute in the IP GUI. • Updated the read latency options at 1,066 MHz for DDR4. • Allowed the *Enable Read DBI* option with 1,066 MHz and 1,200 MHz for LPDDR4. • Improved DDR4 training based on HW validation. • Added cacheable tag to enable caching of the memory address range in Propel.

DDR Memory Controller IP v2.5.2

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2.1	• Improved training time for simulation (TRN_OP_REG=0x01C). • Improved Bit-Level Trim Sweep for LPDDR4. • Added Example Design options in the IP GUI for LPDDR4. • Added automatic pin assignments for Lattice boards.

DDR Memory Controller IP v2.4.0

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2	• Added support for Lattice Nexus 2 device (LN2-CT-20). • Fixed ECO Editor error caused by invalid IP parameter format. • Changed LPDDR4 boot frequency to 50 MHz. • Improved Bit-Level trim sweep for LPDDR4. • Added 2D Vref for LPDDR4; 1,066 MHz and 1,200 MHz.

DDR Memory Controller IP Earlier Versions

IP Version	Summary of Changes
2.3.0	• Changed IP name from Memory Controller for Avant Devices to DDR Memory Controller. • Added support for LKH-CT-20 device. • Updated write and read latency options. • Updated PLL to v2.6.0. • Disabled the Enable Power Down option because of issue found on HW.
2.2.0	• Added driver support for LPDDR4. • Supported APB disable in the Example Design.
2.1.0	• Added support for LAV-AT-E30 device. • Added LPDDR4 read DBI support. • Added Dual Rank support. • Improved DDR4 bus efficiency. • Validated DDR4 666 MHz, 800 MHz, 933 MHz, 1,066 MHz, and 1,200 MHz on the board. • Validated LPDDR4 1,200 MHz on the board.
2.0.0	Added DDR4 support (not HW Validated yet).
1.3.0	• Added support for LAV-AT-G70 and LAV-AT-X70 devices. • Validated 350 MHz, 400 MHz, 533 MHz, 666 MHz, 800 MHz 933 MHz, and 1,066 MHz on the board. • Added Power Down support.
1.2.0	• Enhanced AXI4 I/F to support: • Burst length from 1 to 64 beats • Any combination of burst length and burst size • Unaligned transfer using WSTRB • AXI4 data width less than DDR data width * 8 • Validated 266 MHz, 300 MHz, 350 MHz, 400 MHz, 533 MHz, 666 MHz and 800 MHz on the board. • Added PHY-side and DRAM-side DQ_VREF training support. • Disabled Power Down support for this version.
1.1.0	• Added support for DDR clock frequency != 800 MHz. • Enabled Post-Synthesis and Post-PAR simulations. • Validated at 533 MHz DDR clock, will validate other frequencies in next release.
1.0.0	Initial release.

References

- DDR Memory Controller IP Core (FPGA-IPUG-02208)
- DDR Memory Controller Driver (FPGA-TN-02379)
- Lattice Avant Platform web page
- Avant-E web page
- Avant-G web page
- Avant-X web page
- Certus-N2 web page
- IP Core for Avant devices
- Lattice Propel Builder software
- Lattice Radiant FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

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