DC-SCM LTPI IP

IP Version: v3.0.0

Release Notes

FPGA-RN-02021-1.3

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Contents

1. Introduction

This document contains the Release Notes for the DC-SCM LTPI IP. This DC-SCM LTPI IP is OCP Ready™. For specific details about the IP, refer to the following documents.

- For DC-SCM LTPI IP v3.0.0 and later, refer to: DC-SCM LTPI IP (New Architecture) User Guide (FPGA-IPUG-02312)
- For DC-SCM LTPI IP v2.1.0 and earlier, refer to: DC-SCM LTPI IP (Legacy) User Guide (FPGA-IPUG-02200)

DC-SCM LTPI IP v3.0.0

Software	Software Version	Summary of Changes
Lattice Radiant Propel Builder	2025.2	Added support for the OCP LTPI Specification Revision 1.2, Version 1.0, published in August 2025.

DC-SCM LTPI IP v2.1.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.2	Added support for MachXO4 devices.

DC-SCM LTPI IP v2.0.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1	• Added support for Certus-NX, CertusPro-NX, and Crosslink-NX devices. • Fixed an issue with ECHO detection. • Remapped CSR to follow the offset defined in the LTPI Specification. • Optimized to reduce resource utilization. • Merged CSR and Data Channel APB interfaces. • Changed system clock requirement – now uses a fixed frequency instead of being dependent on the LVDS frequency. • Optimized the implementation of bidirectional I2C. • Simplified and removed certain IP signals – for example, GDDR control signals are now handled internally within the IP. • Software primitives are now visible.

DC-SCM LTPI IP v1.6.0

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2	Updated to support the LTPI specification v1.1 revision 1.1 (May 2024).

DC-SCM LTPI IP Earlier Versions

IP Version	Summary of Changes
1.5.1	Masked unused APB CSR address (31:7) bits for the Propel software compatibility.

1.5.0	• Added MCTP over I2C channel support.
	• Updated CRC implementation:
	  • For LTPI version 1.1 or later, CRC is computed without inverted/reflected input and output.
	  • For older versions, CRC is computed with inverted/reflected input and output.
	• Fixed minor issue in packet parser module.
	• Made other minor GUI enhancements.

IP Version	Summary of Changes

1.4.4	• Added an optional configurable built-in timer for I2C channel.
	• Added an optional STOP event generation feature for I2C CSR reset when built-in timer is disabled.
	• Updated the NL GPIO tunneling implementation:
	  • Number of virtual input and output ports is always the same.
	  • Frame counter starts at count 0 instead of 1.
	• Added I2C-related flags in the interrupt register.
	• Added new debug ports.
	• Made other minor GUI enhancements.

1.4.3	Enhanced IP implementation to resolve issues found in the MachXO5-NX hardware validation.
1.4.2	• Added support for I2C topology with external I2C target devices in the I2C controller side – Previous version of the IP required no other external I2C target device on the I2C controller side. • Fixed an issue in aligner logic. • Fixed an issue in clock compensation logic of SDR mode for MachXO5-NX devices. • Changed default value of *Enable Clock Compensation* attribute to *Enabled*. • Updated *sync_rdy_o* output port to be always available in the generated IP. • Made other minor IP enhancements.
1.4.1	• Fixed an issue with Data Channel read operation. • Fixed a corner case issue related to I2C start and stop operations. • Fixed LTPI version to 1.0 in GUI.
1.4.0	• Enhanced Data Channel support for better usability – Separated APB interface for IP CSR and Data Channel access for SCM mode. • Made minor enhancement in system bus support.

1.3.0	• Added support for MachXO5-NX devices.
	• Expanded UART bus support from 8 to 24 maximum.
	• Enhanced Default and Custom I/O frame:
	  • For Default I/O Frame, channels can now be disabled.
	  • For Custom I/O Frame, sequence of channels in the frame is now customizable.
	• Added a new tab in GUI for Frame Format view.
	• Added descriptions for each attribute in GUI when hovered.
	• Added new debug ports.
	• Made other minor IP enhancements.

1.2.1	Fixed an issue in I2C repeated start operations.
1.2.0	• Added support for Mach-NX devices. • Fixed minor bug in interrupt reporting.
1.1.1	Enhanced word alignment algorithm.
1.1.0	Initial release for OCP DC-SCM 2.0 LTPI version 1.0 compliance.
1.0.0	Initial release.

References

- DC-SCM LTPI IP (New Architecture) User Guide (FPGA-IPUG-02312)
- DC-SCM LTPI IP (Legacy) User Guide (FPGA-IPUG-02200)
- Certus-NX web page
- CertusPro-NX web page
- CrossLink-NX web page
- Mach-NX web page
- MachXO3 web page
- MachXO3D web page
- MachXO4 web page
- MachXO5-NX web page
- DC-SCM LTPI IP Core web page
- Lattice Propel Design Environment web page
- Lattice Radiant Software web page
- Open Compute Project® web page
- Lattice Insights web page for Lattice Semiconductor training courses and learning plans

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