Automatic White Balance IP

IP Version: v1.4.1

Release Notes

FPGA-RN-02055-1.2

June 2026

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Contents

Contents 3
1. Introduction 4
Automatic White Balance IP v1.4.1 4
Automatic White Balance IP v1.4.0 4
Automatic White Balance IP v1.3.0 4
Automatic White Balance IP Earlier Versions 4
References 5
Technical Support Assistance 6

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

1. Introduction

This document contains the Release Notes for the Automatic White Balance IP. For specific details about the IP, refer to the following:

- Automatic White Balance IP User Guide (FPGA-IPUG-02204)

Automatic White Balance IP v1.4.1

Software	Software Version	Summary of Changes
Lattice Radiant	2026.1	• Added support for LFD2NX-15P, LFD2NX-25P, and LFMXO5-25P devices. • Updated clock frequency constraints.

Automatic White Balance IP v1.4.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.2	• Added support for Certus-N2 devices. • Added write strobe signal to AXI4-Lite bus interface. • Updated constraints file. • Minor bug fixes.

Automatic White Balance IP v1.3.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1	• Added support for LFD2NX-9, LFD2NX-28, LFD2NX-25, LFD2NX-35, and LFD2NX-65 devices. • Added support for LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T devices.

Automatic White Balance IP Earlier Versions

IP Version	Summary of Changes
1.2.1	• Removed license strings. • Fixed an issue in proper handling of PPC during vertical blanking period. • Fixed testbench related issues.
1.2.0	• Fixed issues in bus interface connectivity. • Fixed issues in handling TVALID going LOW during vertical blanking period. • Other minor IP enhancements.
1.1.0	• Added support for Lattice Avant devices. • Timing improvements and resource utilization optimizations. • Added support for partial resolution. • Added regression support in Verilog testbench.
1.0.0	Initial release.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

References

- Automatic White Balance IP User Guide (FPGA-IPUG-02204)
- CrossLink-NX web page
- Certus-NX web page
- Certus-N2 web page
- CertusPro-NX web page
- MachXO5-NX web page
- Avant-E web page
- Avant-G web page
- Avant-X web page
- Lattice Propel Design Environment web page
- Lattice Radiant Software web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

www.latticesemi.com