



10G Ethernet IP

IP Version: v3.4.0

Release Notes

FPGA-RN-02031-1.3

December 2025

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language [FAQ 6878](#) for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

Contents 3

1. Introduction 4

 10G Ethernet IP v3.4.0 4

 10G Ethernet IP v3.3.1 4

 10G Ethernet IP v3.3.0 4

 10G Ethernet IP Earlier Versions..... 4

References 6

Technical Support Assistance 7

1. Introduction

This document contains the Release Notes for the 10G Ethernet IP. For specific details about the IP, refer to the following:

- [10G Ethernet IP User Guide \(FPGA-IPUG-02245\)](#)
- [2.5G, 10G, and 25G Ethernet Driver API Reference \(FPGA-TN-02375\)](#)

10G Ethernet IP v3.4.0

Software	Software Version	Summary of Changes
Lattice Radiant™	2025.2	<ul style="list-style-type: none"> • Enabled Avant™ G/X30 device support. • Enabled SDC flow and updated timing constraints for easier integration by replacing <code>set_clock_groups</code> with <code>set_false_paths</code>.

10G Ethernet IP v3.3.1

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1.1	<ul style="list-style-type: none"> • Enabled the FC FEC mode on the PHY for Avant devices. • Changed the Loopback mode naming on Avant devices, from <i>Fabric loopback</i> to <i>Far End Parallel Loopback</i> and <i>Near PMA loopback</i> to <i>Near End Parallel Loopback</i> to match MPPHY Foundation naming notation. • Updated the Avant PHY-based PMA setting and GUI to allow for RX/TXEQ tuning. • Removed MDIO interface. • Reverted IP name in the Radiant software from 10Gb Ethernet MAC + PHY to 10G Ethernet. • Removed MachXO5™-NX device support.

10G Ethernet IP v3.3.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1	<ul style="list-style-type: none"> • Enabled MachXO5-NX (LFMXO5-55T, LFMXO5-100T) device support. • Enabled CertusPro-NX device support for MAC + PHY configuration. • Enabled lane-merging support for Avant devices.

10G Ethernet IP Earlier Versions

IP Version	Summary of Changes
3.2.0	<ul style="list-style-type: none"> • Enabled SyncE support. • Enhanced the statistic counter by adding a counter for cumulative number of bytes transmitted or received. • Enabled the Continuous mode for hardware example design. • Fixed the IPv6 packet reception to enable the ability to detect 0x8100 or 0x88A8. • Enhanced the Time Stamp Unit, which impacts MAC + PHY + 1588 configuration only. • Changed the IP name in the Radiant software from 10Gb Ethernet to 10G Ethernet MAC + PHY.
3.1.0	<ul style="list-style-type: none"> • Added Driver codes. • IP Name only updates to match the catalog.
3.0.0	Added PTP1588 support for CertusPro-NX devices. Enabled MAC-only mode.
2.1.2	Radiant software v2024.2 support (Avant ES version).
2.1.1	Added driver codes for Avant ES (engineering sample) version.
2.0.1	Radiant software v2024.1 support for Avant ES version.

IP Version	Summary of Changes
2.0.0	Initial release.

References

- [10G Ethernet IP User Guide \(FPGA-IPUG-02245\)](#)
- [2.5G, 10G, and 25G Ethernet Driver API Reference \(FPGA-TN-02375\)](#)
- [Avant-G web page](#)
- [Avant-X web page](#)
- [CertusPro-NX web page](#)
- [10Gb Ethernet MAC + PHY IP Core web page](#)
- [Lattice Solutions IP Cores web page](#)
- [Lattice Solutions Reference Designs web page](#)
- [Lattice Solutions Boards web page](#)
- [Lattice Solutions Demonstrations web page](#)
- [Lattice Propel Design Environment web page](#)
- [Lattice Radiant Software web page](#)
- [Lattice Insights](#) for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase



www.latticesemi.com