Lattice Nexus 2 Hardware Checklist

Technical Note

FPGA-TN-02382-0.83

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This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AC	Alternating Current
BGA	Ball Grid Array
BBRAM	Battery-Backed RAM
DC	Direct Current
DLL	Delay-Locked Loop
DDR	Double Data Rate
DQS	Data Strobe
ESR	Equivalent Series Resistance
FPGA	Field-Programmable Gate Array
GND	Ground
GPIO	General-Purpose Input/Output
HCSL	High-Speed Current Steering Logic
HSUL	High-Speed Unterminated Logic
IBIS	I/O Buffer Information Specification
I/O	Input/Output
INITN	Initialization Pin (Active Low)
JTAG	Joint Test Action Group
LDO	Low-Dropout (regulator)
LPDDR	Low-Power Double Data Rate memory
LVDS	Low-Voltage Differential Signaling
LVSTL	Low-Voltage Swing Terminated Logic
MIB	Memory Interface Block
MIPI	Mobile Industry Processor Interface
MSPI	Controller SPI
OTP	One-Time Programmable
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PLL	Phase-Locked Loop
POR	Power-On Reset
RAM	Random Access Memory
RES_EXT	External Resistor
REXT	External Reference Resistor
RoT	Root of Trust
SCLK	SPI Clock
SERDES	Serializer/Deserializer
SI	Signal Integrity
SLVS	Scalable Low-Voltage Signaling
SPI	Serial Peripheral Interface
SRAM	Static RAM
SSO	Simultaneous Switching Output
SSPI	Target SPI
SSTL	Stub Series-Terminated Logic
subLVDS	sub-Low-Voltage Differential Signaling
TCK	Test Clock
TDI	Test Data In
TDO	Test Data Out

Abbreviation	Definition
TMS	Test Mode Select
USB	Universal Serial Bus
VCC	Voltage Common Collector

1. Introduction

When designing complex hardware with the Lattice Nexus™ 2 device, you must pay close attention to critical hardware configuration requirements. This technical note outlines key implementation considerations specific to the Lattice Nexus 2 device. While it does not provide detailed step-by-step instructions, it offers a high-level checklist to support the design process.

Hardware Checklists are developed after evaluation boards and incorporate optimized designs that improve upon the circuitry of evaluation boards. If you copy circuits from evaluation boards, ensure that you optimize your designs according to the hardware checklists.

- The Lattice Nexus 2 platform comprises Lattice Certus™-N2 and Lattice Mach™-N2 devices. The Lattice Certus-N2 family is a general-purpose FPGA. Optimized for edge compute workloads and featuring fast and flexible I/O (with support for 3.3 V I/O), it features 16G SERDES supporting multiple popular protocols including 10G Ethernet and PCIe® Gen 4.
- The Lattice Mach-N2 family is a control- and security-focused FPGA. In addition to Lattice Certus-N2 device capabilities, it features user run-time security and integrated non-volatile flash memory for configuration and data storage. The Root of Trust (RoT) device in the family extends security features to include Post-quantum cryptography (PQC) and provides secure flash access for user keys, security policies, bitstreams, and user data.

This technical note assumes familiarity with the Lattice Nexus 2 device features as described in the Lattice Nexus 2 Platform - Overview Data Sheet (FPGA-DS-02122) and Lattice Nexus 2 Platform - Specifications Data Sheet (FPGA-DS-02121). These data sheets provide the functional specification for the device, including (but not limited to):

- High-level functional overview
- Pinouts and packaging information
- Signal descriptions
- Device-specific information about peripherals and registers
- Electrical specifications

This technical note addresses the following critical hardware areas. For additional details, refer to the Lattice Nexus 2 Platform - Overview Data Sheet (FPGA-DS-02122) and Lattice Nexus 2 Platform - Specifications Data Sheet (FPGA-DS-02121).

- Power supplies and how to connect them to the PCB and the associated system
- Configuration mode selection for proper power-up behavior
- Device I/O interface and critical signals

Important: Refer to the following documents for detailed recommendations.

- Lattice Nexus 2 sysCONFIG User Guide (FPGA-TN-02370)
- Lattice Nexus 2 sysI/O User Guide (FPGA-TN-02365)
- Lattice Nexus 2 sysCLOCK PLL Design and User Guide (FPGA-TN-02364)
- Lattice Nexus 2 Embedded Memory User Guide (FPGA-TN-02366)
- Lattice Nexus 2 High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02372)
- Lattice Nexus 2 sysDSP User Guide (FPGA-TN-02362)
- Thermal Management (FPGA-TN-02044)
- Electrical Recommendations for Lattice SERDES (FPGA-TN-02077)
- High-Speed PCB Design Considerations (FPGA-TN-02178)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- LatticeSC™ SERDES Jitter (TN1084)
- HSPICE SERDES simulation package – Available under NDA, contact the license administrator at lic_admin@latticesemi.com
- Lattice Nexus 2 Pinout (FPGA-SC-02108)

2. Power Supplies

At power up, the V_{CC}, V_{CCAUX}, V_{CCIO1}, and V_{CCIO2} power supplies are monitored to determine when the Lattice Nexus 2 device should deassert its internal Power-On Reset (POR) state and enter power-good condition, initializing device initialization and configuration. These supplies must ramp up monotonically. Other supplies are not monitored during power-up but must reach a valid stable level before configuration completes.

Table 2.1 lists the required power supplies and their corresponding voltage levels for each supply.

Table 2.1. Supply Rails

Supply Rail	Voltage (Nominal Value)[1]	Description
V_{SS}	—	Ground for internal FPGA logic and I/O
V_{SSR}	—	Connect to ground through a 1.0 kΩ resistor.
V_{CC}, V_{CCJB}	0.82 V	FPGA core power supply. Required for power-good condition. V_{CCJB} on Mach-N2 devices only.
$V_{CCA\_PLL\_W}$, V_{CCA_PLL10}, V_{CCA_PLL4}, V_{CCA_PLL7}	0.82 V	Power supply for PLL blocks.
V_{CCAUX}	1.8 V	Auxiliary power supply. Used for generating stable drive current for the I/O. Required for power-good condition.
V_{CCAUXA}	1.8 V	Auxiliary power supply for internal analog circuitry.
V_{CC_BAT}	1.5 V	Optional power supply to allow a battery to preserve the volatile configuration Battery-Backed RAM (BBRAM) when the other DC supplies are absent.
$V_{CCIO[14:0]}$	Certus-N2 Wide Voltage Range Banks: Bank 1: 3.3 V. Banks 0, 2, 12, 13, 14: 1.2 V, 1.8 V, 2.5 V, 3.3 V. Mach-N2 Wide Voltage Range Banks: Banks 0, 1, 2, 12, 13, 14: 1.2 V, 1.8 V, 2.5 V, 3.3 V. Certus-N2 and Mach-N2 High-Performance Banks: Banks 3, 4, 5, 6, 7, 8, 9, 10, 11: 0.9 V, 1.0 V, 1.1 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V.	I/O driver supply voltage for each bank. Each bank has its own V_{CCIO} supply. V_{CCIO1} and V_{CCIO2} are required for power-good conditions as they are used during configuration.
V_{CCA_MPQx}	0.80 V[2]	Power supply for the SERDES block analog circuitry. Voltage depends on data rate speed. X = 0, 1, 2, 3, 4, 5, 6
V_{CCH_MPQx}	1.5 V[2]	Power supply for the SERDES block digital circuitry. Voltage depends on data rate speed. X = 0, 1, 2, 3, 4, 5, 6

Notes:

1. The Lattice Nexus 2 device includes a power-on-reset (POR) state machine that depends on several monitored power supplies. These supplies must ramp up monotonically. Device initialization does not proceed until all monitored power supplies reach their minimum operating voltages.
2. Protocol performance speeds were achieved with the LFG and CBG packages. Other packages are limited to 10 Gbps.

2.1. Power Noise

FPGA power rails allow a worst-case operating tolerance of ±3% of their nominal voltages. This tolerance includes all noise sources. An exception is the V_{CC_BAT} rail, which supports a wider operating range of 1.0 V to 1.55 V.

2.2. Power Source

It is recommended that the designed voltage regulators are accurate to within 2% of the optimum voltage to allow power noise design margin.

When calculating total voltage regulator tolerance, consider the following:

- Regulator voltage reference tolerance
- Regulator line tolerance
- Regulator load tolerance
- Tolerances of any resistors connected to the regulator feedback pin, which sets the regulator output voltage
- Expected voltage drops due to power filtering ferrite bead ESR × expected current draw
- Expected voltage drops due to the current measuring resistor ESR × expected current draw

With 2% tolerance allocated to the voltage source, the design has a remaining 1% tolerance for noise and layout related issues. The lower voltage rails (< 1.2 V) are especially sensitive to noise (for the 0.82 V rail every 8.2 mV is 1% of the rail voltage). For SERDES power rails, aim for ≤ 0.5% peak noise; for PLLs, target ≤ 0.25% peak noise. The Phase-Locked Loop (PLL) power pins are highly sensitive to noise, which can introduce jitter in the PLL output. Do not connect the PLL power pins directly to the VCC rails used by the core fabric.

2.3. Power Regulator Derating

A standard best practice among power supply designers is to derate a regulator's output current to 85% of its maximum rated limit, ensuring that even transient peak current demands remain below this threshold.

As a design approaches full capacity, performance significantly degrades. Datasheet oscilloscope screenshots often illustrate these penalties; a close examination reveals that operating near maximum current leads to poor load regulation, typically causing an additional 1% to 2% drop in output voltage. It also results in a significant increase in output noise, increased internal voltage drops across the power path, reduced efficiency, and excessive waste heat. In linear regulators, this waste heat increases linearly as the input-to-output voltage differential (Vin – Vout) increases. In switching DC-DC regulators, high current operation introduces specific risks to peripheral passives, including magnetic core saturation in the inductor and ripple-current stress on input/output capacitors.

Maintaining a design margin is critical because maximum datasheet ratings assume an ideal PCB layout with extensive copper thermal pads and thermal via arrays, conditions rarely met in real-world designs. Furthermore, these maximum current specifications assume relatively low ambient temperatures. When operating in confined or hot environments, engineers must consult the datasheet's ambient temperature derating curves, as allowable current capacity drops linearly once a critical thermal threshold is exceeded.

Finally, leaving zero headroom provides no margin for applications that may occasionally demand more current than expected. For example, variations in a customer's supply chain may eventually introduce "Fast-Fast" process corners that exhibit higher peak current draws.

Summary

Select regulators so that the nominal design uses no more than 85% of the device maximum rated current during peak transients. For high-reliability applications demanding an extended operational life, high manufacturing yields, and margin for non-ideal PCB designs/layouts, target a stricter 75% utilization limit.

3. Power Supply Filtering

Providing well-filtered power is essential for all supply rails and especially critical for analog rails. Each supply should be decoupled using appropriate power filters. Bypass capacitors must be placed as close as possible to the device package pins, with minimal trace length to reduce inductance.

For optimal performance, assign pins carefully to avoid placing noisy I/O signals near sensitive functional pins. PCB-related crosstalk often originates from FPGA outputs routed too close to sensitive power supply lines. A careful PCB layout is required to ensure noise immunity, particularly for analog supplies affected by switching noise from FPGA outputs. While this document provides filtering guidelines, robust layout practice is essential to prevent noise coupling into sensitive analog rails.

Extremely low-noise, well-filtered supplies are essential for the Lattice Nexus 2 SERDES, PLLs, and V_{CCAUXA} rail.

3.1. Recommended Power Filtering Groups and Components

Table 3.1. Recommended Power Filtering Groups and Components

Power Input	Recommended Filter	Notes
V_{CC}, V_{CCJB} tied together	22 µF x 2 + 10 µF x 3 + 1.0 µF x 3 + 100 nF per pin	Core and clock logic. High current rail; source using switching regulator. V_{CCJB} on Mach-N2 devices only. 0.82 V
$V_{CCA\_PLL\_W}$, V_{CCA_PLL10}, V_{CCA_PLL4}, V_{CCA_PLL7} tied together	600 Ω FB (ESR ≤ 0.4 Ω) + 1.0 µF x 4 + 100 nF + 0.01 µF	Sensitive PLL supply. Low current; Use LDO regulator for low noise. Tie all listed PLL supplies together. 0.82 V
V_{CCAUX}	120 Ω FB (ESR ≤ 0.1 Ω) + 10 µF x 2 + 1.0 µF + 100 nF per pin	Auxiliary power supply for internal analog circuitry. 1.8 V
V_{CCAUXA}	120 Ω FB (ESR ≤ 0.1 Ω) + 10 µF + 1.0 µF + 100 nF per pin	Sensitive auxiliary power supply for internal analog circuitry. This rail must not be combined with V_{CCAUX}. 1.8 V
V_{CC_BAT}	10 µF + 100 nF	Optional power supply to allow a battery to preserve the volatile configuration RAM (BBRAM) when other DC supplies are absent. If not used the rail pin may be left unconnected. 1.5 V

Power Input	Recommended Filter	Notes
V_{CCIOx}	10 µF + 1.0 µF + 100 nF per pin	Power supply for I/O banks. x = Specific bank number. For unused banks, the 10 µF capacitor may be omitted. For banks with > 15 outputs or high capacitive loads, use 22 µF or an additional 10 µF. Use Lattice SSO tool to verify noise levels. Certus-N2 Wide Voltage Range Banks: Bank 1: 3.3 V. Banks 0, 2, 12, 13, 14: 1.2 V, 1.8 V, 2.5 V, 3.3 V. Mach-N2 Wide Voltage Range Banks: Banks 0, 1, 2, 12, 13, 14: 1.2 V, 1.8 V, 2.5 V, 3.3 V. Certus-N2 and Mach-N2 High-Performance Banks: Banks 3, 4, 5, 6, 7, 8, 9, 10, 11: 0.9 V, 1.0 V, 1.1 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V.
V_{CCA_MPQx}	120 Ω FB + 10 µF x 2 + 1.0 µF x 2 + 100 nF per pin	Power supply for the SERDES block analog circuitry. Voltage depends on data rate speed. X = 0, 1, 2, 3, 4, 5, 6 Separate FB + capacitor filter for each V_{CCA_MPQX}. 0.80 V
V_{CCH_MPQx}	120 Ω FB + 10 µF + 1.0 µF x 2 + 100 nF per pin	Power supply for the SERDES block digital circuitry. Voltage depends on data rate speed. X = 0, 1, 2, 3, 4, 5, 6 Separate FB + capacitor filter for each V_{CCH_MPQX}. 1.50 V

Note:

1. Protocol performance speeds were achieved with the LFG and CBG packages. Other packages are limited to 10 Gbps.

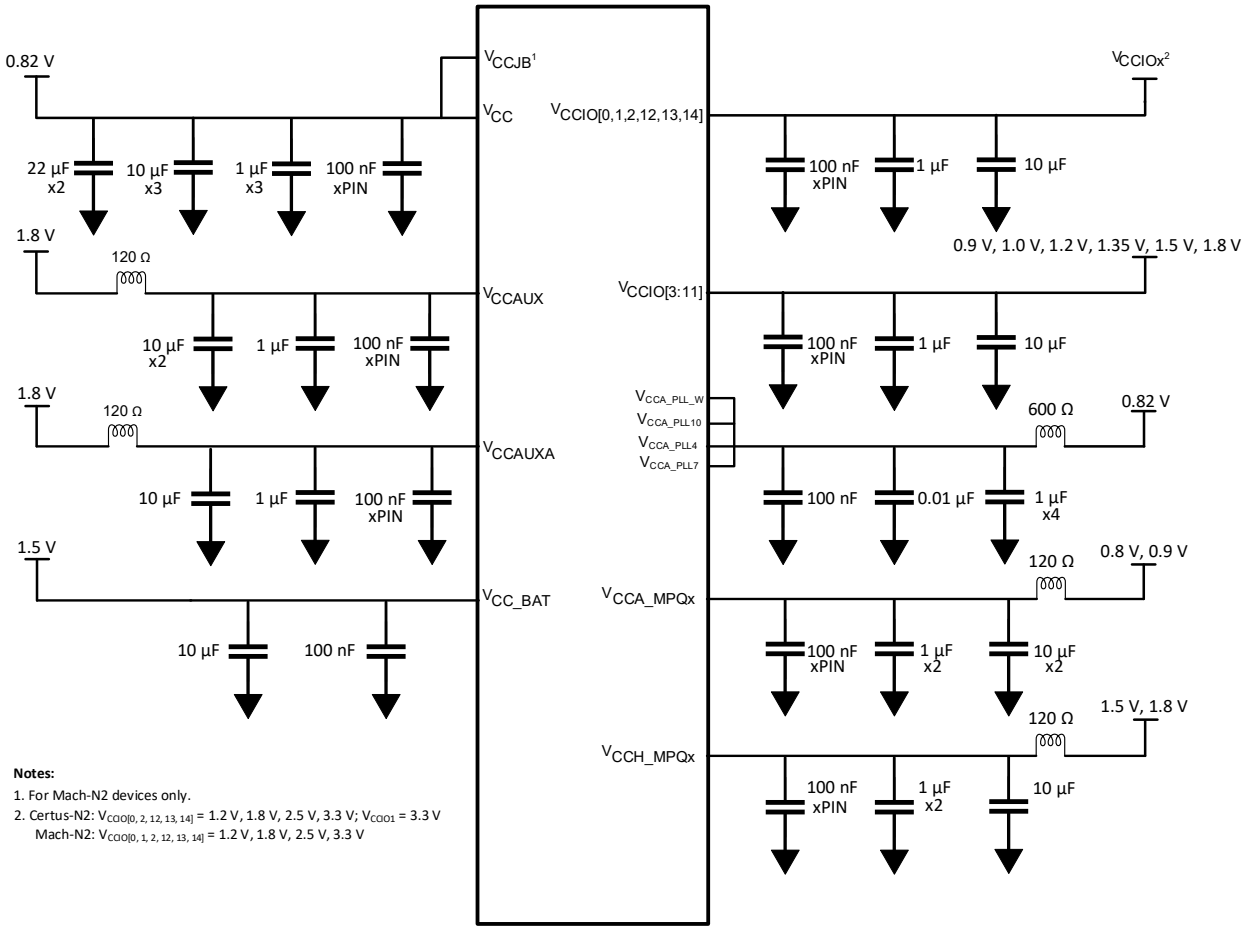

Figure 3.1. Recommended Power Filters

3.2. Ground Pins

All ground pins (V_{SS} and V_{SSR}) need to be connected to the board ground plane.

3.3. EXT_RES pins

- These pins are dedicated to resistor connection to ground or bank V_{CCIO} only.
- Connect 240 Ω ±1% to ground on banks which use LVDS, subLVDS, SLVS, HSUL, POD, and MIPI D-PHY standards.
- Connect 240 Ω ±1% to V_{CCIO} on banks which use LVSTL_I IO standard.
- Connect 180 Ω ±1% to V_{CCIO} on banks which use LVSTL_II IO standard.
- Leave unconnected if the bank is not using one of the above standards.

Refer to the Lattice Nexus 2 High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02372) for more information.

3.4. ERASEKEY

The ERASEKEY pin enables secure erasure of customer keys stored in either One-Time Programmable (OTP) memory or Battery-Backed RAM (BBRAM).

Ground the ERASEKEY pin by default, and when not using the ERASEKEY function. By default, the ERASEKEY pin is disabled. It can be permanently enabled by blowing an OTP fuse. Once enabled, the erase function is initiated by asserting the pin HIGH for at least 350 ms.

Selection of OTP or BBRAM is made using BBRAM_EN fuse:

- **BBRAM_EN=0 (Default)**
  Security processor firmware will trigger a hardware state machine to permanently set all bits to 1s in the OTP memory key space.
- **BBRAM_EN=1**
  Security processor firmware will set all bits to 0s in the BBRAM key space.

3.4.1. ERASEKEY Schematics

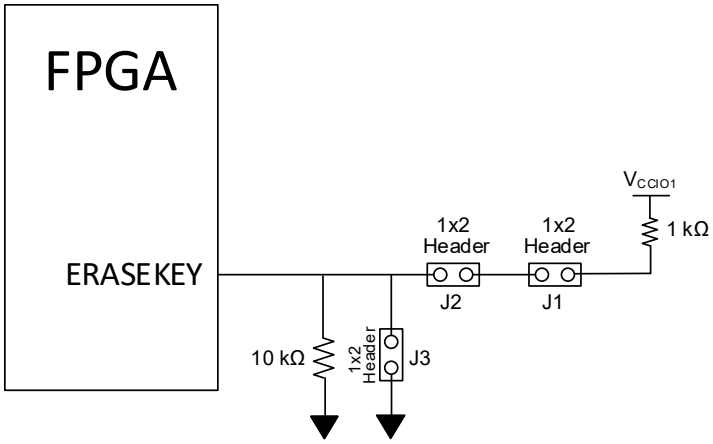

Figure 3.2. ERASEKEY Schematics

Note: J2 and J3 are optional and provide additional protection against accidental ERASEKEY activation.

Default configuration (ERASEKEY pin grounded)

- J1: OPEN
- J2: OPEN
- J3: INSTALLED

To activate ERASEKEY, the ERASEKEY pin must be held high for ≥ 350 ms.

Activation configuration (pin held high ≥ 350 ms)

- J1: INSTALLED
- J2: INSTALLED
- J3: OPEN

After activation, set to default configuration (ERASEKEY pin grounded)

- J1: OPEN
- J2: OPEN
- J3: INSTALLED

3.5. Unused GPIO Pins

Leave all unused GPIO pins open.
It is recommended to connect a few unused GPIOs to test points to facilitate debugging and bring-up rework.

3.6. Unused Banks (V_{CCIOx})

Connect unused V_{CCIOx} pins to a power rail; do not leave them unconnected.
It is recommended to bypass unused bank rail pins with a single 1.0 µF or 100 nF capacitor.

3.7. Unused SERDES Quads (V_{CCH_MPQx} and V_{CCA_MPQx})

For unused SERDES quads, ground the following pins:

- Power pins VCCH_MPQx and VCCA_MPQx.
- Differential input pairs MPQx_RXP/N.
- Clock reference pins MPQx_REFCLKP/N.
- External reference resistor input REXT_MPQx (use 200 Ω).
- Leave differential outputs MPQx_TXP/N, unconnected.

3.8. Clock Oscillator Supply Filtering

When using an external reference clock (single-ended or differential), ensure the oscillator power supply is properly isolated and decoupled. A typical bypassing circuit is shown in Figure 3.3.

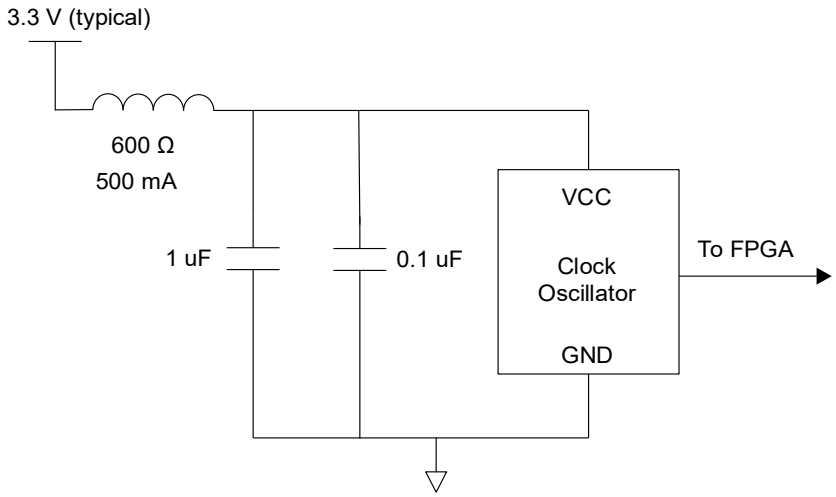

Figure 3.3. Clock Oscillator Bypassing

4. Power

4.1. Power Sequencing

The Lattice Nexus 2 device does not require a specific power rail sequence for either power-up or power-down.

4.2. Power Supply Ramp Rates

Table 4.1. Power Supply Ramp Rates

Symbol	Parameter	Min	Typ	Max	Unit
t_{RAMP}	Power Supply ramp rates for all supplies, non V_{CCIO}[1]	0.1	—	V/0.2	V/ms
$t_{RAMP\_VCCIOCFG}$	Power Supply ramp rate for V_{CCIO1}	1	—	20	V/ms
t_{RAMPIO}	Power Supply ramp rates for all V_{CCIO} supplies[1] except V_{CCIO1}	0.1	—	20	V/ms

Note:

1. Assumes monotonic ramp rates.

4.3. Power Estimation

After selecting the Lattice Nexus 2 device density, package, and logic implementation, estimate the power consumption of the system environment using the power calculator included in the Lattice Radiant™ design tool. When estimating power, consider the following key objectives:

- Ensure power supply capacity accounts for the highest of the following: power-up in-rush current, configuration current, and maximum DC/AC operating current under expected system environmental conditions.
- Confirm that the system environment and the package can maintain the device junction temperature within the specified maximum operating limit.

Addressing these two criteria early in the design phase ensures accurate power budgeting and thermal planning for the Lattice Nexus 2 device.

5. Component Selection

5.1. Ferrite Bead Selection

- Most designs perform well with ferrite beads rated between 120 Ω and 240 Ω at 100 MHz .
- The noise voltage caused by ferrite bead ESR × current should remain below 0.5% of the rail voltage for non-analog rails, and below 0.25% for sensitive analog rails .
- For non-PLL rails, select ferrite beads with ESR between 0.01 Ω and 0.10 Ω based on the expected current load .
- PLL rails draw low current, which allows ferrite beads with ESR ≤ 0.40 Ω.
- Smaller package ferrite beads typically exhibit higher ESR than larger packages of the same impedance rating.
- Within the same package size, higher impedance ferrite beads generally have higher ESR than low impedance ones.

5.2. Capacitor Selection

When specifying components, choose good-quality ceramic capacitors in small packages and place them close to the power oscillator supply pins with short, low-inductance connections. Good quality capacitors for bypassing generally meet the requirements discussed in the following sections.

5.2.1. Capacitor Dielectric

Use stable dielectric types such as X5R, X7R, and similar, which maintain capacitance within ±20% across the operating temperature range. Avoid dielectrics like Y5V, Z5U, and similar, which exhibit poor capacitance.

5.2.2. Voltage Rating

Capacitor working capacitance decreases nonlinearly with a higher voltage bias. To maintain capacitance, the capacitor voltage rating should be at least double the rail voltage. Example: 1.8 V rail bypass capacitors can use the commonly available 6.3 V rating as a minimum. For automotive and aerospace applications, the capacitor voltage rating should be at least triple the rail voltage.

Smaller body capacitors have lower inductance, work at higher frequencies, and improve board layout. For a given voltage rating, smaller body capacitors tend to cost more than larger body capacitors. Optimizing the difference between market pricing and size-related inductance, the following capacitor sizes are recommended:

Table 5.1. Recommended Capacitor Sizes

Capacitance	Size Preferred	Size Next Best
0.1 µF	0201	0402
1.0 µF	0201	0402
2.2 µF	0402	0201
4.7 µF	0402	0603
10 µF	0402	0603
22 µF	0805	0603

5.2.3. Mounting Location

Place the 0.1 µF capacitors as close as possible to the Lattice Nexus 2 FPGA associated power rail pins. Using 0201-sized 0.1 µF capacitors enables placement on the PCB underside, between via holes beneath the FPGA ball pads.

6. Clock Inputs

The Lattice Nexus 2 device designates certain pins in each I/O bank for use as clock inputs. These pins are shared and may also function as general-purpose I/O.

When using these pins for clock input, it is critical to minimize signal noise to ensure reliable clock performance. Refer to the Lattice Nexus 2 High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02372).

These shared clock input pins, typically named GPLL and PCLK, are listed under the *Dual Function* column in the device *pinlist .csv* file. For high-speed differential interfaces (such as MIPI), route the differential clock pair to dedicated differential clock input pins labeled *PCLKTx_y* (+true) or *PCLKRTx_y* (+true) and *PCLKCx_y* (-complement) or *PCLKRCx_y* (-complement). For single-ended I/Os, use only *PCLKT* or *PCLKRT* pins as primary CLK pads.

Dedicated PLL reference clock input pins have lower jitter connections to PLLs than PCLK pins.

Ensure that the output voltage of any external reference oscillator does not exceed the V_{CCIO} voltage of the target I/O bank. For banks operating at $V_{CCIO} \leq 1.5$ V, use an HCSL oscillator to ensure the clock signal remains within the bank voltage limit. Alternatively, an LVDS oscillator may be used if AC-coupled and DC-biased to half the V_{CCIO} voltage. Figure 6.1. illustrates a dual-footprint PCB layout that supports both HCSL and LVDS oscillators.

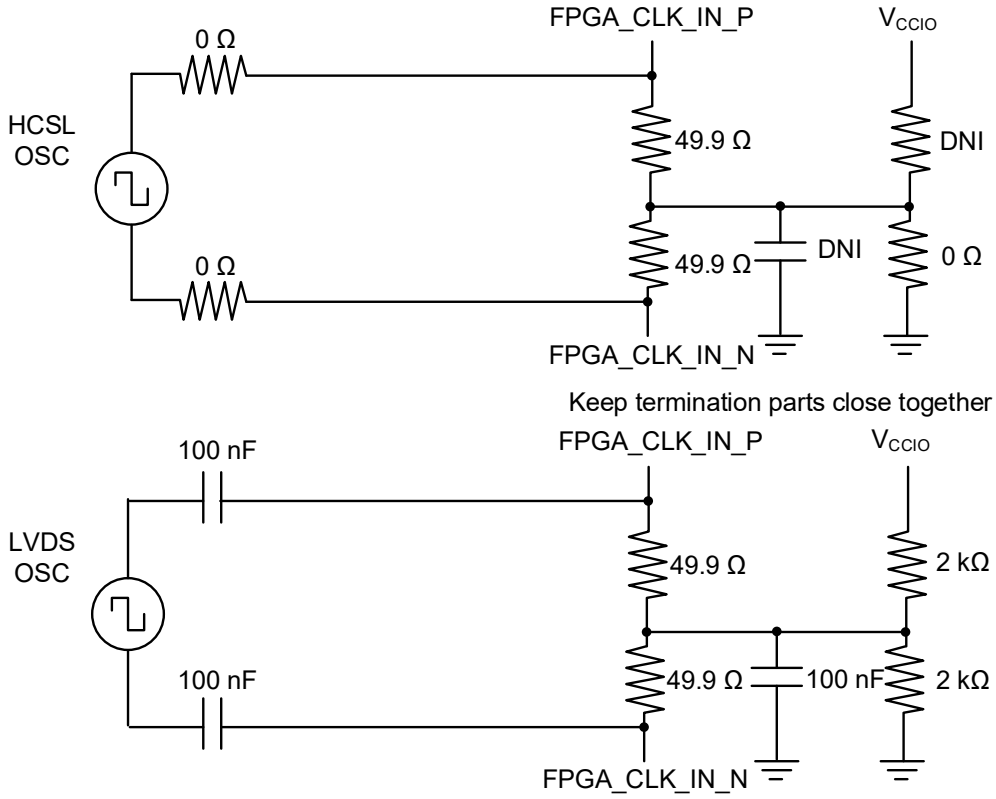

Figure 6.1. PCB Dual Footprint Supporting HCSL and LVDS Oscillators

7. Configuration Considerations

7.1. JTAG

The Lattice Nexus 2 device supports configuration through the JTAG interface as well as through various sysCONFIG modes. The JTAG interface uses a 4-pin connection and requires specific PCB design considerations, detailed in Table 7.1.

Table 7.1. JTAG Pin Recommendations

JTAG Pin	PCB Recommendation
CFGMODE	2.0 kΩ pull-down to GND to enable JTAG Configuration
TCK	2.2 kΩ pull-down to GND
TMS	10 kΩ or 4.7 kΩ pull-up to V_{CCIO2}
TDI	10 kΩ or 4.7 kΩ pull-up to V_{CCIO2}
TDO	10 kΩ or 4.7 kΩ pull-up to V_{CCIO2}

The JTAG port enables debugging in the final system. It is recommended that all PCBs provide accessible JTAG pins, even if JTAG is not the primary configuration method. For best results, route the VCCIO2, TCK, TDI, TDO, TMS, CFGMODE, PROGRAMN, INITN, DONE, GND signals to a common test header.

JTAG Pull Resistors

Active JTAG lines use push-pull drivers and do not rely on pull-ups to set a high logic level. Pull resistors are only necessary when the JTAG interface is disconnected or tri-stated. They prevent inputs from floating and oscillating, which avoids excessive power draw and accidental TAP controller activation.

Either standard 10 kΩ or 4.7 kΩ resistors are ideal for TMS and TDI. For tight layouts with high crosstalk, 4.7 kΩ is preferred over 10 kΩ due to better noise immunity.

A lower-value 2.2 kΩ pull-down resistor on TCK is recommended to increase crosstalk immunity to the sensitive clock line.

A pull-up resistor on TDO is optional due to TDO typically connecting to another TDI in a chain or to the TDI of the JTAG controller, each of which should include a pull-up resistor on its input.

JTAG Signal Integrity

For best signal integrity, it is recommended to add a source series termination resistor close to the driver of TDO (and TCK if buffered on the PCB). Tune the combined output impedance of the driver plus resistor to equal the characteristic impedance of the transmission line (PCB or wires). Often a value from 22Ω to 33Ω works well.

The layout should feature extra spacing on each side of the TCK signal to reduce crosstalk into this sensitive net; the distance from the edge of the TCK trace to any adjacent trace should be at least three times the width of the TCK trace.

7.2. SPI Configuration

The Lattice Nexus 2 device supports configuration through both Controller (MSPI) and Target (SSPI) SPI interfaces.

The pins listed in Table 7.2 have internal weak pull resistors, pull-up resistors to the appropriate bank V_{CCIO} and pull-down resistors to board ground. It is recommended to provide external pull resistors as indicated on the table.

Table 7.2. Pull-up/Pull-down Recommendations for Configuration Pins

Pin	PCB Connection
PROGRAMN	10 kΩ or 4.7 kΩ pull-up to V_{CCIO2}
INITN	10 kΩ or 4.7 kΩ pull-up to V_{CCIO2}
DONE	10 kΩ or 4.7 kΩ pull-up to V_{CCIO2}
CFGMODE	10.0 kΩ or 4.7 kΩ pull-up to V_{CCIO2} for MSPI configuration 2.0 kΩ pull-down to GND for SSPI or JTAG configuration
MCSN	10 kΩ or 4.7 kΩ pull-up to V_{CCIO1}
MCLK	1.0 kΩ pull-down to GND (Not installed by default) 1.0 kΩ pull-up to V_{CCIO1} (Not installed by default) Series resistor placed near TX side[1]
MDQ0/MOSI	10 kΩ or 4.7 kΩ pull-up to V_{CCIO1} (Not installed by default)
MDQ1/MISO	10 kΩ or 4.7 kΩ pull-up to V_{CCIO1} (Not installed by default)
MDQ2–MDQ7	10 kΩ or 4.7 kΩ pull-up to V_{CCIO1} (Not installed by default)
MDS	MSPI octal mode data strobe, 10 kΩ pull-down to GND (Not installed by default)
MRSTN	10 kΩ or 4.7 kΩ pull-up to V_{CCIO1}. Connect to an external flash device with a dedicated reset pin.
SCSN	10 kΩ or 4.7 kΩ pull-up to V_{CCIO2}
SCLK	1.0 kΩ pull-down to GND (Not installed by default) 1.0 kΩ pull-up to V_{CCIO2} (Not installed by default)
SDQ0/MOSI	10 kΩ or 4.7 kΩ pull-up to V_{CCIO2} (Not installed by default)
SDQ1/MISO	10 kΩ or 4.7 kΩ pull-up to V_{CCIO2} (Not installed by default)
SDQ2–SDQ7	10 kΩ or 4.7 kΩ pull-up to V_{CCIO2} (Not installed by default)
SDS	SSPI octal mode data strobe, 10 kΩ pull-down to GND (Not installed by default)

Note:

1. Series resistor value depends on the PCB design. It ranges from 0 Ω (PCB impedance: 50 Ω) to 10 Ω (PCB impedance: 60 Ω).

7.3. Configuration Pins per Programming Mode

Table 7.3 summarizes the required signal pins for each supported configuration-programming mode.

Table 7.3. Configuration Pins Needed per Programming Mode

Configuration Mode	Bank	Enablement	Clock		Bus Size	Pins
			Pin	I/O		
JTAG[1]	2	CFGMODE pin Low	TCLK	Input	1	TCK, TMS, TDI, TDO
MSPI	1	CFGMODE pin High	MCLK	Output	1	MCLK, MCSN, MOSI, MISO
					2	MCLK, MCSN, MD0, MD1
					4	MCLK, MCSN, MD0, MD1, MD2, MD3
					8	MCLK, MCSN, MDS, MD0, MD1, MD2, MD3, MD4, MD5, MD6, MD7
SSPI	1	CFGMODE pin Low	SCLK	Input	1	SCLK, SCSN, SI, SO
					2	SCLK, SCSN, SD0, SD1
					4	SCLK, SCSN, SD0, SD1, SD2, SD3
					8	SCLK, SCSN, SDS, SD0, SD1, SD2, SD3, SD4, SD5, SD6, SD7

Note:

1. The JTAG port takes precedence over SSPI.

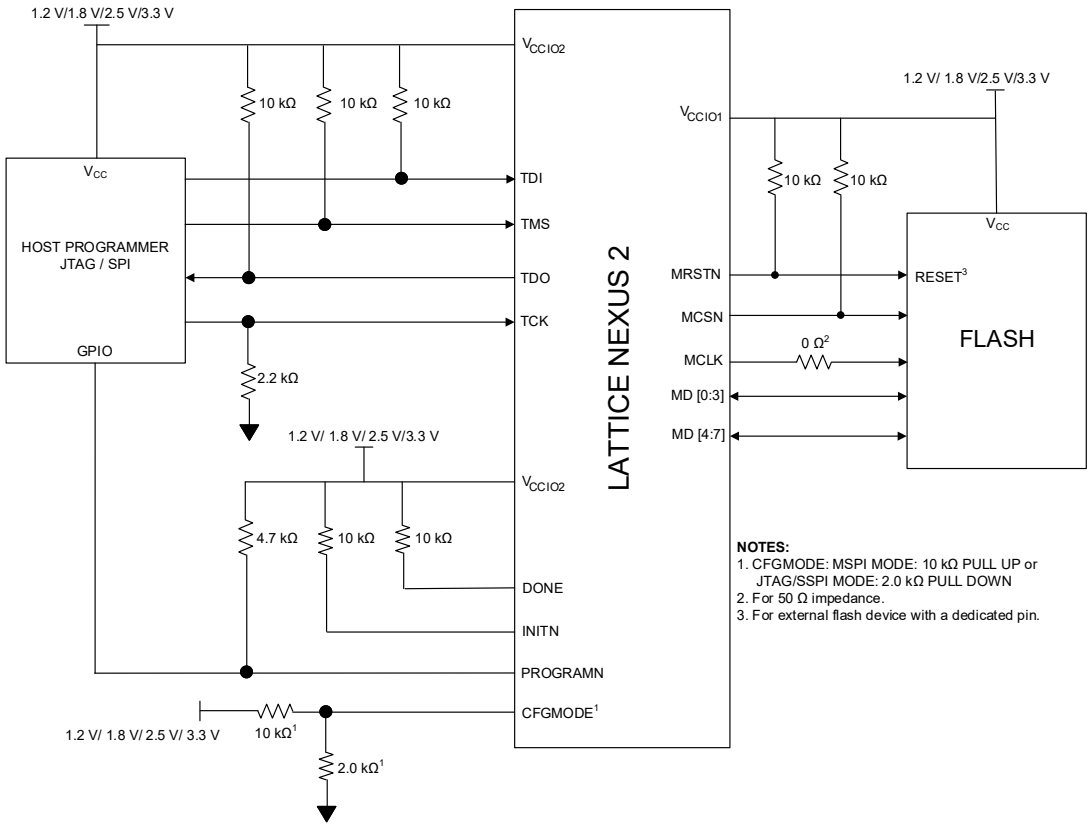

Figure 7.1. Typical Connections for Programming SRAM or External Flash through JTAG

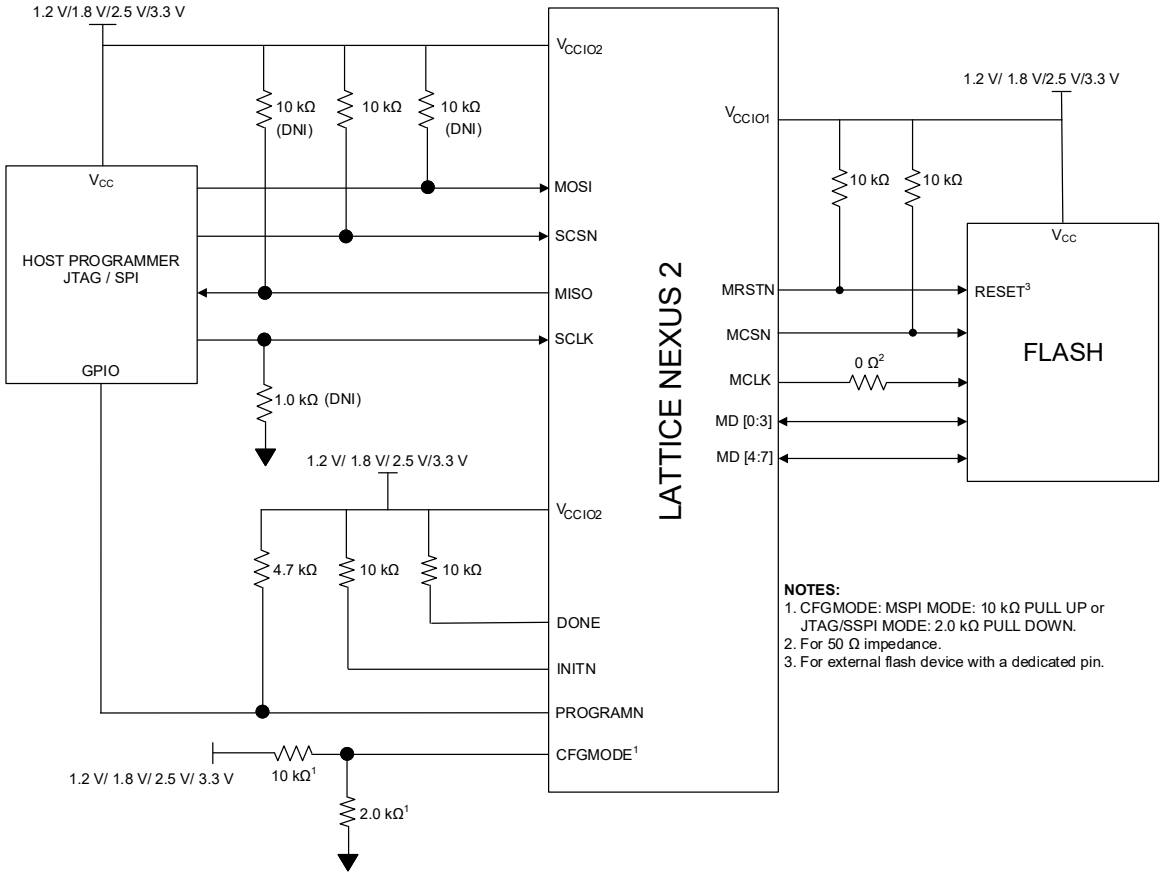

Figure 7.2. Typical Connections for Programming SRAM or External Flash through Target SPI

8. External SPI FLASH

The SPI flash device voltage must match the V_{CCIO1} voltage level.

It is recommended to use an SPI flash device that is supported by the Lattice Radiant Programmer. To view the list of supported devices, open the Lattice Radiant Programmer, navigate to the **Help** menu, and search for **SPI Flash support**.

If your SPI flash device is not listed, you may still be able to use it by configuring the **Custom Flash** option in the Radiant Programmer.

9. I/O Pin Assignments

While the Lattice Nexus 2 device packages help reduce crosstalk coupling, PCB layout can still introduce significant noise due to closely spaced I/O pins and parallel trace routing over long distances. For optimal jitter performance, assign noisy I/O pins away from sensitive power rails such as those for PLL and SERDES. Use a PCB crosstalk or signal integrity simulation tool to evaluate and refine potentially problematic trace layouts.

Refer to the PCB Layout Recommendations for BGA Packages (FPGA-TN-02024) for layout and breakout guidance.

Designers typically select FPGA pinouts early in the design cycle, which requires careful planning. For the FPGA designer, this requires detailed knowledge of the targeted FPGA device. Designers often use a spreadsheet program to initially capture the list of the design I/O. Lattice Semiconductor provides detailed pinout information that can be downloaded from the Lattice Semiconductor website in .csv format for designers to use as a resource to create pinout information. For example, by navigating to the pinout.csv file, you can gather the details for all the different package offerings of the device in the family, including I/O banking, differential pairing, Dual Function of the pins, and input and output details.

9.1. Early I/O Release

The Lattice Nexus 2 device supports an Early I/O release feature, enabling I/Os to assume predefined drive states early during the bitstream processing. The Early I/O release feature releases the I/O after processing the I/O configuration which is located near the head of the bitstream data. Once data is programmed in the left/right Memory Interface Block (MIB) the I/O is released to a predefined state. Enable this feature by setting EARLY_IO_RELEASE to ON in the Lattice Radiant Device Constraint Editor.

9.2. Series Termination Resistors

When using series termination resistors, locate the resistors close to the transmitting pins.

Configuration pins to external devices (such as SPI FLASH) default to 50RS (50 Ω) drive strength. For these pins, start with a value of 0 Ω for PCB impedance of 50 Ω. For higher PCB impedances increase the series termination resistance, for example 10 Ω for PCB impedance of 60 Ω.

Optimum series termination resistance value for user mode output pins depends on the PCB etch impedance and selected output drive strength. Use IBIS models to simulate and determine the optimal starting resistance value. Further, test with oscilloscope and optimize the series termination resistance of critical signals for best signal integrity.

9.3. External Pull Resistor Maximum Values (5% Tolerance)

Table 9.1 lists the maximum standard resistance values required to guarantee a valid logic level. These limits account for worst-case input leakage current when internal GPIO pull resistors are disabled.

Table 9.1. Maximum External Pull Resistance (5% Tolerance, Internal Pulls Disabled)

V_{CCIO}	Standard 5% Resistor Value
0.9 V	20 kΩ
1.0 V	22 kΩ
1.2 V	27 kΩ
1.5 V	33 kΩ
1.8 V	39 kΩ
2.5 V	56 kΩ
3.3 V	75 kΩ

Table 9.2 lists the maximum standard resistance values required to override a default internal pull resistor of the opposite polarity. For example, during configuration, an external pull-down resistor can override a default internal pull-up resistor to force a valid logic low level.

Table 9.2. Maximum External Pull Resistance to Override Opposite Internal Pulls (5% Tolerance)

V_{CCIO}	Standard 5% Resistor Value
0.9 V	1.2 kΩ
1.0 V	1.3 kΩ
1.2 V	1.6 kΩ
1.5 V	2.0 kΩ
1.8 V	2.4 kΩ
2.5 V	3.3 kΩ
3.3 V	4.7 kΩ

10. Functional Blocks Rule-Based Pinout Considerations

The Lattice Nexus 2 devices support a wide-range of high-speed interfaces, each with specific rule-based pinout requirement that must be considered during PCB design. Pinout selection should be guided by a clear understanding of the FPGA internal interface building blocks. These include I/O LOGIC blocks such as soft MIPI, clock resource connectivity, and PLL usage. Refer to the Lattice Nexus 2 High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02372) for rules pertaining to these interface types.

10.1. LVDS, MIPI, and Differential Pair Assignments

True LVDS and MIPI signaling inputs and outputs are available on the bottom I/O pins of the FPGA device (High-Performance banks 3–11). Differential input pairing under the High-Speed column in the *pinlist .csv* file.

- The *positive signal* of a differential pair should connect to an I/O ending in **A** (such as, HPIOx_yA).
- The *negative signal* of a differential pair should connect to an I/O ending in **B** (such as, HPIOx_yB).

The wide-range banks (0, 1, 2, 12, 13, 14) on the top-side I/O banks do not support true LVDS or MIPI standards, but can emulate LVDS outputs using external termination resistors. For implementation details, refer to the Lattice Nexus 2 sysI/O User Guide (FPGA-TN-02365).

- Set the bank voltage to 1.8 V to support LVDS.
- Set the bank voltage to 1.2 V to support MIPI.

10.2. HSUL and SSTL Pin Assignments

The HSUL and SSTL interfaces are referenced to I/O standards that require an external reference voltage (V_{REF}). These standards are supported only on the bottom-side high-performance banks (3–11).

- The V_{REF} pin(s) should be prioritized during PCB pin assignment.
- These pins are labeled V_{REF} in the *Dual Function* column of the *pinlist .csv* file.
- Each bank has its own V_{REF} voltage, which sets the threshold for the referenced input buffers.
- Each I/O is individually configurable based on the bank's supply and reference voltages.

10.3. LVSTL I and LVSTL II Pin Assignments

The LVSTL I and LVSTL II interfaces require an external reference resistor and are supported only on the device bottom-side high-performance banks (3 – 11).

- These pins are labeled RES_EXT in the *Dual Function* column of the *pinlist .csv* file.
- Each bank has a separate RES_EXT voltage.
- Refer to the EXT_RES pins subsection for resistor values and implementations details.
- For pinout and grouping requirements of memory-mapped interfaces, see the Lattice Nexus 2 High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02372).

10.4. SERDES Pin Considerations

High-speed signaling requires meticulous PCB design to maintain proper transmission line characteristics.

- Ensure a continuous ground reference is maintained along high-speed signal paths.
- Differential pairs must be tightly length-matched, with a maximum mismatched of ±4 mil (±0.1 mm).
- Minimize discontinuities such as vias in high-speed routes.

For detailed guidance, refer to the High-Speed PCB Design Considerations (FPGA-TN-02178).

11. Layout Recommendations

A good schematic design should be reflected in a good layout to ensure proper noise and power distribution. Below are some of the recommended layouts in general.

1. All power must come from power planes to ensure reliable power delivery and thermal stability.
2. Each power pin should have its own decoupling capacitor, typically 100 nF, placed as close as possible to the pin.
3. Place analog circuits away from digital circuits and high-switching components.
4. High-speed signals should maintain a clearance of five times the trace width from other signals.
5. High-speed signals transitioning between layers should include a corresponding ground via if both reference planes are ground. If the reference plane is VCC, use a stitching capacitor between ground and V_{CC}.

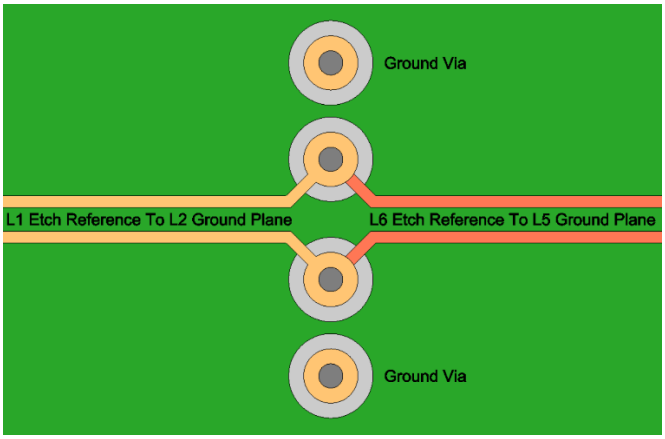

Figure 11.1. Ground Vias Implementation

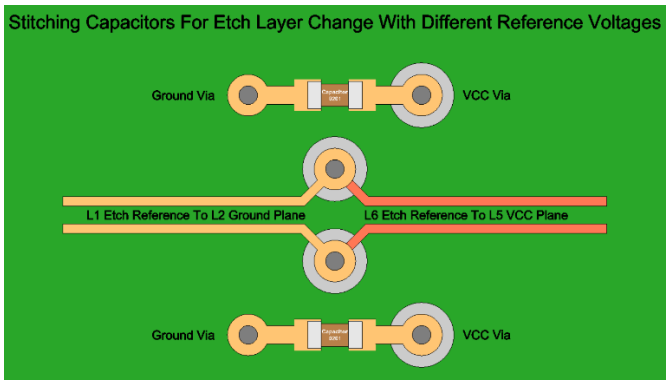

Figure 11.2. Stitching Vias Implementation

6. High-speed signals have specific impedance requirements. Calculate the necessary trace width and differential gap based on the stack-up, and verify dimensions with the PCB vendor.
7. For differential pairs, match trace lengths as closely as possible—ideally within ±5 mils.

For further information on layout recommendations, refer to:

- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)

12. Simulation and Board Measurement of Critical Signals

To ensure design reliability and high manufacturing yield, critical signals should be simulated during the design phase and then measured on the PCB assembly to verify proper function.

12.1. Critical Signals

Signals sensitive to signal integrity (SI) degradation are considered critical and require additional design and verification attention.

Typical critical signals include:

- Differential pairs (LVDS, subLVDS, SLVS, MIPI, USB, and similar interfaces.)
- Clocks (oscillator inputs, output clocks)
- Data with embedded clocks
- Interrupts (edge-triggered)
- Logic signals traveling long distances requiring termination

12.2. Simulation

Lattice Semiconductor provides an IBIS (I/O Buffer Information Specification) file for use with simulation tools. Popular simulation tools include:

- HyperLynx
- Sigrity
- SpectraQuest
- Micro-Cap (Free)

Most SI simulation tools are expensive and often require a recurring subscription fee. The expensive tools can import board design files and can easily supply accurate simulations which include crosstalk and other SI degrading effects.

Free IBIS tools (such as Micro-Cap) can provide basic simulations, but require additional effort to model SI effects across multiple signals with varying transmission line lengths, lossy lines, and crosstalk.

Use simulation results to optimize each critical signal for signal integrity:

- Set output pin drive strength
- Set output pin slew rate
- Design the output pin termination (such as output series termination resistor value)
- Configure internal pin pull-up and pull-down resistors
- Refine PCB layout.

12.3. Board Measurements

Measure critical signals on the assembled PCB using an oscilloscope. Verify proper signal function and integrity (that is, eye diagram, SI parameters).

Use measurement results to optimize each critical signal for signal integrity:

- Adjust output pin drive strength
- Adjust output pin slew rate
- Modify output pin termination design (such as output series termination resistor value).
- Configure internal pin pull-up and pull-down resistors.

Specification compliance testing is recommended for common signaling standards (such as USB, MIPI).

13. SSO (Simultaneous Switching Output) Design Check

Users should verify designs to ensure they do not experience functional failures due to SSO voltage drops (sometimes called SSO noise, ground bounce, or power bounce).

SSO voltage drops result from package inductance combined with dynamic switching current which causes Ldi/dt voltage drops.

The Lattice SSO tool should be used to estimate SSO voltage drop.

13.1. SSO Failures – Each of the following can lead to SSO failures

1. Many simultaneous switching outputs in the same I/O bank. The more outputs that switch simultaneously, the greater the ***di*** current, and consequently, the greater the Ldi/dt voltage drops.
2. I/O slew rates set to FAST (and sometimes MEDIUM). Faster slew rates reduce the ***dt*** time and thus increase Ldi/dt voltage drops.
3. I/O output current set high (for example, 8–16 mA). Higher I/O output current increases the ***di*** current and, therefore, the Ldi/dt voltage drops.
4. I/O capacitive loading is relatively high (especially > 15 pF). High capacitance loading increases the ***di*** current and, therefore, the Ldi/dt voltage drops.
5. I/O banks with low voltage rails (for example LVCMOS 1.0 V – LVCMOS 1.5 V) have smaller voltage margins and are more susceptible to Ldi/dt ground and power violations.

13.2. SSO Mitigations

1. Split up simultaneous switching outputs across multiple banks (where timing permits). Fewer simultaneous outputs per bank reduce the ***di*** current and, therefore, the Ldi/dt voltage drops.
2. Reduce I/O slew rates to MEDIUM or preferably SLOW, if timing allows. Increasing slew time increases ***dt*** and reduces Ldi/dt voltage drops.
3. Reduce I/O output current (for example 4 mA), where timing and signal quality permit. Lower output current reduces di current and, therefore, Ldi/dt voltage drops.
4. Reduce I/O capacitive loading (this typically requires PCB design changes). Lower capacitance reduces di current and, therefore, Ldi/dt voltage drops.
5. Increase I/O bank voltage rails (this often requires PCB design changes). If the above mitigations are insufficient, increasing bank voltage can improve absolute voltage margins and ensure enough design margin for reliable operation.

14. Checklist

Table 14.1. Hardware Checklist

	Item	OK	NA
1	**FPGA Power Supplies**		
1.1	System supplies		
1.1.1	Voltage rails have ±3% tolerance. Use voltage regulator ≤ ±2% tolerance to allow for ±1% power noise.		
1.1.2	Follow Table 3.1 for proper decoupling of each power rail.		
1.1.3	V_{CC}, V_{CCJB} (Mach-N2 devices only), and V_{CCA_PLLx} at 0.82 V ±3%		
1.1.4	Use a PCB plane for V_{CC} core with proper decoupling.		
1.1.5	V_{CC} core sized to meet power requirement calculation from software.		
1.1.6	V_{CCCLK}, V_{CCHP}, V_{CCA_PLLx} must be quiet and isolated from other switching noise and each other.		
1.1.7	V_{CCAUX} and V_{CCAUXA} at 1.8 V ±3%.		
1.1.8	V_{CCAUX} and V_{CCAUXA} must be quiet and isolated from other switching noise and each other.		
1.1.9	V_{CCAUX} pins should be tied together, and a solid PCB plane is recommended.		
1.1.10	V_{CCAUXA} pins are sensitive and should be filtered separately from V_{CCAUX} pins.		
1.1.11	V_{CC_BAT} pin at 1.5 V +3%/-33%; if not used, leave the pin open.		
1.2	I/O supplies		
1.2.1	Certus-N2 wide-range V_{CCIO} Bank 1: 3.3 V. Banks 0, 2, 12, 13, 14: 1.2 V, 1.8 V, 2.5 V, 3.3 V.		
1.2.2	Mach-N2 wide-range V_{CCIO} Banks 0, 1, 2, 12, 13, 14: 1.2 V, 1.8 V, 2.5 V, 3.3 V.		
1.2.3	All high-performance banks (3–11) V_{CCIOx} voltages: 0.9 V, 1.0 V, 1.1 V, 1.2 V, 1.35 V, 1.5 V, or 1.8 V.		
1.2.4	V_{CCH_MPQx} pins must be quiet and isolated from other switching noise.		
1.3	SERDES power supplies		
1.3.1	V_{CCA_MPQx} pin: 0.80 V		
1.3.2	V_{CCA_MPQx} pins must be quiet and isolated from other switching noise.		
1.3.3	V_{CCH_MPQx} pin: 1.5 V		
1.4	Grounds		
1.4.1	All V_{SS} and V_{SSR} ground pins must be connected to a dedicated low-impedance ground plane.		
1.5	Unused blocks		
1.5.1	Connect unused V_{CCIOx} pins to a power rail. Do not leave them open. It is recommended to bypass unused rail pins with a 100 nF capacitor.		
1.5.2	Connect unused quads V_{CCH_MPQx} and V_{CCA_MPQx} pins to ground. Also, tie reference pins $M_{PQx\_REFCLKP}$ and $M_{PQx\_REFCLKN}$ to ground.		
1.6	Power sequencing is not required.		
2	**JTAG**		
2.1	CFGMODE pin pulled high with a 10 kΩ or 4.7 kΩ resistor or low using a 2.0 kΩ resistor per Table 7.1.		
2.2	Keep CFGMODE accessible on the PCB to recover the JTAG port, especially during development.		
2.3	Keep JTAG port pins accessible on the PCB, especially during development.		
2.3.1	JTAG header: V_{CCIO2}, TCK, TDI, TDO, TMS, CFGMODE, PROGRAMN, INITN, DONE, and GND.		
2.4	Apply a pull-down resistor on TCK, as specified in Table 7.1.		
2.5	Apply a pull-up resistor on TMS, TDI, and TDO, as specified in Table 7.1.		

	Item	OK	NA
3	**MSPI and SSPI Configuration**		
3.1	V_{CCIO1}, V_{CCIO2} bank voltages must match the sysCONFIG peripheral devices (for example, SPI flash, external connections).		
3.2	CFGMODE pin Apply a 10 kΩ or 4.7 kΩ pull-up resistor to V_{CCIO2} for MSPI configuration. Apply a 2.0 kΩ pull-down resistor to GND for SSPI configuration.		
3.3	Apply a pull-up or pull-down resistors to persisted configuration specific pins as specified Table 7.1 and Table 7.2.		
4	**External Flash**		
4.1	The external flash voltage must match V_{CCIO1} voltage.		
5	**Special Pin Assignments**		
5.1	Pinout is chosen to address FPGA resource connections to I/O logic and clock resources per Lattice Nexus 2 High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02372).		
5.2	Shared general-purpose I/O are used as inputs for FPGA PLLs and clock input signals.		
5.3	Bank V_{CCIOX} voltage.		
5.3.1	Set the bank voltage to 1.8 V to support LVDS signaling.		
5.3.2	Set the bank voltage to 1.2 V to support MIPI signaling.		
5.4	Referenced I/O standards.		
5.4.1	HSUL and SSTL are supported on the device bottom banks only (high-performance banks 3–11).		
5.4.2	Decouple the V_{REF} pin using a 0.1 µF capacitor.		
5.5	Termination impedance: Rext[1] resistor.		
5.5.1	LVSTL I require a 240 Ω ±1% resistor from Rext[1] to V_{CCIOX} for proper termination impedances.		
5.5.2	LVSTL II requires a 180 Ω ±1% resistor from Rext[1] to V_{CCIOX} for proper termination impedances.		
5.5.3	For POD or SSTL I/O standards, connect a 240 Ω ±1% resistor from Rext[1] to ground.		
5.5.4	For non-memory I/O standards, leave open.		
6	**Clock Inputs**		
6.1	High-speed differential interfaces (such as MIPI), when received by the FPGA, must route their differential clock pair into a pair of inputs that support differential clocking, labeled *PCLKTx_y* (+true) or *PCLKRTx_y* (+true) and *PCLKCx_y* (-complement) or *PCLKRCx_y* (-complement).		
6.2	For single-ended I/Os, use only *PCLKT* or *PCLKRT* pins as primary CLK pads.		
6.3	When providing an external reference clock to the FPGA, ensure that the oscillator output voltage does not exceed the bank voltage.		
6.4	For banks with $V_{CCIO} \leq 1.5$ V, it is recommended to use an HCSL oscillator to keep the clock voltage less than or equal to the bank V_{CCIO}. An LVDS oscillator may also be used if AC-coupled and then DC-biased at half the V_{CCIO}. See Figure 6.1.		
7	**I/O Pin Assignments**		
7.1	Verify the resistance of external pull resistors do not exceed values in Table 9.1 required to guarantee a valid logic level when internal GPIO pull resistors are disabled.		
7.2	Verify the resistance of external pull resistors do not exceed values in Table 9.2 required to override a default internal pull resistor of the opposite polarity.		
8	**MIPI Interface Requirements**		
8.1	Soft MIPI is supported only on bottom banks (high-performance banks 3–11).		
8.2	Set V_{CCIOX} to 1.2 V.		
8.3	Target 100 Ω impedance.		
8.4	Differential pairs must reference a ground plane without slots or breaks. It should be continuous between the FPGA and destination or source.		
8.5	Design differential pairs as *loosely coupled* with separation between the positive and negative traces of a pair of at least twice the etch width (intra-pair spacing).		
8.6	Provide separation between each differential pair of at least six times the etch width (inter-pair spacing).		

	Item	OK	NA
8.7	Match the lengths of clock and data lane pair traces within 0.1 mm for both intra-pair and inter-pair etches.		
8.8	The RX at the FPGA should have the clock differential pair routed to clock pins labeled *PCLKTx_y* (+true) or *PCLKRTx_y* (+true) and *PCLKCx_y* (-complement) or *PCLKRCx_y* (-complement).		
9	**LVDS Interface Requirements**		
9.1	LVDS supported only on bottom banks (high-performance banks 3–11).		
9.2	Set V_{CCIOx} to 1.8 V.		
9.3	Target 100 Ω impedance.		
9.4	Differential pairs must reference a ground plane without slots or breaks. It should be continuous between the FPGA and the destination or source.		
9.5	Design differential pairs as *loosely coupled* with separation between positive and negative traces of a pair of at least twice the etch width (intra-pair spacing).		
9.6	Provide separation between each differential pair of at least six times the etch width (inter-pair spacing).		
9.7	Match lengths of clock and data lane pair traces within 0.1 mm. for both intra-pair and inter-pair etches.		
9.8	The RX at the FPGA should have the clock differential pair routed to clock pins labeled *PCLKTx_y* (+true) or *PCLKRTx_y* (+true) and *PCLKCx_y* (-complement) or *PCLKRCx_y* (-complement).		
10	**LPDDR4 and DDR Interface Requirements**		
10.1	LPDDR4 and DDR interfaces are supported only on bottom banks (high-performance banks 3–11).		
10.2	Set V_{CCIOx} to 1.1 V for LPDDR4 or 1.2V for DDR4.		
10.3	Target 100 Ω impedance for differential pair signal and 50 Ω impedance for single-ended signals.		
10.4	Design differential pairs *loosely coupled* with separation between positive and negative traces of a pair of at least twice the etch width.		
10.5	Data group		
10.5.1	DQ, DM, and DQS signals should be routed as a data group with similar routing and matched through counts. Avoid using more than three vias between the FPGA controller and memory device.		
10.5.2	Each data group has specific DQS pins and groupings, which can be checked in *Pinlist.csv* under DQS column.		
10.5.3	All data groups must reference a ground plane within the stack-up.		
10.5.4	Maintain trace length matching to a maximum of ±4 mil (±0.1 mm) between any DQ or DM signal and its associated DQS strobe within a DQ group. Use careful serpentine routing to meet this requirement.		
10.5.5	Differential pair of DQS to DQS_N trace lengths should be matched to a maximum of ±4 mil (±0.1 mm).		
10.5.6	LDQS/LDQS_N and UDQS/UDQS_N trace lengths should be matched to a maximum of within ±4 mil (±0.1 mm).		
10.5.7	Assigned FPGA I/O within a data group may be swapped to allow clean layout. Do not swap DQS assignments.		
10.5.8	Resistor terminations (DQ), placed in a fly-by fashion at the FPGA, are highly recommended. Stub-style terminations, if used, should not include a stub longer than 600 mil.		
10.6	Control group		
10.6.1	CKE, CS, ODT, RESET signals should be routed as a group with similar routing and matched through counts. Avoid using more than three vias between the FPGA controller and memory device.		
10.6.2	The control group must reference a ground plane within the stack-up.		
10.6.3	Maintain trace length matching within ±4 mil (±0.1 mm) among signals in the control group. Use careful serpentine routing to meet this requirement.		
10.7	Address and Command Group		
10.7.1	WE, RAS, CAS, ACT signals should be routed as a group and within similar routing and matched through counts. Avoid using more than three vias between the FPGA controller and memory device.		
10.7.2	The address and command group must reference a ground plane within the stack-up.		
10.7.3	Maintain trace length matching within ±4 mil (±0.1 mm) among signals in the address and command group. Use careful serpentine routing to meet this requirement.		

	Item	OK	NA
10.7.4	Address and control terminations placed after the memory component using a fly-by technique are highly recommended. Stub-style terminations, if used, should not include a stub longer than 600 mils.		
10.7.5	Address and control signals may be referenced to a power plane if a ground plane is not available; however, ground reference is preferred.		
10.8	Clock		
10.8.1	The clock signal must reference a ground plane within the stack-up.		
10.8.2	CK to CK_N trace lengths must be matched within ±4 mil (±0.1 mm).		
10.8.3	The clock signal should match with the data group and address and command group within ±4 mil (±0.1 mm).		
10.9	Differential terminations used by the CLK/CLKN pair must be located as close as possible to the memory.		
10.10	DDR trace reference must be a solid ground plane without slots or breaks. It should remain continuous between the FPGA and the memory device.		
10.11	Address and control signals should be routed on a separate PCB layer from DQ, DQS, and DM signals to minimize crosstalk.		
11	**SERDES**		
11.1	Use a continuous ground reference plane for all serial channels.		
11.2	Match differential pair trace lengths to within ±4 mil (±0.1 mm).		
11.3	Maintain proper high-speed transmission line routing with at least 10 times spacing from the reference plane to other signals.		
11.4	Do not route other signals above or below high-speed SERDES traces unless proper isolation is provided.		
11.5	Ensure the dedicated reference clock input from the clock source meets both DC and AC requirements.		
11.6	Reference clock termination resistors may be required to ensure compatible signaling levels. See Figure 6.1.		
11.7	External AC coupling capacitors may be required to ensure compatibility with standards like PCIe.		
12	**Layout Notes**		
12.1	Use 0201-size 0.1 µF capacitors to fit on the opposite side of the PCB from the Lattice Nexus 2 FPGA, between ball pad via holes.		
12.2	When using series termination resistors, place them close to the transmitting pin. Configuration pins connected to external devices (for example SPI FLASH) default to 50RS (50 Ω) drive strength. For these, start with a 0 Ω resistor for a PCB impedance of 50 Ω. For higher PCB impedances, increase the series termination resistance accordingly (for example, 10 Ω for 60 Ω impedance). The optimum series termination resistance for user-mode output pins depends on PCB etch impedance and selected output drive strength. Use IBIS model simulations to determine a starting value, then validate and optimize using oscilloscope measurement for best signal integrity.		
12.3	Match the lengths of differential pair traces (positive and negative) within ±4 mil (±0.1 mm) to maintain signal integrity data rates up to 25 Gbps.		
13	**Simulation and Board Measurement of Critical Signals**		
13.1	Simulations: Use IBIS model to simulate critical signals for proper signal integrity.		
13.1.1	Simulate differential pairs (LVDS, subLVDS, SLVS, MIPI, USB, and similar interfaces).		
13.1.2	Simulate clock nets (oscillator inputs, output clocks).		
13.1.3	Simulate data nets with embedded clocks.		
13.1.4	Simulate interrupts (edge-triggered).		
13.1.5	Simulate logic signals traveling long distances that require termination.		
13.1.6	Simulation results should be used to optimize each critical signal for optimal signal integrity: • Define output pin drive strength • Define output pin slew rate • Define output pin termination design (for example, output series termination resistor value) • Define settings of internal pin pull-up and pull-down resistors Improve PCB layout		

	Item	OK	NA
13.2	Board measurements: Use an oscilloscope to measure on PCB assembly critical signals for proper function and signal integrity.		
13.2.1	Measure differential pairs (LVDS, subLVDS, SLVS, MIPI, USB, and similar interfaces).		
13.2.2	Measure clock nets (oscillator inputs, output clocks).		
13.2.3	Measure data nets with embedded clocks.		
13.2.4	Measure interrupts (edge-triggered).		
13.2.5	Measure logic signals traveling long distances that require termination.		
13.2.6	Measurement results should be used to optimize each critical signal for optimal signal integrity: • Adjust output pin drive strength • Adjust output pin slew rate • Adjust output pin termination design (for example, output series termination resistor value) • Adjust settings of internal pin pull-up and pull-down resistors.		
13.3	Specification compliance testing is recommended for popular signaling methods (for example, USB, MIPI).		
14	**SSO (Simultaneous Switching Output)**		
14.1	When a bank has many outputs that switch simultaneously, internal SSO noise may be generated, if excessive, can cause unreliable operation. It is recommended that you verify your design using the Lattice Simultaneous Switching Output (SSO) calculator tool.		
14.2	You should verify your design using the Lattice Simultaneous Switching Output (SSO) calculator tool.		
14.3	Reducing SSO Noise		
14.4	Reduce the number of I/Os switching simultaneously in a bank. (Stagger output switching into smaller groups).		
14.5	Reduce output current drive on the switching I/Os (for example, configure for 4 mA instead of 8 mA).		
14.6	Distribute a large group of I/O across multiple banks instead of placing all in the same bank.		
14.7	Add virtual ground pins to the bank. Connect an I/O to ground on the PCB and program it to output low at maximum current.		
14.8	Add virtual V_{CCIO} pins to the bank. Connect an I/O to the bank V_{CCIO} rail on the PCB and program it to output a high at maximum current.		

Note:

1. The REXT resistor value is 200 Ω.

References

- Lattice Nexus 2 web page
- Certus-N2 web page
- Mach-N2 web page

A variety of technical notes for the Lattice Nexus 2 platform are available.

- High-Speed PCB Design Considerations (FPGA-TN-02178)
- Lattice Nexus 2 Embedded Memory User Guide (FPGA-TN-02366)
- Lattice Nexus 2 High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02372)
- Lattice Nexus 2 Platform - Overview Data Sheet (FPGA-DS-02122)
- Lattice Nexus 2 Platform - Specifications Data Sheet (FPGA-DS-02121)
- Lattice Nexus 2 Power User Guide (FPGA-TN-02381)
- Lattice Nexus 2 sysCLOCK PLL Design and User Guide (FPGA-TN-02364)
- Lattice Nexus 2 sysDSP User Guide (FPGA-TN-02362)
- Lattice Nexus 2 sysCONFIG User Guide (FPGA-TN-02370)
- Lattice Nexus 2 sysI/O User Guide (FPGA-TN-02365)
- Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039)
- Sub-LVDS Signaling Using Lattice Devices (FPGA-TN-02028)
- Thermal Management (FPGA-TN-02044)
- Using TraceID (FPGA-TN-02084)

Other references:

- Lattice Radiant FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at https://www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 0.83, September 2026

Section	Change Summary
All	• Minor editorial fixes. • Added the Mach-N2 device family in this document.
Abbreviations in This Document	Added GND, GPIO, LDO, MSPI, OTP, PCIe, RoT, SLVS, SSPI, and subLVDS to the list.

Power Supplies	• Updated Table 2.1. Supply Rails.
	  • Changed the VSSR pin recommendation from a direct ground connection to a ground connection through a 1.0 kΩ resistor.
	  • Added the VCCJB core power supply pin, applicable to Mach-N2 devices only.
	  • Restructured the wide voltage range bank voltage table to differentiate Certus-N2 (Bank 1 restricted to 3.3 V only) from Mach-N2 (Bank 1 supports the full 1.2-3.3 V range).
	  • Removed the >16 Gbps elevated-voltage tier (0.90 V / 1.8 V) for the SERDES analog and digital supply rails.
	• Added new guidance in Power Source warning against connecting PLL power pins directly to the core fabric VCC rails, to avoid introducing jitter.
	• Added the Power Regulator Derating section, establishing an 85% (or 75% for high-reliability designs) maximum utilization guideline for voltage regulator output current.

Power Supply Filtering	• Updated Table 3.1. Recommended Power Filtering Groups and Components.
	  • Updated the ferrite bead ESR specification for the PLL supply filter from ≤ 0.06 Ω to ≤ 0.4 Ω and changed the capacitor quantity pattern so 1.0 µF (not 100 nF) is now the x4 component.
	  • Added a 1.0 µF capacitor to the recommended filter for the VCC, VCCAUX, VCCAUXA, and VCCIOx power rails.
	  • Updated the VCC filter row to include the new VCCJB pin, noting it applies to Mach-N2 devices only.
	  • Removed the >16 Gbps elevated-voltage tier and added 1.0 µF x2 capacitors to the SERDES analog and digital supply filters.
	  • Updated the recommended filter for VCCA_PLL_W, VCCA_PLL10, VCCA_PLL4, VCCA_PLL7 (tied together).
	• Redrew Figure 3.1. Recommended Power Filters to add the VCCJB pin, additional 1 µF filter capacitors, and Certus-N2, Mach-N2 differentiating footnotes, matching the corresponding Table 2.1. Supply Rails and Table 3.1. Recommended Power Filtering Groups and Components changes.
	• Added a recommendation to connect a few unused GPIO pins to test points to aid debugging and board bring-up.
	• Expanded the unused-bank bypass capacitor recommendation to allow either a 1.0 µF or a 100 nF capacitor, where previously only 100 nF was specified.

Power	Added a new Power Supply Ramp Rates section, with a new table specifying minimum and maximum power-supply ramp rates for VCCIO1 and other supplies.

Component Selection	• Updated the Voltage Rating section.
	  • Increased the recommended capacitor voltage-rating derating from at least 80% higher than the rail voltage to at least double the rail voltage, changed the worked example from a 3.3 V rail to a 1.8 V rail, and added a new requirement of at least triple the rail voltage for automotive and aerospace applications.
	  • Removed the old *Size* section and merged it into this section.
	• Updated Table 5.1. Recommended Capacitor Sizes.
	  • Split the combined 1.0 µF and 2.2 µF row into two separate rows and swapped the preferred and next-best package sizes for 1.0 µF capacitors (now 0201 preferred instead of 0402).

Clock Inputs	Added PCLKRTx_y/PCLKRCx_y as an alternate dedicated PLL reference clock pin naming convention, alongside PCLKTx_y/PCLKCx_y, and added guidance that dedicated PLL reference clock pins have lower jitter than PCLK pins.

Section	Change Summary

Configuration Considerations	• Added 4.7 kΩ as an alternative pull-up resistor value (alongside the existing 10 kΩ) for TMS, TDI, and TDO in Table 7.1. JTAG Pin Recommendations.
	• Added design guidance under two new headings, *JTAG Pull Resistors* and *JTAG Signal Integrity*, covering pull-resistor selection rationale and signal-integrity recommendations (series termination value and TCK trace spacing).
	• Updated Table 7.2. Pull-up/Pull-down Recommendations for Configuration Pins.
	  • Added a new MRSTN pin providing a dedicated reset connection to an external flash device with a reset pin.
	  • Updated multiple rows to offer both 10 kΩ and 4.7 kΩ as acceptable pull-up resistor values, consistent with the JTAG table change.
	• Redrew Figure 7.1. Typical Connections for Programming SRAM or External Flash through JTAG to add the MRSTN-to-FLASH-RESET connection.
	• Redrew Figure 7.2. Typical Connections for Programming SRAM or External Flash through Target SPI to add the MRSTN-to-FLASH-RESET connection and explicit "Do Not Install" (DNI) annotations.

I/O Pin Assignments	Added the External Pull Resistor Maximum Values section, with two new tables specifying maximum external pull-resistor values per VCCIO voltage, for both the internal-pulls-disabled case and the override-opposite-internal-pull case.
Checklist	• Updated item 1.1.3 to include the new *VCCJB supply pin*, applicable to Mach-N2 devices only. • Split item 1.2 into separate Certus-N2 and Mach-N2 *wide-range VCCIO* items, reflecting the new per-device bank voltage differentiation. • Updated item 1.3.1 to specify a single V_{CCA_MPQx} pin voltage of 0.80 V. Removed the previous data rate dependent condition for > or ≤ 16 Gbps. • Updated item 1.3.3 to specify a single V_{CCH_MPQx} pin voltage of 1.5 V. Removed the previous data rate dependent condition for > or ≤ 16 Gbps. • Updated items 2.1 and 3.2 to include 4.7 kΩ as an alternative CFGMODE pull-up resistor value. • Updated items 6.2, 8.8, and 9.8 to include the new PCLKRT/PCLKRC dedicated PLL reference clock pin naming. • Added two new checklist items (7.1, 7.2) directing designers to verify external pull-resistor values. • Removed two duplicate checklist items (14.9 and 14.10) in the SSO section.

Revision 0.82, September 2025

Section	Change Summary
All	• Removed all instances of *VCCJB* in this document. • Minor editorial fixes.
Abbreviations in This Document	Updated section contents.
Introduction	• Added, *Hardware Checklists are developed after evaluation boards and incorporate optimized designs that improve upon the circuitry of evaluation boards. If you copy circuits from evaluation boards, ensure to optimize your designs according to the hardware checklists*, after the first paragraph of this section. • Removed the statement, *The device family consists of FPGA densities ranging from 65k to 220k SLC*.
Power Supplies	• Updated Table 2.1. Supply Rails. • Replaced V_{CCA_PLLx} with $V_{CCA\_PLL\_W}$, V_{CCA_PLL10}, V_{CCA_PLL4}, V_{CCA_PLL7} and removed *x = Specific PLL number*.

Section	Change Summary
Power Supply Filtering	• Updated Table 3.1. Recommended Power Filtering Groups and Components. • Updated values of V_{CC_PLLx} and replaced V_{CCA_PLLx} with $V_{CCA\_PLL\_W}$, V_{CCA_PLL10}, V_{CCA_PLL4}, V_{CCA_PLL7} *tied together*. • Updated V_{CC_PLLx} values and replaced V_{CCA_PLLx} with $V_{CCA\_PLL\_W}$, V_{CCA_PLL10}, V_{CCA_PLL4}, V_{CCA_PLL7} in Figure 3.1. Recommended Power Filters. • Added the ERASEKEY section • Added an External Reference Resistor (REXT_MPQx) value of *200 Ω* in the Unused SERDES Quads section.
Clock Inputs	• Added *GPLL* and *PCLK*. • Added, the statement, *For single-ended I/Os, use only PCLKT pins as primary CLK pads*.
Layout Recommendations	Replaced Figure 11.1 Recommended Layout with Figure 11.1. Ground Vias Implementation and Figure 11.2. Stitching Vias Implementation.
Checklist	• Added item 6.2, *For single-ended I/Os, use only PCLKT pins as primary CLK pads*. • Added, a note that the *REXT resistor value is 200 Ω*.

Revision 0.81, December 2024

Section	Change Summary

Power Supply Filtering	• Updated Figure 3.1. Recommended Power Filters.
	  • Updated capacitance of VCCAUXA from *10 µF x3* to *10 µF x2*.
	  • Updated the capacitance of VCCA_PLLX from 10 *µF* to *1 µF.*
	• Reworked the EXT_RES pins subsection.

Configuration Considerations	• Updated Table 7.1. JTAG Pin Recommendations.
	  • Updated CFGMODE value from *10 kΩ* to *2 kΩ*.
	  • Updated the statement after Table 7.1 to, *For best results, route the V_{CCIO2}, TCK, TDI, TDO, TMS, CFGMODE, PROGRAMN, INITN, DONE, GND signals to a common test header*.
	• Updated Table 7.2. Pull-up/Pull-down Recommendations for Configuration Pins.
	  • Updated the CFGMODE value from *10 kΩ* to *2 kΩ*.
	  • Changed *Serial resistor* to *Series resistor* under MCLK pin.
	  • Updated table note 1.
	• Updated the pull-down resistor of the JTAG/SSPI mode from *10 kΩ* to *2 kΩ* for both Figure 7.1. Typical Connections for Programming SRAM or External Flash through JTAG and Figure 7.2. Typical Connections for Programming SRAM or External Flash through Target SPI.
	• Updated Figure 7.1. Typical Connections for Programming SRAM or External Flash through JTAG and Figure 7.2. Typical Connections for Programming SRAM or External Flash through Target SPI series resistor value from *22 Ω* to *0 Ω* and added note 2 in both figures.

I/O Pin Assignments	Reworked Series Termination Resistors subsection.
Checklist	• Updated item 2.1 to *CFGMODE pin pulled high using 10 kΩ or low using 2 kΩ per* Table 7.1. JTAG Pin Recommendations. • Updated item 2.3.1 to *JTAG header: V_{CCIO2}, TCK, TDI, TDO, TMS, CFGMODE, PROGRAMN, INITN, DONE, GND.* • Updated item 3.2 to *CFGMODE pin 2 kΩ pull-down.* • Reworked item 11.2.

Revision 0.80, September 2024

Section	Change Summary
All	Preliminary release.

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