Lattice Radiant 2024.1.1 Software Release Notes

Welcome to Lattice Radiant® software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs).

What's New in Radiant 2024.1.1 Software

- **Device Support:**
  - Lattice Avant™ (LAV-AT)
    - E70ES1 (-1/-2/-3) 0.82V (COM/IND) – CSG841
    - Designs targeting the E70 device in 2023.2 or 2023.2.1 should now target the E70ES1 device.
    - For Avant products, this release supports targeting of silicon based on their release status. Refer to the following table for details.

2024.1 Designator	Status	Prior Designator
E70ES1	Engineering Sample	E70
E70	Early Access	NA

- **Tool and Other Enhancements**
  - **Bitstream**
    - The IDCODE of LFD2NX-28 and LFD2NX-9 devices have been updated. Due to these changes, regenerating the bitstream is recommended.
  - **Foundation IP**
    - In the Lattice Avant PLL Module configuration interface, when Enable Dynamic Phase Ports is checked, a Use Phase Advance option is added. When this is enabled, the maximum VCO frequency is reduced. Otherwise, the value remains at 4 GHz.
    - Lattice Avant MPP enables 5G and base video protocols, which include SyncE and DP/eDP.
  - **Soft IP**
    - By default, the IP on Server and IP Catalog options to "Show latest IP Version only" and "Show IP supported by target device only" are now enabled.

- **Programmer** – The Verify Public Key operation has been added to Radiant Programmer.

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Radiant software, it may be necessary to re-create some IP, per the procedures described in the following table.

These procedures adapt the project for the changes in Radiant software.

Versions	IP			IP Regeneration Procedures
	Avant (LAV-AT-E)	**CrossLink-NX (LIFCL), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP), MachXO5-NX (LFMXO5)**	**iCE40UP**	
2024.1.1	DDR Generic	FIFO	N/A	These IP used in designs created in Radiant 2024.1 or earlier must be regenerated in Radiant 2024.1.1.
	DDRPHY	FIFO DC		
	MPPHY	ADC Core		
	PLL			
	SEDC			
	FIFO			
	FIFO DC			

The following server IP are not compatible with Radiant 3.0 onwards. Use the latest versions of the IP available on the IP server:

- I2C Master version 1.0.3
- UART 16550 version 1.0.4
- DDR3 SDRAM Controller version 1.1.1
- DDR3 SDRAM Controller version 1.2.1
- LPDDR2 SDRAM Controller Lite version 1.1.1
- LPDDR2 SDRAM Controller Lite version 1.2.1

Supported Devices

Lattice Radiant software can be used with either a free license or a subscription license. The two licenses provide access to different device families.

Device Family	Free License	Subscription License
iCE40 UltraPlus (iCE40UP)	◀	
Lattice Avant (LAV-AT-E)		◀
CertusPro™-NX (LFCPNX)	Evaluation Mode	◀
Certus™-NX (LFD2NX)	◀	
MachXO5™-NX (LFMXO5)	Evaluation Mode	◀
CrossLink-NX (LIFCL)	◀	
Certus™-NX-RT (UT24C)		RT Subscription
CertusPro™-NX-RT (UT24CP)		RT Subscription

Support for Third-Party Synthesis and Simulator Tools

The Synopsys Synplify Pro® for Lattice synthesis tool and the Siemens QuestaSim® Lattice Edition simulator tools are included in the Radiant software.

- **Synopsys Synplify Pro FPGA synthesis software version V-2023.09LR-1**
  - Release Notes for Synplify Pro are located in ..\<*install_directory*>\radiant\2024.1\synpbase\doc\. The file name is release_notes.pdf.
  - A full set of documents for Synplify Pro are also located in \<*install_directory*>\radiant\2024.1\synpbase\doc\.
- **Siemens QuestaSim Lattice Edition 2024.2**
  - Release Notes for QuestaSim Lattice Edition are located in <install_directory>\radiant\2024.1\questasim\.
    The file names are RELEASE_NOTES.html or RELEASE_NOTES.txt.

- A full set of documents for QuestaSim Lattice Edition are located in <install_directory>\radiant\2024.1\questasim\docs\pdfdocs.

- **Siemens Questa® 2022.3**
- **Cadence Xcelium® 24.03.003**
- **Synopsys VCS® U-2023.03-SP2**

Help Resources

- Online Help updated with CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP), and Lattice Avant (LAV-AT) content.
- To view the Online Help, start the Lattice Radiant software and select the  "Getting Started" icon under Information Center.

  Note: The Firefox Snap install is not supported if you are using Ubuntu 20.04 or 22.04 to access the Radiant Help. This is a result of the snap install's inability to open local HTML pages. You may reinstall the latest version of Firefox using Apt install. For installation instructions, please refer to this guide.

System Requirements

The following shows the basic system requirements for Radiant software:

- Intel x86 64-bit or 64-bit-compatible PC
- OS Support:

64-bit OS	Radiant	Synplify Pro	QuestaSim
Windows 10	✓	✓	✓
Windows 11	✓	✓	✓
Red Hat Enterprise Linux 7.9	✓	✓	✓
Red Hat Enterprise Linux 8.8	✓	✓	✓
Ubuntu version 20.04 LTS	✓	✓	✓*
Ubuntu version 22.04 LTS	✓	✓	✓*
CentOS 7.9	✓	✓	✓*

***Note**: The third-party tools have been tested by Lattice on the listed platforms, but the vendors do not officially support them.

- Approximately 50 GB free disk space
- Computer Memory Requirement:
  - Nexus – 16GB
  - Avant – 32GB Recommended for running a single project. If running multiple projects, the memory requirement will be higher.
- 1024 X 768 graphics display
- Network adapter for license and network connectivity
- A Web browser with JavaScript capability
- Acrobat Reader

Issues Fixed in this Release

The following known issues are fixed in this release. Their workarounds are no longer needed.

A synthesis error may be encountered after adding Reveal Inserter into the project.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-22567

False Path Constraint gets ignored even if the pin is valid or present in the design.

Devices affected: All devices

Bug number: DNG-22189

Unique IDCODEs need to be assigned for the LFD2NX-9 and LFD2NX-28 virtual devices.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-22301

Deployment tool generates blocks in a way that causes issues in some cases for ping pong boot.

Devices affected: All devices

Bug number: DNG-21418

Map and PAR Timing Analysis crashes due to unchecked value before referencing.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-22484 / DNG-22534

Programmer encounters issues when three HW-USB-2B Cables are connected.

Devices affected: All devices

Bug Number: DNG-21262

Map encounters an error on dual-rank LPDDR4 Memory controller when running Radiant Flow

Device affected: CertusPro-NX (LFCPNX)

Bug number: DNG-20832

LMMIRDATA port does not output data correctly during RTL simulation of CONFIG_LMMIE.

Devices affected: MachXO5-NX (LFMXO5-100T)

Bug number: DNG-20666

Synplify Pro infers unsupported primitive "SP16K_1" during synthesis for CrossLink-NX.

Device affected: CrossLink-NX (LIFCL-33U)

Bug number: DNG-20643

RAM_DP_True outputs zeroes and does not retain data from address 800h during certain transactions.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-20532

Create_generated_clock constraint may be overwritten by Synplify pro, changing the destination clock path.

Devices affected: All devices

Bug number: DNG-20228

Unexpanded interface port error during synthesis with Synplify Pro for some designs using the System Verilog interface construct.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-19872

"Identifier not declared" error encountered during simulation with VCS in encrypted lmmis_init_fsm.v file.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-19861

Post-route simulation error when using GDDR for Avant devices due to parameters not being passed correctly from the original RTL.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-18794

Synplify Pro implements RAM using LUTs instead of EBRs for certain Lattice RISC-V IP on Avant.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-18479

"Not user declared module (VERIFIC_AND)" error during post-synthesis when using LSE when the modulus operator is used in RTL.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-16713

The LDC file generated from the Synplify Pro FDC file contains an additional get_pins object, which causes a "No pin matched" warning.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-15310

Known Issues for Radiant 2024.1.1

The following are known issues for the Radiant Software 2024.1.1. For assistance with these issues, please contact Lattice Technical support.

An error occurs when Reveal Analyzer continuously triggers and when the Start Polling button of virtual LED is clicked.

Workaround: If you are using the SEDC primitive in the design, you should use the 2024.1 version of Reveal Controller/Analyzer. You can also use the 2024.1 version of the Reveal stand-alone tool.

If the 2024.1.1 version is used, Reveal will exit the user mode in the device.

Devices affected: All Nexus devices

Bug number: DNG-23417

PLL Foundation IP encounters timing issue when using the *Select Register Interface* = APB attribute

The PLL foundation IP implements bandwidth initialization logic that uses the PLL Hard IP's LMMI I/F to set some internal registers for more stable initialization. The timing is guaranteed by the logic design by extending the write access to multiple clock cycles. This logic is disabled when the PLL lock asserts and the control of the PLL Hard IP's LMMI I/F goes to the APB2LMMI bridge. The timing issue occurs because the bandwidth initialization logic runs on the internal PLL clock while the APB2LMMI runs on the APB clock. The switch between these two logics is only done when the PLL lock asserts and de-asserts, in these cases the state machine guarantees the proper switch.

For assistance with this issue, please contact Lattice Technical support.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-23345

PLL Foundation IP has a chance of having a timing issue when the attribute *Select Register Interface* = None

The PLL foundation IP implements bandwidth initialization logic that uses the PLL Hard IP's LMMI I/F to set some internal registers for more stable initialization. The timing is guaranteed by the logic design by extending the write access to multiple clock cycles. This logic is only active when PLL lock is de-asserted and is deactivated when PLL lock asserts. There is a chance of getting hold time issue on the PLL's LMMI I/F when the system design has high utilization.

Workaround:

```
set_false_path -to   [get_pins {<PLL_instance_path> /lscc_pll_inst/gen_ext_outclkdiv.u_pll.PLLC_MODE_inst/LMMIOFFSET*}]
set_false_path -to   [get_pins {<PLL_instance_path> /lscc_pll_inst/gen_ext_outclkdiv.u_pll.PLLC_MODE_inst/LMMIREQUEST}]
set_false_path -to   [get_pins {<PLL_instance_path> /lscc_pll_inst/gen_ext_outclkdiv.u_pll.PLLC_MODE_inst/LMMIWDATA*}]
set_false_path -to   [get_pins {<PLL_instance_path> /lscc_pll_inst/gen_ext_outclkdiv.u_pll.PLLC_MODE_inst/LMMIWRRDN}]
```

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-23312

Synplify Pro incorrectly removes virtual wire signals that were preserved using the "syn_rvl_debug" attribute.

Devices affected: All devices

Bug number: DNG-21236

QuestaSim simulation fails for DDR5 IP due to undeclared Micron model packages.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-21086

Synplify Pro does not report an error or warning for clocks that are driven by logic.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-21048

The PDPSC32K primitive does not have an output path despite outreg being used.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-20772

You may encounter an issue with CONFIG_LMMI and CONFIG_LMMA's lmmi_ready signal during simulation.

Devices affected: Certus-NX (LFD2NX), CrossLink-NX (LIFCL)

Bug number: DNG-20717

CONFIG_LMMI RTL simulation error occurs and data missing in output ports.

Devices affected: Certus-NX (LFD2NX), CrossLink-NX (LIFCL)

Bug number: DNG-20543

Synplify Pro does not correctly process macro creation constraints with escape characters.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-20134

When using Synplify Pro, you may encounter the following error during macro reuse: “Synthesis exit by 9. Child process exited abnormally. Done: error code 1.”

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-20116

IBIS reports I/O models of some sysCONFIG pins even if they are used as GPIO.

Workaround: Remove duplicated pins in IBIS file.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19646

Simulation with XCELIUM may fail when simulating projects using the CNTL_LR_U_POWER primitive due to incorrect compilation order of cmpl_libs.

Devices affected: CrossLink-NX (LIFCL-33U)

Bug number: DNG-19623

Cannot assign input ports as MIPI_DPHY type for Avant.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19199

Reveal Power-on Reset (POR) Debug function does not work when using LSE with only one Trigger Unit (TU).

Workaround: Add another Trigger Unit (TU) that can be unrelated to POR Debug.

Devices affected: All devices except iCE40UP

Bug number: DNG-13901

The CSI-2/DSI D-PHY Transmitter and Receiver Soft IP simulations fail when using Synopsys VCS as simulation tool.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-13225

Post-route simulation error when using GDDR for Nexus devices due to parameters not being passed correctly from the original RTL.

Workaround: Intrinsic delay similar to the delay value on the vo.vo file needs to be added to the IP testbench.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-9639

MAP incorrectly reports number of DPHY and PCIE/ADC resources for CrossLink-NX (LIFCL) QFN72 package.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-8297