



NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM [C].

4. PRIMARY DATUM [C] AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.

6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.

7. JEDEC REFERENCE: JEP95 DG4.18

* VALUES ARE BASED ON SUBCON CAPABILITY

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOM.	MAX.
Total Thickness	A	0.760	0.800	0.840
Stand Off	A1	0.206	0.236	0.266
Wafer Thickness	A2	0.564	±0.025	
Backside Coating Thickness	A3	—		
Si Die Thickness		0.531	REF	
Body Size	D	9.000		BSC
	E	11.000		BSC
Ball Diameter (Size)		0.300		
Ball/Bump Width	b	0.289	0.319	0.349
Ball/Bump Pitch	eD	0.500		
	eE	0.500		
Ball/Bump Count	n	410		
Edge Ball Center to Center	D1	8.227		BSC
	E1	10.000		BSC
Package Edge Tolerance	aaa	0.030		
Coplanarity (whole wafer)	ddd	0.050		
Ball/Bump Offset (Package)	*eee	0.060		
Ball/Bump Offset (Ball)	*fff	0.030		

Title: Package Outline Drawing

Pkg Type: FOWLP

Document No:

Product Family: LAV-AT

Pin Count: 410

POD-240094

Product Name: LAV-AT-30-ASGA410

Pkg Size: 9x11 mm

Rev: C

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