RISC-V I/O Physical Memory Protection IP – Lattice Propel Builder 2024.2

IP Version: v1.0.0

User Guide

FPGA-IPUG-02272-1.0

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This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AXI	Advanced eXtensible Interface
CPU	Central Processing Unit
DMA	Direct Memory Access
RISC-V	Reduced Instruction Set Computer-V (five)
FPGA	Field Programmable Gate Array
GUI	Graphic User Interface
HDL	Hardware Description Language
IOPMP	I/O Physical Memory Protection
IP	Intellectual Property
IRQ	Interrupt Request
DMA	Direct Memory Access
LUT	Look Up Table
MD	Memory Domain
TOR	Top of Range
WARL	Write Any Read Legal
RRID	Request Role ID

1. Introduction

The Lattice Semiconductor RISC-V I/O Physical Memory Protection (IOPMP) IP is a separate physical memory protection unit that prevents illegal or unexpected access to some specific regions. These regions can be accessed by the RISC-V CPU but should not be accessed by some controllers, such as DMA or Ethernet. The RISC-V IOPMP IP includes an AXI-Lite Interface and an AXI-based bridge. The AXI-Lite Interface is for control and status registers and the AXI-based bridge is for the data path. The control path justifies the accessibility based on the address and entry settings. It decides whether or not to block this access, raise an interrupt, and respond with errors when the access is illegal.

The IOPMP IP is implemented using Verilog HDL and it can be configured and generated using the Lattice Propel™ Builder software. The IP supports Certus™-N2, Lattice Avant™, MachXO5™-NX, CrossLink™-NX, Certus-NX, and CertusPro™-NX FPGA devices.

1.1. Quick Facts

Table 1.1 presents a summary of the RISC-V IOPMP IP.

Table 1.1. RISC-V IOPMP IP Quick Facts

IP Requirements	Supported FPGA Family	Certus-N2, Lattice Avant, MachXO5-NX, CrossLink-NX, Certus-NX, and CertusPro-NX
Resource Utilization	Targeted Devices	LN2-CT, LAV-AT, LFMXO5, LIFCL, LFD2NX, and LFCPNX
	Supported User Interfaces	AXI Interface and AXI-Lite Interface
	Resources	See Table A.1.
Design Tool Support	Lattice Implementation	IP v1.0.0 – Lattice Propel Builder 2024.2, Lattice Radiant™ Software 2024.2
	Simulation	For a list of supported simulators, see the Lattice Radiant software user guide.

1.2. Features

The RISC-V IOPMP IP has the following features:

- AXI4 interface bridge
- AXI-Lite interface memory-mapped registers
- Compact-K model based controller
- Up to four IOPMP entries with TOR support

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal Names that end with:

- _n are active low.
- _i are input signals.
- _o are output signals.
- _io are bi-directional input/output signals.

1.4. Licensing and Ordering Information

The IOPMP IP is provided at no additional cost with the Lattice Propel design environment. The IP can be fully evaluated in hardware without requiring an IP license string.

2. Functional Descriptions

2.1. Overview

The RISC-V IOPMP IP has three interfaces, as shown in Figure 2.1. The AXI-Lite interface is for memory-mapped registers. Refer to Table 2.1 for more details. The two AXI interfaces are the data path. The controller is enabled by default. Therefore, the AXI Manager is connected to the Error Subordinate by default. To enable the data path, the registers need to be set by a processor. For register settings, refer to the Modules Description section.

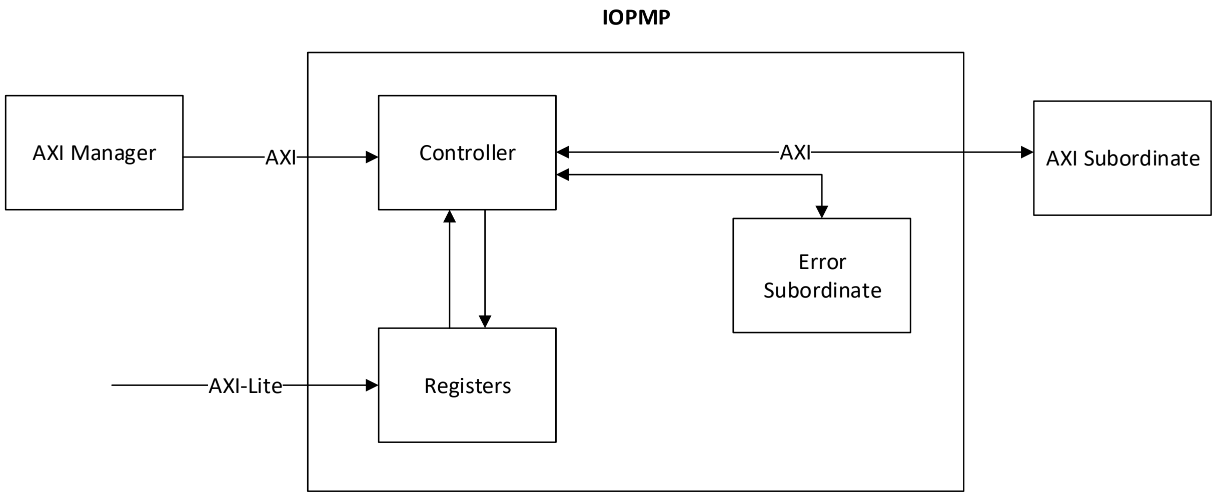


Figure 2.1. RISC-V IOPMP IP Diagram

2.2. Modules Description

2.2.1. Compact-K Model

The Lattice RISC-V IOPMP IP follows the compact-K model. The module defines that the entire Lattice RISC-V subsystem is in one memory domain (MD), and the MD has exactly four entries. Either the number of memory domains or the number of entries is not configurable.

The request role ID (RRID) associated with the MD is based on the AXI ID number. The IOPMP IP passes the ID information from the manager to the subordinate and only stores the information when the access is denied to specific registers. To check the AXI ID naming rules, refer to the AMBA AXI Protocol Specification.

Table 2.1. RISC-V IOPMP Control and Status Registers

Address	Register Name	Access	Fields
0x0000	VERSION	read-only	• vendor[23:0]: Vendor ID. • specver[31:24]: Specification version.
0x0004	IMPLEMENTATION	read-only	impid[31:0]: Implementation ID.
0x0008	HWCFG0	read-only	• model[3:0]: 0x4 – Compact-K model. • tor_en[4]: 0x1 – Top of Range (TOR) is supported. • sps_en[5]: 0x0 – Secondary permission settings is not supported. • user_cfg_en[6]: 0x0 – User customized attributes are not supported. • prient_progp[7]: 0x0 – Priority is not programmable. • rrid_transl_en[8]: 0x0 – Tagging a new RRID is not supported. • chk_x[10]: 0x0 – Instruction fetch is not supported. • no_w[12]: 0x1 – Write accesses always fail, as no rule is matched. • stall_en[13]:0x0 – Stall-related features are not supported. • peis[14]: 0x0 – Interrupt suppression is not supported. • pees[15]: 0x0 – Error suppression is not supported. • mfr_en[16]: 0x0 – Multi Faults Record Extension is not supported. • md_num[30:24]: 0x1 – One MD is supported. • enable[31]: 0x1 – IOPMP check is always enabled.
0x000C	HWCFG1	read-only	• rrid_num[15:0]: Indicates the supported number of RRID in the instance. • entry_num[31:16]: Indicates the supported number of entries in the instance.
0x0010	HWCFG2	WARL	• prio_entry[15:0]: Indicates the number of entries that are matched with certain priority. These rules should be placed in the lowest order. Within these rules, the lower the order, the higher the priority. • rrid_transl[31:16]: RRID tagged to outgoing transactions. Support only for HWCFG0.rrid_transl_en=1.
0x0014	ENTRYOFFSET	read-only	offset[31:0]: Indicates the offset address of the IOPMP array from the base of an IOPMP instance.
0x0048	MDCFGLCK	read-only	lock[0]: Lock bit to the MDCFGLCK register. It is hardwired to be one for the Compact-K model.
0x004C	ENTRYLCK	WARL	• lock[0:0]: Lock bit to the ENTRYLCK register. • f[16:1]: Indicates the number of locked IOPMP entries.

Address	Register Name	Access	Fields
0x0060	ERR_CFG	read-write	• lock[0:0]: Lock bit to the ERR_CFG register. • ie[1:1]: Enables the interrupt of IOPMP. • rs[2:2]: Response to an illegal read access. • 0x0 – Responds with an implementation-dependent error. • 0x1 – Responds with the success of a pre-defined value.
0x0064	ERR_REQINFO	bit[0] : read & W1C bit[6:1]: read-only	• valid[0:0]: Indicates if the illegal capture recorder has valid content and keeps the content until the bit is cleared. • ttype[2:1]: Indicates the transaction type. • 0x1 – Read. • 0x2 – Write. • 0x3 – Instruction fetch. • etype[6:4]: Indicates the type of violation. • 0x0 – No error. • 0x1 – Illegal read access. • 0x2 – Illegal write access. • 0x3 – Illegal instruction fetch. • 0x4 – Partial hit on a priority rule. • 0x5 – Does not hit any rule. • 0x6 – Unknown RRID. • 0x7 – User-defined error.
0x0070	ERR_REQID	read-only	Indicates the error address[33:2].
0x0800	MDCFG	read-only	t[15:0]: Indicates the number of entries.
ENTRYOFFSET + i * 16	ENTRY_ADDR(i)	WARL	addr[31:0]: Physical address[33:2] of the protected memory region.
ENTRYOFFSET + i * 16 + 8	ENTRY_CFG(i)	WARL	• r[0:0]: Read permission to the protected memory region. • w[1:1]: Write permission to the protected memory region. • x[2:2]: Instruction fetch permission to the protected memory region. • a[4:3]: Address mode of the IOPMP entry. • 0x0 – OFF • 0x1 – TOR • sire[5:5]: Suppresses the interrupt for an illegal read. • siwe[6:6]: Suppresses the interrupt for an illegal write. • sixe[7:7]: Suppresses the interrupt for an illegal instruction fetch. • sere[8:8]: Suppresses the error for an illegal read. • siwe[9:9]: Suppresses the error for an illegal write. • sexe[10:10]: Suppresses the error for an illegal instruction fetch.

2.2.2. IOPMP Entry

The IOPMP entries are described by a group of configurable registers. There are four entries in the Lattice RISC-V IOPMP IP. Each entry includes an address register and a configuration register. These entries control the accessible memory range from the lower limit to the upper limit. All the registers are Write Any Read Legal (WARL). The fields that are not supported are zeros and cannot be revised.

2.2.3. Address Matching

The IOPMP IP supports the top boundary of an arbitrary range only, with the support of four-byte granularity. When selecting TOR, each entry controls an address range. This range starts either from the address of the previous entry and includes the address of the previous entry, or, if it is entry 0, it starts from 0. The range then extends up to but does not include the address of the current entry. If the address of the current entry is less than or equal to the previous entry, this entry does not work.

For each memory region, the IOPMP IP can block either the read or write access. When the access violates the entry rules, the IP receives either an error response, or a fake success response based on the ERR_CFG register. It can also raise an interrupt, which can inform the processor there is an illegal access from IOPMP.

2.2.4. Lock

The IOPMP entries can be locked by the ENTRYLOCK register. The number stores in the field of ENTRYLCK.f means the number of entries that are locked, counting from entry 0. If the number is equal to or larger than 4, all the entries are locked. When entries are locked, they cannot be modified by the hart.

The ENTRYLOCK can be locked by its bit 0. When this bit is locked, it cannot be unlocked until the system is reset.

2.2.5. Priority

Priority is not supported in this release.

2.3. Programming Flow

2.3.1. Program IOPMP Entry

- Read the offset of the PMP entries from ENTRYOFFSET.
- Setup the correct upper limit of each memory region to ENTRY_ADDR.
- Setup the accessible and enable TOR to ENTRY_CFG.
- Setup the error response type and interrupt to ERR_CFG.
- Lock the entries to ENTRYLOCK if necessary.
- Lock the ENTRYLOCK register if necessary.

2.3.2. Interrupt Handler

- Read the information of error from ERR_REQINFO and ERR_REQID.
- Set the bit 0 of ERR_REQINFO to clear the interrupt.

2.4. Signal Description

Table 2.2 to Table 2.6 list the ports of the soft IP in different categories.

2.4.1. Clock and Reset

Table 2.2. Clock and Reset Ports

Name	Direction	Width	Description
clk	In	1	IOPMP soft IP clock.
rst_n	In	1	Global reset, active low.

2.4.2. AXI Interface

Table 2.3. AXI Manager Ports to AXI Subordinate

Name	Direction	Width	Group	Description
AWREADY_m	In	1	AXI4 Mandatory Write Address Channel	—
AWVALID_m	Out	1		—
AWADDR_m	Out	32		—
AWLEN_m	Out	8		—
AWSIZE_m	Out	3		—

Name	Direction	Width	Group	Description
AWBURST_m	Out	2		Not implemented.
AWLOCK_m	Out	1		Not implemented.
AWCACHE_m	Out	4		Not implemented.
AWPROT_m	Out	3		Not implemented.
AWQOS_m	Out	4		Not implemented.
AWREGION_m	Out	4		Not implemented.
AWID_m	Out	1		Not implemented.
WREADY_m	In	1	AXI4 Mandatory Write Data Channel	—
WVALID_m	Out	1		—
WDATA_m	Out	32		—
WLAST_m	Out	1		Not implemented.
WSTRB_m	Out	4		—
BVALID_m	In	1	AXI4 Mandatory Write Response Channel	—
BRESP_m	In	2		b’00: OKAY[1] b’10: SLVERR[1] b’11: DECERR[1]
BID_m	In	1		Not implemented.
BREADY_m	Out	1		—
ARVALID_m	Out	1	AXI4 Mandatory Read Address Channel	—
ARREADY_m	In	1		—
ARCACHE_m	Out	4		Not implemented.
ARPROT_m	Out	3		Not implemented.
ARQOS_m	Out	4		Not implemented.
ARREGION_m	Out	4		Not implemented.
ARID_m	Out	1		Not implemented.
ARADDR_m	Out	32		—
ARLEN_m	Out	8		—
ARSIZE_m	Out	3		—
ARBURST_m	Out	2		Fixed 2'b01.
ARLOCK_m	Out	1		Not implemented.
RID_m	In	1	AXI4 Mandatory Read Data Channel	Not implemented.
RDATA_m	In	32		—
RRESP_m	In	2		b’00: OKAY[1] b’10: SLVERR[1] b’11: DECERR[1]
RLAST_m	In	1		—
RVALID_m	In	1		—
RREADY_m	Out	1		—

Note:

1. Refer to the AMBA AXI Protocol Specification for more detailed descriptions of these responses.

Table 2.4. AXI Subordinate Ports to AXI Manager

Name	Direction	Width	Group	Description
AWREADY_s	Out	1	AXI4 Mandatory Write Address Channel	—
AWVALID_s	In	1		—

Name	Direction	Width	Group	Description
AWADDR_s	In	32		—
AWLEN_s	In	8		—
AWSIZE_s	In	3		—
AWBURST_s	In	2		Not implemented.
AWLOCK_s	In	1		Not implemented.
AWCACHE_s	In	4		Not implemented.
AWPROT_s	In	3		Not implemented.
AWQOS_s	In	4		Not implemented.
AWREGION_s	In	4		Not implemented.
AWID_s	In	1		Not implemented.
WREADY_s	Out	1	AXI4 Mandatory Write Data Channel	—
WVALID_s	In	1		—
WDATA_s	In	32		—
WLAST_s	In	1		Not implemented.
WSTRB_s	In	4		—
BVALID_s	Out	1	AXI4 Mandatory Write Response Channel	—
BRESP_s	Out	2		b’00: OKAY[1] b’10: SLVERR[1] b’11: DECERR[1]
BID_s	Out	1		Not implemented.
BREADY_s	In	1		—
ARVALID_s	In	1	AXI4 Mandatory Read Address Channel	—
ARREADY_s	Out	1		—
ARCACHE_s	In	4		Not implemented.
ARPROT_s	In	3		Not implemented.
ARQOS_s	In	4		Not implemented.
ARREGION_s	In	4		Not implemented.
ARID_s	In	1		Not implemented.
ARADDR_s	In	32		—
ARLEN_s	In	8		—
ARSIZE_s	In	3		—
ARBURST_s	In	2		Fixed 2'b01.
ARLOCK_s	In	1		Not implemented.
RID_s	Out	1	AXI4 Mandatory Read Data Channel	Not implemented.
RDATA_s	Out	32		—
RRESP_s	Out	2		b’00: OKAY[1] b’10: SLVERR[1] b’11: DECERR[1]
RLAST_s	Out	1		—
RVALID_s	Out	1		—
RREADY_s	In	1		—

Note:

1. Refer to the AMBA AXI Protocol Specification for more detailed descriptions of these responses.

2.4.3. AXI-Lite Interface

Table 2.5. AXI-Lite Subordinate Ports

Name	Direction	Width	Group	Description
AWREADY_ctr	Out	1	AXI4 Mandatory Write Address Channel	—
AWVALID_ctr	In	1		—
AWADDR_ctr	In	32		—
AWPROT_ctr	In	3		Not implemented.
WREADY_ctr	Out	1	AXI4 Mandatory Write Data Channel	—
WVALID_ctr	In	1		—
WDATA_ctr	In	32		—
WSTRB_ctr	In	4		—
BVALID_ctr	Out	1	AXI4 Mandatory Write Response Channel	—
BRESP_ctr	Out	2		b'00: OKAY[1] b'10: SLVERR[1] b'11: DECERR[1]
BREADY_ctr	In	1		—
ARVALID_ctr	In	1	AXI4 Mandatory Read Address Channel	—
ARREADY_ctr	Out	1		—
ARPROT_s	In	3		Not implemented.
ARADDR_s	In	32		—
RDATA_s	Out	32		—
RRESP_s	Out	2		b'00: OKAY[1] b'10: SLVERR[1] b'11: DECERR[1]
RLAST_s	Out	1		—
RVALID_s	Out	1		—
RREADY_s	In	1		—

Note:

1. Refer to the AMBA AXI Protocol Specification for more detailed descriptions of these responses.

2.4.4. Interrupt Interface

Table 2.6. Interrupt Ports

Name	Type	Width	Description
Irq	In	1	Peripheral interrupts.

2.5. Attribute Summary

The configurable attributes of the RISC-V IOPMP IP are described in Table 2.7.

The attributes can be configured through the Lattice Propel Builder software.

Table 2.7. Attributes Description

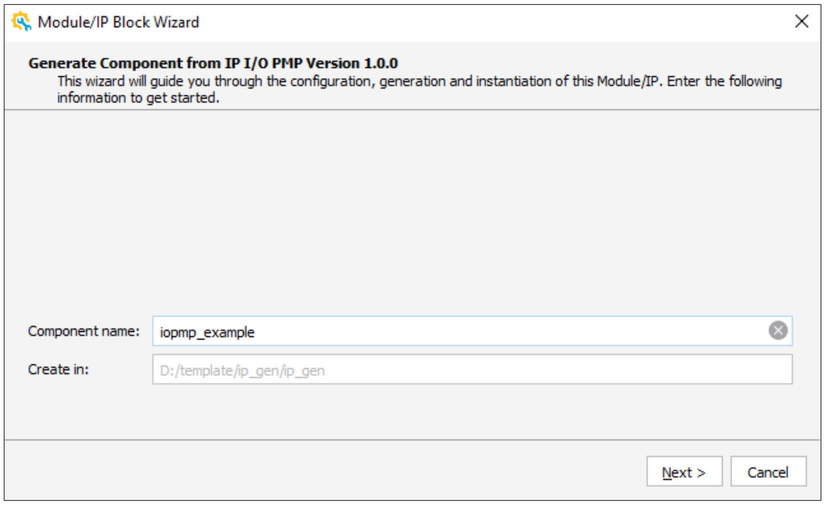
Attribute	Description
AXI ID Width	AXI ID width. Use for RRID.

3. RISC-V IOPMP IP Generation

This section provides information on how to generate the IOPMP IP module using the Lattice Propel Builder software.

To generate the IOPMP IP module:

1. In the Lattice Propel Builder software, create a new design. Select the IOPMP package.
2. Enter the component name. Click **Next**, as shown in Figure 3.1.



Generate Component from IP I/O PMP Version 1.0.0

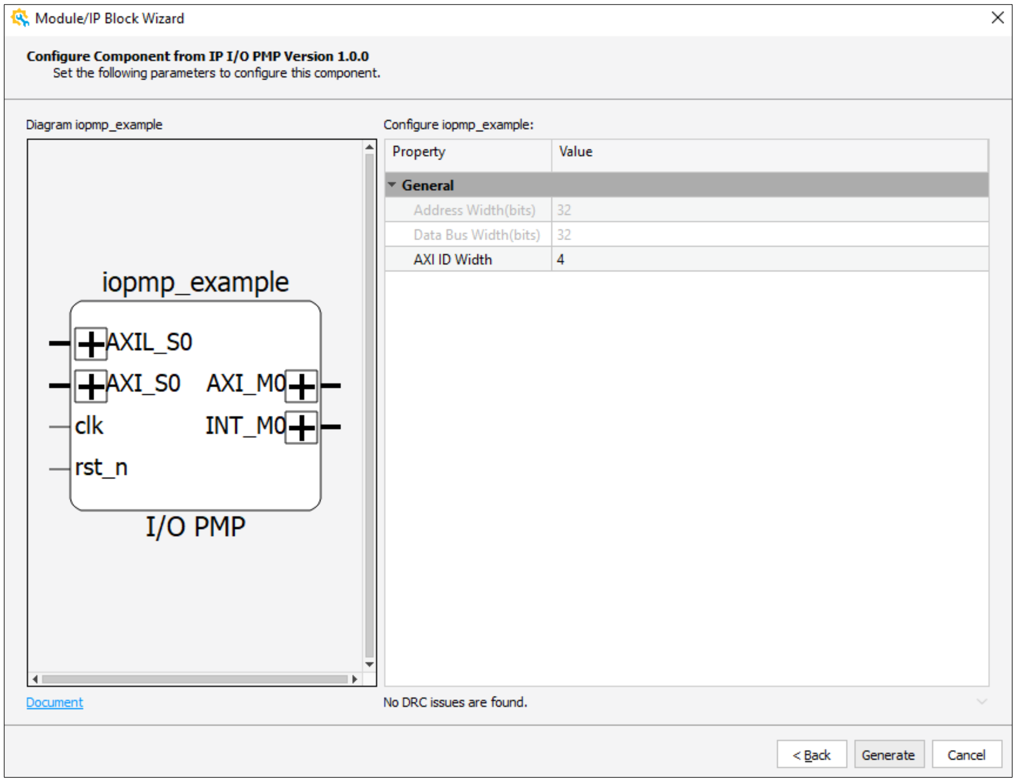
This wizard will guide you through the configuration, generation and instantiation of this Module/IP. Enter the following information to get started.

Component name: iopmp_example

Create in: D:/template/ip_gen/ip_gen

Figure 3.1. Entering Component Name

3. Configure the parameters as needed. Click **Generate** (Figure 3.2).



Configure Component from IP I/O PMP Version 1.0.0

Set the following parameters to configure this component.

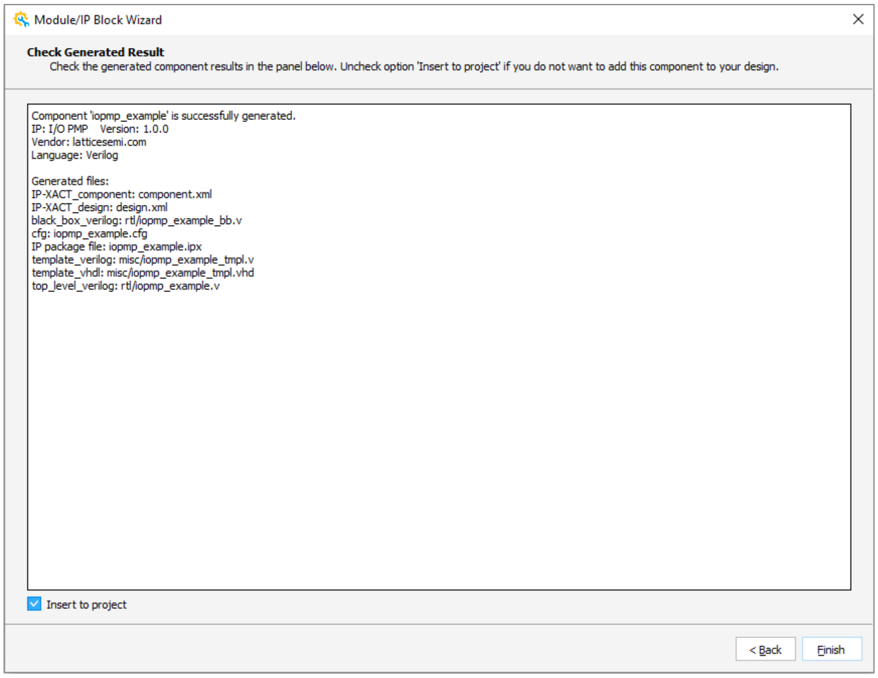
Configure iopmp_example:

Property	Value
General	
Address Width(bits)	32
Data Bus Width(bits)	32
AXI ID Width	4

No DRC issues are found.

Figure 3.2. Configuring Parameters

4. Verify the information. Click **Finish** (Figure 3.3).



Check Generated Result
Check the generated component results in the panel below. Uncheck option 'Insert to project' if you do not want to add this component to your design.

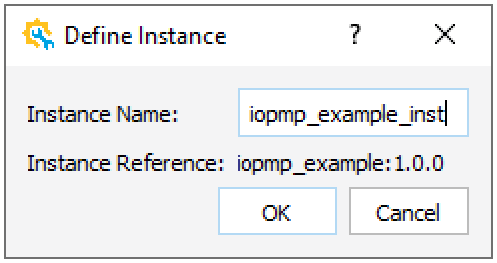
```
Component 'iopmp_example' is successfully generated.
IP: I/O PMP    Version: 1.0.0
Vendor: latticesemi.com
Language: Verilog

Generated files:
IP-XACT_component: component.xml
IP-XACT_design: design.xml
black_box_verilog: rtl/iopmp_example_bb.v
cfg: iopmp_example.cfg
IP package file: iopmp_example.ipx
template_verilog: misc/iopmp_example_tmpl.v
template_vhdl: misc/iopmp_example_tmpl.vhd
top_level_verilog: rtl/iopmp_example.v
```

☑ Insert to project

Figure 3.3. Verifying Results

5. Confirm or modify the module instance name. Click **OK** (Figure 3.4).



Instance Name: iopmp_example_inst

Instance Reference: iopmp_example:1.0.0

Figure 3.4. Specifying Instance Name

6. The IOPMP IP instance is successfully generated, as shown in Figure 3.5.

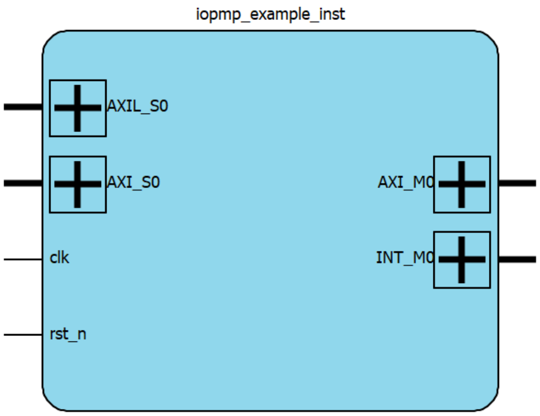


Figure 3.5. Generated Instance

Appendix A. Resource Utilization

Table A.1. Resource Utilization in CertusPro-NX Device

Configuration	LUTs	Registers	sysMEM EBRs
IOPMP	715	419	0

References

- Lattice Propel Builder 2024.2 User Guide (FPGA-UG-02219)
- Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039)
- AMBA AXI and ACE Protocol Specification

For more information, refer to:

- Lattice Propel web page
- Lattice Avant-E Family Devices web page
- Lattice Avant-G Family Devices web page
- Lattice Avant-X Family Devices web page
- MachXO5-NX Family Devices web page
- Certus-NX Family Devices web page
- CertusPro-NX Family Devices web page
- CrossLink-NX Family Devices web page
- Lattice Insights for Training Series and Learning Plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.0, IP v1.0.0, October 2024

Section	Change Summary
All	Production release.

www.latticesemi.com