Lattice Propel 2024.2

Release Notes

FPGA-AN-02095-1.0

December 2024

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

About Lattice Propel™ 2024.2

Welcome to the Lattice Propel 2024.2 design environment for Lattice FPGA system design. Lattice Propel is a complete set of graphical and command-line tools to create, analyze, compile, and debug both FPGA-based hardware and software processor systems.

What's New in Lattice Propel 2024.2

New Device Support

- Lattice ECP3
- Lattice iCE40 UltraPlus (iCE40UP)
- Lattice Certus™-N2 (LN2-CT)
- Lattice Avant™ (LAV-AT), Certus™-NX (LFD2NX), and MachXO5™-NX (LFMXO5) new device variants

Tools and Enhancements

- Supports license debugger in Propel Builder.
- Supports connections on individual ports within interfaces.
- Supports scalable design flow to create SoC with multiple peripherals based on RISC-V processors.
- Improved Builder Engine to only regenerate RTL when real modification on the design performed.
- Adds IP Wrapper Creator tool to generate an empty IP wrapper with pre-defined ports and interfaces.
- Supports IP generation before it gets packaged.
- Adds IP information hyperlink in the Module/IP Block Wizard.
- Supports IP availability check when opening an SoC design.
- Supports automatic download and installation of sever IP to local IP Catalog when generate IP.
- Improved Tcl inline help.
- Adds more TCL command supports.
- Supports logging Tcl history, organized by date, and displayed via a dedicated tab in Builder.
- Adds Project Summary tab in Builder GUI with SoC opened in Builder.
- Supports cacheable address range display in Address tab of Builder GUI.
- Adds a new RISC-V Nano SoC Project to support RISC-V Nano core.
- Adds version for newly added or updated templates.
- Supports register access test on peripherals for connectivity check in scalable SoC design.
- Supports custom application templates export as a zip archive.
- Supports CXU demonstration usage in updated *SHA3 CXU Template*.
- Supports standalone Code Coverage application template.
- Extends the ability of the Application Template Framework to support advanced SDK features.
- Supports SDK awareness of RISC-V extensions when creating or updating C/C++ projects.
- Adds "Browse for System Environment XML" in creating C/C++ project.
- Adds warning of inconsistent versions of Lattice Propel and Lattice Radiant™ software.
- Supports PUR_INST in Lattice Diamond® device simulation.
- Miscellaneous bug fixes and enhancements.

Key Features

Device Family Support

- Lattice LAV-AT (Avant)
- Lattice LFMXO5 (MachXO5™-NX)
- Lattice LIFCL (CrossLink™-NX)
- Lattice LFCPNX (CertusPro™-NX)
- Lattice LFMNX (Mach™-NX)
- Lattice LFD2NX (Certus-NX)
- Lattice MachXO3D™
- Lattice MachXO2™
- Lattice MachXO3L™
- Lattice MachXO3LF™
- Lattice ECP5U
- Lattice ECP5UM
- Lattice ECP5UM5G
- Lattice ECP3
- Lattice iCE40UP (iCE40 UltraPlus)
- Lattice LN2-CT (Certus-N2)

Processor Support

- RISC-V Micro Controller (MC)
- RISC-V State Machine (SM)
- RISC-V Real Time OS (RX)
- RISC-V NANO (NANO)
- Dual processors

Operating System Support

- Microsoft Windows 11 Pro (64-bit)
- Microsoft Windows 10 Enterprise (64-bit)
- Red Hat Enterprise Linux 7.9 (64-bit)
- Red Hat Enterprise Linux 8.8 (64-bit)
- Ubuntu 20.04 LTS (64-bit)
- Ubuntu 22.04 LTS (64-bit)

Lattice Propel SDK

- Integrated picolibc as the default standard C library to support three levels of printf.
- Built-in industry standard components and tools for embedded software development and debugging.
- Optimized project management flow for Lattice FPGA platform.
- Supports creating both C and C++ software projects based on Lattice SoC platform.
- Supports Lattice Diamond, Lattice Radiant, and Propel Builder bridges.
- Integrated GNU Debugger (GDB) and Open On-Chip-Debugging (OCD) with chained JTAG.
- Supports peripherals view with register description during debug session.
- Supports syntax highlighting for various development languages.
- Supports semihosting for On-Chip-Debugging and QEMU Virtual Platform.
- Supports multiple channels for On-Chip-Debugging.
- Supports “Attach to running target” for On-Chip-Debugging.
- Supports user custom application templates.
- Supports QEMU Virtual Platform.

Lattice Propel Builder

- Supports adding some Lattice Radiant foundation IP.
- Supports creating SoC and SoC verification project in project wizard Graphic User Interface (GUI).
- Supports Lattice Diamond, Lattice Radiant, QuestaSim, and Propel SDK bridges.
- Supports generating simulation environment, testbench, and script.
- Integrated QuestaSim Original Equipment Manufacturer (OEM).
- Supports creating more flexible AXI-based SoC.
- Supports reference IP RTL from user-specified library in IP Packager.
- Supports generation and reconfiguration of IP from centralized IP repository.
- Improves customized templates with constraint file included.
- Optimizes warnings and disables modifying Propel IP in Radiant software.

- Supports TCL in IP Packager.
- Supports GUI color customization options for schematic.
- Supports a new entry to distinguish SoC creation from custom templates or built-in templates.
- Supports generating default value in top RTL file for AMBA4 interface dangling input ports.
- Supports DRC of cacheable address range on SoC including RISC-V RX processor.
- Supports DRC of connection compatibility between RISC-V RX processor and TCM.
- Supports Verilog/VHDL for RTL module of glue logic.
- Supports friendlier interface names in IP Packager GUI Display.
- Supports license debugger tool.
- Supports Tcl mode entry for Builder and IP Packager.

IP Support

For IP support, refer to related IP user guides for detailed information.

SoC Template Design and System Simulation

- Provides template design *RISC-V MC SoC Project* on CertusPro-NX, Certus-NX, CrossLink-NX, MachXO5-NX.
- Provides template design *RISC-V RX SoC Projec*t on CertusPro-NX, Certus-NX, CrossLink-NX, MachXO5-NX.
- Provides template design *RISC-V MC SoC Project* on MachXO2.
- Provides template design *RISC-V SM SoC Project* on MachXO2.
- Provides template design *RISC-V Nano SoC Project* on CertusPro-NX, Certus-NX, CrossLink-NX.
- Provides MachXO3D template design, the *RISC-V MC SoC Project* and *Lattice Sentry RoT Project*.
- Provides Mach-NX template design, the *Lattice Sentry RoT Project (484)* and *Lattice Sentry RoT Project (256)*.
- Provides CertusPro-NX template design, the *RISC-V MC Dual Processor Project.*
- Provides CertusPro-NX template design, the *RISC-V RX SHA-3 CXU Project.*
- Provides Avant template design, the *RISC-V MC SoC Project.*
- Provides Avant template design, the *RISC-V RX SoC Project.*
- Provides ECP5 template design, the *RISC-V MC SoC Project.*
- Provides template design *Scalable RISC-V SoC Project.*
- Provides template design *Empty Project* to build from scratch.
- Supports functional verification using system-level simulation environment for templates.
- Supports DUT with one-level sub SBX in verification project.
- Simulation Tool Update.

Application Template Design

- Provides template design *Hello World Project.*
- Provides template design *FreeRTOS-LTS PMP-Blinky Project.*
- Provides template design *RISC-V RX Demo Project*.
- Provides template design *QEMU_helloworld Project*.
- Provides template design *Timing Profiling Project*.
- Provides template design *Code Coverage Project*.
- Provides template design *FreeRTOS-LTS minimal Project.*

Release Contents

- Propel_2024.2.exe (Windows 10/11 64-bit Operating System)
- Propel_2024.2_lin.run (Red Hat Enterprise Linux 64-bit & Ubuntu LTS Operating System)

Validation Platforms

- AVANT-AT-E Evaluation Board (REV D P/N: LAV-E70-EVN)
- CertusPro-NX Evaluation Board (REV A P/N: LFCPNX-EVN)
- Certus-NX Versa Evaluation Board (REV B P/N: LFD2NX-VERSA-EVN)
- CrossLink-NX Evaluation Board (REV B P/N: LIFCL-40-EVN)
- MachXO2 Breakout Board (REV B P/N: LCMXO2-7000HE-B-EVN)
- MachXO3D Breakout Board (REV A P/N: LCMXO3D-9400HC-B-EVN)
- LatticeECP3 Versa Evaluation Board (REV B P/N: LFE3-35EA-VERSA-EVN)
- ECP5 Versa Development Kit (Rev B LFE5UM-45F-VERSA-EVN)

System Requirements

The basic system requirements for Lattice Propel 2024.2 on Microsoft Windows and Linux Operating System (OS):

- Windows 10/11 64-bit OS
- Red Hat Enterprise Linux 64-bit OS (RHEL7.9/8.8)
- Ubuntu 20.04/22.04 LTS OS
- Free Disk Space: approximately 11 GB
- Network adapter and network connectivity for IP server access

Known Limitations

This release of Lattice Propel 2024.2 has the following limitations:

- DUT with one-level sub SBX is with limited support in verification project.
- Encrypted VHDL IP is only supported in Lattice Radiant flow, but not in Lattice Diamond flow.
- The MAX_PATH inside Windows file I/O API is restricted to 260 characters, but the usable path is even more constrained. The MAX_PATH must contain the drive letter and the NULL character to terminate the string correctly.
- Current OpenOCD cannot read Float Point Unit (FPU) registers, which makes Propel SDK unable to show FPU related register values.
- Lattice Propel software does not support HW-USBN-2A cable.

Known Issues

This release of Lattice Propel 2024.2 has the following known issues:

- An invalid read error occurs during the QEMU launch, but it does not actually affect functionality.
- Questa Sim vendor hasn't officially supported Ubuntu OS.

Note

It is recommended to use the same version of Lattice Radiant and Lattice Propel for best compatibility.

Technical Support

- For assistance, submit a technical support case at www.latticesemi.com/techsupport.
- For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/en/Support/AnswerDatabase.
- Previous Lattice Propel software versions are available on Software Archive page on Company Public website: https://www.latticesemi.com/Support/SoftwareArchive

Revision History

Revision 1.0, December 2024

Section	Change Summary
All	Production release.

www.latticesemi.com