RISC-V Nano CPU IP – Lattice Propel Builder 2024.2

IP Version: v1.0.0

User Guide

FPGA-IPUG-02271-1.0

October 2024

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Contents

Figures

Tables

Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AHB-L	Advanced High-performance Bus – Lite
CPU	Central Processing Unit
CSR	Control and Status Register
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
IP	Intellectual Property
IRQ	Interrupt Request
ISA	Instruction Set Architecture
LUT	Lookup-Table
PIC	Programmable Interrupt Controller
RISC-V	Reduced Instruction Set Computer-V (Five)
RV32I	RISC-V Integer Instruction Sets
WFI	Wait For Interrupt

1. Introduction

The Lattice Semiconductor RISC-V Nano CPU IP contains a 32-bit RISC-V processor core and a lightweight interrupt merge controller. The CPU core supports the RV32I instruction set and external interrupt. The interrupt controller submodule aggregates up to four external interrupt inputs into one external interrupt.

The design is implemented using Verilog HDL, and it can be configured and generated using the Lattice Propel™ Builder software. It supports Certus™-N2, iCE40 UltraPlus™, Lattice Avant™, MachXO5™-NX, CrossLink™-NX, Certus-NX, CertusPro™-NX, MachXO3D™, MachXO3™, and MachXO2™ FPGA devices.

1.1. Quick Facts

Table 1.1 presents a summary of the RISC-V Nano CPU IP.

Table 1.1 RISC-V Nano CPU IP Quick Facts

IP Requirements	Supported FPGA Family	Certus-N2, iCE40 Ultra Plus, Lattice Avant, MachXO5-NX, CrossLink-NX, Certus-NX, CertusPro-NX, MachXO3D, MachXO3L™, MachXO3LF™, and MachXO2
Resource Utilization	Targeted Devices	LN2-CT, iCE40UP, LAV-AT, LFMXO5, LIFCL, LFD2NX, LFCPNX, LAMXO3D, LCMXO3D, LCMXO3L, LAMXO3LF, LCMXO3LF, and LCMXO2
	Supported User Interfaces	AHB – Lite Interface
	Resources	See Table A.1, Table A.2, Table A.3, Table A.4, Table A.5, and Table A.6.
Design Tool Support	Lattice Implementation	IP v1.0.0 – Lattice Propel Builder 2024.2, Lattice Radiant™ Software 2024.2
	Simulation	For a list of supported simulators, see the Lattice Radiant and Lattice Diamond™ software user guide.

1.2. Features

The RISC-V Nano CPU IP has the following features:

- RV32I instruction set
- Five stage pipeline
- Supports the AHB-L bus standard for instruction/data ports.
- Lightweight interrupt merge controller module
- Interrupt and exception handling with the Machine mode in RISC-V privileged ISA Specification Revision 1.10
- The f_{max} is approximately 40 MHz in MachXO2 devices, 50 MHz in MachXO3D devices, and 100 MHz in CrossLink-NX devices, as tested on Hello World templates provided in the Lattice Propel design environment.

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal Names that end with:

- _n are active low.
- _i are input signals.
- _o are output signals.
- _io are bi-directional input/output signals.

1.4. Licensing and Ordering Information

The Nano CPU IP is provided at no additional cost with the Lattice Propel design environment. The IP can be fully evaluated in hardware without requiring an IP license string.

2. Functional Descriptions

2.1. Overview

The RISC-V Nano CPU IP processes data and instructions while monitoring external interrupts. As shown in Figure 2.1, the CPU IP has a 32-bit processor core and optional submodules. It uses one read-only AHB-L interface for instruction fetch and another AHB-L interface with Read/Write access for data access. Refer to Table 2.3 and Table 2.4. for the AHB-L Instruction Fetch and Data Accessing ports definition. The CPU core and AHB-L multiplexor run in the system clock domain.

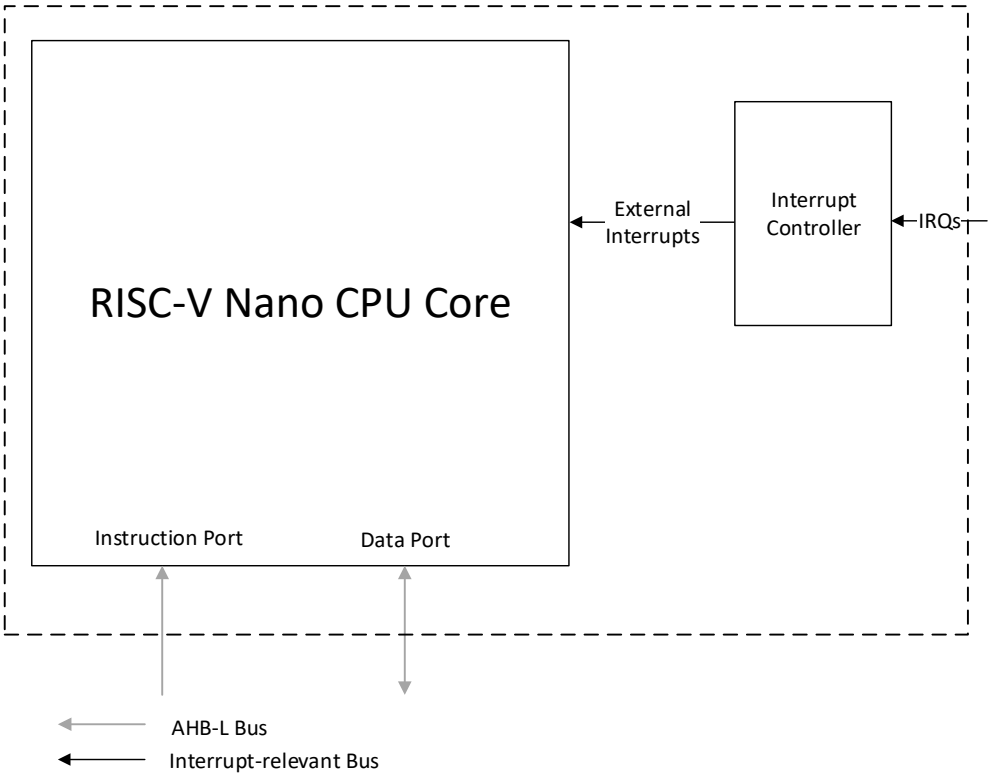

Figure 2.1. RISC-V Nano CPU IP Diagram

2.2. Modules Description

2.2.1. RISC-V Nano CPU Core

The processor core follows the RV32I instruction set. Figure 2.2 shows the processor core block diagram.

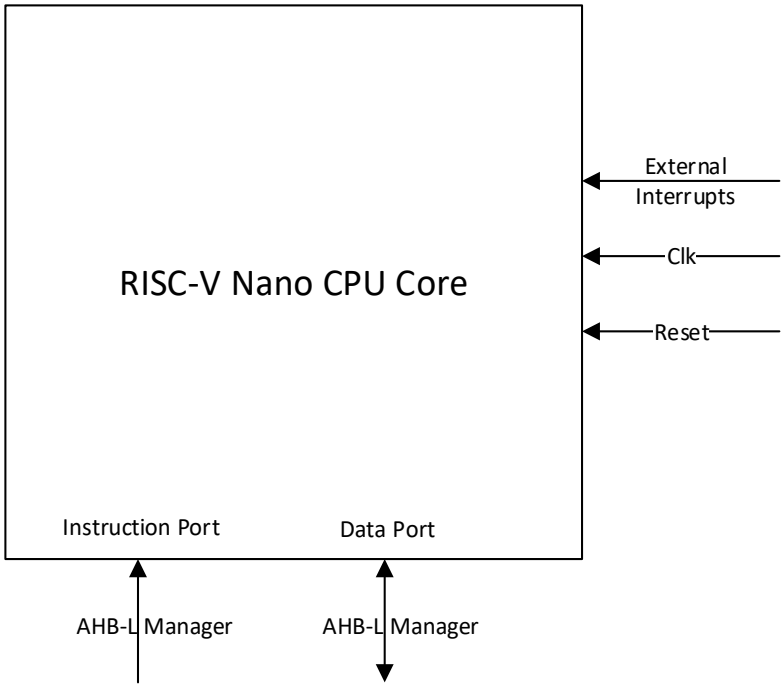

Figure 2.2. RISC-V Nano CPU Core Block Diagram

2.2.1.1. Interrupt

The core CPU's interrupts are level-sensitive and high active. A given interrupt should remain asserted until cleared by the corresponding interrupt service routine.

If an interrupt occurs, before jumping to the interrupt service routine, the processor core stops the prefetch stage and waits for all instructions in the later pipeline stages to complete their execution.

The processor iterates every interrupt source to find out which source is issuing an interrupt signal.

2.2.1.2. Exception

If an exception occurs, the processor core stops the corresponding instruction, flushes all previous instructions, and waits until the terminated instruction reaches the writeback stage before jumping to the exception service routine.

2.2.1.3. Low Power Mode

The processor core enters into the low power mode with the Wait For Interrupt (WFI) instruction. The program counter halts during low power mode, and the processor wakes up if there is external/timer interrupt.

2.2.1.4. Reset Vector

The reset vector of the processor is 0x0000_0000 and it is fixed.

2.2.1.5. Control and Status Registers

The processor core supports the Control and Status Registers (CSRs) listed in Table 2.1.

Table 2.1. RISC-V Nano CPU Core Control and Status Registers

CSR Number	CSR Name	Access	Fields
0x300	Machine Status (mstatus)	read/write	bits[12:11]: mpp, privilege mode before entering a trap. This should always be 2'b11 in the machine mode in this CPU core. bit [7]: mpie, mie before entering a trap. Updated to the mie value when entering a trap. bit [3]: mie, global interrupt enable.
0x304	Machine Interrupt Enable (mie)	read/write	bit[11]: meie, machine mode external interrupt enable. bit[7]: mtie, machine mode timer interrupt enable. bit[3]: msie, machine mode software interrupt enable.
0x305	Machine Trap-Vector Base-Address (mtvec)	read-only	bit[31:2]: trap vector base address, 4-byte aligned. bit[1:0]: trap vector mode. All traps set the program counter to the base address in the RISC-V Nano CPU core.
0x340	Machine Scratch (mscratch)	read-write	bits[31:0]: scratch register for machine trap handlers.
0x341	Machine Exception Program Counter (mepc)	read-write	bits[31:0]: when a trap is taken into machine mode, mepc is used to store the address of the instruction that encounters the exception.
0x342	Machine Cause (mcause)	read-only	bit[31]: 1'b1 – interrupt, 1'b0 – exception bit[3:0]: exception code For interrupt: • 3 – machine software interrupt • 7 – machine timer interrupt • 11 – machine external interrupt For exception: • 0 – instruction address misaligned • 1 – instruction access fault • 2 – illegal instruction • 4 – load address misaligned • 5 – load access fault
0x343	Machine Trap Value (mtval)	read-only	bits[31:0]: when a hardware breakpoint is triggered, or an instruction fetch, load, or store address is misaligned, or access exception occurs, mtval is written with the fault address. It may also be written with an illegal instruction when an illegal instruction occurs.

2.2.1.6. System Reset Output

The system_resetn_o signal is driven by the input reset signal, rst_n_i.

2.3. Signal Description

Table 2.2. to Table 2.5. list the ports of the CPU soft IP in different categories.

2.3.1. Clock and Reset

Table 2.2. Clock and Reset Ports

Name	Direction	Width	Description
clk_i	In	1	RISC-V soft IP clock.
rst_n_i	In	1	Global reset, active low.
system_resetn_o	Out	1	Combined global reset, active low.

2.3.2. Instruction and Data Interface

Table 2.3. Instruction Ports

Name	Direction	Width	Description
AHBL_M0_INSTR – HADDR	Out	32	—
AHBL_M0_INSTR – HWRITE	Out	1	Fixed to 1'b0.
AHBL_M0_INSTR – HSIZE	Out	3	Fixed to 3'b010.
AHBL_M0_INSTR – HPROT	Out	4	Fixed to 4'b1110.
AHBL_M0_INSTR – HTRANS	Out	2	—
AHBL_M0_INSTR – HBURST	Out	3	Fixed to 3'b000.
AHBL_M0_INSTR – HMASTLOCK	Out	1	Fixed to 1'b0.
AHBL_M0_INSTR – HWDATA	Out	32	—
AHBL_M0_INSTR – HRDATA	In	32	—
AHBL_M0_INSTR – HREADY	In	1	—
AHBL_M0_INSTR – HRESP	In	1	—

Table 2.4. Data Ports

Name	Direction	Width	Description
AHBL_M1_DATA – HADDR	Out	32	—
AHBL_M1_DATA – HWRITE	Out	1	—
AHBL_M1_DATA – HSIZE	Out	3	—
AHBL_M1_DATA – HPROT	Out	4	Fixed to 4'b1111.
AHBL_M1_DATA – HTRANS	Out	2	—
AHBL_M1_DATA – HBURST	Out	3	Fixed to 3'b000.
AHBL_M1_DATA – HMASTLOCK	Out	1	—
AHBL_M1_DATA – HSEL	Out	1	—
AHBL_M1_DATA – HWDATA	Out	32	—
AHBL_M1_DATA – HRDATA	In	32	—
AHBL_M1_DATA – HREADY	In	1	—
AHBL_M1_DATA – HRESP	In	1	—

For more information, refer to AMBA 3 AHB-Lite Protocol V1.0.

2.3.3. Interrupt Interface

Table 2.5. Interrupt Ports

Name	Type	Width	Description
IRQ_Sx	In	1–4	Peripheral interrupts

2.4. Attribute Summary

The configurable attributes of the RISC-V Nano CPU IP are shown in Table 2.6 and described in Table 2.7.

The attributes can be configured through the Lattice Propel Builder software.

Table 2.6. Configurable Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
General			
COMPRESS_EXT	Checked, Unchecked	Unchecked	—
Number of Interrupt Requests	1–4	4	Enabled when PIC Enable is enabled.
PIC Enable	Checked, Unchecked	Checked	—

Table 2.7. Attributes Description

Attribute	Description
COMPRESS_EXT	1: Enable compress extension for the CPU. 0: Disable compress extension for the CPU.
Number of Interrupt Requests	Specify the number of peripheral interrupts.
PIC Enable	1: Enable PIC. 0: Disable PIC.

3. RISC-V Nano CPU IP Generation

This section provides information on how to generate the Nano CPU IP using the Lattice Propel Builder software.

To generate the CPU IP module:

1. In the Lattice Propel Builder software, create a new design. Select the CPU package.
2. Enter the component name. Click **Next**, as shown in Figure 3.1.

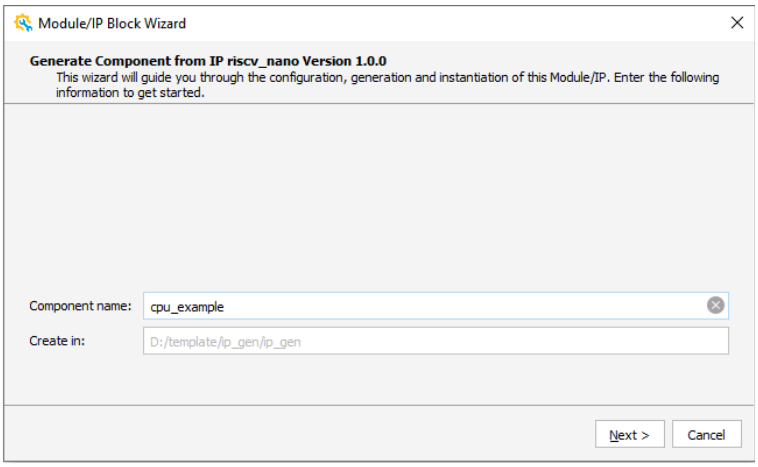

Figure 3.1. Entering Component Name

3. Configure the parameters as needed. Click **Generate**.

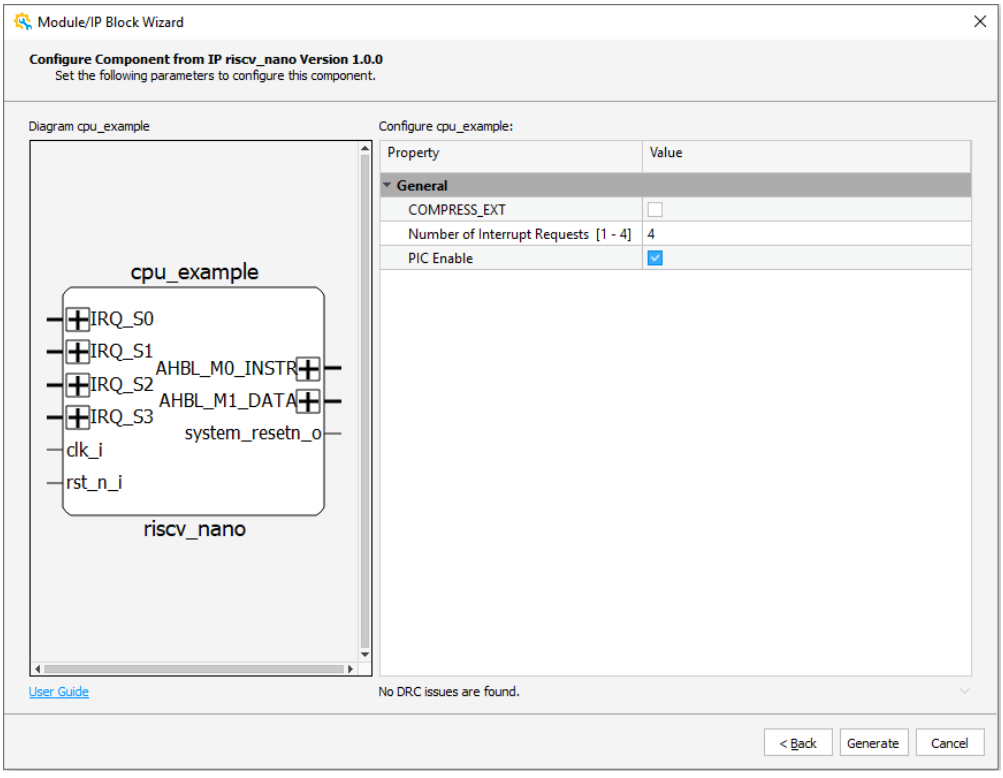

Figure 3.2. Configuring Parameters

4. Verify the information. Click **Finish**.

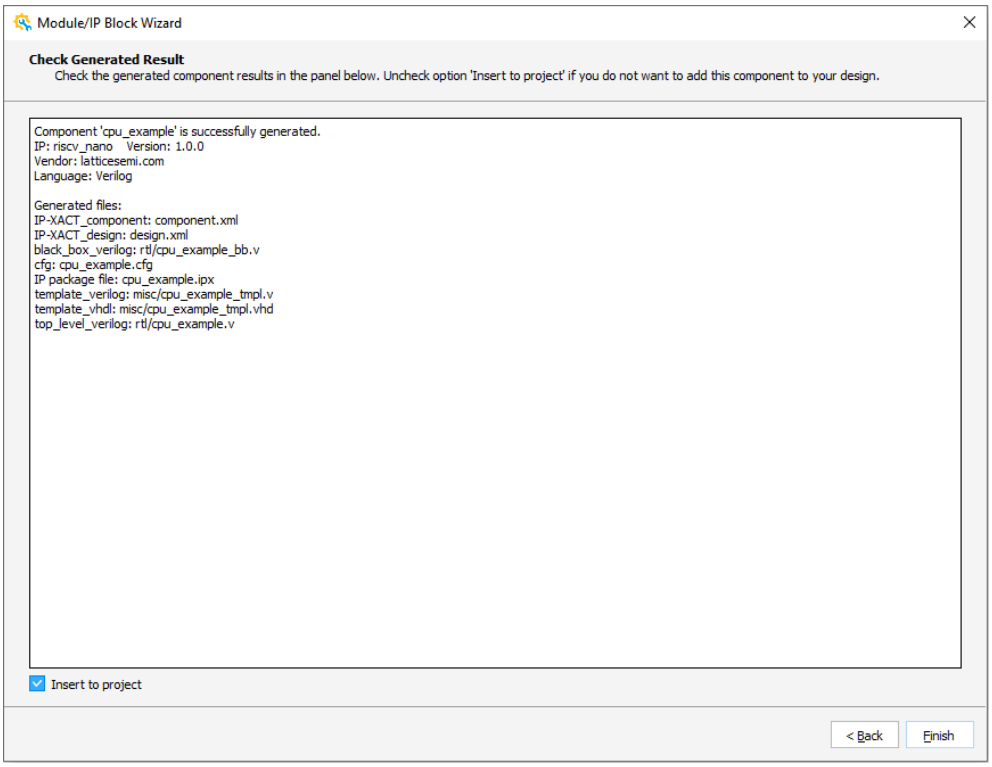

Figure 3.3. Verifying Results

5. Confirm or modify the module instance name. Click **OK**.

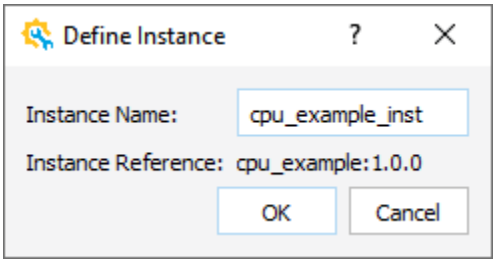

Figure 3.4. Specifying Instance Name

6. The CPU IP instance is successfully generated, as shown in Figure 3.5.

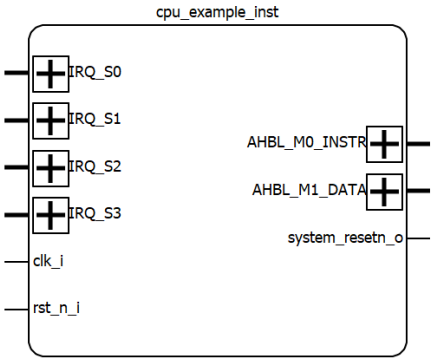

Figure 3.5. Generating CPU IP Instance

Appendix A. Resource Utilization

Table A.1. Resource Utilization in MachXO2 Device

Configuration	LUTs	Registers	sysMEM EBRs
Processor core only	293	188	1
Processor core + PIC	283	188	1
Processor core + COMPRESS_EXT	501	206	1
Processor core + COMPRESS_EXT + PIC	492	206	1

Note: Resource utilization characteristics are generated using Lattice Diamond software.

Table A.2. Resource Utilization in MachXO3D Device

Configuration	LUTs	Registers	sysMEM EBRs
Processor core only	317	188	1
Processor core + PIC	323	188	1
Processor core + COMPRESS_EXT	535	206	1
Processor core + COMPRESS_EXT + PIC	529	206	1

Note: Resource utilization characteristics are generated using Lattice Diamond software.

Table A.3. Resource Utilization in CrossLink-NX Device

Configuration	LUTs	Registers	sysMEM EBRs
Processor core only	328	188	1
Processor core + PIC	338	188	1
Processor core + COMPRESS_EXT	621	407	1
Processor core + COMPRESS_EXT + PIC	627	408	1

Note: Resource utilization characteristics are generated using Lattice Radiant software.

Table A.4. Resource Utilization in CertusPro-NX Device

Configuration	LUTs	Registers	sysMEM EBRs
Processor core only	306	175	1
Processor core + PIC	332	188	1
Processor core + COMPRESS_EXT	599	394	1
Processor core + COMPRESS_EXT + PIC	603	407	1

Note: Resource utilization characteristics are generated using Lattice Radiant software.

Table A.5. Resource Utilization in Lattice Avant Device

Configuration	LUTs	Registers	sysMEM EBRs
Processor core only	313	199	1
Processor core + PIC	320	198	1
Processor core + COMPRESS_EXT	632	400	1
Processor core + COMPRESS_EXT + PIC	648	406	1

Note: Resource utilization characteristics are generated using Lattice Radiant software.

Table A.6. Resource Utilization in Lattice iCE40UP Device

Configuration	LUTs	Registers	sysMEM EBRs
Processor core only	501	198	1
Processor core + PIC	504	200	1
Processor core + COMPRESS_EXT	804	228	1
Processor core + COMPRESS_EXT + PIC	845	229	1

Note: Resource utilization characteristics are generated using Lattice Radiant software.

References

- Lattice Propel Builder 2024.2 User Guide (FPGA-UG-02219)
- AMBA 3 AHB-Lite Protocol V1.0
- RISC-V Privileged Specification (20211203)
- RISC-V Instruction Set Manual (20190608)
- Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039)

For more information, refer to:

- Lattice Propel Design Environment web page
- Lattice Avant-E Family Devices web page
- Lattice Avant-G Family Devices web page
- Lattice Avant-X Family Devices web page
- MachXO5-NX Family Devices web page
- Certus-NX Family Devices web page
- CertusPro-NX Family Devices web page
- CrossLink-NX Family Devices web page
- MachXO3D Family Devices web page
- MachXO3 Family Devices web page
- MachXO2 Family Devices web page
- iCE40 UltraPlus web page
- Lattice Insights for Training Series and Learning Plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.0, IP v1.0.0, October 2024

Section	Change Summary
All	Production release.

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