M-PESTI Initiator IP

IP Version: v2.1.0

Release Notes

FPGA-RN-02005-1.6

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1. Introduction

This document contains the Release Notes for the M-PESTI Initiator IP and M-PESTI Initiator Driver. This IP is OCP Ready™. For specific details about the IP and driver, refer to the following:

- M-PESTI Initiator IP User Guide (FPGA-IPUG-02258)
- M-PESTI Initiator IP web page
- M-PESTI Initiator Driver API Reference (FPGA-TN-02413)

M-PESTI Initiator IP v2.1.0

Software	Software Version	Summary of Changes
Lattice Radiant™	2026.1	• Added support for MachXO4 devices. • Driver update release: v25.02.01.

M-PESTI Initiator IP v2.0.1

Software	Software Version	Summary of Changes
Lattice Radiant™	2025.2	Driver update release: v25.02.00.

M-PESTI Initiator IP v2.0.0

Software	Software Version	Summary of Changes

Lattice Radiant	2025.2	• Added support for specification version 1.2 of M-PESTI protocol.
		• Added optional discovery phase bypass feature support.
		• Added optional active phase Packet Error Checking (PEC) support.
		• Modified the following GUI parameters:
		  • Added Specification Version Support
		  • Added IP Block ID
		  • Added IP Block Version (Major)
		  • Added IP Block Version (Minor)
		  • Added IP Block Version
		  • Added Presence Detection Timeout Enable
		  • Added Discovery Bypass Enable (in hex)
		  • Added Active Phase PEC Enable (in hex)
		  • Updated TDBreak Assertion Time Presence Detection Timeout (us) (multiples of 2us) to Presence Detection Timeout (us) (multiples of 2us)
		  • Updated Static Discovery Payload Size to Maximum Static Discovery Payload Size
		• Changed default value of Number of Target Devices from 1 to 8.
		• Changed default value of Maximum Static Discovery Payload Size GUI parameter from 8 to 16 and removed selectable value 8.
		• Removed selectable options for Maximum User Receive Byte Size GUI parameter and fixed it to 16.
		• Modified the following register address mapping:
		  • Added IP Information register 0x0_0000
		  • Added Configuration 0 register 0x0_0004
		  • Added Configuration 1 register 0x0_0008
		  • Added Global Software Reset register 0x0_0010
		  • Added Discovery Payload: Page Select register 0x0_0014
		  • Removed Interrupt Status register 0x0_0018
		  • Removed Interrupt Enable register 0x0_001C
		  • Removed Interrupt Set register 0x0_0020
		  • Added User Command Status 0x0_0020

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Software	Software Version	Summary of Changes
		• Changed User Command register address from 0x0_0104 to 0x0_0024. • Changed User Write Data register address from 0x0_0108 to 0x0_0028. • Changed User Read Data register address from 0x0_010C to 0x0_002C. • Changed Clock Configuration register address from 0x0_0000 to 0x1_0000. • Changed Software Reset register address from 0x0_0004 to 0x1_0004. • Added Global Interrupt Status register 0x1_0008. • Added Global Interrupt Enable register 0x1_000C. • Added Global Interrupt Set register 0x1_0010. • Added User Command Interrupt Enable register 0x1_0014. • Added User Command Interrupt Set register 0x1_0018. • Changed Secondary Wire Control Status register address from 0x0_0040 to 0x1_0040. • Changed Secondary Wire Select register address from 0x0_0044 to 0x1_0044. • Removed M-PESTI Target 0 Status register 0x0_0400+(N*16). • Removed M-PESTI Target 0 Control Status register 0x0_0404+(N*16). • Added MPESTI Target N Error, Status, Control and Configuration 0x1_0000+(N*4). • Moved Target Payload from 0x2_0000+(Maximum Static Discovery Payload Size * N) to 0x0_1000+(Maximum Static Discovery Payload Size * N). • Added M-PESTI Target N Virtual Wire Input 0x3_0000+(N*32). • Added M-PESTI Target N Virtual Wire Output 0x3_0010+(N*32). • Added M-PESTI Target N Status 0x4_0000+(N*16). • Changed M-PESTI Target N Virtual Wire Configuration register address from 0x0_0408+(N*16) to 0x4_0004+(N*4). • Enhanced customer testbench.

M-PESTI Initiator IP v1.3.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1	• Added support for LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T devices. • Initial driver release v25.01.00.

M-PESTI Initiator IP v1.2.0

Software	Software Version	Summary of Changes

Lattice Radiant	2025.1	• Fixed APB Data Width to 32 bits.
		• Added support for the programmable number of virtual wire input and output bytes.
		• Added support for the virtual wire as ports for each target.
		• Added support for multiple virtual wire bytes.
		• Added ports for the virtual wire as ports.
		• Modified the following register address mapping:
		  • Added M-PESTI Target Virtual Wire Configuration (0x408*N+16) given Enable Programmable Virtual Wire Bytes attribute is checked.
		  • Modified Virtual Wire Input register address range. This is dependent on the configured Number of Virtual Wire Input Bytes.
		  • Modified Virtual Wire Output register address range. This is dependent on the configured Number of Virtual Wire Output Bytes.
		• Enhanced customer testbench.

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M-PESTI Initiator IP v1.1.0

Software	Software Version	Summary of Changes

Lattice Radiant	2024.2	• Added device support for MachXO3D™, MachXO3™, Mach-NX™, Certus™-N2, and Lattice Avant™ devices.
		• Enabled dynamic payload size capability.
		• Enhanced maximum target supported from 32 to 64.
		• Enabled support for the source and destination cable coupling discovery feature.
		• Added Allow Multiple User Receive Bytes and Maximum User Receive Byte Size GUI parameters.
		• Added ports for the source and destination cable coupling discovery feature.
		• Modified maximum System Clock Frequency from 50 MHz to 100 MHz.
		• Added TDBREAK Assertion Time configurable condition of multiples of 2us.
		• Modified the following register address mapping:
		  • Corrected clock pulse width bit fields of Configuration register (0x004) from [7:1] to [7:0].
		  • Added Secondary Wire Control Status (0x040) and Secondary Wire Select (0x044) registers.
		  • Added Target Select (0x100) register, removed from User Command register.
		  • Moved User Command register from 0x00C to 0x104.
		  • Moved User Write Data register from 0x010 to 0x108.
		  • Moved User Read Data register from 0x014 to 0x10C.
		  • Moved M-PESTI Target Status Register offset from 0x040 to 0x400.
		  • Moved M-PESTI Target Control Status Register offset from 0x044 to 0x404.
		  • Moved M-PESTI Target Virtual Wire Out Register offset from 0x048 to 0xC00.
		  • Moved M-PESTI Target Virtual Wire In Register offset from 0x04C to 0x800.
		  • Moved M-PESTI Target Payload offset from 0x800 to 0x1000.
		  • Changed User Command register bit 6 behavior when the Allow Multiple User Receive Bytes parameter is disabled.
		• Enhanced round robin servicing supporting multiple targets.
		• Enhanced user command, broadcast, and abort support.
		• Changed internal RAM from pmi_ram_dp to pmi_ram_dp_true.
		• Enhanced customer testbench.

M-PESTI Initiator IP v1.0.0

Software	Software Version	Summary of Changes
Lattice Radiant	2024.1	Initial release.

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References

- M-PESTI Initiator IP User Guide (FPGA-IPUG-02258)
- M-PESTI Initiator IP web page
- M-PESTI Initiator Driver API Reference (FPGA-TN-02413)
- Open Compute Project® web page
- Avant-E web page
- Avant-G web page
- Avant-X web page
- MachXO5-NX web page
- MachXO4 web page
- MachXO3D web page
- MachXO3 web page
- Mach-NX web page
- Lattice Radiant Software web page
- Lattice Propel Design Environment web page
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