



JESD204B IP

IP Version: v1.3.0

User Guide

FPGA-IPUG-02259-1.4

April 2026

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Inclusive Language

This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language [FAQ 6878](#) for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Abbreviations in This Document

A list of abbreviations used in this document.

| Abbreviation | Definition |
|--------------|---|
| ADC | Analog-to-Digital Converter |
| AXI | Advanced eXtensible Interface |
| CGS | Code Group Synchronization |
| CMOS | Complementary Metal Oxide Semiconductor |
| CSR | Control and Status Register |
| DAC | Digital-to-Analog Converter |
| DUT | Device Under Test |
| DW | Double Word |
| EBR | Embedded Block RAM |
| EOF | End of Frame |
| EOMF | End of Multiframe |
| ES | Engineering Sample |
| FMC | FPGA Mezzanine Card |
| FPGA | Field Programmable Gate Array |
| FSM | Finite State Machine |
| FTDI | Future Technology Devices International |
| GUI | Graphical User Interface |
| ILA | Initial Lane Alignment |
| ILAS | Initial Lane Alignment Sequence |
| IP | Intellectual Property |
| IQ | In-Phase (I) Component and Quadrature (Q) Component |
| LFC | Local Frame Clock |
| LMFC | Local Multiframe Clock |
| LMMI | Lattice Memory Mapped Interface |
| LUT4 | 4-bit Look-up Table |
| LVDS | Low-Voltage Differential Signaling |
| MPCS | Multi-protocol Physical Coding Sublayer |
| PFU | Programmable Functional Unit |
| PHY | Physical |
| RBD | Release Buffer Delay |
| Rx | Receiver |
| SERDES | Serializer/Deserializer |
| SOF | Start of Frame |
| SOMF | Start of Multiframe |
| Tx | Transmitter |
| /A/ | Control character K28.3 |
| /F/ | Control character K28.7 |
| /K/ | Control character K28.5 |
| /Q/ | Control character K28.4 |
| /R/ | Control character K28.0 |

1. Introduction

JESD204B is a high-speed serial interface used between data converters, such as analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), and the FPGA device to replace traditional interfaces, such as CMOS and LVDS. With converter sampling rates and data throughput increasing, the JESD204B interface offers advantages in terms of size, cost, and speed.

1.1. Overview of the IP

The Lattice JESD204B IP supports both the Tx and Rx directions, with corresponding PHY, link, and embedded transport layers, on Lattice FPGA devices.

1.2. Quick Facts

Table 1.1. Summary of the JESD204B IP

| | | |
|-----------------------------|--------------------------|---|
| IP Requirements | Supported Devices | CertusPro™-NX, Lattice Avant™-G ¹ , Avant-X ¹ , Certus™-N2 (except LN2-CT-20ES) |
| | IP Changes ² | Refer to the JESD204B IP Release Notes (FPGA-RN-02006) . |
| Resource Utilization | Supported User Interface | AXI4-Lite, AXI4-Stream |
| | Resources | Refer to Appendix A for resource utilization samples. |
| Design Tool Support | Lattice Implementation | IP Core v1.3.0 – Lattice Radiant™ Software 2025.2 Lattice Propel™ Design Environment 2025.2 |
| | Synthesis | Synopsys® Synplify Pro® for Lattice |
| | Simulation | Refer to the Lattice Radiant Software User Guide for the list of supported simulators. |
| Driver Support | API Reference | Refer to the JESD204B Driver API Reference (FPGA-TN-02412) . |

Notes:

1. Excluding engineering sample (ES) devices.
2. In some instances, the IP may be updated without changes to the user guide. This user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

1.3. IP Support Summary

Table 1.2. JESD204B IP Support Readiness

| Device Family | Simulation Provided | Radiant Timing Model |
|------------------|---------------------|----------------------|
| CertusPro-NX | Yes | Final |
| Avant-G, Avant-X | Yes | Preliminary |
| Certus-N2 | Yes | Preliminary |

The example design for the JES204B IP allows for simulation and deployment to development boards for testing. Refer to the [Example Design](#) section for more details on how to run the example design on hardware and simulation.

1.4. Features

Key features of the JESD204B IP include:

- JESD204B subclass 0 and 1
- Lane rates up to:
 - 8.192 Gb/s for CertusPro-NX devices
 - 9.8304 Gb/s for Avant-G, Avant-X, and Certus-N2 devices
- Configurable lane counts of:
 - 1, 2, or 4 lanes for CertusPro-NX and Certus-N2 devices

- 1, 2, 4, or 8 lanes for Avant-G and Avant-X devices
- Scrambler and descrambler support
- SYSREF modes: One-shot and periodic (always)
- Link layer and PHY layer separation modes
- Configurable embedded transport layer

1.5. Licensing and Ordering Information

An IP specific license string is required to enable full use of the JESD204B IP in a complete, top-level design.

The IP can be fully evaluated through functional simulation and implementation (synthesis, map, place and route) without an IP license string. This IP supports Lattice’s IP hardware evaluation capabilities. You can create versions of the IP to operate in hardware for a limited time (approximately four hours) without requiring an IP license string. A license string is required to enable timing simulation and to generate a bitstream file that does not include the hardware evaluation timeout limitation.

For more information about pricing and availability of the JESD204B IP, contact your [local Lattice Sales Office](#).

1.5.1. Ordering Part Number

Table 1.3. Ordering Part Number

| Device Family | Part Number | |
|---------------|--------------------|-----------------------|
| | Single Seat Annual | Single Seat Perpetual |
| CertusPro-NX | JESD-204B-CPNX-US | JESD-204B-CPNX-UT |
| Avant-G | JESD-204B-AVG-US | JESD-204B-AVG-UT |
| Avant-X | JESD-204B-AVX-US | JESD-204B-AVX-UT |
| Certus-N2 | JESD-204B-CN2-US | JESD-204B-CN2-UT |

1.6. Minimum Device Requirements

The minimum device requirements for the JESD204B IP with selected link speeds are as follows:

Table 1.4. Minimum Device Requirements for JESD204B IP

| Device Family | Link Speed | Speed Grades |
|------------------|-------------|-------------------------|
| CertusPro-NX | 8.192 Gb/s | 9_High-Performance_1.0V |
| | 7 Gb/s | 8_High-Performance_1.0V |
| | 6 Gb/s | 7_High-Performance_1.0V |
| | 6 Gb/s | 9_Low-Power_1.0V |
| | 5 Gb/s | 8_Low-Power_1.0V |
| | 4 Gb/s | 7_Low-Power_1.0V |
| Avant-G, Avant-X | 9.8304 Gb/s | 2 and 3 |
| | 8.5 Gb/s | 1 |
| Certus-N2 | 9.8304 Gb/s | 2 and 3 |
| | 8.5 Gb/s | 1 |

1.7. Naming Conventions

1.7.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.7.2. Signal Names

Signal names that end with:

- `_n` are active low signals (asserted when value is logic 0)
- `_i` are input signals
- `_o` are output signals

1.7.3. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

2. Functional Description

2.1. IP Architecture Overview

The JESD204B IP supports parameterizable PHY layer, link layer, and embedded transport layer, thus providing the capability for custom configuration based on application needs. Figure 2.1 shows the block diagram of the JESD204B IP.

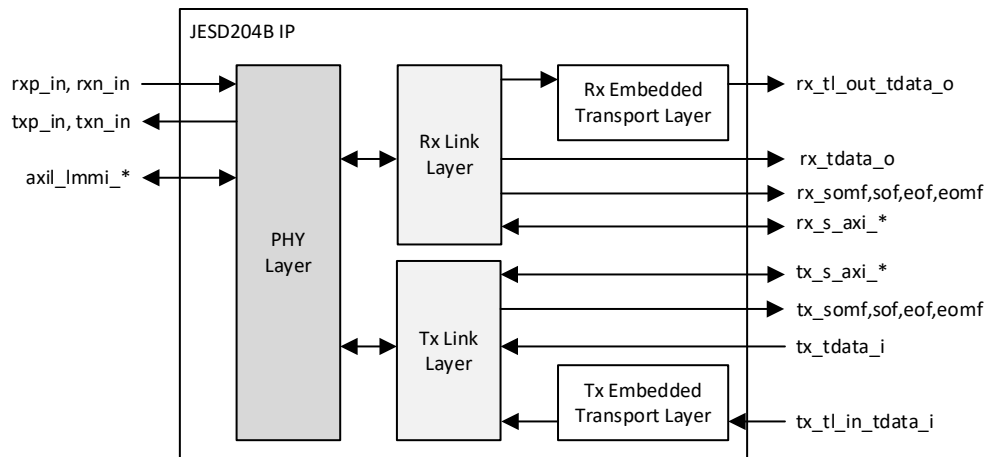


Figure 2.1. JESD204B IP Block Diagram

2.2. Rx Link Layer

Figure 2.2 shows the JESD204B Rx link layer block diagram. An 8b10b decoder is implemented in the PHY layer, which outputs decoded parallel symbols to the Rx multilane alignment module in the Rx link layer.

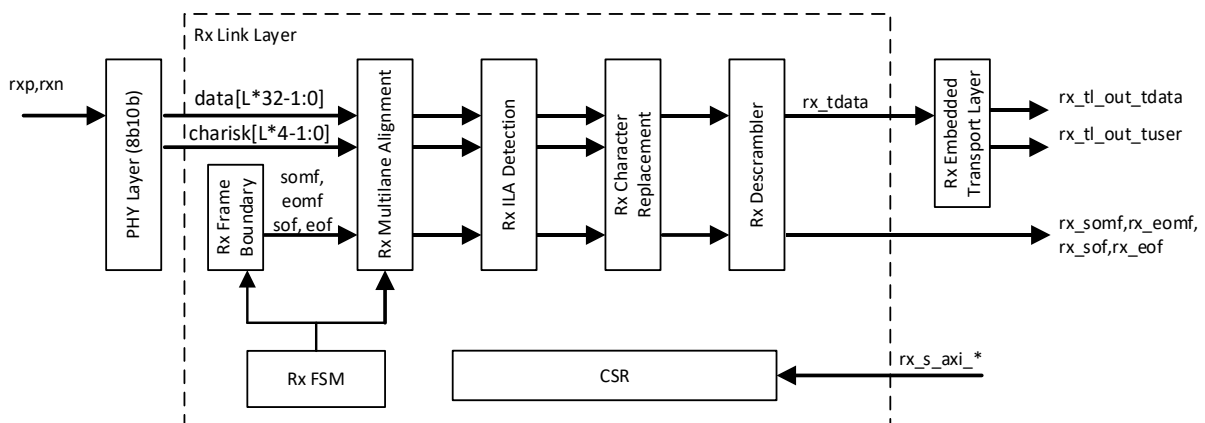


Figure 2.2: JESD204B Rx Link Layer Block Diagram

2.2.1. Frame Boundary and State Machine

The Rx frame boundary module regenerates the local frame clock (LFC) and local multiframe clock (LMFC) in the form of SOF-EOF and SOMF-EOMF close loops, respectively. For subclass 1, the module detects SYSREF assertion as a condition to generate the frame clock. For subclass 0, the module generates the frame clock upon exiting reset.

Figure 2.3 illustrates the LMFC correlation with Rx data frame. SOF to EOF indicates the number of octets per frame (F) while SOMF to EOMF indicates the number of frames per multiframe (K) and number of octets per multiframe (F × K). SOMF is aligned with the LMFC arrow as illustrated in Figure 2.3.

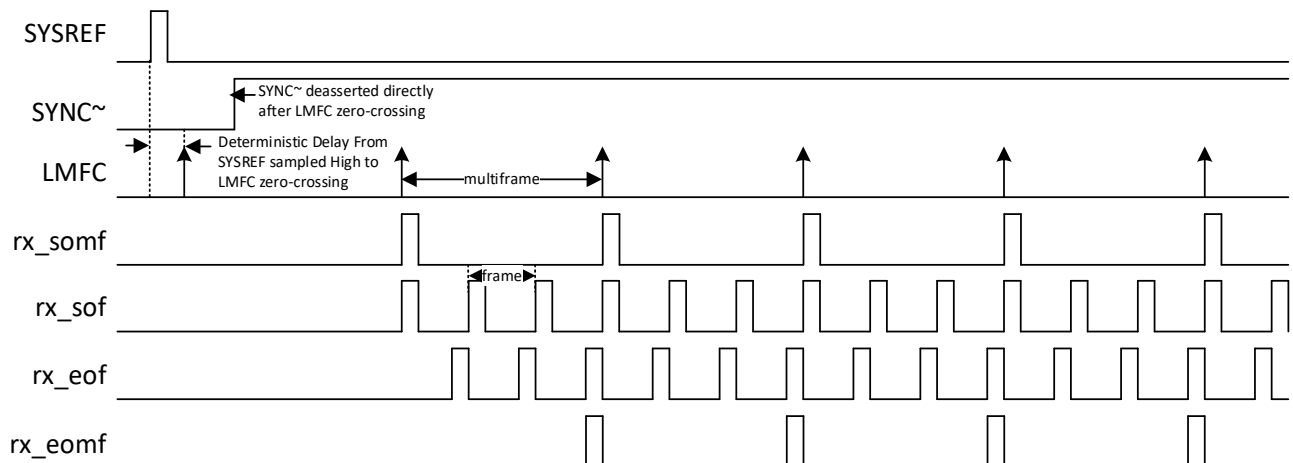


Figure 2.3. Timing Diagram Illustration for LMFC and Rx Frames Interface

The Rx finite state machine (FSM) module indicates the current Rx state through rx_state_o. Table 2.1 shows the four JESD204B Rx states. The rx_sync signal is generated when the link enters the ILA state.

Table 2.1. JESD204B Rx States

| Port | Bit Setting | State | Description |
|------------|-------------|-------|--|
| rx_state_o | 2'd0 | IDLE | Default state. Link waits for Rx SYSREF detection before entering code group synchronization (CGS) state. |
| | 2'd1 | CGS | SYSREF detected and link is detecting the CGS pattern. Once the CGS pattern for all lanes are detected, link enters ILA state. |
| | 2'd2 | ILA | Link is detecting the initial lane alignment sequence (ILAS) symbol and decoding the JESD204B ILA configuration. Link waits for all ILAS multiframe symbols (default is four multiframe symbols) before entering DATA state. |
| | 2'd3 | DATA | Rx link is receiving user data. Link enters IDLE state when: <ul style="list-style-type: none"> Link reinitialization request is received through Rx register. Link is reset. |

2.2.2. Multilane Alignment

The Rx multilane alignment module has two main functions:

- CGS pattern detection – Upon comma character (/K/) detection on each lane, this module asserts the respective cgs_over signal to indicate that the CGS pattern has been detected.
- Interlane symbol deskew – During serial data transmission, interlane symbol skew may occur causing symbols across lanes to arrive at different times. This module detects the first ILA character (/R/) of the start of ILA multiframe symbol of each lane in order to later release the characters across lanes at the same time through the FIFO with a depth of 2X the number of octets per multiframe.

Note: Octets per multiframe can range from 1 to 8,192. Therefore, FIFO depth can go up to 16K.

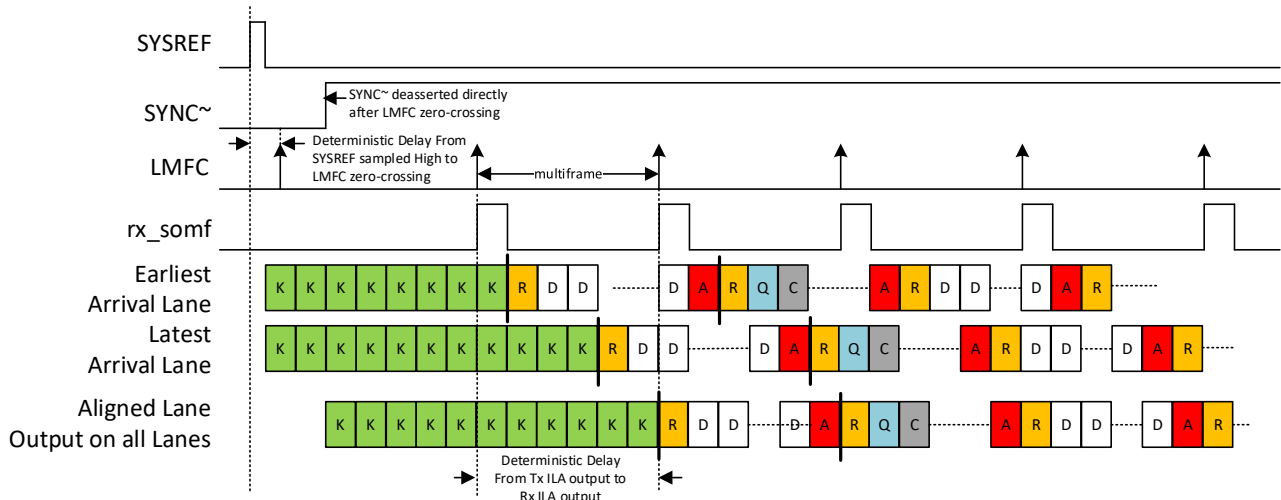


Figure 2.4. Timing Diagram Illustration for Deterministic Latency Equal to Multiples of Multiframe Period

2.2.3. ILA Detection

The Rx ILA detection module detects the ILA sequence and decodes the link configuration parameter. The minimum and default number of ILA multiframe is 4 but the JESD204B specification allows for more than 4 ILA multiframe. The ILA detection module supports an ILA multiframe range of 4 to 256. The `Ila_over` signal, when asserted, indicates that all ILA multiframe have been detected.

2.2.4. Character Replacement

The JESD204B specification mandates character replacement during the DATA phase depending on whether the scrambler is enabled or disabled (refer to sections 5.3.3.4.2 and 5.3.3.4.3 of the JESD204B specification for more information).

The following are conditions for character replacement by the Rx character replacement module:

- Scrambler is enabled
 - When the last scrambled octet in a frame (`rx_eof`), but not at the end of multiframe (`rx_eomf`), equals to control character /F/, Rx character replacement module will decode it as data 0xFC.
 - When the last scrambled octet in a multiframe (`rx_eomf`) equals control character /A/, Rx character replacement module will decode it as data 0x7C.
- Scrambler is disabled
 - When the last octet in current frame (`rx_eof`), not coinciding with the end of multiframe (`rx_eomf`), equals to control character /F/, it will replace current character with the last octet in previous frame (`rx_eof`).
 - When the last octet in current frame at the end of multiframe (`rx_eomf`) equals to control character /A/, it will replace current character with the last octet in the previous frame (`rx_eof`).
 - It is illegal to have two continuous /F/ in back-to-back frames but legal to have /F/ and /A/ in back-to-back frames (because /A/ is EOMF). It is legal to have /F/, /A/, and /F/ in three back-to-back frames.
- Error condition
 - An error condition occurs when the link receives any control character apart from EOF and EOMF. This module passes the receive data through as legal data without fixing the error but increases the error counter.

2.2.5. Descrambler

The JESD204B scrambler is self-synchronous with a scrambler polynomial as follows:

$$1+x^{14}+x^{15}$$

The period of this polynomial is long enough (32,767 bits) to meet the spectral requirements of sensitive radio applications while allowing the descrambler to self-synchronize in two octets.

The scrambler is disabled during the CGS and ILA phases and enabled during the Data phase after the last ILA EOMF character /A/ is detected.

The descrambler is defined via its serial implementation, processing the received data frame by frame. The left-most bit of the frame is shifted in first as illustrated in Figure 2.5. The actual implementation produces the same result as the serial definition.

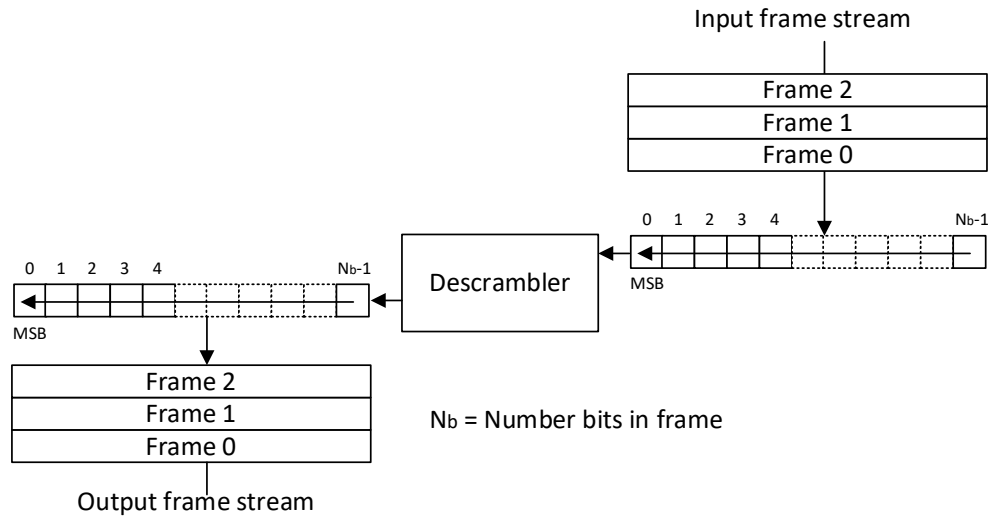


Figure 2.5. Serial Descrambling

2.3. Tx Link Layer

Figure 2.6 shows the JESD204B Tx link layer block diagram. The Tx link layer packetizes tx_tdata from the transport layer with CGS and ILA sequences and transmits to the PHY layer. The Tx scrambler can be enabled or disabled before the ILA sequence.

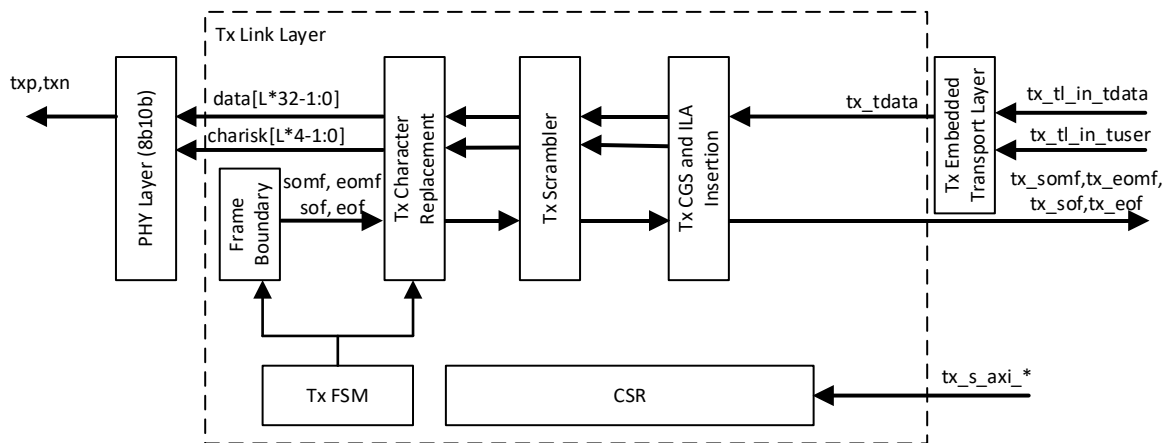


Figure 2.6. JESD204B Tx Link Layer Block Diagram

2.3.1. Frame Boundary and State Machine

The Tx frame boundary module regenerates the LFC and LMFC in form of SOF-EOF and SOMF-EOMF. For subclass 1, the module detects SYSREF assertion as a condition to generate the frame clock. For subclass 0, the module generates the frame clock upon exiting reset.

The SOF-EOF period depends on the number of octets per frame (F). The SOMF-EOMF period depends on the number of octets per frame (F) and number of frames per multiframe (K).

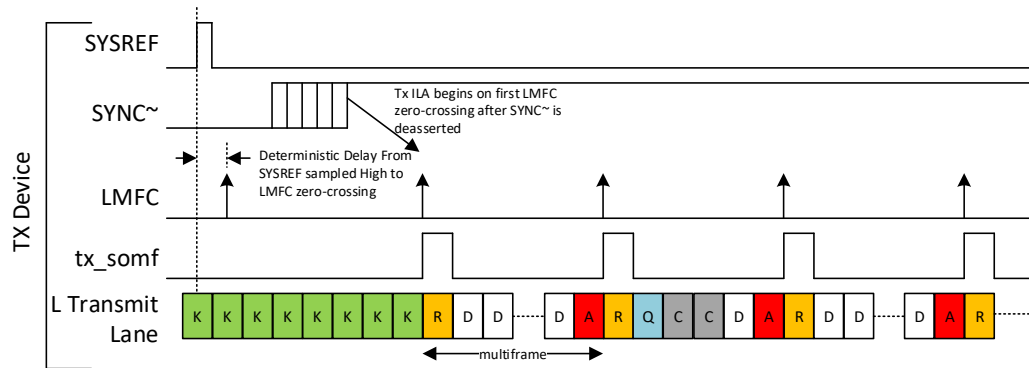


Figure 2.7. Tx LMFC Timing Diagram Correlation with tx_somf Signal

SOMF is aligned with the LMFC arrow as illustrated in Figure 2.7. SOMF and EOMF are aligned with SOF and EOF, respectively.

The Tx FSM module indicates the current Tx state through tx_state_o. Table 2.2 shows the four JESD204B Tx states. This module also detects any resynchronization request from Rx when SYNC~ is asserted (tx_sync_i==0) for at least four LMFC periods (refer to section 8.4 of the JESD204B specification for more information).

Table 2.2. JESD204B Tx States

| Port | Bit Setting | State | Description |
|------------|-------------|-------|---|
| tx_state_o | 2'd0 | IDLE | Default state. Link waits for Tx SYSREF detection before entering CGS state. |
| | 2'd1 | CGS | SYSREF detected and link is transmitting the CGS pattern. Link enters ILA state when SYNC (tx_sync_i==1) is detected. |
| | 2'd2 | ILA | Link is transmitting the ILAS. Once the ILAS is transmitted for all multiframe (default is four multiframe), the link enters DATA state. |
| | 2'd3 | DATA | Tx link is transmitting user data received from the transport layer. Link enters IDLE state when: <ul style="list-style-type: none"> Link reinitialization request is received – SYNC~ is asserted (tx_sync_i==0) for more than four consecutive LMFC periods. Link is reset. |

2.3.2. CGS and ILA Insertion

The Tx CGS and ILA insertion module inserts CGS and ILA sequence depending on tx_state_o from the Tx FSM. During the CGS phase, the module transmits repeated /K/ symbols until the Rx asserts the SYNC signal. Upon detection of SYNC, the module transmits the ILA sequence that aligns with the LMFC period (tx_somf_i).

The ILA multiframe starts with /R/ and ends with /A/. The ILA sequence consists of at least four multiframe or up to 256 multiframe, configurable through the MULTI_FRAME_IN_ILA parameter. The second multiframe contains the JESD204B link configuration information (refer to sections 8.2 and 8.3 of the JESD204B specification).

Note: A multiframe is defined as a group of K successive frames, where K is between 1 and 32, such that the number of octets per multiframe is between 17 and 1,024:

$$\text{ceil}(17/F) \leq K \leq \text{min}(32, \text{floor}(1024/F))$$

| Configuration octet no. | Bits | | | | | | | |
|----------------------------|--------------------------|--------|-------|----------|----------|---|---|-----|
| | MSB | 6 | 5 | 4 | 3 | 2 | 1 | LSB |
| 0 | DID[7:0] | | | | | | | |
| 1 | ADJCNT[3:0] | | | | BID[3:0] | | | |
| 2 | X | ADJDIR | PHADJ | LID[4:0] | | | | |
| 3 | SCR | X | X | L[4:0] | | | | |
| 4 | F[7:0] | | | | | | | |
| 5 | X | X | X | K[4:0] | | | | |
| 6 | M[7:0] | | | | | | | |
| 7 | CS[1:0] | | X | N[4:0] | | | | |
| 8 | SUBCLASSV[2:0] | | | | Np[4:0] | | | |
| 9 | JESDV[2:0] | | | | S[4:0] | | | |
| 10 | HD | X | X | CF[4:0] | | | | |
| 11 | RES1[7:0] - Set to all X | | | | | | | |
| 12 | RES2[7:0] - Set to all X | | | | | | | |
| 13 | FCHK[7:0] | | | | | | | |

Figure 2.8. Mapping of Link Configuration Fields to Octets

2.3.3. Scrambler

The JESD204B scrambler is self-synchronous with a scrambler polynomial as follows:

$$1+x^{14}+x^{15}$$

The scrambler is disabled during the CGS and ILA phases and enabled during the Data phase.

The scrambler is defined via its serial implementation, processing the transmitted data frame by frame. The left-most bit of the frame is shifted in first as illustrated in Figure 2.5. The actual implementation produces the same result as the serial definition.

2.3.4. Character Replacement

The JESD204B specification mandates character replacement during the DATA phase depending on whether the scrambler is enabled or disabled (refer to sections 5.3.3.4.2 and 5.3.3.4.3 of the JESD204B specification for more information).

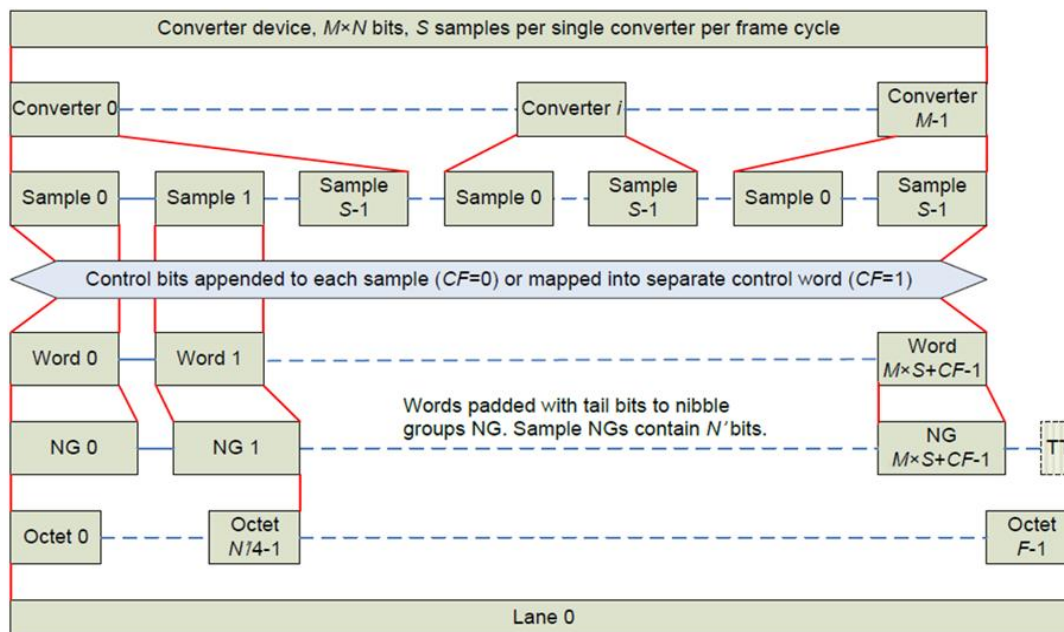
The following are conditions for character replacement by the Tx character replacement module:

- Scrambler is enabled
 - When the last scrambled octet in a frame (tx_eof), but not at the end of multiframe (tx_eomf), equals 0xFC, Tx character replacement module will encode it as control character /F/.
 - When the last scrambled octet in a multiframe (tx_eomf) equals 0x7C, Tx character replacement module will encode it as control character /A/.
- Scrambler is disabled
 - When the last octet in current frame (tx_eof), not coinciding with the end of multiframe (tx_eomf), equals to the last octet in previous frame (tx_eof), it will be encoded as control character /F/.
 - When the last octet in current frame at the end of multiframe (tx_eomf) equals the last octet in the previous frame (tx_eof), it will be encoded as control character /A/.

2.4. Embedded Transport Layer

The function of the transport layer is to map the data samples from the converter to a non-scrambled octet. In addition, since the input data width of the core is 32 bits per lane, the transport layer is also responsible to output octets that match the expected data width.

Figure 2.9 shows a simple example of how data is mapped from converter samples to octets and output in a lane. Refer to section 5.1 of the JESD204B specification for more examples.



Notes:

1. CF = Number of control words per frame clock period per link
2. F = Number of octets per frame
3. M = Number of converters per device
4. N = Converter resolution
5. N' = Total number of bits per sample
6. S = Number of samples per converter per frame cycle
7. T = Tail bit

Figure 2.9. User Data Format for Independent Lane with Oversampling

Figure 2.10 shows the embedded transport layer block diagrams for Tx and Rx. The transport layers can be enabled through the respective options in the IP GUI. Refer to the [IP Parameter Description](#) and [Signal Description](#) sections for the lists of parameters and signals, respectively.

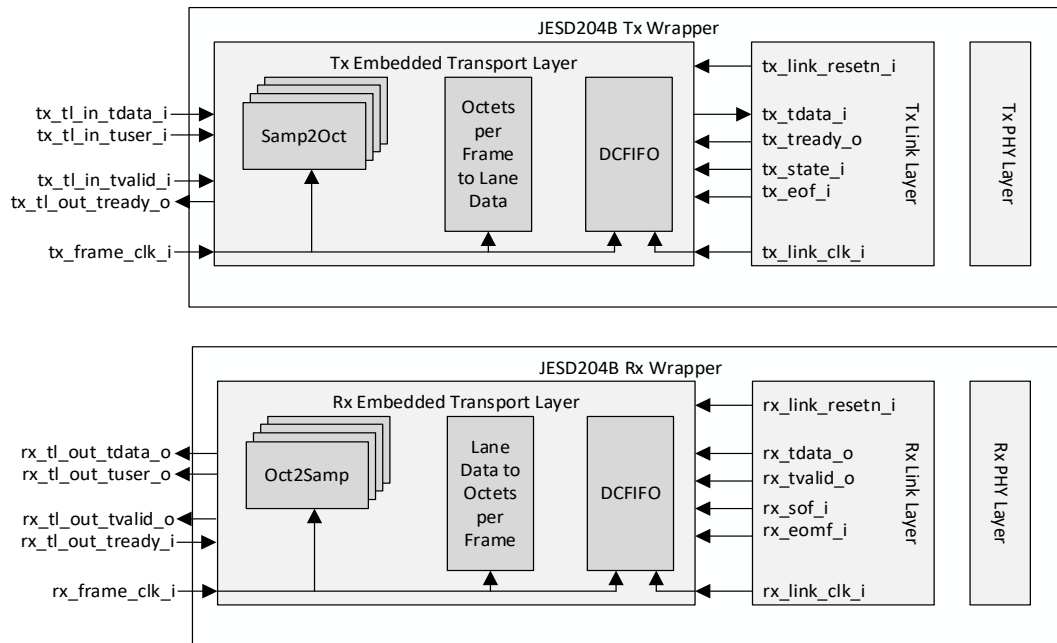


Figure 2.10. Embedded Transport Layer Block Diagrams for Tx and Rx

To calculate the required frame clock frequency, it is important to know that the underlying core is operating at 32 bits per lane in every link clock cycle. These 32 bits are encoded/decoded with 8b10b encoding in the transceiver as required by the JESD204B specification. Hence, the actual link clock frequency can be calculated as follows:

$$\text{Total Bits Transmitted per Lane per Link Clock Period} = 32b \times (10/8) = 40b$$

$$\text{Link Clock Frequency} = \text{Data Rate} / 40b$$

Since the core is expecting 32 bits of data in every link clock cycle, the frame clock frequency required by the transport layer can be calculated using the JESD204B link parameter octets per frame (F), since F determines how many bits are transmitted per frame clock period (see the data mapping diagram in [Figure 2.9](#)), as follows:

$$\text{Frame Clock Frequency} \times (F \times 8) = \text{Link Clock Frequency} \times 32$$

In the scenario where $F < 4$, the required frame clock frequency may exceed the supported fabric speed depending on the data rate configuration. For example, when data rate = 8.1 Gb/s and $F = 1$, the required frame clock frequency is 810 MHz. A parameter `TL_FRAME_PER_CLK` is added to allow multiple frames to be processed at the transport layer in one clock cycle which then lowers the required clock frequency. The updated calculation for the frame clock frequency is as follows:

$$\text{Frame Clock Frequency} \times (F \times 8) \times \text{TL_FRAME_PER_CLK} = \text{Link Clock Frequency} \times 32$$

For `TL_FRAME_PER_CLK > 1`, the samples from all converters for the first frame should be placed at LSB, then only followed by the samples for the second frame and so on. For example, if `TL_FRAME_PER_CLK = 4`, the tdata bus data bit locations are assigned as follows: {Frame 3 samples, Frame 2 samples, Frame 1 samples, Frame 0 samples}. The transport layer tdata width is byte oriented (8, 16, 24, 32 ... bits). Any remaining MSB bits, after packing of all sample data, are padded with 0s.

$$\text{Transport Layer Data Width} = \text{ceil}((\text{ILA_M}+1) \times (\text{ILA_S}+1) \times (\text{ILA_N}+1) \times \text{TL_FRAME_PER_CLK}/8) \times 8$$

Note: ILA_M, ILA_S, and ILA_N are registers whose values are offset by minus one from the actual values the registers are representing. For example, ILA_M = 0 indicates one converter, ILA_S = 1 indicates 2 samples per converter, and ILA_N = 2 indicates 3 bits per sample.

The following examples are simple illustrations for the timing diagrams of incoming samples from converter devices and the outgoing octet data to the JESD core.

In the first example, the timing diagrams with the link parameter OCTET_PER_FRAME set to 2 and TL_FRAME_PER_CLK set to 2 and 1 are shown in Figure 2.11 and Figure 2.12, respectively.

1. When tx_tl_in_tready is asserted at cycle 0, this indicates that the Tx transport layer is ready to accept data. The first sample from the converter comes in at the same cycle as when tx_tl_in_tvalid is asserted.
2. Later when the transport layer sees tx_tready from the core is asserted, it starts to transmit the lane data to the core at the tx_tdata bus. The data are the remapped samples in octet format where each lane is fixed to a 32-bit wide data bus.

The LSB of the data bus is usually Octet 0 of the frame and the subsequent byte is followed by Octet 1. Note that these data also need to be aligned with tx_sof output from the core where a bit in tx_sof indicates that a specific byte location in the tx_tdata bus is the start of frame.

For instance, in the diagram, tx_sof = 0101 indicates that the core is expecting the data at start of frame to be placed at byte locations 0 and 2 in the tx_tdata bus. Hence, at the F0 and F2 positions in the tdata_bus of every lane, the octet is expected to be the data at start of frame from the in*_tdata bus.

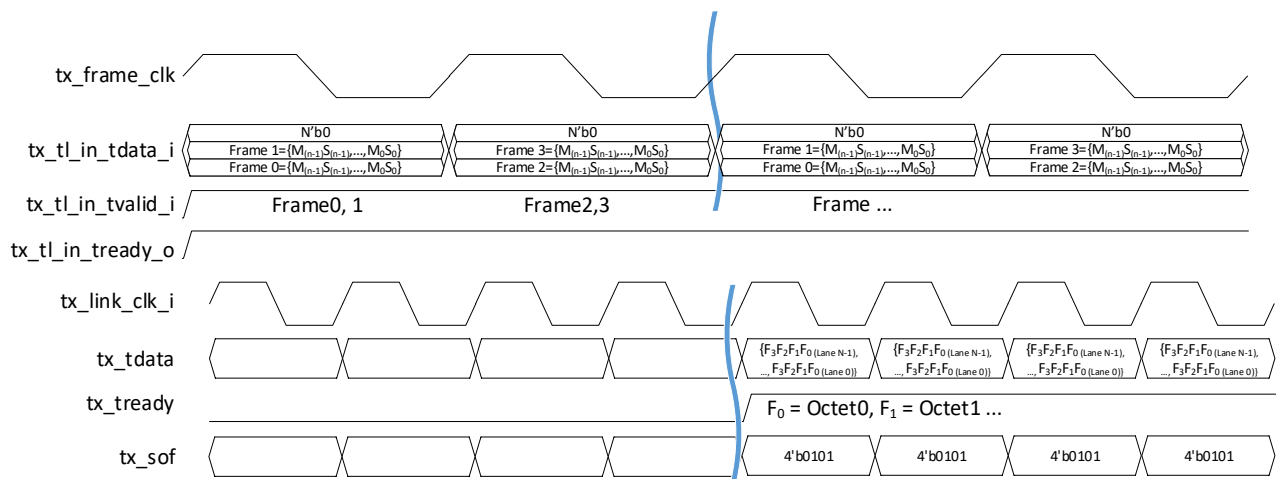


Figure 2.11. Timing Diagram with OCTET_PER_FRAME = 2 and TL_FRAME_PER_CLK = 2

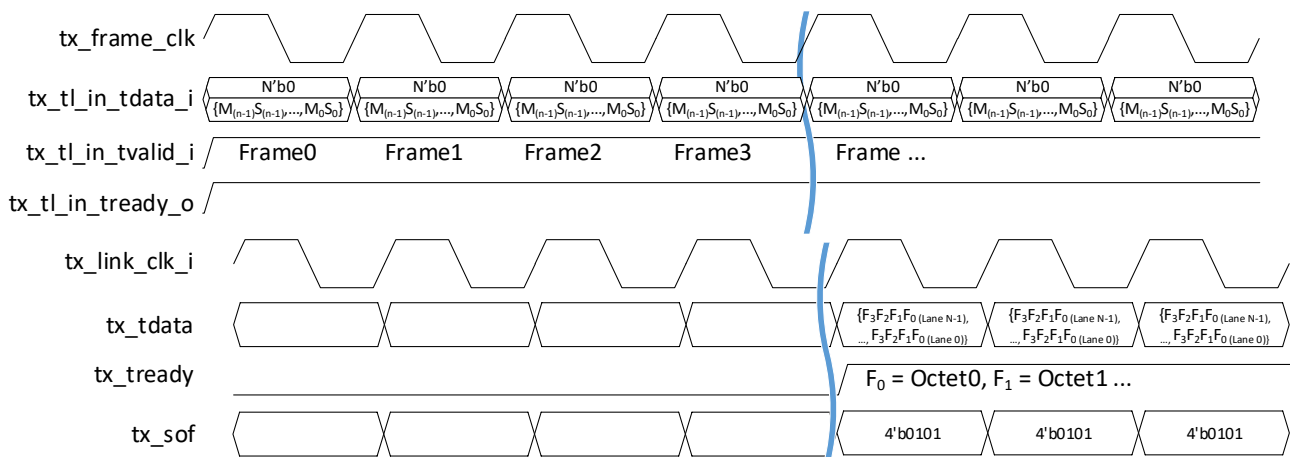


Figure 2.12. Timing Diagram with OCTET_PER_FRAME = 2 and TL_FRAME_PER_CLK = 1

In the second example, the timing diagrams at the Rx transport layer with OCTET_PER_FRAME set to 3 and TL_FRAME_PER_CLK set to 1 and 2 are shown in Figure 2.13 and Figure 2.14, respectively.

1. As the rx_tvalid signal is asserted, the transport layer starts to accept data from Rx core. Note that at clock cycle 0, rx_sof = 1001 indicates that byte locations 0 and 3 at rx_tdata are the data at start of frame, which means that the data at the F0, F1, and F2 positions of every lane from rx_tdata form the samples of the first frame to the converter while the data at the F3 position are part of the subsequent second frame.
2. At clock cycle 1, the value of rx_sof changes to 0100 indicating that the data at start of frame has changed to byte location 2 at rx_tdata. This means that the data at the F0 and F1 positions in this clock cycle form the samples of the second frame to the converter along with the data at the F3 position from the previous clock cycle. The data at the F2 and F3 positions in this clock cycle are part of the third frame with F2 at lane 0 forming the start of frame.
3. At clock cycle 2, the value of rx_sof changes to 0010 indicating that the data at the F0 position of all lanes in this clock cycle form the last few missing data for the third frame. The data at the F1, F2, and F3 positions of rx_tdata together form the samples of the fourth frame.
4. When the transport layer sees the rx_tl_in_tready signal asserted, it starts outputting the remapped data to the application layer as well as asserting the rx_tl_out_tvalid signal. Note that rx_tl_out_tready and rx_tl_out_tvalid have no dependency on each other and one may assert earlier than the other. Data transfer between manager and subordinate only occurs when both signals are asserted. The Rx_tl_out_tready_i signal is not expected toggle once it gets asserted as the incoming frame clock and link clock have the same ratio as the input and output data widths, and hence equal in throughput.

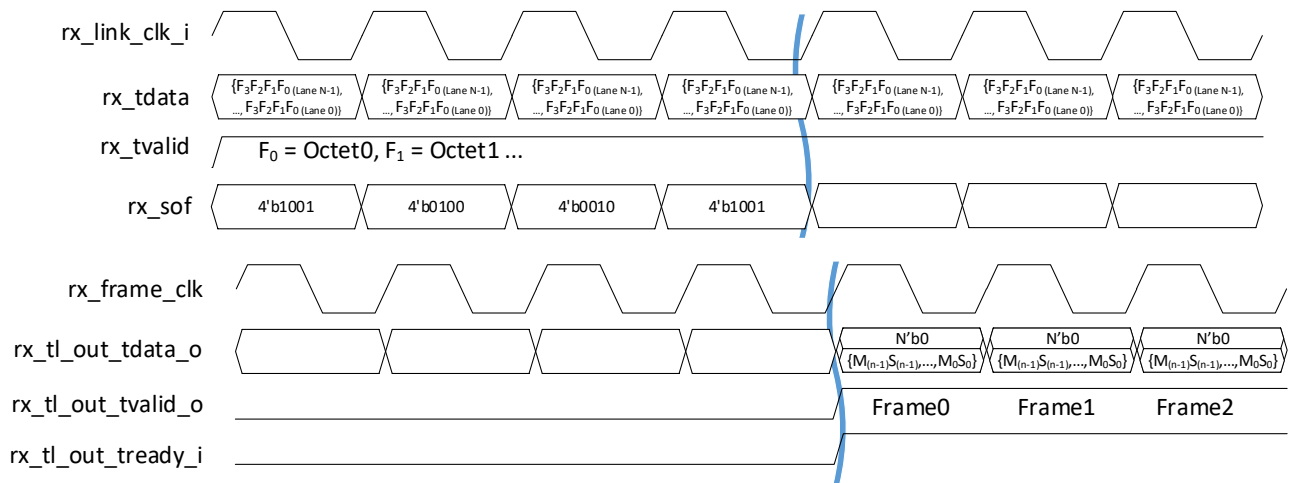


Figure 2.13. Timing Diagram with OCTET_PER_FRAME = 3 and TL_FRAME_PER_CLK = 1

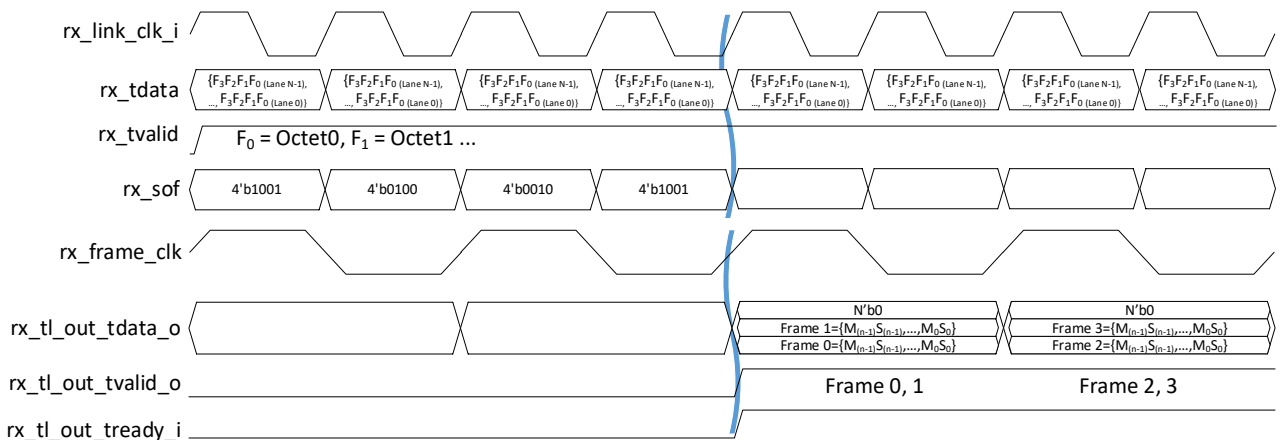


Figure 2.14. Timing Diagram with OCTET_PER_FRAME = 3 and TL_FRAME_PER_CLK = 2

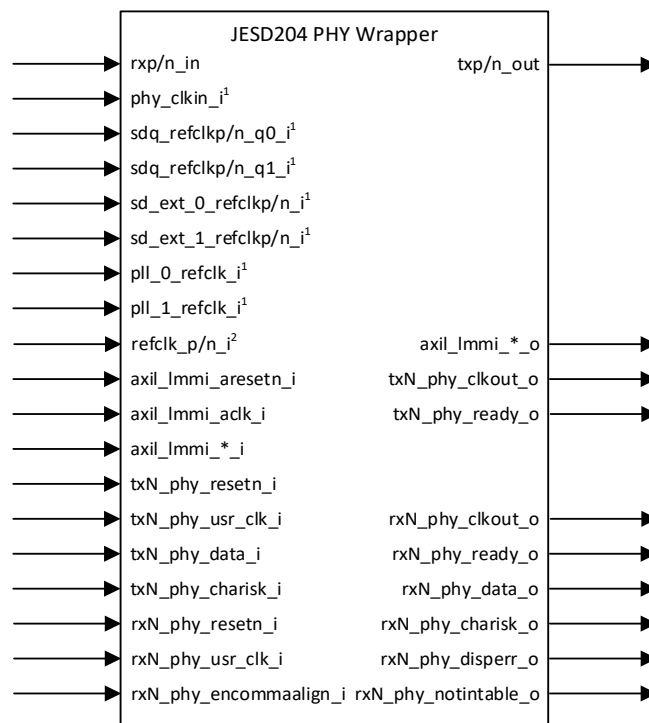
2.5. JESD204B PHY Layer

The JESD204B PHY layer is enabled and preconfigured as part of the JESD204B IP. The IP also handles the reset sequence for the JESD204B PHY layer. You only need to configure the *Data Rate*, *Number of Lanes*, and *Ref Clk Freq* attributes as shown in the [IP Parameter Description](#) section.

The JESD204B IP offers the flexibility of enabling or disabling generation of the JESD204B PHY layer through the *JESD204 IP Core Generation Enable* attribute. The JESD204B IP also offers the flexibility of generating only the JESD204B PHY layer (JESD204B PHY layer separation mode). This is accomplished by setting the *JESD204B IP Core Generation Enable* attribute to unchecked and *JESD204 PHY Generation Enable* attribute to checked.

When the JESD204B PHY layer separation mode is enabled, only the JESD204B PHY wrapper and respective interfaces are generated. You need to connect the PHY layer to the link layer manually.

[Figure 2.15](#) shows the JESD204B PHY layer module.



- Notes:**
1. Applicable for the CertusPro-NX device only.
 2. Applicable for the Avant-G/X device only.

Figure 2.15. JESD204B PHY Layer Module

2.5.1. PLL Reference Clock for CertusPro-NX Device

The JESD204B PHY layer supports reference clock selection through the *PMA Reference Clock* attribute. You can select one of six options (*sd_ext_0_refclk*, *sd_ext_1_refclk*, *sdq0_refclk*, *sdq1_refclk*, *pclk0*, *pclk1*) as the PMA reference clock source. The JESD204B PHY layer constrains mux select according to the selection internally so that the output is the selected reference clock. For PCS reference clock information, refer to [CertusPro-NX SerDes/PCS User Guide \(FPGA-TN-02245\)](#).

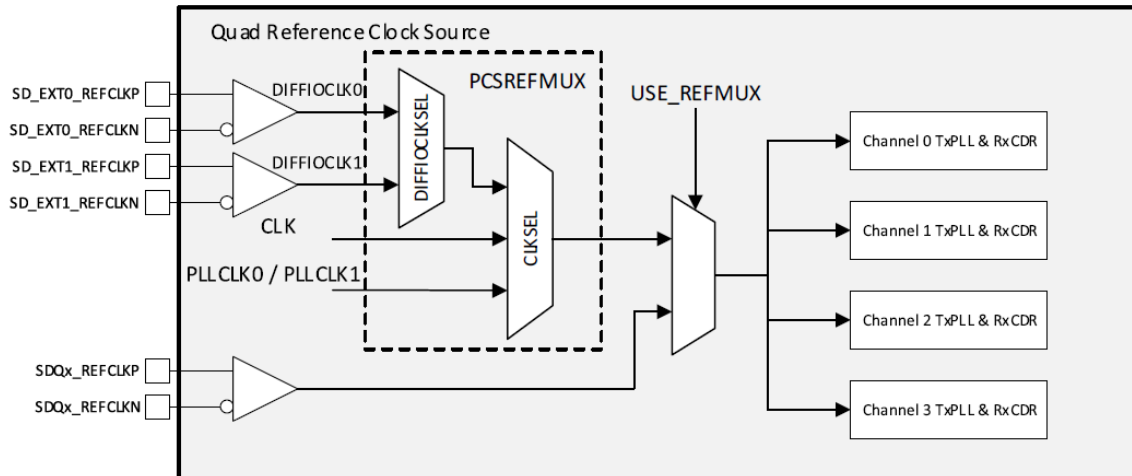


Figure 2.16. CertusPro-NX PCS REFCLK Architecture

2.5.2. AXI4-Lite to LMMI

The JESD204B PHY layer supports access to the PHY layer configuration register through the AXI4-Lite to LMMI interface. AXI4-Lite read and write data are double word (DW) aligned. For register information, refer to the following:

- [Lattice Avant SERDES/PCS User Guide \(FPGA-TN-02313\)](#)
- [CertusPro-NX SerDes/PCS User Guide \(FPGA-TN-02245\)](#)
- [Lattice Nexus 2 SERDES/PCS User Guide \(FPGA-TN-02395\)](#)

Figure 2.17 shows the supported AXI4-Lite aligned transfer with respect to 8-bit, 16-bit, or 32-bit transfer. JESD204B AXI4-Lite to LMMI does not support AXI4 unaligned transfer (refer to the AMBA AXI Protocol Specification document). Figure 2.18 and Figure 2.19 show the AXI4-Lite timing diagrams.

| Register offset access | | 31 | 24 | 23 | 16 | 15 | 8 | 7 | 0 |
|------------------------|------------|-------------|-------|-------|-------|-------|-------|-------|-------|
| 8-bits transfer | Offset 0x0 | | | | | | | | BYTE0 |
| | Offset 0x1 | | | | | | BYTE1 | | |
| | Offset 0x2 | | | BYTE2 | | | | | |
| | Offset 0x3 | BYTE3 | | | | | | | |
| 16-bits transfer | Offset 0x0 | | | | | BYTE1 | | BYTE0 | |
| | Offset 0x1 | Not allowed | | | | | | | |
| | Offset 0x2 | BYTE3 | BYTE2 | | | | | | |
| | Offset 0x3 | Not allowed | | | | | | | |
| 32-bits transfer | Offset 0x0 | BYTE3 | BYTE2 | BYTE1 | BYTE0 | | | | |
| | Offset 0x1 | Not allowed | | | | | | | |
| | Offset 0x2 | Not allowed | | | | | | | |
| | Offset 0x3 | Not allowed | | | | | | | |

Figure 2.17. AXI4-Lite to LMMI Aligned Transfer on 8-bit, 16-bit, and 32-bit Buses

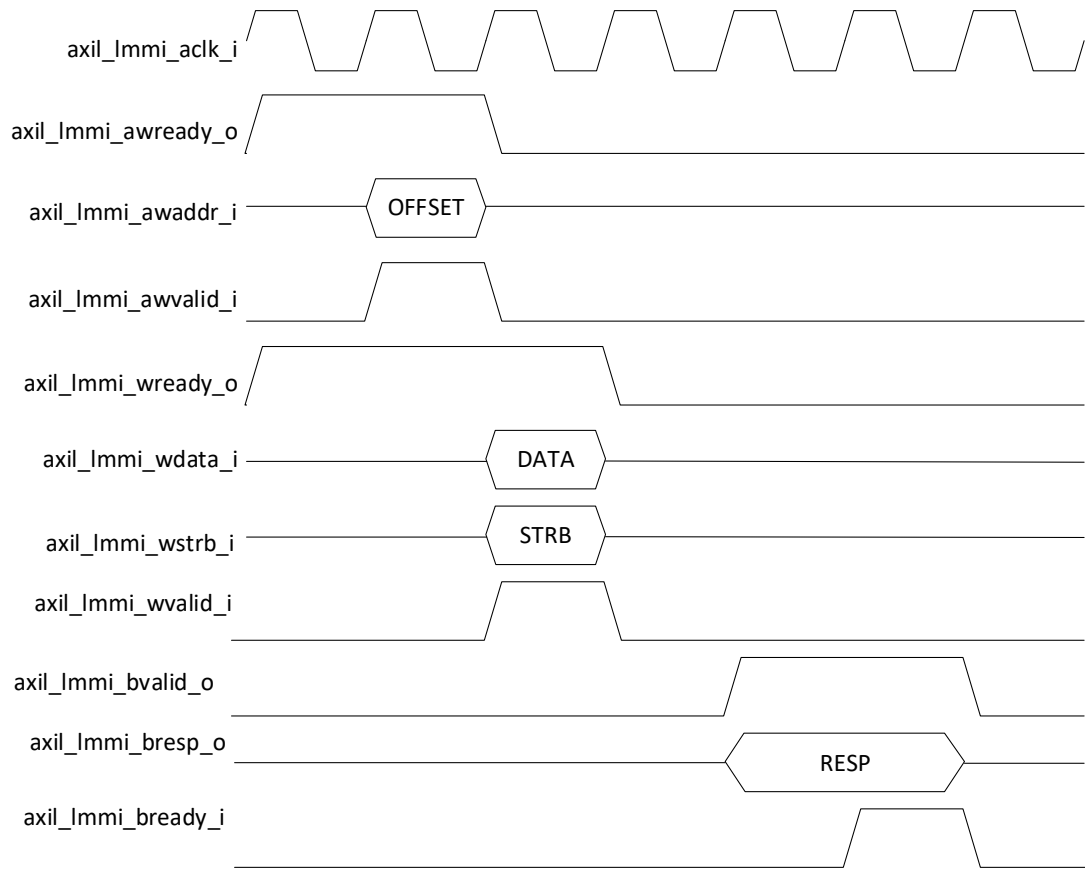


Figure 2.18. AXI4-Lite to LMMI Write Timing Diagram

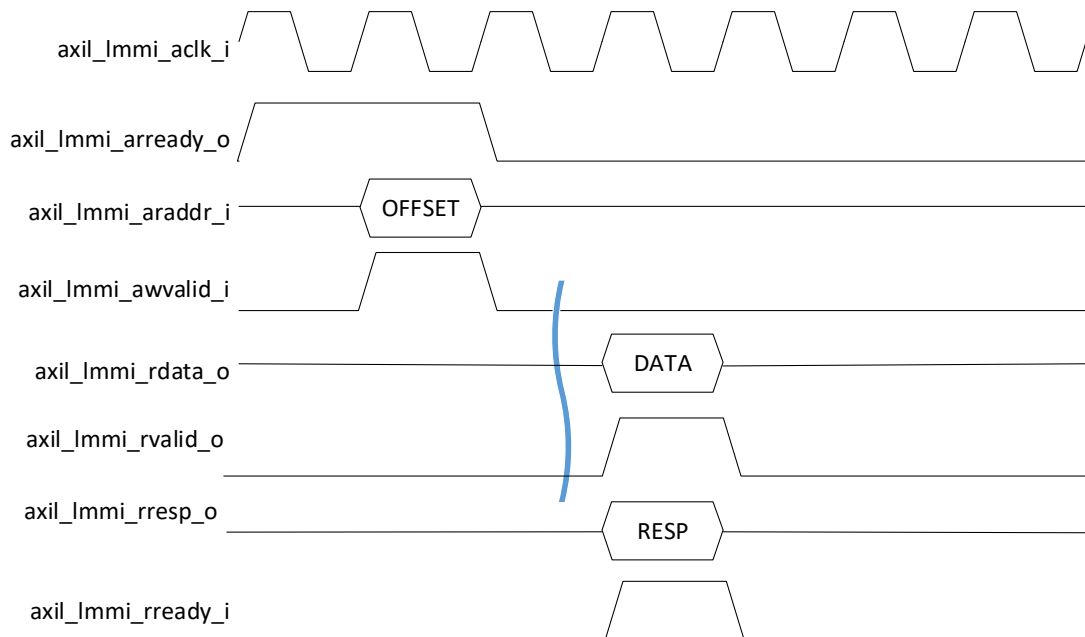


Figure 2.19. AXI4-Lite to LMMI Read Timing Diagram

2.6. Clocking Overview

This section describes the JESD204B IP clock architecture. Figure 2.20 shows an overview of the JESD204B IP clock domain. All clock domain crossings are handled in the IP.

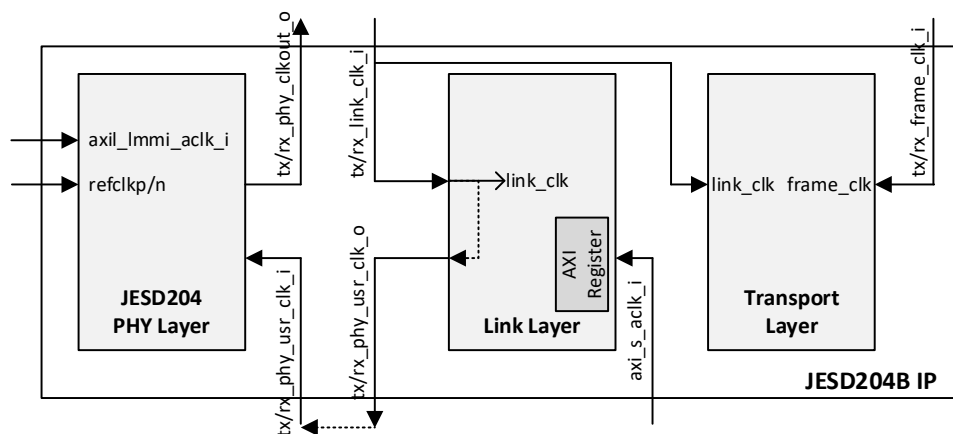


Figure 2.20. JESD204B IP Clock Domain Block Diagram

Refer to the [Clock Interface](#) section for descriptions of the JESD204B IP clock signals.

2.7. Reset

This section describes the JESD204B IP reset scheme.

Table 2.3. JESD204B IP Reset Input Overview

| Reset | Type | Component to be Reset | | | | | | |
|--|------|-----------------------|----|-------------------------|----|----------|-----|-----|
| | | CSR (AXI4-Lite) | | Link and Transport Core | | PHY | | |
| | | Tx | Rx | Tx | Rx | LMMI Reg | PCS | PMA |
| Link Wrapper | | | | | | | | |
| tx_s_axi_aresetn_i | Pin | ✓ | — | ✓ | — | — | ✓ | ✓ |
| tx_link_resetn_i | Pin | — | — | ✓ | — | — | ✓ | ✓ |
| Tx Core Reset (CSR offset 0x00 bit[0]) | Reg | — | — | ✓ | — | — | ✓ | ✓ |
| rx_s_axi_aresetn_i | Pin | — | ✓ | — | ✓ | — | ✓ | ✓ |
| rx_link_resetn_i | Pin | — | — | — | ✓ | — | ✓ | ✓ |
| Rx Core Reset (CSR offset 0x00 bit[0]) | Reg | — | — | — | ✓ | — | ✓ | ✓ |
| PHY Wrapper | | | | | | | | |
| axil_lmmi_aresetn_i | Pin | — | — | — | — | ✓ | ✓ | ✓ |
| txN_phy_resetn_i (see note ¹) | Pin | — | — | — | — | — | ✓ | ✓ |
| rxN_phy_resetn_i (see note ¹) | Pin | — | — | — | — | — | ✓ | ✓ |

Note:

- When the PHY is in Rx_only or Tx_only mode, asserting the respective rxN/txN_phy_resetn_i resets both PMA and PCS. When the PHY is in Rx_and_Tx mode, both txN_phy_resetn_i and rxN_phy_resetn_i must be asserted to reset the PMA and PCS. Otherwise, only the respective Tx PCS and Rx PCS are reset.

Table 2.4. JESD204B IP Reset Output Overview

| Reset | Type | Description |
|-----------------------------------|------|--|
| Link and Transport Wrapper | | |
| tx_aresetn_o | Pin | Output reset signal from Tx indicating that link is in reset when de-asserted. |
| rx_aresetn_o | Pin | Output reset signal from Rx indicating that link is in reset when de-asserted. |
| PHY Wrapper | | |
| txN_phy_ready_o | Pin | Output ready signal from PHY to indicate that Tx PHY is ready. Used as reset to link layer (excludes AXI register) when phy_ready = 0. |
| rxN_phy_ready_o | Pin | Output ready signal from PHY to indicate that Rx PHY is ready. Used as reset to link layer (excludes AXI register) when phy_ready = 0. |

3. IP Parameter Description

The configurable attributes of the JESD204B IP are shown in the following tables. You can configure the IP by setting the attributes accordingly in the IP Catalog Module/IP Block wizard of the Lattice Radiant software.

Wherever applicable, default values are in bold.

3.1. General

Table 3.1. General Attributes

| Attribute | Selectable Values | Description |
|-------------------------------------|---|---|
| JESD204 IP Core Generation Enable | Checked , Unchecked | Enables JESD204B link layer IP generation. |
| Mode | Rx_and_Tx , Rx_only, Tx_only | Selects the IP mode. |
| Data Rate (Gbps) | CertusPro-NX: 0.7425 – 8.192 ¹ Avant-G/X, Certus-N2: 1.2288 – 9.8304 ² | For CertusPro-NX devices, enter the JESD204B data rate in the range from 0.7425 to 8.192 Gb/s. For Avant-G, Avant-X, and Certus-N2 devices, enter the JESD204B data rate in the range from 1.2288 to 9.8304 Gb/s. Note: Valid values or ranges are as follows: <ul style="list-style-type: none"> • 1.2288 Gbps • 1.25 – 1.289 Gbps • 1.375 – 2.57812 Gbps • 2.75 – 5.15625 Gbps • 5.5 – 6.64062 Gbps • 7.34 – 9.8304 Gbps |
| Number of Lanes (L) | 1, 2, 4, 8 | Number of lanes. Only Avant devices support 8 lanes. |
| Converters per Device (M) | 0-255 | Sets the number of converters per device. The lowest selectable value corresponds with the lowest allowable setting. |
| Samples per Converter per Frame (S) | 0-31 | Sets the number of samples per converter per frame. The lowest selectable value corresponds with the lowest allowable setting. |
| Converter Resolution (N) | 0-31 | Sets the number of bits per converter sample. The lowest selectable value corresponds with the lowest allowable setting. |
| Number of Bits per Sample (Nt) | 0-31 | Sets the number of bits per sample in user data format. The lowest selectable value corresponds with the lowest allowable setting. |
| Control Bits (CS) | 0-3 | Sets the number of control bits per device. |
| Control Words (CF) | 0-31 | Sets the number of control words per frame clock per link. |
| High Density Format (HD) | 0, 1 | Enables or disables high density format. 0 – Disable high density user data format 1 – Enable high density user data format |
| Octets per Frame (F) | 0-255 | Sets the number of octets per frame. The lowest selectable value corresponds with the lowest allowable setting. |
| Frames per Multiframe (K) | 0-31 | Sets the number of frames per multiframe. The lowest selectable value corresponds with the lowest allowable setting. Note: (Octets per Frame + 1) × (Frames per Multiframe + 1) must be a multiple of 4. |
| Multi Frames in ILA | 3-255 | Sets the number of multiframe required in ILAS phase. |
| Subclass (SUBCLASSV) | 0, 1 | Selects the JESD204B subclass mode. 0 – Subclass 0 1 – Subclass 1 |
| SYSREF Always | SYSREF_ONCE, SYSREF_ALWAYS | Selects the incoming SYSREF operating mode. SYSREF_ONCE – One shot SYSREF_ALWAYS – Periodic |

| Attribute | Selectable Values | Description |
|------------------|-------------------|---|
| Scrambling (SCR) | ENABLED, DISABLED | Enables or disables the scrambler/descrambler. |
| ILA_DID | 0-255 | Device (= link) identification number. |
| ILA_ADJCNT | 0-15 | Number of adjustment resolution steps to adjust DAC LMFC. |
| ILA_BID | 0-15 | Bank ID – Extension to DID |
| ILA_ADJDIR | 0, 1 | Direction to adjust DAC LMFC 0 – Advance 1 – Delay |
| ILA_PHADJ | 0, 1 | Phase adjustment request to DAC |
| ILA_JESDV | 0, 1 | JESD204 version 000 – JESD204A 001 – JESD204B |
| ILA_LID | 0-31 | Lane identification number (within link) for Lane 0. The LID of a subsequent lane is an increment of the LID of the previous lane. For example, for <i>Number of Lanes</i> =4 and <i>ILA_LID</i> =5, Lane0 LID=5, Lane1 LID=6, Lane2 LID=7, and Lane3 LID=8. The valid range is dependent on the number of lanes: If <i>Number of Lanes</i> =1, the valid range is 0-31. If <i>Number of Lanes</i> =2, the valid range is 0-30. If <i>Number of Lanes</i> =4, the valid range is 0-28. |

Notes:

1. The CertusPro-NX device supports data rates up to 8.192 Gb/s.
2. The Avant-G, Avant-X, and Certus-N2 devices support multiple continuous data rate ranges up to 9.8304 Gb/s.

3.2. PHY

Table 3.2. PHY Attributes

| Attribute | Selectable Values | Description |
|-------------------------------|--|--|
| JESD204 PHY Generation Enable | Checked , Unchecked | Enables JESD204B PHY layer generation. |
| Lane ID | CertusPro-NX: 0-7 Avant-G/X: 0-27 Certus-N2: 0-7 | Selects lane placement location. |
| PMA Reference Clock | sd_ext_0_refclk , sd_ext_1_refclk, sdq0_refclk, sdq1_refclk, pclk0, pclk1 | Selects PHY PLL REFCLK source for CertusPro-NX devices. |
| Ref Clk Freq (MHz) | 156.25 | PHY PLL REFCLK Supported reference clock frequency: <ul style="list-style-type: none"> • CertusPro-NX: 74.25 – 162 MHz <ul style="list-style-type: none"> • For data rates in the range from 2.97 to 6.48 Gb/s, the recommended frequency is $Data\ Rate / 40$. • For data rates > 6.48 Gb/s, divide $Data\ Rate / 40$ by a factor of 2 to get a frequency within the recommended range. For example, with the data rate of 8.192 Gb/s, use 102.4 MHz. • For data rates < 2.97 Gb/s, multiply $Data\ Rate / 40$ by one or more factors of 2 to get a frequency within the recommended range. For example, with the data rate of 1.5 Gb/s, use 150 MHz. • Avant-G/X and Certus-N2: 20 – 312.5 MHz <ul style="list-style-type: none"> • Select the reference clock frequency from the list of available clock frequencies. |

| Attribute | Selectable Values | Description |
|---------------|-------------------|---|
| PLL M Setting | 1, 2, 4, 8 | PHY PLL M setting. Only applicable for CertusPro-NX device. |

3.3. Transport Layer Setup

Note: The transport layer setup attributes are optional, contingent upon the *JESD204 IP Core Generation Enable* attribute being set to checked.

Table 3.3. Transport Layer Setup Attributes

| Attribute | Selectable Values | Description |
|------------------------|---------------------------|---|
| Transport Layer Enable | Checked, Unchecked | Enables the embedded transport layer. ¹ |
| Frame Per Clock | 1, 2, 4 | Sets the number of frames per frame clock in the transport layer. |

Note:

1. Only supported when F = 0, 1, 2, 3, 5, or 7.

3.4. Test Mode Setup

Note: The test mode setup attributes are optional, contingent upon the *JESD204 IP Core Generation Enable* attribute being set to checked.

Table 3.4. Test Mode Setup Attributes

| Attribute | Selectable Values | Description |
|---------------------------------------|---------------------------|---|
| Test Mode Enable | Checked, Unchecked | Enables the JESD204B test mode. |
| Supports Continuous /K28.5/ Character | Always | Specifies support for the JESD204B Tx repetitive K28.5 character generator. |
| Supports Continuous /D21.5/ Character | Always | Specifies support for the JESD204B Tx repetitive D21.5 character generator. |
| Supports RPAT Pattern Generator | Checked, Unchecked | Enables or disables support for the JESD204B Tx RPAT pattern generator. |
| Supports JSPAT Pattern Generator | Checked, Unchecked | Enables or disables support for the JESD204B Tx JSPAT pattern generator. |

3.5. IP Parameter Settings for Example Use Cases

In addition to the JESD204B PHY and Link Layer mode, the JESD204B IP also supports the JESD204B PHY layer and JESD204B link layer separation modes. Link and PHY separation allows for customization of the JESD204B application through:

- Channel lane reversal connection – connections between the PHY layer and link layer can be between different lane numbers for example Lane 0 in PHY layer to Lane 3 in link layer.
- Different Tx and Rx configurations – transmitter and receiver can be configured with different number of lanes such as 1T2R (transmitter configured to one lane, receiver configured to two lanes). This cannot be achieved in the JESD204B PHY and Link Layer mode.

3.5.1. JESD204B PHY and Link Layer Mode

This mode embeds the JESD204B PHY and link layers within a single top module instance. The PHY to link data is handled internally except PHY to link clock.

The Tx PHY clock out and Rx PHY clock out need to be manually connected to the Tx link clock in and Rx link clock in, respectively. It is recommended that the main channel of PHY clock out be connected to the link clock.

[Figure 3.1](#) shows an example clock connection from PHY to link with channel 0 as the main channel.

Table 3.5. Attributes to Enable JESD204B PHY and Link Layer Mode

| Attribute | Configuration Value | Description |
|-----------------------------------|----------------------------|---|
| JESD204 IP Core Generation Enable | Checked | Check to enable JESD204B link layer generation. |
| JESD204 PHY Generation Enable | Checked | Check to enable JESD204B PHY layer generation. |
| Transport Layer Enable | Checked (if needed) | Check to enable the embedded transport layer if needed. |

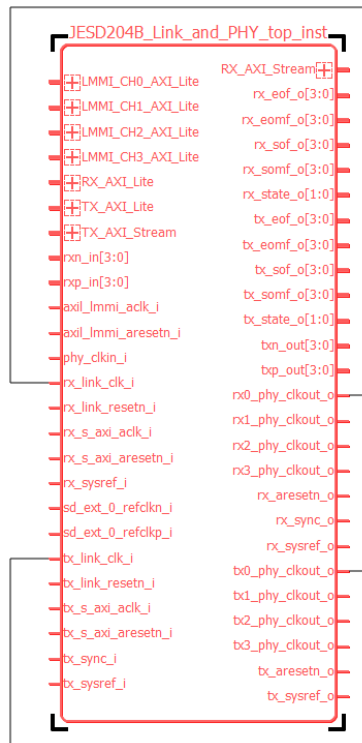


Figure 3.1. JESD204B PHY to Link Connection Example with Main Channel (Channel 0)

3.5.2. JESD204B Link Layer Only Mode

In this mode, only the JESD204B link layer and embedded transport layer are generated within the top module instance with the JESD204B PHY layer excluded. All necessary PHY-to-link interfaces are exported to the top level and connections need to be completed manually.

These PHY-to-link interfaces are grouped as JESD204_TX/RX_CORE_CHn interface buses to ease connection using Propel. The PHY clock to link clock connections are as described in the [JESD204B PHY and Link Layer Mode](#) section.

[Figure 3.2](#) shows an example PHY-to-link connection through Propel for the JESD240B Link Only mode.

Table 3.6. Attributes to Enable JESD204B Link Only Mode

| Attribute | Config Values | Description |
|-----------------------------------|----------------------------|---|
| JESD204 IP Core Generation Enable | Checked | Check to enable JESD204B link layer generation. |
| JESD204 PHY Generation Enable | Unchecked | Uncheck to disable JESD204B PHY layer generation. |
| Transport Layer Enable | Checked (if needed) | Check to enable the embedded transport layer if needed. |

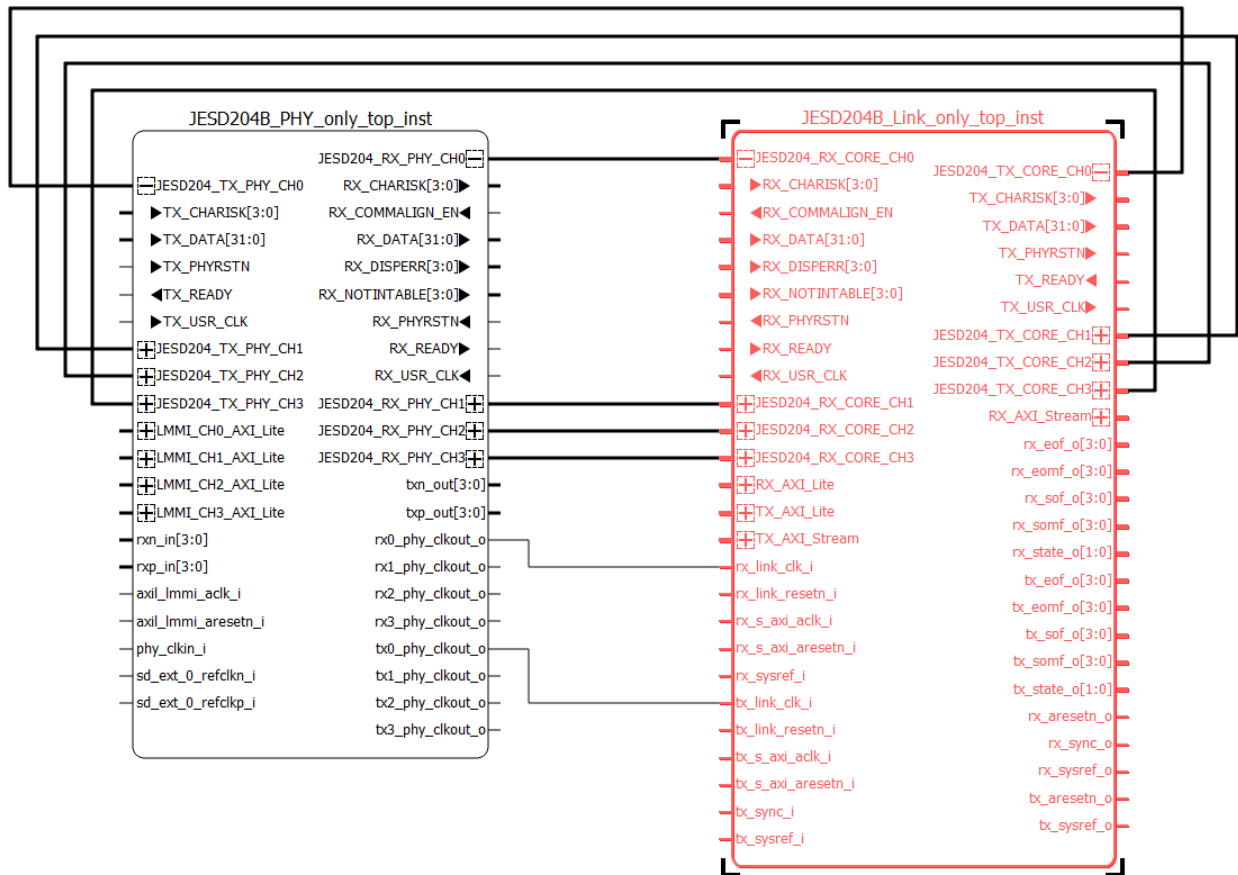


Figure 3.2. JESD204B Link Only Mode Connection Example

3.5.3. JESD204B PHY Layer Only Mode

In this mode, only the JESD204B PHY layer is generated within the top module instance. All necessary PHY-to-link interfaces are exported to the top level and connections need to be completed manually.

These PHY-to-link interfaces are grouped as JESD204_TX/RX_PHY_CHn interface buses to ease connection using Propel. The PHY clock to link clock connections are as described in the [JESD204B PHY and Link Layer Mode](#) section.

[Figure 3.3](#) shows an example PHY-to-link connection through Propel for the JESD204B PHY Only mode.

Table 3.7. Attributes to Enable JESD204B PHY Only Mode

| Attribute | Config Values | Description |
|-----------------------------------|------------------|--|
| JESD204 IP Core Generation Enable | Unchecked | Uncheck to disable JESD204B link layer generation. |
| JESD204 PHY Generation Enable | Checked | Check to enable JESD204B PHY layer generation. |

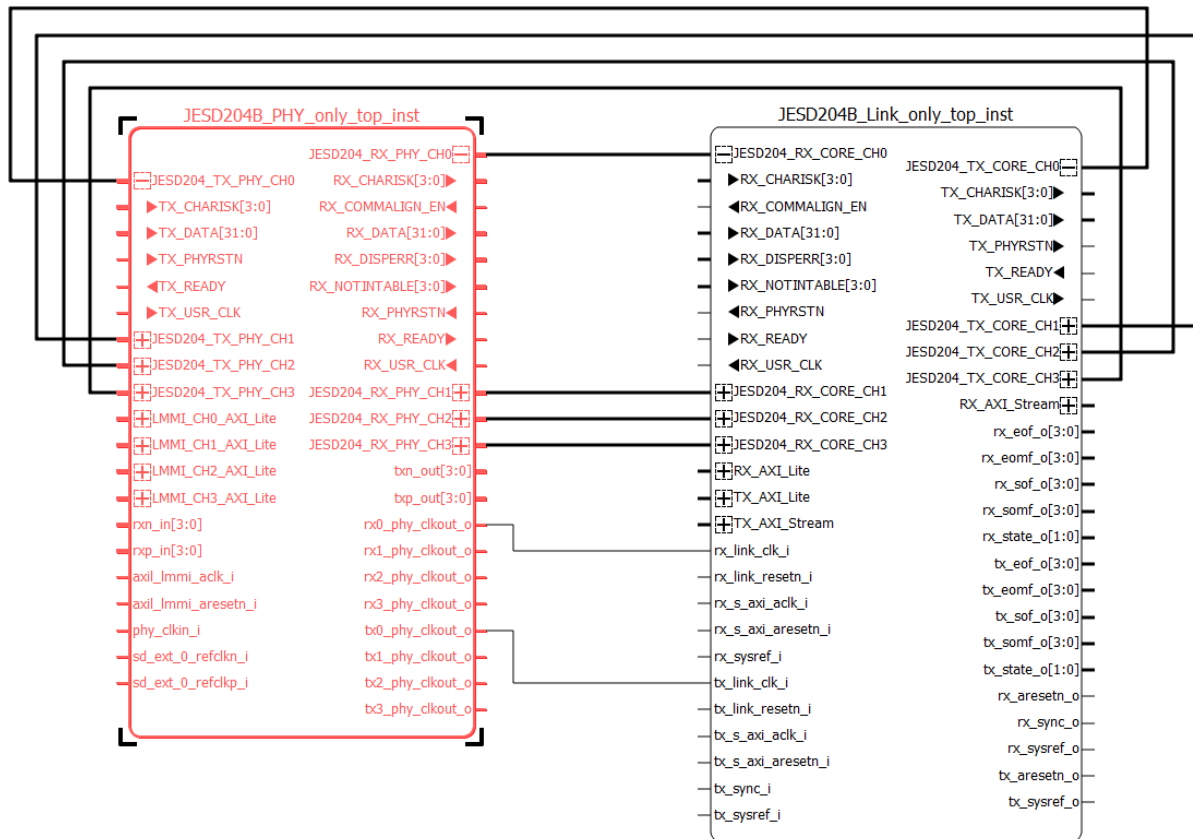


Figure 3.3. JESD204B PHY Only Mode Connection Example

4. Signal Description

This section describes the JESD204B IP ports.

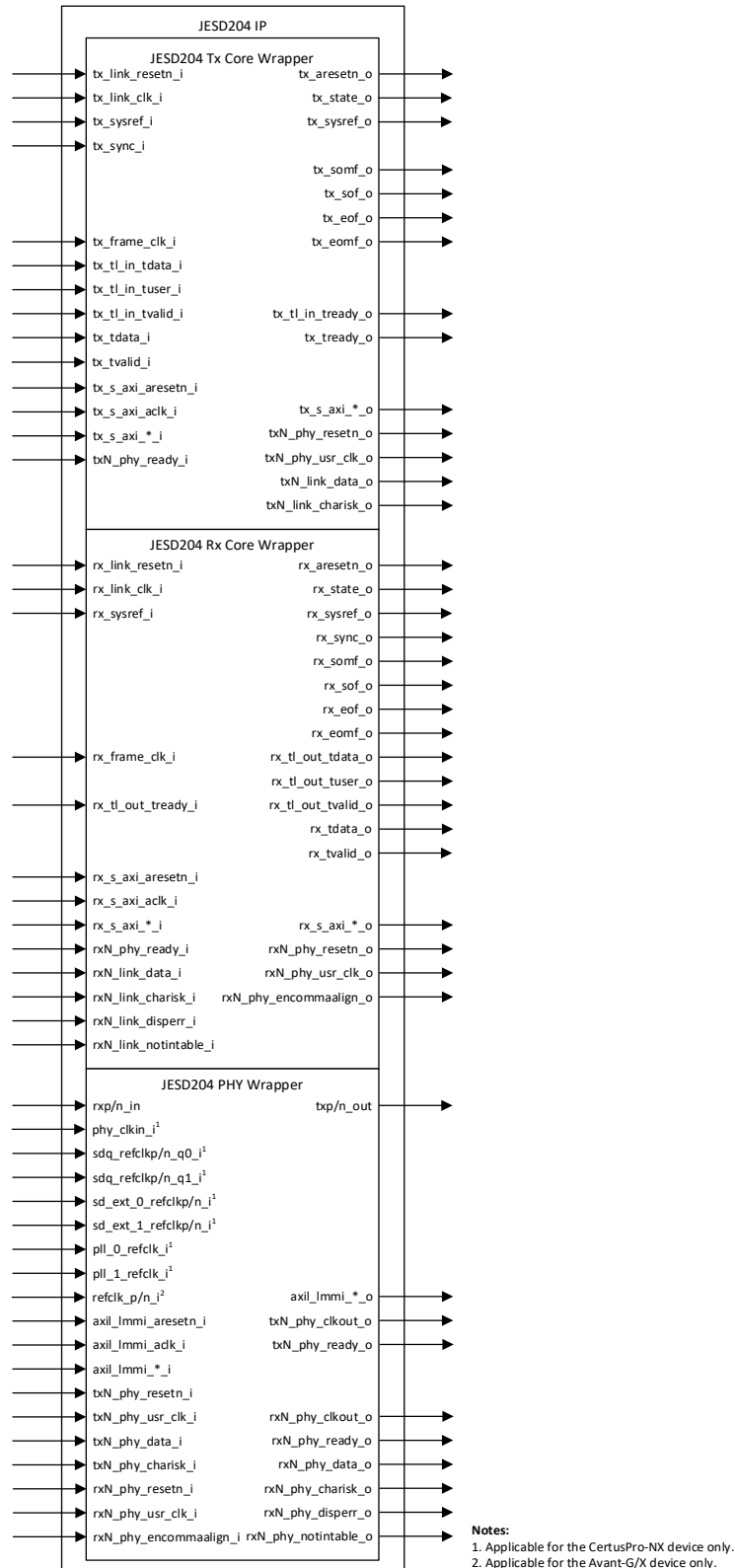


Figure 4.1. JESD204B IP Port Interface Overview

4.1. Signal Interface

Table 4.1. Signal Ports

| Port ¹ | Type | Width | Description |
|---|--------|----------------------|---|
| JESD Tx Link and Transport Layer Interface | | | |
| [Clock domain = tx_link_clk_i] | | | |
| tx_link_resetn_i | Input | 1 | Tx link layer and transport layer reset (active low). Resets PHY wrapper PCS and PMA. |
| tx_link_clk_i | Input | 1 | JESD204B link clock to Tx link. Recommended to connect to device clock from an external clock chip which is generating SYSREF. |
| tx_sysref_i | Input | 1 | SYSREF input for JESD204B subclass 1 implementation. Tied off for subclass 0. Recommended to generate this signal from an external clock chip which has a matched trace length with the device clock. |
| tx_sysref_o | Output | 1 | Retransmit of tx_sysref_i. |
| tx_sync_i | Input | 1 | SYNC input from JESD204B Rx or converter device. 0 – Synchronization request or error reporting from Rx. 1 – Rx in SYNC and ready for ILAS and data phase. |
| tx_state_o | Output | 2 | Indicates Tx link progress. 2'b00 – IDLE stage 2'b01 – CGS in progress 2'b10 – ILAS in progress 2'b11 – User data phase |
| tx_sof_o | Output | 4 | Indicates start of frame. |
| tx_somf_o | Output | 4 | Indicates start of multiframe. |
| tx_eof_o | Output | 4 | Indicates end of frame. |
| tx_eomf_o | Output | 4 | Indicates end of multiframe. |
| tx_aretstn_o | Output | 1 | Active low output reset. Assert (reset) when JESD core is in reset or PHY is not ready. |
| tx_tdata_i | Input | NUMBER_OF_LANES × 32 | Tx link data input from external transport layer where four octets are packed into 32-bit data per lane. Channel 0 always start from LSB. Available when <i>Transport Layer Enable</i> attribute is set to unchecked. |
| tx_tvalid_i | In | 1 | Indicates that tdata is valid. This signal is unused internally but exported for AXI-Streaming protocol compliance. You may tie this input signal to 1'b1. Available when <i>Transport Layer Enable</i> attribute is set to unchecked. |
| tx_tready_o | Output | 1 | Ready signal indicating that the Tx link is ready to accept data. Available when <i>Transport Layer Enable</i> attribute is set to unchecked. |

| Port ¹ | Type | Width | Description |
|--|--------|---|--|
| JESD Rx Embedded Transport Layer Interface (Available when <i>Transport Layer Enable</i> attribute is set to checked) | | | |
| [Clock domain = tx_frame_clk_i] | | | |
| tx_frame_clk_i | Input | 1 | Frame clock. This clock must be derived from the device clock source in a JESD204B system. The required clock frequency is (Data Rate) / ((F × 10) × (TL_FRAME_PER_CLK)). Refer to the Clock Interface section for more information. |
| tx_tl_in_tdata_i | Input | $\text{ceil}((\text{ILA_M}+1) \times (\text{ILA_S}+1) \times (\text{ILA_N}+1) \times \text{TL_FRAME_PER_CLK} / 8) \times 8$ | Input data port from application layer to transport layer. Refer to the Embedded Transport Layer section for information. |
| tx_tl_in_tuser_i | Input | $(\text{ILA_M}+1) \times (\text{ILA_S}+1) \times (\text{ILA_CS}+1) \times \text{TL_FRAME_PER_CLK}$ | Input data port for control bits to transport layer from application layer. Refer to the Embedded Transport Layer section for information. |
| tx_tl_in_tvalid_i | Input | 1 | Valid signal to indicate that the incoming data is valid. Once asserted, it is expected to stay asserted as the data must be streamed to the link layer continuously, unless there is a reset to the system or tx_tl_in_tready_o signal goes low. |
| tx_tl_in_tready_o | Output | 1 | Ready signal indicating that the embedded transport layer is ready to accept data. |
| JESD Tx AXI4 Lite Register Interface | | | |
| [Clock domain = tx_s_axi_aclk_i] | | | |
| tx_s_axi_aclk_i | Input | 1 | JESD204B Tx register AXI4-Lite clock interface (50 – 150 MHz). Refer to the AMBA AXI and ACE Protocol Specification for more information. |
| tx_s_axi_aresetn_i | Input | 1 | AXI reset to Tx AXI register, link layer, and transport layer. Resets PHY wrapper PCS and PMA. Refer to the AMBA AXI and ACE Protocol Specification for more information. |
| tx_s_axi_awaddr_i | Input | 32 | JESD204B Tx register AXI4-Lite interface ports. Refer to the AMBA AXI and ACE Protocol Specification for more information. |
| tx_s_axi_awprot_i | Input | 3 | |
| tx_s_axi_awvalid_i | Input | 1 | |
| tx_s_axi_awready_o | Output | 1 | |
| tx_s_axi_wdata_i | Input | 32 | |
| tx_s_axi_wstrb_i | Input | 4 | |
| tx_s_axi_wvalid_i | Input | 1 | |
| tx_s_axi_wready_o | Output | 1 | |
| tx_s_axi_bresp_o | Output | 2 | |
| tx_s_axi_bvalid_o | Output | 1 | |
| tx_s_axi_bready_i | Input | 1 | |
| tx_s_axi_araddr_i | Input | 32 | |
| tx_s_axi_arprot_i | Input | 3 | |
| tx_s_axi_arvalid_i | Input | 1 | |
| tx_s_axi_arready_o | Output | 1 | |
| tx_s_axi_rdata_o | Output | 32 | |
| tx_s_axi_rresp_o | Output | 2 | |
| tx_s_axi_rvalid_o | Output | 1 | |
| tx_s_axi_rready_i | Input | 1 | |

| Port ¹ | Type | Width | Description |
|--|--------|-----------------|--|
| JESD Tx Link to PHY Bus Interface | | | |
| [Clock domain = tx_link_clk_i] | | | |
| txN_phy_usr_clk_o | Output | 1 | PHY usr clk to be connected to Tx PHY. Sourced from tx_link_clk_i. Available when <i>JESD204 PHY Generation Enable</i> attribute is set to unchecked. |
| txN_link_charisk_o | Output | 4 | Per channel Tx PHY byte control to Tx PHY. Available when <i>JESD204 PHY Generation Enable</i> attribute is set to unchecked. |
| txN_link_data_o | Output | 32 | Per channel Tx PHY parallel data to Tx PHY. Available when <i>JESD204 PHY Generation Enable</i> attribute is set to unchecked. |
| txN_phy_resetrn_o | Output | 1 | Tx link trigger Tx PHY reset. Available when <i>JESD204 PHY Generation Enable</i> attribute is set to unchecked. |
| txN_phy_ready_i | Input | 1 | PHY ready indicator from Tx PHY. Used to reset Tx link. Available when <i>JESD204 PHY Generation Enable</i> attribute is set to unchecked. |
| JESD Tx PHY to or from Link Bus Interface | | | |
| [Clock domain = txN_phy_user_clk_i] | | | |
| txN_phy_clkout_o | Output | 1 | JESD204B Tx recovered clock out. |
| txN_phy_usr_clk_i | Input | 1 | PHY Tx user clock in. Recommended to connect to link layer txN_phy_usr_clk_o. Available when <i>JESD204 IP Core Generation Enable</i> attribute is set to unchecked. |
| txN_phy_charisk_i | Input | 4 | Per channel Tx PHY byte control input from Tx link. Available when <i>JESD204 IP Core Generation Enable</i> attribute is set to unchecked. |
| txN_phy_data_i | Input | 32 | Per channel Tx PHY parallel data input from Tx link. Available when <i>JESD204 IP Core Generation Enable</i> attribute is set to unchecked. |
| txN_phy_resetrn_i | Input | 1 | Reset signal from link layer to reset Tx PHY. PHY reset triggered by link layer reset source tx_s_arsetrn_i, tx_link_resetrn_i, or tx_reg_reset (see note ²). Available when <i>JESD204 IP Core Generation Enable</i> attribute is set to unchecked. |
| txN_phy_ready_o | Output | 1 | Indicates Tx PHY is locked and ready to transmit data. Available when <i>JESD204 IP Core Generation Enable</i> attribute is set to unchecked. |
| JESD Tx PHY Serial Data Interface | | | |
| txp_out | Output | NUMBER_OF_LANES | JESD204B Tx serial data out (positive pin) |
| txn_out | Output | NUMBER_OF_LANES | JESD204B Tx serial data out (negative pin) |
| JESD Rx Link Layer Interface | | | |
| [Clock domain = rx_link_clk_i] | | | |
| rx_link_resetrn_i | Input | 1 | Rx link layer and transport layer reset (active low). Resets PHY wrapper PCS and PMA. |
| rx_link_clk_i | Input | 1 | JESD204B link clock to Rx link. Recommended to connect to device clock from an external clock chip which is generating SYSREF. |
| rx_sysref_i | Input | 1 | SYSREF input for JESD204B subclass 1 implementation. Tied off for subclass 0. Recommended to generate this signal from an external clock chip which has a matched trace length with the device clock. |
| rx_sysref_o | Output | 1 | Retransmit of rx_sysref_i. |

| Port ¹ | Type | Width | Description |
|--|--------|---|--|
| rx_sync_o | Output | 1 | SYNC output to JESD204B transmitter or converter device. 0 – Synchronization request. 1 – Rx in SYNC and ready for ILAS and data phase. |
| rx_state_o | Output | 2 | Indicates Tx link progress. 2'b00 – IDLE stage 2'b01 – CGS in progress 2'b10 – ILAS in progress 2'b11 – User Data Phase |
| rx_sof_o | Output | 4 | Indicates start of frame. |
| rx_somf_o | Output | 4 | Indicates start of multiframe. |
| rx_eof_o | Output | 4 | Indicates end of frame. |
| rx_eomf_o | Output | 4 | Indicates end of multiframe. |
| rx_aresetn_o | Output | 1 | Active low reset output. Assert (reset) when JESD core is in reset, PHY is not ready, or Rx reinit register set. |
| rx_tdata_o | Output | NUMBER_OF_LANES × 32 | Rx link data output to external transport layer where four octets are packed into 32-bit data per lane. Channel 0 always start from LSB. Available when <i>Transport Layer Enable</i> attribute is unchecked. |
| rx_tvalid_o | Output | 1 | Valid signal indicating that the tdata is valid. Available when <i>Transport Layer Enable</i> attribute is unchecked. |
| JESD Rx Embedded Transport Layer Interface (Available when <i>Transport Layer Enable</i> attribute is set to checked) | | | |
| [Clock domain = rx_frame_clk_i] | | | |
| rx_frame_clk_i | Input | 1 | Frame clock. This clock must be derived from the device clock source in a JESD204B system. The required clock frequency is (Data Rate) / ((F × 10) × (TL_FRAME_PER_CLK)). Refer to the Clock Interface section for more information. |
| rx_tl_out_tdata_o | Output | $\text{ceil}((\text{ILA_M}+1) \times (\text{ILA_S}+1) \times (\text{ILA_N}+1) \times \text{TL_FRAME_PER_CLK} / 8) \times 8$ | Output data port for converter samples from embedded transport layer to application layer. Refer to the Embedded Transport Layer section for information. |
| rx_tl_out_tuser_o | Output | $(\text{ILA_M}+1) \times (\text{ILA_S}+1) \times (\text{ILA_CS}+1) \times \text{TL_FRAME_PER_CLK}$ | Output data port for control bits from embedded transport layer to application layer. Refer to the Embedded Transport Layer section for information. |
| rx_tl_out_tvalid_o | Output | 1 | Indicates that the data on tdata and tuser bus are valid. |
| rx_tl_out_tready_i | Input | 1 | Indicates that the AXI-Stream subordinate is ready to accept data. This signal can be always tied to 1 if the subordinate is always able to accept data. |
| JESD Rx AXI4 Lite Register Interface | | | |
| [Clock domain = rx_s_axi_aclk_i] | | | |
| rx_s_axi_aclk_i | Input | 1 | JESD204B Rx register AXI4-Lite clock interface (50 – 150 MHz). Refer to the AMBA AXI and ACE Protocol Specification for more information. |
| rx_s_axi_aresetn_i | Input | 1 | AXI reset to Rx AXI register, link layer, and transport layer. Resets PHY wrapper PCS and PMA. Refer to the AMBA AXI and ACE Protocol Specification for more information. |
| rx_s_axi_awaddr_i | Input | 32 | JESD204B Rx register AXI4-Lite interface ports. Refer to the AMBA AXI and ACE Protocol Specification for more information. |
| rx_s_axi_awprot_i | Input | 3 | |
| rx_s_axi_awvalid_i | Input | 1 | |
| rx_s_axi_awready_o | Output | 1 | |
| rx_s_axi_wdata_i | Input | 32 | |

| Port ¹ | Type | Width | Description |
|--|--------|-------|--|
| rx_s_axi_wstrb_i | Input | 4 | |
| rx_s_axi_wvalid_i | Input | 1 | |
| rx_s_axi_wready_o | Output | 1 | |
| rx_s_axi_bresp_o | Output | 2 | |
| rx_s_axi_bvalid_o | Output | 1 | |
| rx_s_axi_bready_i | Input | 1 | |
| rx_s_axi_araddr_i | Input | 32 | |
| rx_s_axi_arprot_i | Input | 3 | |
| rx_s_axi_arvalid_i | Input | 1 | |
| rx_s_axi_arready_o | Output | 1 | |
| rx_s_axi_rdata_o | Output | 32 | |
| rx_s_axi_rresp_o | Output | 2 | |
| rx_s_axi_rvalid_o | Output | 1 | |
| rx_s_axi_rready_i | Input | 1 | |
| JESD Rx Link to or from PHY Bus Interface | | | |
| [Clock domain = rx_link_clk_i] | | | |
| rxN_link_charisk_i | Input | 4 | Per channel Rx PHY byte control from Rx PHY. Available when <i>JESD204 PHY Generation Enable</i> attribute is set to unchecked. |
| rxN_link_data_i | Input | 32 | Per channel Rx PHY parallel data from Rx PHY. Available when <i>JESD204 PHY Generation Enable</i> attribute is set to unchecked. |
| rxN_link_disperr_i | Input | 4 | Disparity error indicator from Rx PHY. Available when <i>JESD204 PHY Generation Enable</i> attribute is set to unchecked. |
| rxN_link_notintable_i | Input | 4 | Not in table error indicator from Rx PHY. Available when <i>JESD204 PHY Generation Enable</i> attribute is set to unchecked. |
| rxN_phy_ready_i | Input | 1 | PHY ready indicator from Rx PHY. Used to reset Rx link. Available when <i>JESD204 PHY Generation Enable</i> attribute is set to unchecked. |
| rxN_phy_usr_clk_o | Output | 1 | PHY usr clk to be connected to Rx PHY. Sourced from rx_link_clk_i. Available when <i>JESD204 PHY Generation Enable</i> attribute is set to unchecked. |
| rxN_phy_resetrn_o | Output | 1 | Rx link trigger PHY reset. Available when <i>JESD204 PHY Generation Enable</i> attribute is set to unchecked. |
| rxN_phy_encommaalign_o | Output | 1 | Rx link enable PHY comma alignment. PHY comma alignment occurs during the PHY initialization stage. Available when <i>JESD204 PHY Generation Enable</i> attribute is set to unchecked. |
| JESD Rx PHY to Link Bus Interface | | | |
| [Clock domain = rxN_phy_usr_clk_i] | | | |
| rxN_phy_clkout_o | Output | 1 | JESD204B Rx recovered clock out. |
| rxN_phy_data_o | Output | 32 | Per channel Rx PHY parallel data out to link. Available when <i>JESD204 IP Core Generation Enable</i> attribute is set to unchecked. |
| rxN_phy_charisk_o | Output | 4 | Per channel Rx PHY byte control out to link. Available when <i>JESD204 IP Core Generation Enable</i> attribute is set to unchecked. |
| rxN_phy_disperr_o | Output | 4 | Indicates per byte disparity error. Available when <i>JESD204 IP Core Generation Enable</i> attribute is set to unchecked. |

| Port ¹ | Type | Width | Description |
|--|--------|-----------------|--|
| rxN_phy_notintable_o | Output | 4 | Indicates per error when data not in 8b10 encoding table. Available when <i>JESD204 IP Core Generation Enable</i> attribute is set to unchecked. |
| rxN_phy_ready_o | Output | 1 | Indicates Rx PHY is locked and ready to receive external data. Available when <i>JESD204 IP Core Generation Enable</i> attribute is set to unchecked. |
| rxN_phy_resetrn_i | Input | 1 | Reset signal from link layer to reset Rx PHY. PHY reset trigger by link layer reset source rx_s_aresetrn_i, rx_link_resetrn_i, or rx_reg_reset (see note ⁴). Available when <i>JESD204 IP Core Generation Enable</i> attribute is set to unchecked. |
| rxN_phy_encommaalign_i | Input | 1 | To enable PHY comma alignment from link layer. Available when <i>JESD204 IP Core Generation Enable</i> attribute is set to unchecked. |
| rxN_phy_usr_clk_i | Input | 1 | PHY Rx user clock in. Recommended to connect to link layer rxN_phy_usr_clk_o. Available when <i>JESD204 IP Core Generation Enable</i> attribute is set to unchecked. |
| JESD Rx PHY Serial Data Interface | | | |
| rxp_in | Input | NUMBER_OF_LANES | JESD204B Rx serial data in (positive pin) |
| rxn_in | Input | NUMBER_OF_LANES | JESD204B Rx serial data in (negative pin) |
| AXI-Lite to PHY LMMI Interface | | | |
| [Clock domain = axil_lmml_aclk_i] | | | |
| axil_lmml_aresetrn_i | Input | 1 | AXI reset to PHY LMMI interface (active low). Resets PHY LMMI interface. |
| axil_lmml_aclk_i | Input | 1 | AXI4-L clock to LMMI interface (LMMI AXI clock source). CertusPro-NX: 50 – 150 MHz Avant-G/X and Certus-N2: 100 MHz |
| axil_lmml_awvalid_N_i | Input | 1 | AXI4 Lite to LMMI interface ports (per channel). Refer to AMBA AXI Protocol Specification document for AXI4 Lite Protocol specification. Refer to AXI4-Lite to LMMI for AXI4 Lite to LMMI conversion information. For Avant-G/X and Certus-N2 devices, follow the Byte Offset values (LMMI address in Word size x 2) given in the Lattice Avant SERDES/PCS User Guide (FPGA-TN-02313) and Lattice Nexus 2 SERDES/PCS User Guide (FPGA-TN-02395) , respectively, for the axil_lmml_awaddr_N_i and axil_lmml_araddr_N_i signals. |
| axil_lmml_awready_N_o | Output | 1 | |
| axil_lmml_awaddr_N_i | Input | 9 | |
| axil_lmml_awprot_N_i | Input | 3 | |
| axil_lmml_wvalid_N_i | Input | 1 | |
| axil_lmml_wready_N_o | Output | 1 | |
| axil_lmml_wdata_N_i | Input | 32 | |
| axil_lmml_wstrb_N_i | Input | 4 | |
| axil_lmml_bvalid_N_o | Output | 1 | |
| axil_lmml_bready_N_i | Input | 1 | |
| axil_lmml_bresp_N_o | Output | 2 | |
| axil_lmml_arvalid_N_i | Input | 1 | |
| axil_lmml_arready_N_o | Output | 1 | |
| axil_lmml_araddr_N_i | Input | 9 | |
| axil_lmml_arprot_N_i | Input | 3 | |
| axil_lmml_rvalid_N_o | Output | 1 | |
| axil_lmml_rready_N_i | Input | 1 | |
| axil_lmml_rdata_N_o | Output | 32 | |
| axil_lmml_rresp_N_o | Output | 2 | |

Notes:

- For the CertusPro-NX device, N in port names represents channel number (for example, 0, 1, 2, or 3). For the Avant-G/X and Certus-N2 devices, N in the port names represents the quad number (for example, quad 0 for channels 0 to 3 and quad 1 for channels 4 to 7).

- When the PHY is in Rx_and_Tx mode, both txN_phy_resetrn_i and rxN_phy_resetrn_i must be asserted to reset the PMA and PCS. Otherwise, only the PCS is reset. When the PHY is in Rx_only or Tx_only mode, asserting rx_phy_resetrn_i or tx_phy_resetrn_i, respectively, resets both the PMA and PCS.

4.2. Clock Interface

Table 4.2. Clock Ports

| Port ¹ | Type | Width | Description |
|-----------------------------------|-------|-------|--|
| PHY Layer for CertusPro-NX | | | |
| phy_clkln_i | Input | 1 | PHY MPCS CLKIN. Recommended frequency is 100 MHz – 162 MHz. |
| sd_ext_0_refclkp_i | Input | 1 | MPCS PHY PMA REFCLK source from external REFCLK 0 ² . Available when <i>PMA Reference Clock</i> is set to sd_ext_0_refclk. Recommended to generate this signal from an external clock chip which has a matched trace length with link_clk and SYSREF pulse. |
| sd_ext_0_refclkn_i | Input | 1 | MPCS PHY PMA REFCLK source from external REFCLK 0 ² . Available when <i>PMA Reference Clock</i> is set to sd_ext_0_refclk. Recommended to generate this signal from an external clock chip which has a matched trace length with link_clk and SYSREF pulse. |
| sd_ext_1_refclkp_i | Input | 1 | MPCS PHY PMA REFCLK source from external REFCLK 1 ² . Available when <i>PMA Reference Clock</i> is set to sd_ext_1_refclk. Recommended to generate this signal from an external clock chip which has a matched trace length with link_clk and SYSREF pulse. |
| sd_ext_1_refclkn_i | Input | 1 | MPCS PHY PMA REFCLK source from external REFCLK 1 ² . Available when <i>PMA Reference Clock</i> is set to sd_ext_1_refclk. Recommended to generate this signal from an external clock chip which has a matched trace length with link_clk and SYSREF pulse. |
| sdq_refclkp_q0_i | Input | 1 | MPCS PHY PMA REFCLK source from Quad 0 REFCLK ² . Available when <i>PMA Reference Clock</i> is set to sdq0_refclk. Recommended to generate this signal from an external clock chip which has a matched trace length with link_clk and SYSREF pulse. |
| sdq_refclkn_q0_i | Input | 1 | MPCS PHY PMA REFCLK source from Quad 0 REFCLK ² . Available when <i>PMA Reference Clock</i> is set to sdq0_refclk. Recommended to generate this signal from an external clock chip which has a matched trace length with link_clk and SYSREF pulse. |
| sdq_refclkp_q1_i | Input | 1 | MPCS PHY PMA REFCLK source from Quad 1 REFCLK ² . Available when <i>PMA Reference Clock</i> is set to sdq1_refclk. Recommended to generate this signal from an external clock chip which has a matched trace length with link_clk and SYSREF pulse. |
| sdq_refclkn_q1_i | Input | 1 | MPCS PHY PMA REFCLK source from Quad 1 REFCLK ² . Available when <i>PMA Reference Clock</i> is set to sdq1_refclk. Recommended to generate this signal from an external clock chip which has a matched trace length with link_clk and SYSREF pulse. |

| Port ¹ | Type | Width | Description |
|--|--------|-------|--|
| pll_0_refclk_i | Input | 1 | MPCS PHY PMA REFCLK source from GPLL0 ² . Available when PMA Reference Clock is set to pclk0. Using a clock source from GPLL to PHY REFCLK is not recommended ³ . Recommended to generate this signal from an external clock chip which has a matched trace length with link_clk and SYSREF pulse. |
| pll_1_refclk_i | Input | 1 | MPCS PHY PMA REFCLK source from GPLL1 ² . Available when <i>PMA Reference Clock</i> is set to pclk1. Using a clock source from GPLL to PHY REFCLK is not recommended ³ . Recommended to generate this signal from an external clock chip which has a matched trace length with link_clk and SYSREF pulse. |
| PHY Layer for Avant-G/X and Certus-N2 | | | |
| refclk_p_i | Input | 1 | Quad reference clock, positive polarity. Recommended to generate this signal from an external clock chip which has a matched trace length with link_clk and SYSREF pulse. The reference clock frequency must match the <i>Ref Clk Freq</i> attribute. |
| refclk_n_i | Input | 1 | Quad reference clock, negative polarity. |
| PHY Layer across All Devices | | | |
| axil_lmml_aclk_i | Input | 1 | AXI4-Lite clock to LMMI interface. CertusPro-NX: 50 – 150 MHz Avant-G/X and Certus-N2: 100 MHz |
| txN_phy_clkout_o | Output | 1 | Tx PHY recovered clock. Output frequency is Data Rate / 40 bits. Use this clock out as the Tx link clock if needed. If more than one channel is enabled, use the main channel clock out as the link clock. |
| txN_phy_usr_clk_i | Input | 1 | Tx PHY user clock input. Clock source from Tx link layer output txN_phy_usr_clk_o, which is connected to the Tx link clock within the Tx link layer. |
| rxN_phy_clkout_o | Output | 1 | Rx PHY recovered clock. Output frequency is Data Rate / 40 bits. Use this clock out as the Rx link clock if needed. If more than one channel is enabled, use the main channel clock out as the link clock. |
| rxN_phy_usr_clk_i | Input | 1 | Rx PHY user clock input. Clock source from Rx link layer output rxN_phy_usr_clk_o, which is connected to the Rx link clock within the Rx link layer. |
| Link and Transport Layer | | | |
| tx_link_clk_i | Input | 1 | JESD204B Tx link clock. Recommended clock source from Tx PHY recovered clock txN_phy_clkout_o. Connect to the main channel if more than one channel is enabled. |
| rx_link_clk_i | Input | 1 | JESD204B Rx link clock. Recommended clock source from Rx PHY recovered clock rxN_phy_clkout_o. Connect to the main channel if more than one channel is enabled. |
| tx_s_axi_aclk_i | Input | 1 | AXI4-Lite clock Tx register interface (50 – 150 MHz). |
| rx_s_axi_aclk_i | Input | 1 | AXI4-Lite clock Rx register interface (50 – 150 MHz). |
| txN_phy_usr_clk_o | Output | 1 | Tx PHY user clock output from Tx link. Clock source to Tx link output txN_phy_usr_clk_i. Source from tx_link_clk_i. |
| rxN_phy_usr_clk_o | Output | 1 | Rx PHY user clock output from Rx link. Clock source to Rx link output rxN_phy_usr_clk_i. Source from rx_link_clk_i. |

| Port ¹ | Type | Width | Description |
|-------------------|-------|-------|---|
| tx_frame_clk_i | Input | 1 | <p>JESD204B Tx frame clock into embedded transport layer. This clock must be derived from a common clock source in a JESD204B system. The required clock frequency is: $(\text{Data Rate}) / ((F \times 10) \times (\text{TL_FRAME_PER_CLK}))$.</p> <p>Note: F = actual number of octets per frame (not attribute setting or register value).</p> <p>Note: For CertusPro-NX devices, the maximum supported frequency for the Tx frame clock is 185 MHz for the 7_High-Performance_1.0V speed grade and all low power devices.</p> |
| rx_frame_clk_i | Input | 1 | <p>JESD204B Rx frame clock into embedded transport layer. This clock must be derived from a common clock source in a JESD204B system. The required clock frequency is: $(\text{Data Rate}) / ((F \times 10) \times (\text{TL_FRAME_PER_CLK}))$.</p> <p>Note: F = actual number of octets per frame (not attribute setting or register value).</p> <p>Note: For CertusPro-NX devices, the maximum supported frequency for the Rx frame clock is 185 MHz for the 7_High-Performance_1.0V speed grade and all low power devices.</p> |

Notes:

1. N in port names represents channel number (for example, 0, 1, 2, or 3).
2. REFCLK frequency is a value between 74.25 and 162 MHz. Refer to [MPCS Module – Lattice Radiant Software User Guide \(FPGA-IPUG-02118\)](#) for more information.
3. Refer to [CertusPro-NX SerDes/PCS User Guide \(FPGA-TN-02245\)](#) for more information.

5. Register Description

All registers are accessed through the AXI4-Lite interface. [Table 5.1](#) defines the register access types.

Table 5.1. Register Access Types

| Access Type | Access Type Abbreviation | Behavior on Read Access | Behavior on Write Access |
|---------------------------|--------------------------|-------------------------|---|
| Read only | RO | Returns register value | Ignores write access |
| Write only | WO | Returns 0 | Updates register value |
| Read and write | RW | Returns register value | Updates register value |
| Read and write 1 to clear | RW1C | Returns register value | Writing 1'b1 on register bit clears the bit to 1'b0. Writing 1'b0 on register bit is ignored. |
| Reserved | RSVD | Returns 0 | Ignores write access |

5.1. Tx Register

5.1.1. Tx Register Map Overview

Table 5.2. Tx Register Map Overview

| Offset | Name | Description |
|-------------|------------------------|-----------------------------------|
| 0x00 – 0x03 | Control Register | Tx IP control register |
| 0x04 – 0x07 | Status Register | Tx IP status register |
| 0x08 – 0x0B | Reserved | Reserved |
| 0x0C – 0x0F | Test Mode Register | Tx IP test mode register |
| 0x10 – 0x13 | Link Config 0 Register | Tx IP link configuration register |
| 0x14 – 0x17 | Link Config 1 Register | Tx IP link configuration register |
| 0x18 – 0x1B | Link Config 2 Register | Tx IP link configuration register |
| 0x1C – 0x1F | Link Config 3 Register | Tx IP link configuration register |
| 0x20 – 0x23 | Link Config 4 Register | Tx IP Link Configuration Register |
| 0x24 – 0x27 | Link Config 5 Register | Tx IP Link Configuration Register |
| 0x28 – 0x2B | Link Config 6 Register | Tx IP Link Configuration Register |
| 0x2C – 0x2F | Link Config 7 Register | Tx IP Link Configuration Register |

5.1.2. Control Register

Table 5.3. Tx Control Register

| Field | Name | Description | Access | Default |
|---------|--------------------|--|--------|---------|
| [31:29] | Reserved | Reserved | RO | 0 |
| [28:16] | LMFC Buffer Adjust | To delay LMFC buffering. Configuring this register delays SOMF-SOF-EOF-EOMF. This register needs to be configured before the first SYSREF trigger. | RW | 0 |
| [15:10] | Reserved | Reserved | RO | 0 |
| [9] | SYSREF Mask | To mask incoming SYSREF. 0 – Unmask incoming SYSREF 1 – Mask incoming SYSREF SYSREF mask needs to be enabled before the first SYSREF trigger. | RW | 0 |

| Field | Name | Description | Access | Default |
|-------|----------------------|--|--------|--|
| [8] | SYSREF Always Enable | Indicates incoming SYSREF is in one-shot or periodic mode. 0 – SYSREF one-shot mode 1 – SYSREF always mode | RW | SYSREF_ Always attribute mode set in GUI |
| [7:1] | Reserved | Reserved | RO | 0 |
| [0] | Tx Core Reset | Tx Core reset. 0 – Release reset 1 – Reset JESD IP Tx core | RW | 0 |

5.1.3. Status Register

Table 5.4. Tx Status Register

| Field | Name | Description | Access | Default |
|---------|-------------------------|--|--------|---------|
| [31:24] | Reserved | Reserved | RO | 0 |
| [15:8] | SYSREF Mismatch Counter | Number of SYSREF period mismatches detected. Read this offset to reset the counter. SYSREF mismatch detection is only enabled in the SYSREF always mode. | RO | 0 |
| [7:4] | Reserved | Reserved | RO | 0 |
| [3] | PHY Ready | Indicates that PHY calibration is done and ready to accept SYSREF. | RO | 0 |
| [2] | SYSREF Captured | Indicates SYSREF detected and captured. | RO | 0 |
| [1:0] | TX Link State | Indicates the Tx link state. 2'b00 – IDLE state 2'b01 – CGS state 2'b10 – ILA state 2'b11 – User data state | RO | 0 |

5.1.4. Test Mode Register

Table 5.5. Tx Test Mode Register

| Field | Name | Description | Access | Default |
|--------|---------------------|---|--------|---------|
| [31:3] | Reserved | Reserved | RO | 0 |
| [2:0] | Test Pattern Select | Selects the test pattern ¹ . 3'b000 – Tx user data from tx_tdata input 3'b001 – Continuous K28.5 pattern 3'b010 – Continuous D21.5 pattern 3'b011 – RPAT pattern 3'b100 – JSPAT pattern | RW | 0 |

Note:

- When the K28.5 pattern is selected, the JESD204B Tx continuously outputs K28.5 characters without the regular JESD CGS-ILA sequence. When other test patterns are selected, the JESD204B Tx must comply with the regular JESD CGS-ILA sequence before transmitting the test pattern.

5.1.5. Link Config Register

5.1.5.1. Link Config 0 Register

Table 5.6. Tx Link Config 0 Register

| Field | Name | Description | Access | Default |
|---------|------------|--|--------|--|
| [31] | ILA_SCR | Enables or disables the scrambler ¹ . 1 – Enables Tx scrambler 0 – Disables Tx scrambler | RW | Scrambling mode set in GUI |
| [30:29] | Reserved | Reserved | RO | 0 |
| [28:24] | ILA_L | Number of lanes per converter device (link) ² . If number of lanes is 4, ILA_L value is 5'd3. If number of lanes is 8, ILA_L value is 5'd7. | RO | (NUMBER_OF_LANES attribute value set in GUI) – 1 |
| [23] | Reserved | Reserved | RO | 0 |
| [22] | ILA_ADJDIR | Direction to adjust DAC LMFC. | RO | ILA_ADJDIR attribute value set in GUI |
| [21] | ILA_PHADJ | Phase adjustment request to converter device. | RO | ILA_PHADJ attribute value set in GUI |
| [20:16] | Reserved | Reserved | RO | 0 |
| [15:12] | ILA_ADJCNT | Number of adjustment resolution steps to adjust DAC LMFC. | RO | ILA_ADJCNT attribute value set in GUI |
| [11:8] | ILA_BID | Bank ID – Extension to DID | RO | ILA_BID attribute value set in GUI |
| [7:0] | ILA_DID | Device (= link) identification number. | RO | ILA_DID attribute value set in GUI |

Notes:

1. The scrambler is always disabled in the CGS and ILA phases.
2. The configured number of lanes shall not exceed the *Number of Lanes* configured in the IP GUI.

5.1.5.2. Link Config 1 Register

Table 5.7. Tx Link Config 1 Register

| Field | Name | Description | Access | Default |
|---------|----------|--|--------|--|
| [31:30] | ILA_CS | Number of control bits per sample. | RO | Control Bits attribute value set in GUI |
| [29] | Reserved | Reserved | RO | 0 |
| [28:24] | ILA_N | Converter resolution. 5'd0 – Converter resolution is 1 bit 5'd1 – Converter resolution is 2 bits ... 5'd31 – Converter resolution is 32 bits | RO | Converter Resolution attribute value set in GUI |
| [23:16] | ILA_M | Number of converters per device. 8'd0 – 1 converter per device 8'd1 – 2 converters per device ... 8'd255 – 256 converters per device | RO | Converters per Device attribute set in GUI |
| [15:13] | Reserved | Reserved | RO | 0 |
| [12:8] | ILA_K | Number of frames per multiframe. 5'd0 – 1 frame per multiframe 5'd1 – 2 frames per multiframe ... 5'd31 – 32 frames per multiframe | RO | Frames per Multiframe attribute value set in GUI |
| [7:0] | ILA_F | Number of octets per frame. 8'd0 – 1 octet per frame 8'd1 – 2 octets per frame ... 8'd255 – 256 octets per frame | RO | Octets per Frame attribute value set in GUI |

5.1.5.3. Link Config 2 Register

Table 5.8. Tx Link Config 2 Register

| Field | Name | Description | Access | Default |
|---------|-----------|--|--------|--|
| [31:24] | Reserved | Reserved | RO | 0 |
| [23] | ILA_HD | High density format | RO | High Density Format attribute value set in GUI |
| [22:21] | Reserved | Reserved | RO | 0 |
| [20:16] | ILA_CF | Number of control words per frame clock period per link. | RO | Control Words attribute value set in GUI |
| [15:13] | ILA_JESDV | JESD204 version. 000 – JESD204A 001 – JESD204B | RO | ILA_JESDV attribute value set in GUI |

| Field | Name | Description | Access | Default |
|--------|---------------|--|--------|--|
| [12:8] | ILA_S | Number of samples per converter per frame cycle. 5'd0 – 1 sample per converter 5'd1 – 2 samples per converter ... 5'd31 – 32 samples per converter | RO | Samples per Converter per Frame attribute value set in GUI |
| [7:5] | ILA_SUBCLASSV | Device subclass version. 3'b000 – Subclass 0 3'b001 – Subclass 1 | RO | Subclass attribute value set in GUI |
| [4:0] | ILA_Nt | Total number of bits per sample. 5'd0 – 1 bit per sample 5'd1 – 2 bits per sample ... 5'd31 – 32 bits per sample | RO | Number of Bits per Sample attribute value set in GUI |

5.1.5.4. Link Config 3 Register

Table 5.9. Tx Link Config 3 Register

| Field | Name | Description | Access | Default |
|---------|-----------------------------|---|--------|--|
| [31:24] | Reserved | Reserved | RO | 0 |
| [23:16] | Multiframes in ILA Sequence | Number of multiframes during ILA sequence. Default (and minimum) is 4 multiframes. 8'd0 to 8'd2 – Not supported 8'd3 – 4 multiframes (default) 8'd4 – 5 multiframes ... 8'd127 – 128 multiframes | RO | Multi Frames in ILA attribute value set in GUI |
| [15:13] | Reserved | Reserved | RO | 0 |
| [12:0] | Octets per Multiframe | Number of octets per multiframe. This parameter needs to be updated whenever ILA_F or ILA_K changes. Register value: $((ILA_F+1) \times (ILA_K+1)) - 1$ Octets per multiframe: $((ILA_F+1) \times (ILA_K+1))$ Note: Register value + 1 must be a multiple of 4. The lowest register value corresponds to the lowest allowable setting. For example, 0 represents 1 octet per multiframe. | RO | (Octets per Frame attribute value set in GUI + 1) × (Frames per Multiframe attribute value set in GUI + 1) |

5.1.5.5. Link Config 4 Register

Table 5.10. Tx Link Config 4 Register

| Field | Name | Description | Access | Default |
|---------|------------|---------------------------------------|--------|---|
| [31:29] | Reserved | Reserved | RO | 0 |
| [28:24] | ILA_LID_L3 | Lane identification number for Lane 3 | RO | (ILA_LID attribute value set in GUI + 3) if 4 lanes or more, else 0 |
| [23:21] | Reserved | Reserved | RO | 0 |

| Field | Name | Description | Access | Default |
|---------|------------|---------------------------------------|--------|---|
| [20:16] | ILA_LID_L2 | Lane identification number for Lane 2 | RO | (ILA_LID attribute value set in GUI + 2) if 4 lanes or more, else 0 |
| [15:13] | Reserved | Reserved | RO | 0 |
| [12:8] | ILA_LID_L1 | Lane identification number for Lane 1 | RO | (ILA_LID attribute value set in GUI + 1) if 2 lanes or more, else 0 |
| [7:5] | Reserved | Reserved | RO | 0 |
| [4:0] | ILA_LID_L0 | Lane identification number for Lane 0 | RO | ILA_LID attribute value set in GUI |

5.1.5.6. Link Config 5 Register

Table 5.11. Tx Link Config 5 Register

| Field | Name | Description | Access | Default |
|---------|------------|---------------------------------------|--------|---|
| [31:29] | Reserved | Reserved | RO | 0 |
| [28:24] | ILA_LID_L7 | Lane identification number for Lane 7 | RO | (ILA_LID attribute value set in GUI + 7) if 8 lanes, else 0 |
| [23:21] | Reserved | Reserved | RO | 0 |
| [20:16] | ILA_LID_L6 | Lane identification number for Lane 6 | RO | (ILA_LID attribute value set in GUI + 6) if 8 lanes, else 0 |
| [15:13] | Reserved | Reserved | RO | 0 |
| [12:8] | ILA_LID_L5 | Lane identification number for Lane 5 | RO | (ILA_LID attribute value set in GUI + 5) if 8 lanes, else 0 |
| [7:5] | Reserved | Reserved | RO | 0 |
| [4:0] | ILA_LID_L4 | Lane identification number for Lane 4 | RO | (ILA_LID attribute value set in GUI + 4) if 8 lanes, else 0 |

5.1.5.7. Link Config 6 Register

Table 5.12. Tx Link Config 6 Register [Offset 0x28 – 0x2B]

| Field | Name | Description | Access | Default |
|---------|-------------|--|--------|---------|
| [31:24] | ILA_FCHK_L3 | Lane 3 checksum $\Sigma(\text{all ILA fields})\text{mod } 256$. | RO | 0 |
| [23:16] | ILA_FCHK_L2 | Lane 2 checksum $\Sigma(\text{all ILA fields})\text{mod } 256$. | RO | 0 |
| [15:8] | ILA_FCHK_L1 | Lane 1 checksum $\Sigma(\text{all ILA fields})\text{mod } 256$. | RO | 0 |
| [7:0] | ILA_FCHK_L0 | Lane 0 checksum $\Sigma(\text{all ILA fields})\text{mod } 256$. | RO | 0 |

5.1.5.8. Link Config 7 Register

Table 5.13. Tx Link Config 7 Register

| Field | Name | Description | Access | Default |
|---------|-------------|--|--------|---------|
| [31:24] | ILA_FCHK_L7 | Lane 7 checksum $\Sigma(\text{all ILA fields})\text{mod } 256$. | RO | 0 |
| [23:16] | ILA_FCHK_L6 | Lane 6 checksum $\Sigma(\text{all ILA fields})\text{mod } 256$. | RO | 0 |
| [15:8] | ILA_FCHK_L5 | Lane 5 checksum $\Sigma(\text{all ILA fields})\text{mod } 256$. | RO | 0 |
| [7:0] | ILA_FCHK_L4 | Lane 4 checksum $\Sigma(\text{all ILA fields})\text{mod } 256$. | RO | 0 |

5.2. Rx Register

5.2.1. Rx Register Map Overview.

Table 5.14. Rx Register Map Overview

| Offset | Name | Description |
|-------------|----------------------------|--|
| 0x00 – 0x03 | Control Register | Rx IP control register |
| 0x04 – 0x07 | Status Register | Rx IP status register |
| 0x08 – 0x0B | Error Status Register | Rx IP Error Status Register |
| 0x0C – 0x0F | Reserved | Reserved |
| 0x10 – 0x13 | Link Config 0 Register | Rx IP Link Configuration Status Register |
| 0x14 – 0x17 | Link Config 1 Register | Rx IP Link Configuration Status Register |
| 0x18 – 0x1B | Link Config 2 Register | Rx IP Link Configuration Status Register |
| 0x1C – 0x1F | Link Config 3 Register | Rx IP Link Configuration Status Register |
| 0x20 – 0x23 | Link Config 4 Register | Rx IP Link Configuration Status Register |
| 0x24 – 0x27 | Link Config 5 Register | Rx IP Link Configuration Status Register |
| 0x28 – 0x2B | Link Config 6 Register | Rx IP Link Configuration Status Register |
| 0x2C – 0x2F | Link Config 7 Register | Rx IP Link Configuration Status Register |
| 0x30 – 0x33 | Error Counter Register | Rx IP Error Counter Register |
| 0x34 – 0x37 | Buffer Fill Level Register | Rx IP Buffer Fill Level Register |

5.2.2. Control Register

Table 5.15. Rx Control Register

| Field | Name | Description | Access | Default |
|---------|--------------------------|--|--------|--|
| [31:29] | Reserved | Reserved | RO | 0 |
| [28:16] | LMFC Buffer Adjust | To delay LMFC buffering. Configuring this register delays SOMF-SOF-EOF-EOMF. This register needs to be configured before the first SYSREF trigger. The input value must be less than (Octets per Multiframe – 1) / 4 because four octets are processed every one cycle of internal LMFC. | RW | 0 |
| [15:10] | Reserved | Reserved | RO | 0 |
| [9] | SYSREF Mask | To mask incoming SYSREF. 0 – Unmask incoming SYSREF 1 – Mask incoming SYSREF SYSREF mask needs to be enabled before the first SYSREF trigger. | RW | 0 |
| [8] | SYSREF Always Enable | Indicates incoming SYSREF is in one-shot or periodic mode. 0 – SYSREF one-shot mode 1 – SYSREF always mode | RW | SYSREF_ Always attribute mode set in GUI |
| [7:2] | Reserved | Reserved | RO | 0 |
| [1] | Rx Core Reinitialization | The JESD204B IP reinitializes the Rx core to enter the IDLE stage and deasserts SYNC output (low). Write 1 to de-assert SYNC and reenter IDLE. This bit automatically clears after the write operation. | WO | 0 |
| [0] | Rx Core Reset | Rx core reset. 0 – Release reset 1 – Reset JESD IP Rx core | RW | 0 |

5.2.3. Status Register

Table 5.16. Rx Status Register

| Field | Name | Description | Access | Default |
|---------|-------------------------|--|--------|---------|
| [31:24] | Reserved | Reserved | RO | 0 |
| [15:8] | SYSREF Mismatch Counter | Number of SYSREF period mismatches detected. Read this offset to reset the counter. SYSREF mismatch detection is only enabled in the SYSREF always mode. | RO | 0 |
| [7:4] | Reserved | Reserved | RO | 0 |
| [3] | PHY Ready | Indicates that PHY calibration is done and ready to accept SYSREF | RO | 0 |
| [2] | SYSREF Captured | Indicates SYSREF detected and captured. | RO | 0 |
| [1:0] | RX Link State | Indicates the Rx link state. 2'b00 – IDLE state 2'b01 – CGS state 2'b10 – ILA state 2'b11 – User data state | RO | 0 |

5.2.4. Error Status Register

Table 5.17. Rx Error Status Register

| Field | Name | Description | Access | Default |
|---------|---|---|--------|---------|
| [31] | Reserved | Reserved | RO | 0 |
| [30:28] | Error Counter Read Channel Select (ERRCNT_CH_SEL) | Selects which channel's error counter to be read from the Rx error counter register (Rx register offset 0x30). Applies simultaneously to the disparity error, not in table error, and unexpected control character counters. | RW | 0 |
| [27:24] | Reserved | Reserved | RO | 0 |
| [23:16] | Unexpected Control Character Flag | Unexpected control character (per channel) detected in character replacement since the previous read of this register. The error counter can be read from the Rx error counter register after selecting the channel via ERRCNT_CH_SEL. Write 1 to clear the selected channel counter and this flag. When operating in Subclass 0 mode, the Rx state machine directly enters the DATA phase after one clock cycle in the ILA state. The character replacement block activates from this point of time. If Rx receives ILA data during this period, some of the control characters in the ILA data will be reported as unexpected control character errors. The error count stabilizes after Tx enters the DATA phase. | RW1C | 0 |
| [15:8] | Not In Table Error Flag | Not In table error (per channel) detected since the previous read of this register. The error counter can be read from the Rx error counter register after selecting the channel via ERRCNT_CH_SEL. Write 1 to clear the selected channel counter and this flag. | RW1C | 0 |
| [7:0] | Disparity Error Flag | Disparity error (per channel) detected since the previous read of this register. The error counter can be read from Rx error counter register after selecting the channel via ERRCNT_CH_SEL. Write 1 to clear the selected counter and this flag. | RW1C | 0 |

5.2.5. Link Config Register

5.2.5.1. Link Config 0 Register

Table 5.18. Rx Link Config 0 Register

| Field | Name | Description | Access | Default |
|---------|------------|--|--------|--|
| [31] | ILA_SCR | Scrambler enable status ¹ . 0 – Tx scrambler disabled 1 – Tx scrambler enabled | RO | Scrambling mode set in GUI |
| [30:29] | Reserved | Reserved | RO | 0 |
| [28:24] | ILA_L | Number of lanes per converter device (link) ² . If number of lanes is 4, ILA_L value is 5'd3. If number of lanes is 8, ILA_L value is 5'd7. | RO | (NUMBER_OF_LANES attribute value set in GUI) – 1 |
| [23] | Reserved | Reserved | RO | 0 |
| [22] | ILA_ADJDIR | Direction to adjust DAC LMFC. | RO | ILA_ADJDIR attribute value set in GUI |
| [21] | ILA_PHADJ | Phase adjustment request to converter device. | RO | ILA_PHADJ attribute value set in GUI |

| Field | Name | Description | Access | Default |
|---------|------------|---|--------|---------------------------------------|
| [20:16] | Reserved | Reserved | RO | 0 |
| [15:12] | ILA_ADJCNT | Number of adjustment resolution steps to adjust DAC LMFC. | RO | ILA_ADJCNT attribute value set in GUI |
| [11:8] | ILA_BID | Bank ID – Extension to DID | RO | ILA_BID attribute value set in GUI |
| [7:0] | ILA_DID | Device (= link) identification number. | RO | ILA_DID attribute value set in GUI |

Notes:

1. The scrambler is always disabled in the CGS and ILA phases.
2. The configured number of lanes shall not exceed the *Number of Lanes* configured in the IP GUI.

5.2.5.2. Link Config 1 Register

Table 5.19. Rx Link Config 1 Register

| Field | Name | Description | Access | Default |
|---------|----------|--|--------|--|
| [31:30] | ILA_CS | Number of control bits per sample. | RO | Control Bits attribute value set in GUI |
| [29] | Reserved | Reserved | RO | 0 |
| [28:24] | ILA_N | Converter resolution. 5'd0 – Converter resolution is 1 bit 5'd1 – Converter resolution is 2 bits ... 5'd31 – Converter resolution is 32 bits | RO | Converter Resolution attribute value set in GUI |
| [23:16] | ILA_M | Number of converters per device. 8'd0 – 1 converter per device 8'd1 – 2 converters per device ... 8'd255 – 256 converters per device | RO | Converters per Device attribute value set in GUI |
| [15:13] | Reserved | Reserved | RO | 0 |
| [12:8] | ILA_K | Number of frames per multiframe. 5'd0 – 1 frame per multiframe 5'd1 – 2 frames per multiframe ... 5'd31 – 32 frames per multiframe | RO | Frames per Multiframe attribute value set in GUI |
| [7:0] | ILA_F | Number of octets per frame. 8'd0 – 1 octet per frame 8'd1 – 2 octets per frame ... 8'd255 – 256 octets per frame | RO | Octets per Frame attribute value set in GUI |

5.2.5.3. Link Config 2 Register

Table 5.20. Rx Link Config 2 Register

| Field | Name | Description | Access | Default |
|---------|---------------|--|--------|--|
| [31:24] | Reserved | Reserved | RO | 0 |
| [23] | ILA_HD | High density format | RO | High Density Format attribute value set in GUI |
| [22:21] | Reserved | Reserved | RO | 0 |
| [20:16] | ILA_CF | Number of control words per frame clock period per link | RO | Control Words attribute value set in GUI |
| [15:13] | ILA_JESDV | JESD204 version. 000 – JESD204A 001 – JESD204B | RO | ILA_JESDV attribute value set in GUI |
| [12:8] | ILA_S | Number of samples per converter per frame cycle. 5'd0 – 1 sample per converter 5'd1 – 2 samples per converter ... 5'd31 – 32 samples per converter | RO | Samples per Converter per Frame attribute value set in GUI |
| [7:5] | ILA_SUBCLASSV | Device subclass version. 3'b000 – Subclass 0 3'b001 – Subclass 1 | RO | Subclass attribute value set in GUI |
| [4:0] | ILA_Nt | Total number of bits per sample. 5'd0 – 1 bit per sample 5'd1 – 2 bits per sample ... 5'd31 – 32 bits per sample | RO | Number of Bits per Sample attribute value set in GUI |

5.2.5.4. Link Config 3 Register

Table 5.21. Rx Link Config 3 Register

| Field | Name | Description | Access | Default |
|---------|-----------------------------|---|--------|--|
| [31:24] | Reserved | Reserved | RO | 0 |
| [23:16] | Multiframes in ILA Sequence | Number of multiframes during ILA Sequence. Default (and minimum) is 4 multiframes. 8'd0 to 8'd2 - Not supported 8'd3 – 4 multiframes (default) 8'd4 – 5 multiframes ... 8'd127 – 128 multiframes | RW | Multi Frames in ILA attribute value set in GUI |
| [15:13] | Reserved | Reserved | RO | 0 |

| Field | Name | Description | Access | Default |
|--------|-----------------------|---|--------|--|
| [12:0] | Octets per MultiFrame | Number of octets per multiframe. This parameter needs to be updated whenever ILA_F or ILA_K changes. Register value: $((ILA_F+1) \times (ILA_K+1)) - 1$ Octets per multiframe: $((ILA_F+1) \times (ILA_K+1))$ Note: Register value + 1 must be a multiple of 4. The lowest register value corresponds to the lowest allowable setting. For example, 0 represents 1 octet per multiframe. | RW | (Octets per Frame attribute value set in GUI + 1) × (Frames per Multiframe attribute value set in GUI + 1) |

5.2.5.5. Link Config 4 Register

Table 5.22. Rx Link Config 4 Register

| Field | Name | Description | Access | Default |
|---------|------------|---------------------------------------|--------|---|
| [31:29] | Reserved | Reserved | RO | 0 |
| [28:24] | ILA_LID_L3 | Lane identification number for Lane 3 | RO | (ILA_LID attribute value set in GUI + 3) if 4 lanes or more, else 0 |
| [23:21] | Reserved | Reserved | RO | 0 |
| [20:16] | ILA_LID_L2 | Lane identification number for Lane 2 | RO | (ILA_LID attribute value set in GUI + 2) if 4 lanes or mode, else 0 |
| [15:13] | Reserved | Reserved | RO | 0 |
| [12:8] | ILA_LID_L1 | Lane identification number for Lane 1 | RO | (ILA_LID attribute value set in GUI + 1) if 2 lanes or more, else 0 |
| [7:5] | Reserved | Reserved | RO | 0 |
| [4:0] | ILA_LID_L0 | Lane identification number for Lane 0 | RO | ILA_LID attribute value set in GUI |

5.2.5.6. Link Config 5 Register

Table 5.23. Rx Link Config 5 Register

| Field | Name | Description | Access | Default |
|---------|------------|---------------------------------------|--------|---|
| [31:29] | Reserved | Reserved | RO | 0 |
| [28:24] | ILA_LID_L7 | Lane identification number for Lane 7 | RO | (ILA_LID attribute value set in GUI + 7) if 8 lanes, else 0 |
| [23:21] | Reserved | Reserved | RO | 0 |
| [20:16] | ILA_LID_L6 | Lane identification number for Lane 6 | RO | (ILA_LID attribute value set in GUI + 6) if 8 lanes, else 0 |
| [15:13] | Reserved | Reserved | RO | 0 |
| [12:8] | ILA_LID_L5 | Lane identification number for Lane 5 | RO | (ILA_LID attribute value set in GUI + 5) if 8 lanes, else 0 |
| [7:5] | Reserved | Reserved | RO | 0 |
| [4:0] | ILA_LID_L4 | Lane identification number for Lane 4 | RO | (ILA_LID attribute value set in GUI + 4) if 8 lanes, else 0 |

5.2.5.7. Link Config 6 Register

Table 5.24. Rx Link Config 6 Register

| Field | Name | Description | Access | Default |
|---------|-------------|---|--------|---------|
| [31:24] | ILA_FCHK_L3 | Lane 3 checksum $\Sigma(\text{all ILA fields}) \bmod 256$. | RO | 0 |
| [23:16] | ILA_FCHK_L2 | Lane 2 checksum $\Sigma(\text{all ILA fields}) \bmod 256$. | RO | 0 |
| [15:8] | ILA_FCHK_L1 | Lane 1 checksum $\Sigma(\text{all ILA fields}) \bmod 256$. | RO | 0 |
| [7:0] | ILA_FCHK_L0 | Lane 0 checksum $\Sigma(\text{all ILA fields}) \bmod 256$. | RO | 0 |

5.2.5.8. Link Config 7 Register

Table 5.25. Rx Link Config 7 Register

| Field | Name | Description | Access | Default |
|---------|-------------|---|--------|---------|
| [31:24] | ILA_FCHK_L7 | Lane 7 checksum $\Sigma(\text{all ILA fields}) \bmod 256$. | RO | 0 |
| [23:16] | ILA_FCHK_L6 | Lane 6 checksum $\Sigma(\text{all ILA fields}) \bmod 256$. | RO | 0 |
| [15:8] | ILA_FCHK_L5 | Lane 5 checksum $\Sigma(\text{all ILA fields}) \bmod 256$. | RO | 0 |
| [7:0] | ILA_FCHK_L4 | Lane 4 checksum $\Sigma(\text{all ILA fields}) \bmod 256$. | RO | 0 |

5.2.6. Error Counter Register

Table 5.26. Rx Error Counter Register

| Field | Name | Description | Access | Default |
|---------|------------------------------|--|--------|---------|
| [31:24] | Reserved | Reserved | RO | 0 |
| [23:16] | Unexpected Control Character | Unexpected control character error counter during character replacement. Configure ERRCNT_CH_SEL (Rx error status register bit[30:28]) to select which channel's error counter to be read. When operating in Subclass 0 mode, the Rx state machine directly enters the DATA phase after one clock cycle in the ILA state. The character replacement block activates from this point of time. If Rx receives ILA data during this period, some of the control characters in the ILA data will be reported as unexpected control character errors. The error count stabilizes after Tx enters the DATA phase. | RO | 0 |
| [15:8] | Not In Table Error Count | Not In table error counter. Configure ERRCNT_CH_SEL ((Rx error status register bit[30:28])) to select which channel's error counter to be read. | RO | 0 |
| [7:0] | Disparity Error Counter | Disparity error counter. Configure ERRCNT_CH_SEL ((Rx error status register bit[30:28]) to select which channel's error counter to be read. | RO | 0 |

5.2.7. Buffer Fill Level Register

Table 5.27. Buffer Fill Level Register

| Field | Name | Description | Access | Default |
|---------|-------------------|--|--------|---------|
| [31:13] | Reserved | Reserved | RO | 0 |
| [12:0] | Buffer Fill Level | Buffer fill level in multilane alignment block. This register indicates the buffer fill level from the latest arrival lane (the last lane to exit CGS state) to the release point of internal LMFC counter. Configure LMFC Buffer Adjust (Rx Control Register bit[28:16]) to manipulate the release point. For example, if the current octets per multiframe is set to 128 and the IP processes four octets per clock cycle, the LMFC counter cycles through a maximum value of $128 / 4 = 32$ (<i>Max LMFC count value</i>). Consequently, the buffer fill level must remain below this threshold. To control the release point, read this register when the core is in the DATA state following initial power up. As an example, if the observed fill level is 30, configure LMFC Buffer Adjust register to 6. The expected fill level after the next reset is calculated as follows: $\text{Fill Level} = (30 + 6) - 32 = 4$ It is recommended that the buffer fill level stay above 2 but below $\text{Max LMFC count value} - 2$ to account for temperature or process variation. Note: The subtraction of 32 accounts for the circular nature of the LMFC counter. | RO | 0 |

6. Example Design

Lattice provides example designs for simulation and hardware validation. For simulation, an example design is available through the simulation testbench for you to compile, simulate, and test the JESD204B IP. Refer to the [Running Functional Simulation](#) section for more information. For hardware validation, the example designs allow you to compile and test the JESD204B IP on the following evaluation boards:

- CertusPro-NX Evaluation Board
- Avant-X Versa Board

6.1. CertusPro-NX Device Example Design

This section shows an example design to validate the JESD204B IP in the CertusPro-NX device using the CertusPro-NX Evaluation Board and ADI ADRV9009 Dual RF Evaluation Board. The design is configured to run at a lane rate of 4.9152 Gb/s with four Tx lanes and two Rx lanes being utilized.

6.1.1. Example Design Supported Configuration

Table 6.1. JESD204B IP Configuration Supported by the CertusPro-NX Device Example Design

| JESD204B IP GUI Parameter | JESD204B IP configuration in example demo design | | |
|-------------------------------------|--|-------------|-------------|
| | JESD PHY | JESD Tx | JESD Rx |
| General | | | |
| JESD204 IP Core Generation Enable | Unchecked | Checked | Checked |
| Mode | Rx_and_Tx | Tx_only | Rx_only |
| Data Rate (Gb/s) | 4.9152 | 4.9152 | 4.9152 |
| Number of Lanes (L) | 4 | 4 | 2 |
| Converters per Device (M) | — | 3 | 3 |
| Samples per Converter per Frame (S) | — | 0 | 0 |
| Converter Resolution (N) | — | 15 | 15 |
| Number of Bits per Sample (Nt) | — | 15 | 15 |
| Control Bits (CS) | — | 0 | 0 |
| Control Words (CF) | — | 0 | 0 |
| High Density Format (HD) | — | 0 | 0 |
| Octets per Frame (F) | — | 1 | 3 |
| Frames per Multiframe (K) | — | 31 | 31 |
| Multi Frames in ILA | — | 3 | 3 |
| Subclass (SUBCLASSV) | — | 1 | 1 |
| SYSREF Always | — | SYSREF_ONCE | SYSREF_ONCE |
| Scrambling (SCR) | — | DISABLED | DISABLED |
| ILA_DID | — | 85 | 85 |
| ILA_ADJCNT | — | 0 | 0 |
| ILA_BID | — | 0 | 0 |
| ILA_ADJDIR | — | 0 | 0 |
| ILA_PHADJ | — | 0 | 0 |
| ILA_JESDV | — | 1 | 1 |
| ILA_LID | — | 0 | 0 |
| PHY Settings | | | |
| JESD204 PHY Generation Enable | Checked | Unchecked | Unchecked |

| JESD204B IP GUI Parameter | JESD204B IP configuration in example demo design | | |
|---------------------------|--|-----------|-----------|
| | JESD PHY | JESD Tx | JESD Rx |
| Lane ID | 0 | — | — |
| PMA Reference Clock | sd_ext_1_refclk | — | — |
| Ref Clk Freq (MHz) | 122.88 | — | — |
| PMA Clock Divider | 1 | — | — |
| PLL M Settings | 2 | — | — |
| Optional Features | | | |
| Transport Layer Enable | Unchecked | Checked | Checked |
| Frame per Clock | — | 2 | 1 |
| Test Mode Enable | Unchecked | Unchecked | Unchecked |

6.1.2. Overview of the Example Design and Features

Key features of the example design include:

- Interoperability with ADI ADRV9009 Dual RF Evaluation Board configured to 4T2R (transmitter configured to four lanes, receiver configured to two lanes).
- Lane rate of 4.9152 Gb/s.
- IP core includes an embedded transport layer which allows IQ data to be directly connected to the IP core interface.
- Utilized RISC V MC IP core to configure ADI ADRV9009 Dual RF Evaluation Board settings through SPI interface, as well as to control or read status from JESD IP instances through AHB and AXI-Lite interfaces.

6.1.3. Example Design Components

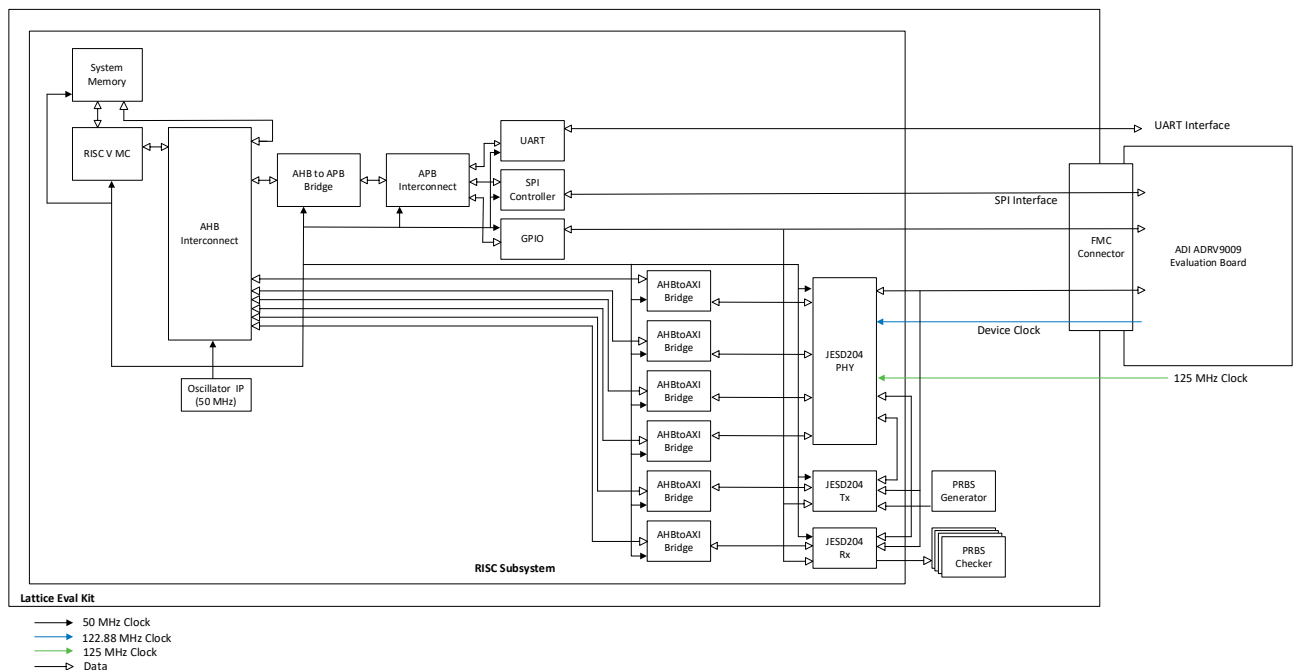


Figure 6.1. JESD204B Example Design Block Diagram

The JESD204B example design includes the following blocks:

- JESD204B Tx
- JESD204B Rx
- JESD204B PHY

- PRBS Generator
- PRBS Checker
- AHB to AXI Bridge
- RISC subsystem

6.1.3.1. JESD204B Tx

This block receives the IQ data from a PRBS generator and packetizes the data into JESD204B compliant packets before transmitting the data to the JESD204B PHY block. It contains an internal transport layer which can remap the data directly from data converter to the internal core. This block is instantiated separately from the JESD204B Rx block as both have a different configuration in this example design.

6.1.3.2. JESD204B Rx

This block receives the data from the JESD204B PHY block and outputs the sample data to multiple PRBS checkers to check for data correctness. It has an internal transport layer which remaps the data from internal core to the converter's sample format. This block is instantiated separately from the JESD204B Tx block as both have a different configuration in this example design.

6.1.3.3. JESD204B PHY

This block wraps around the SERDES IP of the targeted device family and connects to both the JESD204B Tx and Rx blocks. The function of this block is to serialize the parallel data from the JESD204B Tx and transmit the serial data to an external component, as well as to de-serialize the serial data from an external component and send the parallel data for further processing in the JESD204B Rx block. This block is instantiated separately from the JESD204B Tx and Rx blocks, as Tx and Rx have different core configurations but shares the same transceiver channel on the physical port.

6.1.3.4. PRBS Generator

This block generates a PRBS7 data sequence to the IP core.

6.1.3.5. PRBS Checker

Each checker receives the data from the JESD204B Rx block for one converter's samples and performs the PRBS data sequence checking. It makes sure that the data received matches the PRBS7 data sequence and flags an error if any error is detected.

6.1.3.6. AHB to AXI Bridge

This block converts the data from the AHB interconnect data bus in the RISC subsystem and outputs the equivalent transfer on the AXI4 output interface. The AXI4 interfaces are then connected to each AXI4-Lite interface on the JESD204B blocks so that these blocks can be controlled via the RISC-V MC IP module contained in the RISC subsystem.

6.1.3.7. RISC Subsystem

This block is essentially a subsystem which is comprised of a RISC V MC IP, System Memory IP, AHB and APB Interconnect IPs, AHB to APB Bridge IP, UART IP, SPI Controller IP, GPIO IP, and Oscillator IP. All blocks are connected to the RISC V MC IP which serves as the brain of the design. It controls the GPIO and SPI Controller IPs, whose outputs are directly connected to the ADI ADRV9009 Dual RF Evaluation Board via the FMC connector, to power on the daughter card and configure the JESD link and clock chip on the daughter card. It can also control and read the status from the JESD204B PHY, Tx, and Rx blocks and output the log message via the UART terminal.

6.1.4. Hardware Testing

6.1.4.1. Running the Hardware without Rebuilding the Design

1. Connect the ADI ADRV9009 Dual RF Evaluation Board to the Lattice CertusPro-NX (CPNX) Evaluation Board.
2. Connect a 30.72 MHz clock source to REF_CLK_IN (J401) SMA connector of the ADRV9009 evaluation board.
3. Make sure that the UART debug jumpers (JP1 and JP2) on the CPNX evaluation board are connected with a jumper pin.
4. Connect a USB cable from your PC to the mini-USB connector on the CPNX evaluation board.
5. Unzip the CPNX_EVAL_ADRV9009.zip file from the eval folder within the IP core directory.
6. Open the Radiant Programmer tool.
7. Go to the source directory and locate the impl_1.xcf file.

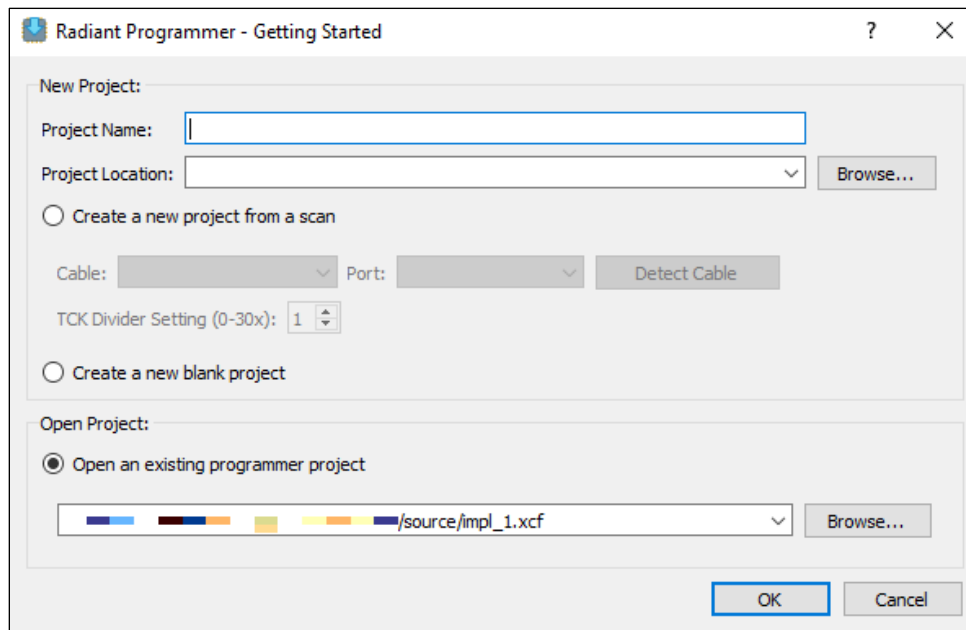


Figure 6.2. Opening a Programmer Project

8. Program the FPGA device with the generated bitstream file.

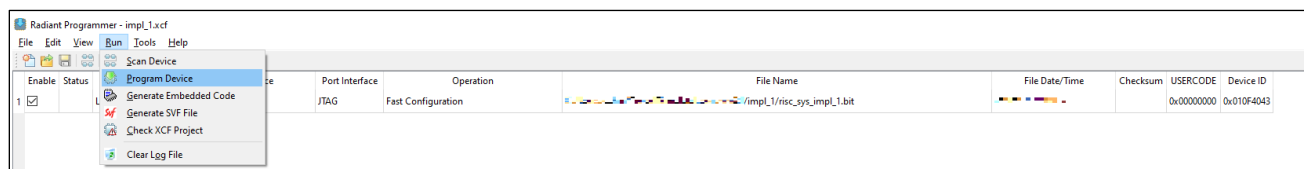


Figure 6.3. Programming the Device through the Run Menu

You should see seven green LEDs lighting up sequentially. If you have a serial port communication program such as PuTTY, you may also open a terminal to see the log messages. Note that before programming, in PuTTY, set the **Serial line** to the correct value, **Speed** (baud rate) to 115200, and **Connection type** to Serial. Alternatively, you can also use the terminal in Lattice Propel.

```

Hello
talise: Booting up ADRV9009 device.
talise: Device Revision 192, Firmware 6.2.1, API 3.6.2.1
talise: Running ARM Initialization Calibrations.
talise: Setting up JESD link on ADRV9009.
talise: Enable Framer Test with PRBS7.
fpga: Reset FPGA PHY and wait for ready...
fpga: Before SYSREF - JESD TX PHY ready = 1
fpga: Before SYSREF - JESD TX PHY ready = 1
fpga: Core is ready to accept SYSREF...
fpga: Request for SYSREF...
fpga: After SYSREF - JESD TX register 0x04 = f
fpga: After SYSREF - JESD RX register 0x04 = f
talise: TAL_DEFRAMER_A status 0x86
talise: TAL_FRAMER_A status 0x25
    
```

Figure 6.4. Programming Log Messages

Four yellow LEDs should also light up at the end of programming. The LEDs represent different status or signals of the design as summarized in [Table 6.2](#).

Table 6.2. Summary of LED Indicators on CPNX Evaluation Board

| Schematic Signal Name | Label On Board | RTL Signal Name | Description |
|-----------------------|----------------|-----------------|---|
| LED_0 | D6 | led_g_o[0] | SYNC input from ADRV9009. JESD Rx on ADRV9009 has passed the CGS state when the LED lights up. |
| LED_1 | D7 | led_g_o[1] | Tx PHY has gone through calibration and is ready when the LED lights up. |
| LED_2 | D8 | led_g_o[2] | Tx JESD core is in the user data phase when the LED lights up. |
| LED_3 | D9 | led_g_o[3] | TREADY signal from JESD Tx core transport layer. The core is ready to accept user data when the LED lights up. |
| LED_4 | D10 | led_g_o[4] | Rx PHY has gone through calibration and is ready when the LED lights up. |
| LED_5 | D11 | led_g_o[5] | Rx JESD core is in the user data phase when the LED lights up. |
| LED_6 | D12 | led_g_o[6] | TVALID signal from JESD Rx core transport layer. The Rx core is outputting valid samples data when the LED lights up. |
| LED_7 | D13 | led_g_o[7] | PRBS checker status. The PRBS checker does not detect any error (for PRBS7 data sequence) in the incoming data stream. This LED is expected to be initially off when led_g_o[6] first lights up. Toggle the SW4 push button to clear the initial PRBS error and this LED should light up if there is no PRBS error detected afterwards. |
| LED_8 | D14 | led_y_o[0] | Bit[1] of the JESD Tx core tx_state_o output signal. Serves as a debug signal to determine the state in which the core is stuck when led_g_o[2] does not light up. |
| LED_9 | D15 | led_y_o[1] | Bit[0] of the JESD Tx core tx_state_o output signal. Serves as a debug signal to determine the state in which the core is stuck when led_g_o[2] does not light up. |
| LED_14 | D20 | led_y_o[6] | Bit[1] of the JESD Rx core rx_state_o output signal. Serves as a debug signal to determine the state in which the core is stuck when led_g_o[5] does not light up. |
| LED_15 | D21 | led_y_o[7] | Bit[0] of the JESD Rx core rx_state_o output signal. Serves as a debug signal to determine the state in which the core is stuck when led_g_o[5] does not light up. |
| LED_23 | D29 | led_r_o[7] | PRBS checker status. The PRBS checker has detected an error (for PRBS7 data sequence) in the incoming data stream. This LED is expected to light up initially when led_g_o[6] first lights up. Toggle the SW4 push button to clear the initial PRBS error and this LED should be off if there is no PRBS error detected afterwards. |

9. After running testing for the desired amount of time to verify the PRBS data sequence, press the SW5 push button to shut down the ADRV9009 evaluation board as well as to assert and hold the reset signals to the JESD IP core blocks. This marks the end of the hardware testing process.

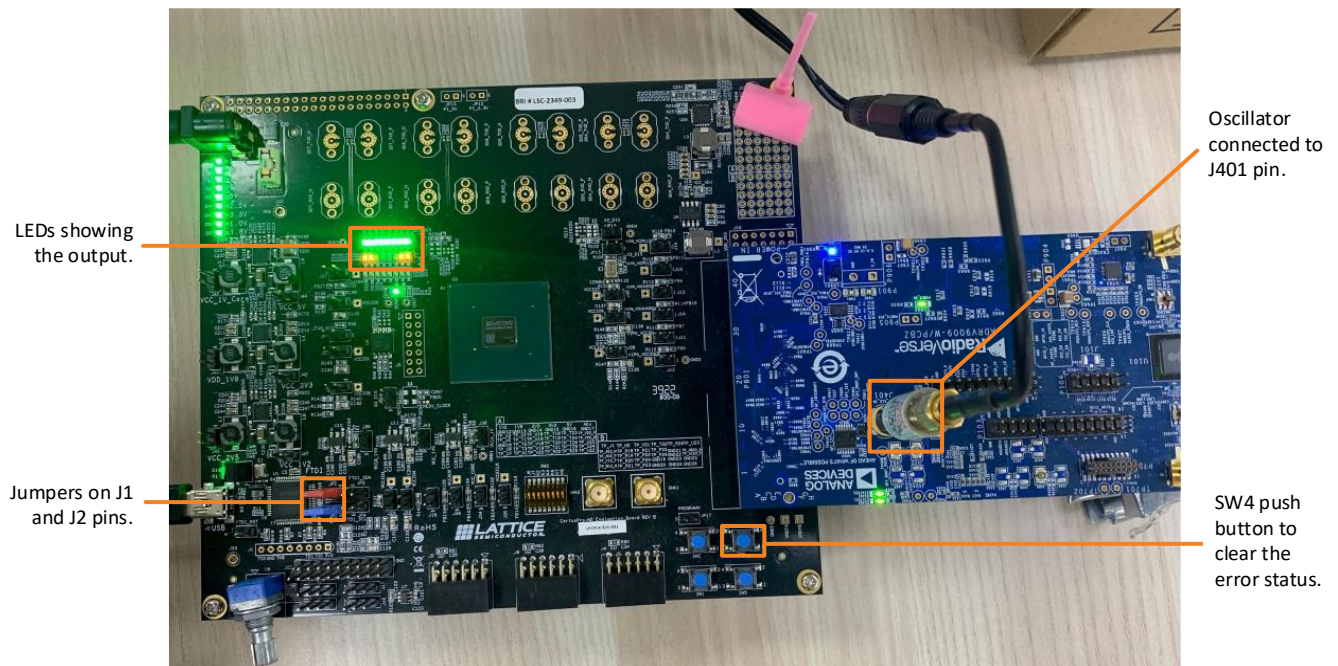


Figure 6.5. CertusPro-NX Evaluation Board (Left) with ADI ADRV9009 Dual RF Evaluation Board (Right)

6.1.4.2. Known Issues

The following are known issues:

- The PRBS checker on the ADI ADRV9009 Dual RF Evaluation Board constantly reports max error count. This is attributed to some issues with the ADI software. Hence, the Tx data transmitted from the FPGA is not being validated currently.
- Pressing the reset button (SW1 push button) does not rerun the main program. The current workaround is to reprogram the bitstream file if you wish to rerun the program.

6.1.4.3. Rebuilding the Design

RISC V Software

1. Copy the CPNX_EVAL_ADRV9009.zip file from the eval folder within the IP core directory, then paste and unzip the file in your working directory.
2. Go to [this ADI page](#) to read and accept the license agreement before proceeding to download the required software.
3. Download the ADRV9008/ADRV9009 Evaluation Software with GUI for Evaluation Board and ADRV9008/ADRV9009 API Source Code. The versions tested are as follows:
 - ADRV9008/ADRV9009 Evaluation Software with GUI for Evaluation Board Ver. 6.0 (3.6.2.1)
 - ADRV9008/ADRV9009 API Source Code Ver. 6.0 (6.2.1)

| | | |
|--------------------------|-------------------------------|---|
| ADRV9009 | ADRV9009/PCBZ | ADRV9008/ADRV9009 Evaluation Software with GUI for Evaluation Board (ZIP) |
| | | ADRV9008/ADRV9009 API Source Code (ZIP) |

Figure 6.6. ADI Software and Source Code to Download

4. Install the ADRV9008/ADRV9009 Evaluation Software and open the GUI.
5. Click **Connect** on the top left. The GUI shows the ADRV9008/ADRV9009 diagram. Ignore the *Cannot Connect to the Device* error message if it appears.
6. Click **File** and select the **Load GUI Setup** option.
7. From the extracted folder in Step 1, select the `cpnx_ed_profile.xml` file in the `advr9009_profile` folder which loads the target configuration for this example design. A pop-up dialog box appears once the setup loads successfully. The device shown should be ADRV9009.
8. Go to **Tools > Create Script > Init .c Files** to generate some of the necessary software code for the design in the same `advr9009_profile` folder. Setup the JESD204B interface as shown in [Figure 6.7](#).

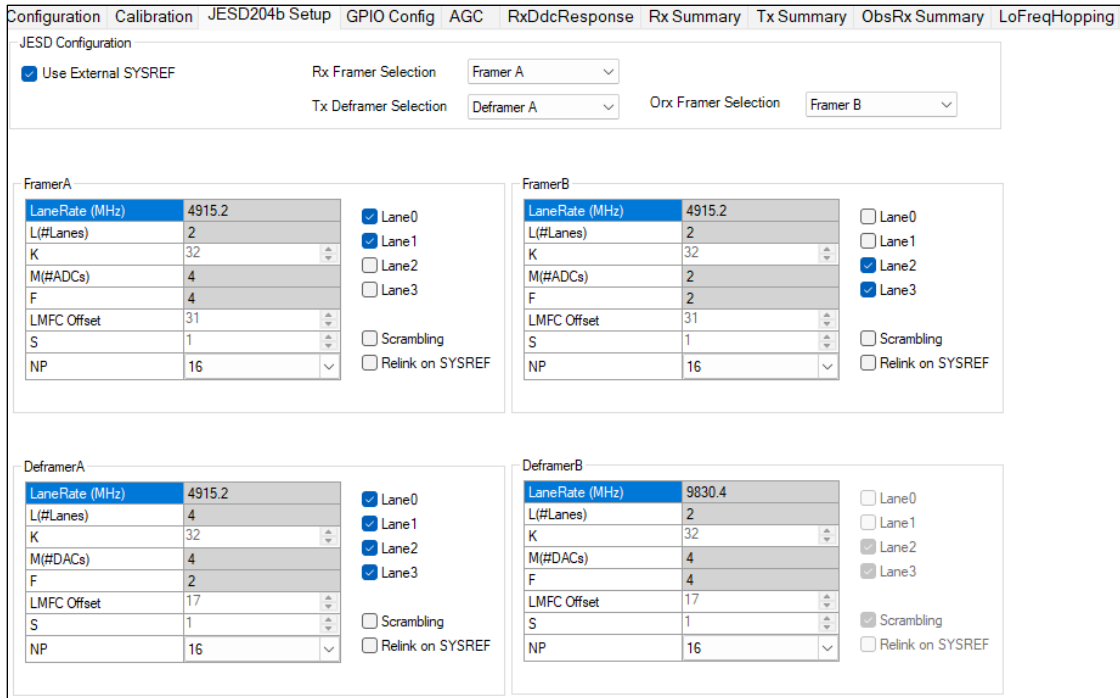


Figure 6.7. JESD204B Setup Information

9. Unzip the downloaded `advr9009-api-source-code.zip` file. Locate the software codes required for the design in the `API\src\devices` folder.

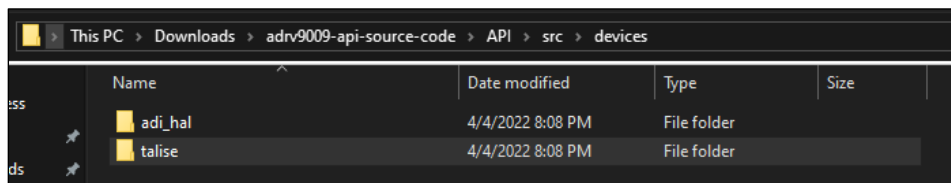


Figure 6.8. Locating the Software Codes

10. Copy the `advr9009-api-source-code` folder to the extracted `CPNX_EVAL_ADRV9009.zip` folder as well. This folder should be at the same level as the `advr9009_profile` folder.
11. Open a command prompt terminal and change the directory to the extracted folder.
12. Run the `gitclone_patch.bat` file in Windows or `gitclone_patch.sh` (bash shell script) file in Linux. This downloads the necessary software files from the [ADI GitHub page](#) and makes the necessary changes for this design.

Note: In Windows, ensure the git client software is first installed before running the `gitclone_patch.bat` file.
13. After this process is done, open the Lattice Propel software to import the project.

- Right-click on the Project Explorer tab area and select **Import**. The Import window appears. Expand the General folder and select *Existing Projects into Workspace*.

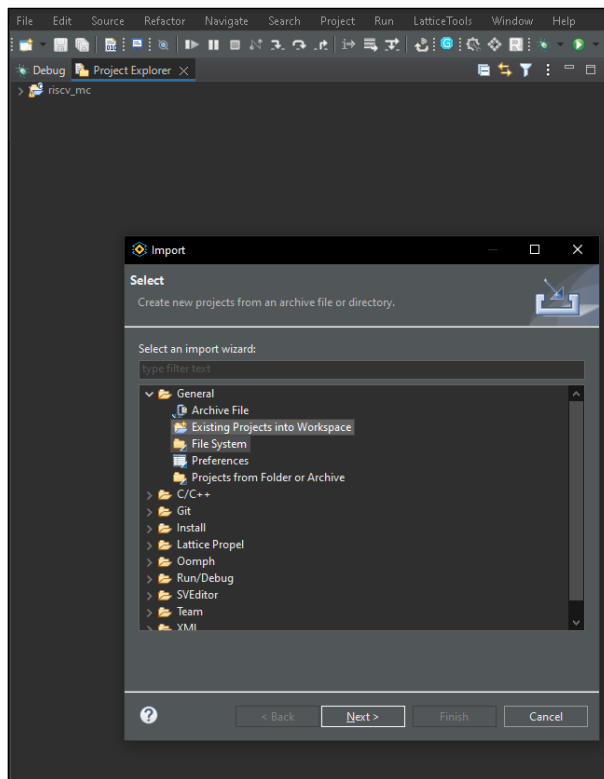


Figure 6.9. Project Explorer Import Window in Propel

- Browse to the propel_sw folder and select it as your root directory. Click **Finish** to complete importing the project.
- Right-click on the project folder and select **Build Project** to start building the software. This generates a .mem file in a new Debug folder which can be used for initializing the system memory in the design.

RTL Design

1. Ensure that you have run the `gitclone_patch.bat` or `gitclone_patch.sh` file from Step 12 in the [RISC V Software](#) section. Also, ensure that you have a `.mem` file generated and two RTL files named `ad_pngen.v` and `ad_pnmon.v` are present in the `CPNX_EVAL_ADRV9009` folder.
2. Open the Lattice Propel Builder program and select **Open Design** from the File tab.
3. Browse to the `CPNX_EVAL_ADRV9009/risc_sys` folder and select the `risc_sys.sbx` file to bring up the schematic design of the SoC design.
4. Locate the system memory module as shown in [Figure 6.10](#) and select **Reconfig**. If a newer version of the system memory module is available, click **Yes** to update the IP to proceed.

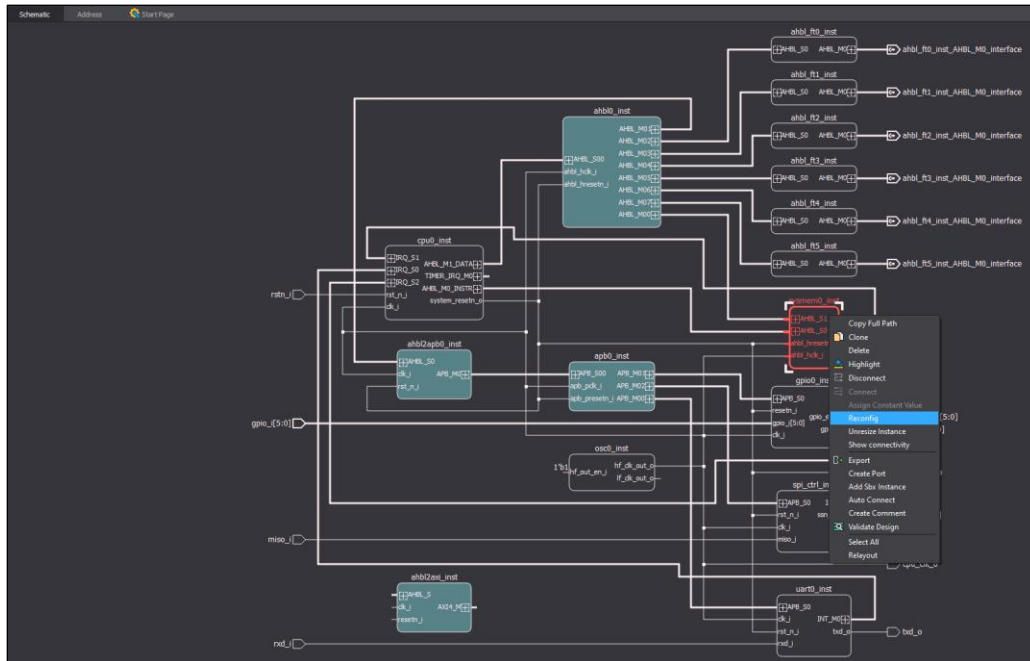


Figure 6.10. Locating System Memory Module and Selecting Reconfig

5. For *Initialization File* attribute, browse to the `.mem` file (located in the `propel_sw/Debug` folder) that you generated in the Propel project from Step 16 in the [RISC V Software](#) section. Click **Generate** at the bottom right corner of the IP GUI.

| Configure IP | | Port S0 Settings | Port S1 Settings |
|---|-------------------------------------|------------------|------------------|
| Property | Value | | |
| General | | | |
| Interface | AHBL | | |
| Memory Address Depth [1 - 114688] | 98304 | | |
| Data Bus Width(bits) | 32 | | |
| Memory Type | LRAM | | |
| Port Count | 2 | | |
| ECC Enable | <input type="checkbox"/> | | |
| Enable Arbiter | <input type="checkbox"/> | | |
| Data Streamer | | | |
| Enable Data Streamer | <input type="checkbox"/> | | |
| Data Streamer Interface | Generic FIFO | | |
| Data Streamer Clock Bypass | <input type="checkbox"/> | | |
| Data Streamer Write Start Address [0 - 98303] | 0 | | |
| Initialization | | | |
| Initialize Memory | <input checked="" type="checkbox"/> | | |
| Initialization File Format | hex | | |
| Initialization File | ../riscv_mc.mem | | |

Figure 6.11. Selecting the Initialization File

6. Next, in the TCL Console, type `source <project directory>/regen_ip_files.tcl` to regenerate RTL files for the other IP components. Make sure the following IP components are installed in your IP catalog before entering the command:
 - AHB-Lite to AXI4 Bridge v1.3.0
 - GPIO v1.8.0
 - SPI Controller v2.4.0
 - UART v1.4.0
 - AHB Lite Interconnect v1.4.0
 - AHB Lite to APB Bridge v1.1.2
 - APB Interconnect v1.3.0

This ensures the IP versions in `regen_ip_files.tcl` match the versions of the installed IP components.
7. Select **Design > Generate**. This regenerates the wrapper files and software files for the SoC design.

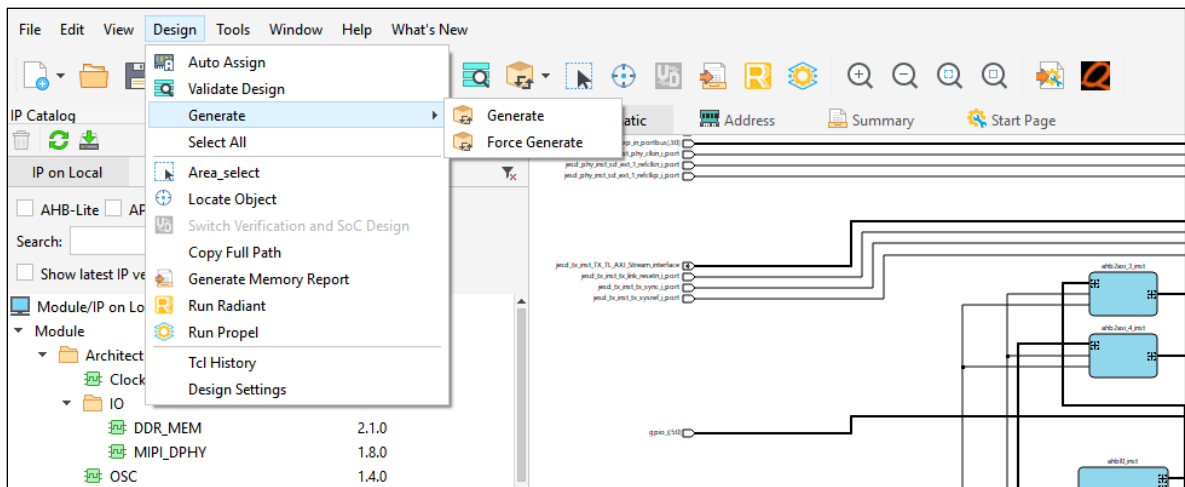


Figure 6.12. Regenerating the SoC Design RTL

8. Open the Radiant software and select **Open Project**.
9. Select the `risc_sys.rdf` file in the `CPNX_EVAL_ADRV9009` folder to open the RTL project.
10. Click the **Play** button at the top left of the GUI to start compiling the design.
11. After compilation has completed, a bitstream file is generated in the `impl_1` folder. Follow the steps from Step 8 onwards in the [Running the Hardware without Rebuilding the Design](#) section to program the board with the new bitstream file.

6.2. Avant-X Versa Board Rx Example Design

This section shows an example design to validate the JESD204B IP in the Avant-X device using the Avant-X Versa Board and Texas Instruments (TI) ADC32RF44EVM Evaluation Board (ADC32RF44EVM). The design is configured to run at a data rate of 9.8304 Gb/s with eight lanes.

6.2.1. Example Design Supported Configuration

Table 6.3. JESD204B IP Configuration Supported by the Avant-X Versa Board Rx Example Design

| JESD204B IP GUI Parameter | JESD204B IP configuration in example demo design |
|-------------------------------------|--|
| | JESD Rx + PHY |
| General | |
| JESD204 IP Core Generation Enable | Checked |
| Mode | Rx_only |
| Data Rate (Gb/s) | 9.8304 |
| Number of Lanes (L) | 8 |
| Converters per Device (M) | 1 |
| Samples per Converter per Frame (S) | 19 |
| Converter Resolution (N) | 11 |
| Number of Bits per Sample (Nt) | 11 |
| Control Bits (CS) | 0 |
| Control Words (CF) | 0 |
| High Density Format (HD) | 0 |
| Octets per Frame (F) | 7 |
| Frames per Multiframe (K) | 31 |
| Multi Frames in ILA | 3 |
| Subclass (SUBCLASSV) | 1 |
| SYSREF Always | SYSREF_ALWAYS |
| Scrambling (SCR) | DISABLED |
| ILA_DID | 85 |
| ILA_ADJCNT | 0 |
| ILA_BID | 0 |
| ILA_ADJDIR | 0 |
| ILA_PHADJ | 0 |
| ILA_JESDV | 1 |
| ILA_LID | 0 |
| PHY Settings | |
| JESD204 PHY Generation Enable | Checked |
| Lane ID | 0 |
| Ref Clk Freq (MHz) | 122.88 |
| Optional Features | |
| Transport Layer Enable | Checked |
| Frame per Clock | 2 |
| Test Mode Enable | Unchecked |

6.2.2. Overview of the Example Design and Features

Key features of the example design include:

- Interoperability with ADC32RF44EVM Evaluation Board configured to eight transmission lanes.
- Lane rate of 9.8304 Gb/s.

- IP core includes an embedded transport layer which allows IQ data to be directly connected to the IP core interface.
- Example design includes a ramp checker logic that validates incoming ramp signal from the ADC32RF44EVM Evaluation Board.

6.2.3. Example Design Components

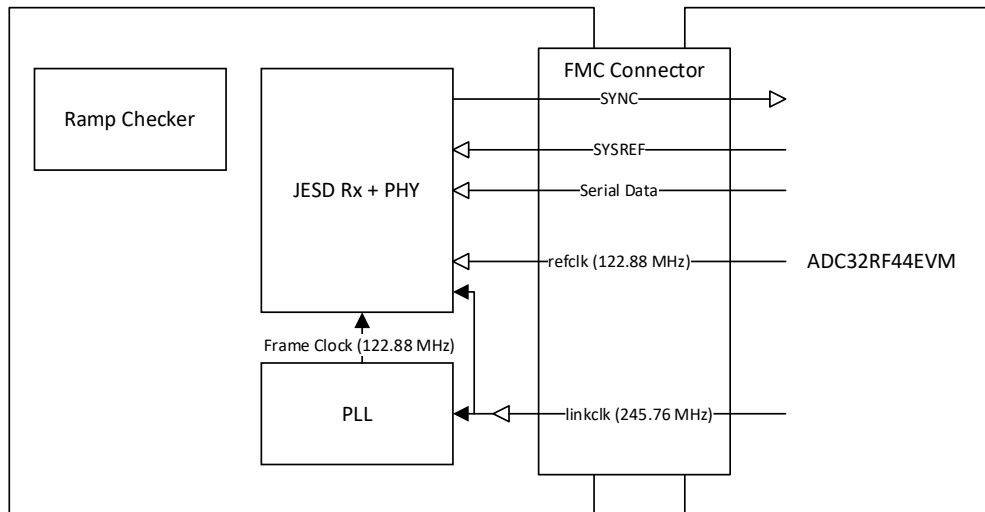


Figure 6.13. JESD204B Example Design Block Diagram (with Avant-X and TI Evaluation Boards)

The JESD204B Rx example design includes the following blocks:

- JESD204B Rx + PHY
- Ramp Checker
- PLL

6.2.3.1. JESD204B Rx + PHY

This block wraps around the serializer/de-serializer (SERDES) IP of the targeted device and connects to both the JESD204B PHY and Rx blocks. The PHY de-serializes the serial data from an external component and sends parallel data for further processing in the JESD204B Rx block. The JESD204B Rx then outputs the sample data to the ramp checkers to check for data correctness. It has an internal transport layer which remaps the data from the internal core to the converter's sample format.

6.2.3.2. Ramp Checker

The JESD configuration is set to $M=2$, $S=20$, and $N=12$. The ramp checker receives sample data as two distinct ramp signals from the JESD204B Rx. The first 20 samples of 12-bit output carries the ramp signal for channel B while the second 20 samples of 12-bit output carries the ramp signal for channel A. The ramp signals are expected to increment from the first data N to $12'hFFF$ before returning to 0. The checker asserts the passed flag once valid data is received from the JESD204B Rx output. If a mismatch is detected, the passed flag is held low until reset.

6.2.3.3. PLL

This block generates the frame clock by dividing the link clock by 2.

6.2.4. Hardware Testing

6.2.4.1. Pre-requisites

- TI ADC32RF44EVM
- TI ADC32RFxxEVM SPI GUI (v4.1)
- Avant-X Versa Board

6.2.4.2. Generating Bitstream

1. Copy the lav_versa_adc32rf44_8l_9p8g.zip file from the eval folder within the IP core directory, then paste and unzip the file in your working directory.
2. Open the Radiant software and select **Open project**.
3. Select the lav_versa_adc32rf44_8l_9p8g.rdf file from the unzipped directory to open the RTL project.
4. Right-click on any .ipx file and select **Regenerate ALL IPs** to regenerate all IP instances in the design.

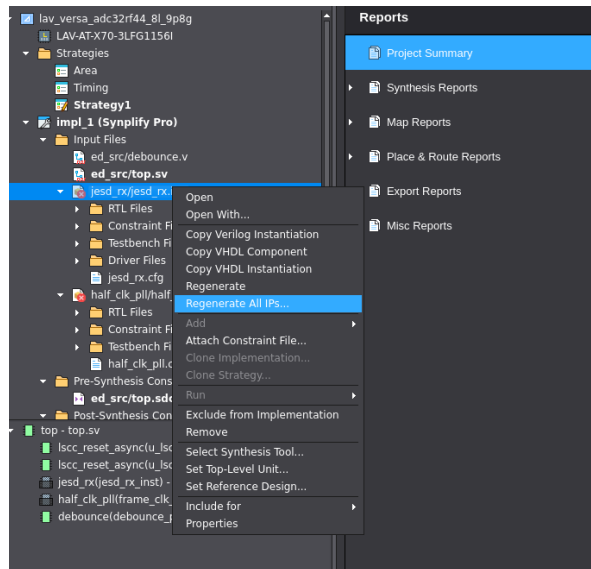


Figure 6.14. Regenerating All IP Instances

5. Click on the **Play** button at the top left of the GUI to start compiling the design. A bitstream file is generated in the impl_1 folder after the compilation process completes.

6.2.4.3. TI ADC32RF44EVM Setup

Because the ADC32RF44EVM provides all the clocks required by the Avant-X Versa Board, you must set up the ADC32RF44EVM first before the Avant-X Versa Board.

1. Connect the ADC32RF44EVM to the Avant-X Versa Board.
2. Connect the required power supply to the ADC32RF44EVM.
3. Connect a mini-USB cable between the ADC32RF44EVM and the PC with the ADC32RFxxEVM SPI GUI installed. The GUI installer can be found in the [TI ADC32RF45EVM Evaluation Board](#) web page.
4. Configure the ADC32RFxxEVM SPI GUI as follows:
 - a. In Quick Setup:
 - i. Select LMX2582 as the clock source to ADC.
 - ii. Set ADC32RFxx mode to bypass.
 - iii. Set resolution to 12-bit. This in turn sets Lanes=8, M=2, F=8, and S=20.
 - iv. Internal Clk Freq defaults to 2457.6 Msps.
 - v. Click **PROGRAM EVM**.
 - b. In LMK04828:
 - i. Set **CLKout 0 and 1 FPGA Clock & SYSREF DCLK Divider** to 20 to achieve 122.88 MHz for refclk.
 - ii. Set **CLKout 12 and 13 Extra FMC Clocks DCLK Divider** to 10 to achieve 245.76 MHz for linkclk. Then, set **DCLK Type** to LVDS and uncheck the **Group Powerdown** checkbox.
 - c. In Low Level View, go to ADC32RFxx_DIGITAL block in the **Register Name** tab:

- i. Configure the lane mapping registers JESD_DIG_CHA_0x16 and JESD_DIG_CHB_0x16 to 0xF2 by inserting the value and clicking **Write Register** at the bottom right of the window.
- ii. Similarly, configure the output to ramp pattern by setting registers JESD_DIG_CHA_0x03 and JESD_DIG_CHB_0x03 to 0x01.

The ADC is now ready to transmit.

6.2.4.4. Avant-X Versa Board Setup

1. Make sure that the JP1 jumper on the Avant evaluation board is connected with a jumper pin to allow configuring from the JTAG port.
2. Connect a USB cable from your PC to the mini-USB connector on the Avant evaluation board.
3. Open the Radiant Programmer tool.
4. Locate the generated bitstream file in the impl_1 folder, then program the FPGA device with the file.
5. Press the SW13 push button to start the ramp checker after both the qsfm_link_led and zsfm1_link_led LEDs light up. Three LEDs on the Avant-X Versa Board (see Figure 6.15) are mapped to the following design statuses. A working design is indicated by all 3 LEDs lighting up.

Table 6.4. Summary of LED Indicators on Avant-X Versa Board (Rx Example Design)

| LED | Pin | Description |
|----------------|------|--|
| qsfm_link_led | AN10 | jesd_rxphy_ready. Indicates that PHY is up and receiving data from ADC when the LED lights up. |
| zsfm1_link_led | AJ13 | rx_state_o == 2'b11. Indicates that JESD Rx is up and receiving data when the LED lights up. |
| zsfm2_link_led | AH13 | Passed flag from ramp checker. Flag is asserted when the LED lights up. |

This marks the end of the hardware testing process.

Note that the SW12 push button is connected as the master reset of the ramp checker, JESD Rx, and PHY. You can reset as needed.



Figure 6.15. Avant Versa Board (Bottom) with TI ADC32RF44EVM Evaluation Board (Top)

6.3. Avant-X Versa Board Tx Example Design

This section shows an example design to validate the JESD204B IP in the Avant-X device using the Avant-X Versa Board and TI DAC39RF10EVM Evaluation Board (DAC39RF10EVM). The design is configured to run at a data rate of 9.8304 Gb/s with eight lanes.

6.3.1. Example Design Supported Configuration

Table 6.5. JESD204B IP Configuration Supported by the Avant-X Versa Board Tx Example Design

| JESD204B IP GUI Parameter | JESD204B IP configuration in example demo design |
|-------------------------------------|--|
| | JESD Tx + PHY |
| General | |
| JESD204 IP Core Generation Enable | Checked |
| Mode | Tx_only |
| Data Rate (Gb/s) | 9.8304 |
| Number of Lanes (L) | 8 |
| Converters per Device (M) | 1 |
| Samples per Converter per Frame (S) | 3 |
| Converter Resolution (N) | 15 |
| Number of Bits per Sample (Nt) | 15 |
| Control Bits (CS) | 0 |
| Control Words (CF) | 0 |
| High Density Format (HD) | 0 |
| Octets per Frame (F) | 1 |
| Frames per Multiframe (K) | 31 |
| Multi Frames in ILA | 3 |
| Subclass (SUBCLASSV) | 1 |
| SYSREF Always | SYSREF_ALWAYS |
| Scrambling (SCR) | DISABLED |
| ILA_DID | 85 |
| ILA_ADJCNT | 0 |
| ILA_BID | 0 |
| ILA_ADJDIR | 0 |
| ILA_PHADJ | 0 |
| ILA_JESDV | 1 |
| ILA_LID | 0 |
| PHY Settings | |
| JESD204 PHY Generation Enable | Checked |
| Lane ID | 0 |
| Ref Clk Freq (MHz) | 122.88 |
| Optional Features | |
| Transport Layer Enable | Checked |
| Frame per Clock | 2 |
| Test Mode Enable | Unchecked |

6.3.2. Overview of the Example Design and Features

Key features of the example design include:

- Interoperability with TI DAC39RF10EVM Evaluation Board configured to eight receiving lanes.
- Lane rate of 9.8304 Gb/s.

- IP core includes an embedded transport layer which allows IQ data to be directly connected to the IP core interface.
- A constant square wave pattern is sent to the DAC for viewing in an external oscilloscope.

6.3.3. Example Design Components

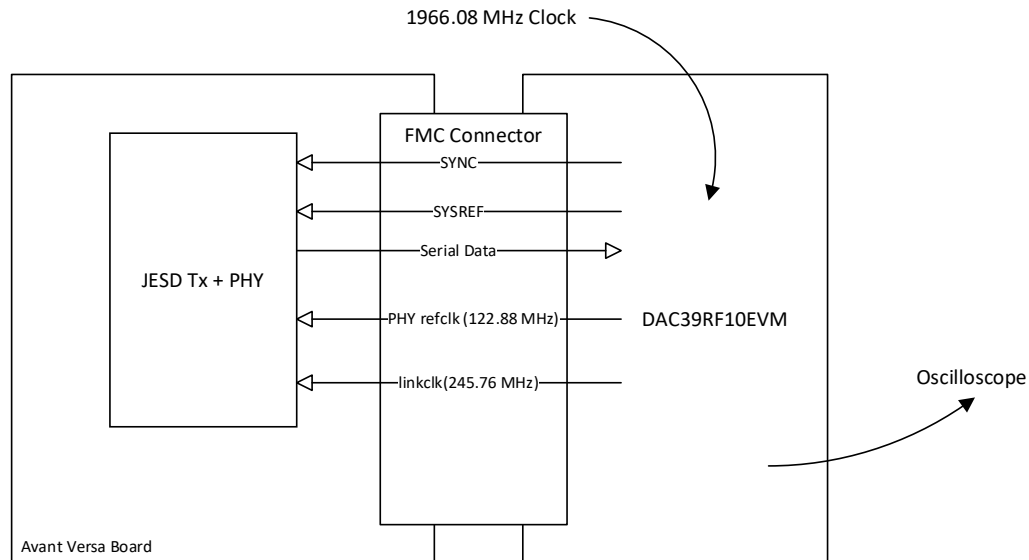


Figure 6.16. JESD204B Example Design Block Diagram (with Avant-X and TI Evaluation Boards)

The JESD204B Tx example design includes the following block:

- JESD204B Tx + PHY

6.3.3.1. JESD204B Tx + PHY

The JESD204B IP receives the IQ data and packetizes the data into JESD204B-compliant packets before transmitting the data to the JESD204B PHY block. It contains an internal transport layer which can remap a square wave pattern to the internal core. The PHY block then serializes the parallel data from the JESD204B Tx and transmits the serial data to an external component.

6.3.4. Hardware Testing

6.3.4.1. Pre-requisites

- TI DAC39RF10EVM
- TI DAC39RF10EVM-GUI (v3.1.2)
- Avant-X Versa Board
- A clock generator that can generate a 1966.08-MHz clock
- An oscilloscope to observe the output waveform

6.3.4.2. Generating Bitstream

1. Copy the `lav_versa_dac39rf10_8l_9p8g.zip` file from the eval folder within the IP core directory, then paste and unzip the file in your working directory.
2. Open Radiant software and select **Open project**.
3. Select the `lav_versa_dac39rf10.rdf` file from the unzipped directory to open the RTL project.
4. Right-click on any `.ipx` file and select **Regenerate All IPs** to regenerate all IP instances in the design.
5. Click on the **Play** button at the top left of the GUI to start compiling the design. A bitstream file is generated in the `impl_1` folder after the compilation process completes.

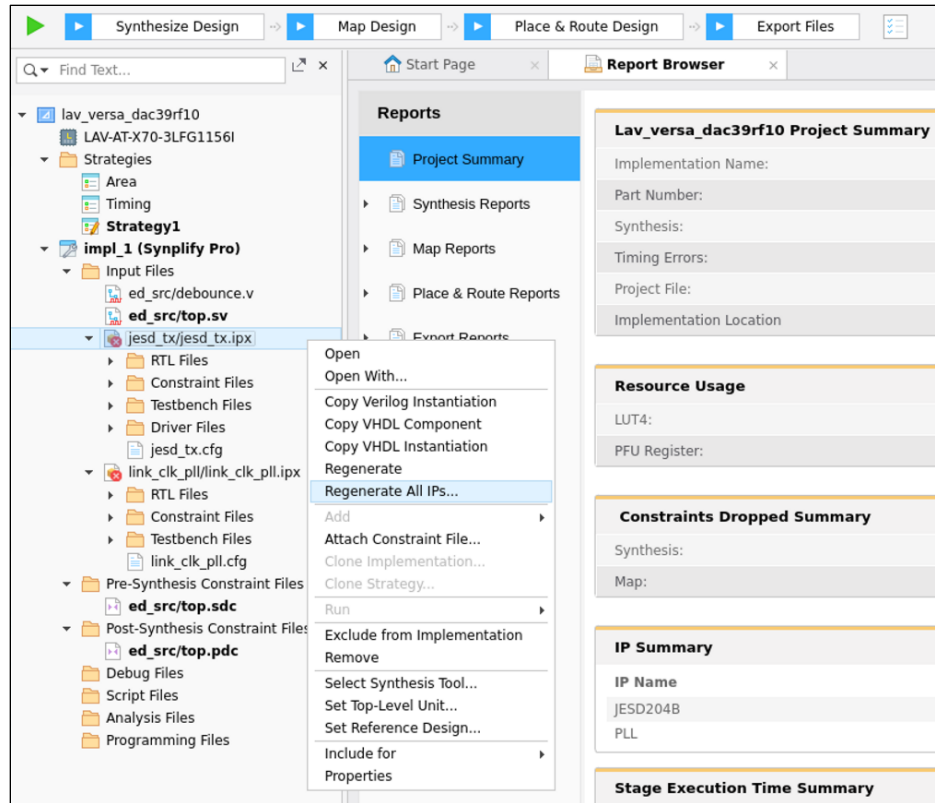


Figure 6.17. Regenerating All IP Instances

6.3.4.3. Hardware Setup

1. Connect the TI DAC39RF10EVM to the Avant-X Versa Board.
2. Make sure that the JP1 jumper on the Avant-X Versa Board is connected with a jumper pin to allow configuring from the JTAG port.
3. Connect a USB cable from your PC to the mini-USB connector on the Avant-X Versa Board.
4. Connect the required 12-V power supply to the DAC39RF10EVM.
5. Connect a mini-USB cable between the DAC39RF10EVM and your PC with the DAC39RF10EVM GUI installed.
6. Connect a 1966.08-MHz clock to the DAC39RF10EVM through the LMX CLKP/N SMA connector port.
7. Connect the OUTAp SMA connector to an external oscilloscope to view the generated waveform.

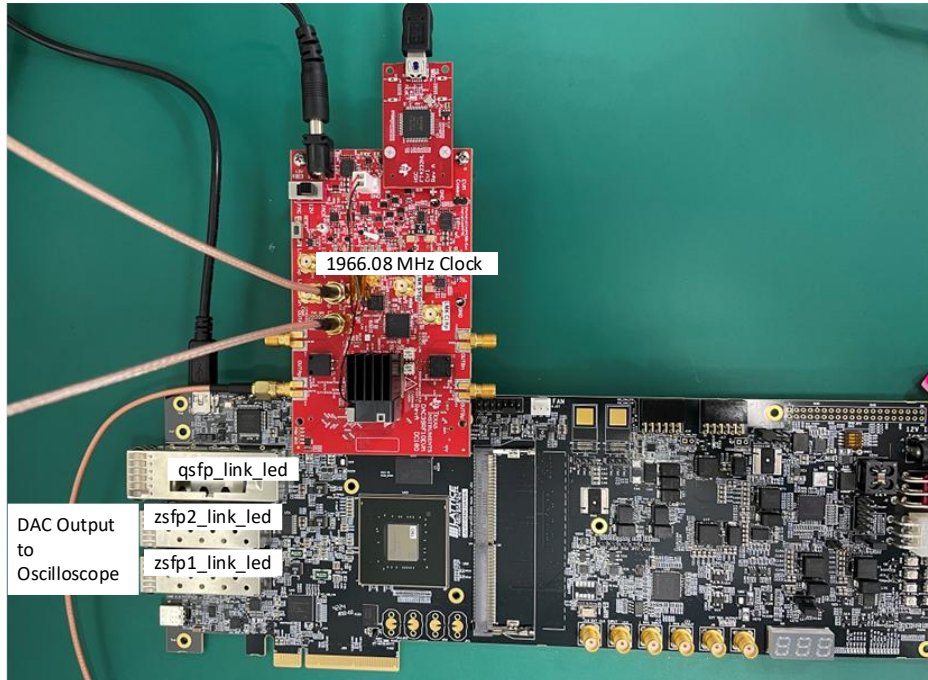


Figure 6.18. Avant Versa Board (Top) with TI DAC39RF10EVM Evaluation Board (Bottom)

6.3.4.4. Running the Design

1. Open the DAC39RF10EVM GUI software. Ensure that the installed version is v3.1.2.
2. In the **Select FTDI Device** window, select the FTDI and board type, then click **Select FTDI and Board Type**.

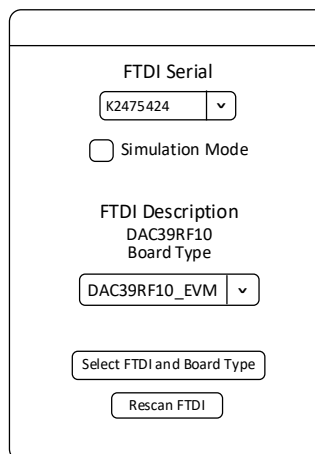


Figure 6.19. DAC39RF10EVM GUI (Select FTDI Device Window)

3. On the **JESD Configuration** tab of the **DAC39RF1xEVM** window, configure the settings to the following values:
 - Update Rate: 1.96608G
 - Real Data: Enabled
 - Channel Count: 2
 - Interpolation: 1
 - DAC Resolution: 16 bit
 - JESD Protocol: 8b10b

- JESD Subclass: 1
- JESD Format: Two's Comp
- JMODE: 2

JESD Configuration Analog Output NCO Configuration Low Level

Update Rate : 1.96608G Real Data

Channel Count : 2 DAC Resolution : 16 bit

Interpolation : 1 JESD Protocol : 8b10b

Data Rate = 1966.08 MSPS JESD Subclass : 1

Input BW = 983.04 MHz JESD Format : Two's Comp

| Select | JMODE | Ln/Strm | Ln Count | L-M-F-S | LR (Gbps) |
|-------------------------------------|-------|---------|----------|----------|-----------|
| <input type="checkbox"/> | 1 | 8 | 16 | 16-2-2-8 | 4.9152 |
| <input checked="" type="checkbox"/> | 2 | 4 | 8 | 8-2-2-4 | 9.8304 |
| <input type="checkbox"/> | | | | | |
| <input type="checkbox"/> | | | | | |
| <input type="checkbox"/> | | | | | |
| <input type="checkbox"/> | | | | | |

Current DAC JESD Config

JMODE: 2 Channel Count: 2
Subclass: 1 Interpolation: 1

SYSREF Proc: SYS Window

RBD: 0

Protocol: 8b10b

Format: Two's Comp

SERDES PLL Lock :

JESD Link :

8b/10b SYNC :

Elastic Buff :

SYREF Align :

SYSREF Re-Align :

SYSREF/Reference Clock

Enable SYSREF

SYSREF K : 32

SYSREF Frequency : 15.36 MHz

Core Clock : 122.88 MHz

SERDES Clock : 122.88 MHz

Figure 6.20. DAC39RF10EVM GUI (DAC39RF1xEVM Window)

4. Click **Config JESD Crossbar**. The **JESD Crossbar Configuration** window opens.

Load Standard Board

FMC Standard

Active Lane Count: 8

| Logical Lane | Physical Lane | PHY Inversion |
|--------------|---------------|-------------------------------------|
| 0 | 9 | <input checked="" type="checkbox"/> |
| 1 | 11 | <input checked="" type="checkbox"/> |
| 2 | 15 | <input checked="" type="checkbox"/> |
| 3 | 5 | <input checked="" type="checkbox"/> |
| 4 | 3 | <input checked="" type="checkbox"/> |
| 5 | 0 | <input checked="" type="checkbox"/> |
| 6 | 1 | <input checked="" type="checkbox"/> |
| 7 | 2 | <input checked="" type="checkbox"/> |
| 8 | 7 | <input checked="" type="checkbox"/> |
| 9 | 13 | <input checked="" type="checkbox"/> |
| 10 | 12 | <input checked="" type="checkbox"/> |
| 11 | 14 | <input checked="" type="checkbox"/> |
| 12 | 6 | <input checked="" type="checkbox"/> |
| 13 | 4 | <input checked="" type="checkbox"/> |
| 14 | 10 | <input checked="" type="checkbox"/> |
| 15 | 8 | <input checked="" type="checkbox"/> |

Figure 6.21. JESD Crossbar Configuration Window

5. Check to enable **Load Standard Board**, then select **FMC Standard** from the drop-down list.
6. Click **Setup JESD Crossbar**.
7. Close the **JESD Crossbar Configuration** window after configuration is done.
8. On the **JESD Configuration** tab, click **Setup Clocks** followed by **Brink Up Link**. The *Current DAC JESD Config* information displayed at the bottom left of the GUI must match the expected values for JMODE, Subclass, Channel Count, Interpolation, Protocol, and Format. **Enable SYSREF** under *SYSREF/Reference Clock* must also be checked. If the values are different from the expected values, repeat Steps 3 to 8.
9. Click **Refresh** under *Current DAC JESD Config*. The *SERDES PLL Lock* status turns green.
10. Open the Radiant Programmer tool.
11. Locate the bitstream generated in the impl_1 folder and program the bitstream to the FPGA. Upon successful programming, three green LEDs on the Avant-X Versa Board light up.

Table 6.6. Summary of LED Indicators on Avant-X Versa Board (Tx Example Design)

| LED | Pin | Description |
|----------------|------|--|
| qsfp_link_led | AN10 | Tx PHY has gone through calibration and is ready when the LED lights up. |
| zsfp1_link_led | AJ13 | Tx JESD core is in the user data phase when the LED lights up. |
| zsfp2_link_led | AH13 | TREADY signal from JESD Tx core transport layer. The core is ready to accept user data when the LED lights up. |

12. In the DAC39RF10EVM GUI software, click **Refresh** under *Current DAC JESD Config* on the **JESD Configuration** tab. When the link is up, you can see the waveform on your oscilloscope.

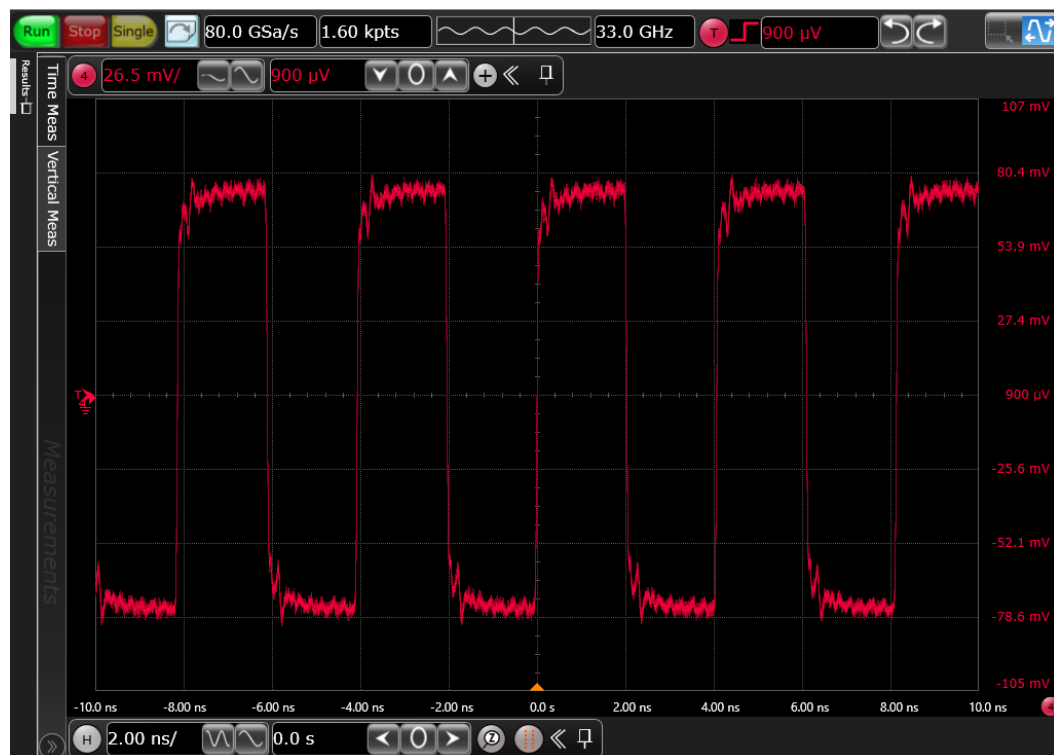


Figure 6.22. Output Waveform on Oscilloscope

7. Designing with the IP

This section provides information on how to generate the IP Core using the Lattice Radiant software and how to run simulation and synthesis. For more details on the Lattice Radiant software, refer to the Lattice Radiant Software User Guide.

Note: The screenshots provided are for reference only. Details may vary depending on the version of the IP or software being used. If there have been no significant changes to the GUI, a screenshot may reflect an earlier version of the IP.

7.1. Generating and instantiating the IP

You can use the Lattice Radiant software to generate IP modules and integrate them into the device architecture. The steps below describe how to generate the JESD204B IP in the Lattice Radiant software.

To generate the JESD204B IP:

1. Create a new Lattice Radiant software project or open an existing project.
2. In the **IP Catalog** tab, double-click **JESD204B** under **IP, Connectivity** category. The **Module/IP Block Wizard** opens as shown in [Figure 7.1](#). Enter values in the **Component name** and the **Create in** fields and click **Next**.



Figure 7.1. Module/IP Block Wizard

3. In the next **Module/IP Block Wizard** window, customize the selected JESD204B IP using drop-down lists and check boxes. [Figure 7.2](#) shows an example configuration of the JESD204B IP. For details on the configuration options, refer to the [IP Parameter Description](#) section.

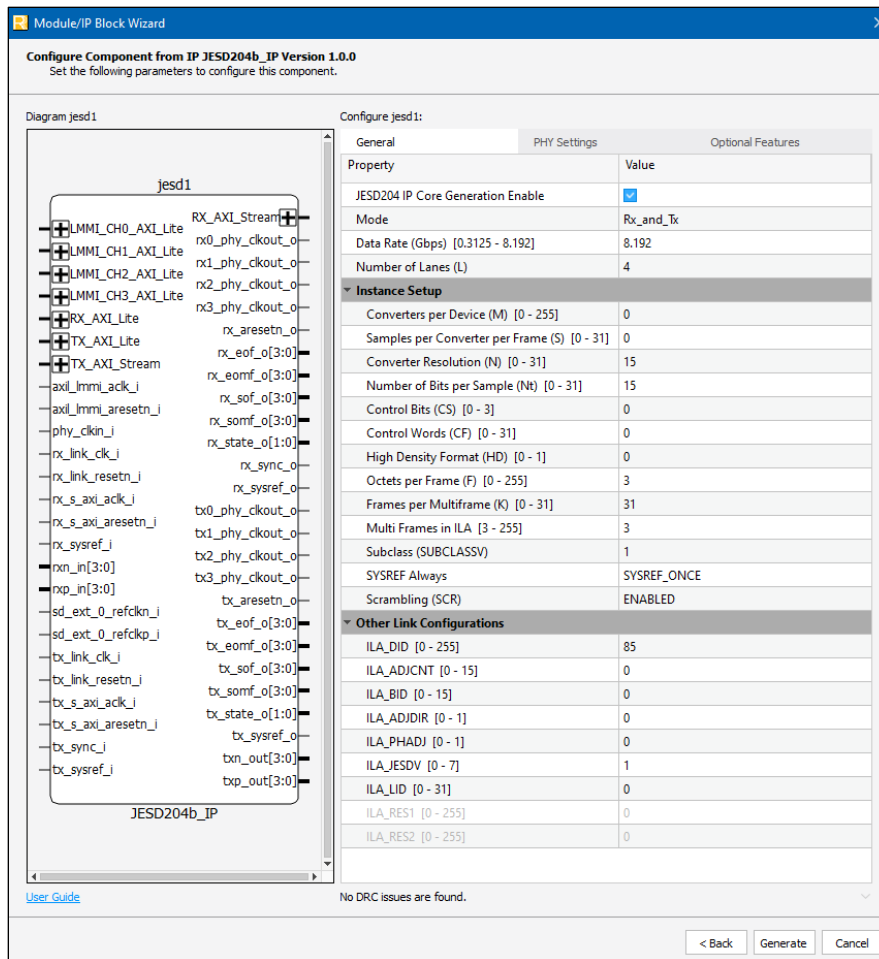


Figure 7.2. IP Configuration

4. Click **Generate**. The **Check Generated Result** dialog box opens, showing design block messages and results as shown in Figure 7.3.

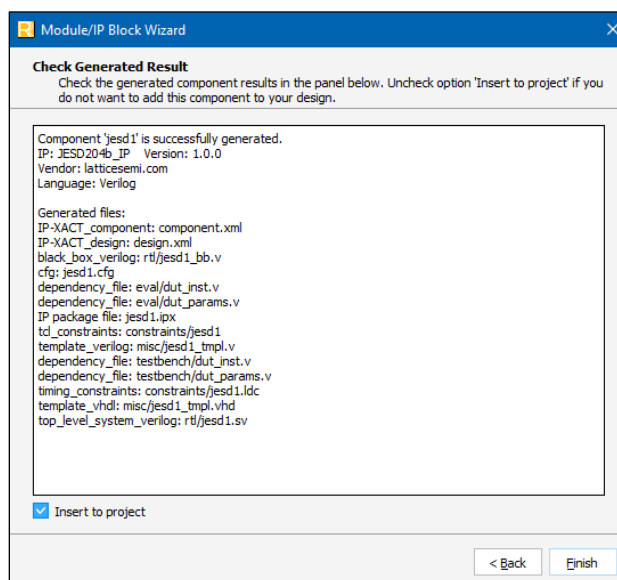


Figure 7.3. Check Generated Result

- Click **Finish**. All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields shown in [Figure 7.1](#).

7.1.1. Generated Files and File Structure

The generated JESD204B module package includes the closed-box (<Component name>_bb.v) and instance templates (<Component name>_tmpl.v/vhd) that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file (<Component name>.sv) that can be used as an instantiation template for the module is also provided. You may also use this example as the starting template for your top-level design. The generated files are listed in [Table 7.1](#).

Table 7.1. Generated File List

| Attribute | Description |
|---|--|
| <Component name>.ipx | Contains the information on the files associated to the generated IP. |
| <Component name>.cfg | Contains the parameter values used in IP configuration. |
| component.xml | Contains the ipxact: component information of the IP. |
| design.xml | Documents the configuration parameters of the IP in IP-XACT 2014 format. |
| rtl/<Component name>.sv | Provides an example RTL top file that instantiates the module. |
| rtl/<Component name>_bb.v | Provides the synthesis closed-box. |
| misc/<Component name>_tmpl.v misc /<Component name>_tmpl.vhd | Provide instance templates for the module. |

7.2. Design Implementation

Completing your design includes additional steps to specify analog properties, pin assignments, and timing and physical constraints. You can add and edit the constraints using the Device Constraint Editor or by manually creating a .pdc file.

Post-Synthesis constraint files (.pdc) contain both timing and non-timing constraint.pdc source files for storing logical timing/physical constraints. Constraints that are added using the Device Constraint Editor are saved to the active .pdc file. The active post-synthesis design constraint file is then used as input for post-synthesis processes.

Refer to the relevant sections in the Lattice Radiant Software User Guide for more information on how to create or edit constraints and how to use the Device Constraint Editor.

7.3. Specifying the Strategy


The Radiant software provides two predefined strategies: Area and Timing. It also enables you to create customized strategies. For details on how to create a new strategy, refer to the Strategies section of the Lattice Radiant Software user guide.

For CertusPro-NX devices, if you face timing issues at a high data rate, configure Radiant Strategies: *Place & Route Design: Path-based Placement* to *OFF* and *Pack Logic Block Utility* to a smaller number to improve the place and route performance for this IP.

7.4. Running Functional Simulation

You can run functional simulation after the IP is generated.

To run functional simulation:

- Click the  button located on the **Toolbar** to initiate the **Simulation Wizard** shown in [Figure 7.4](#).

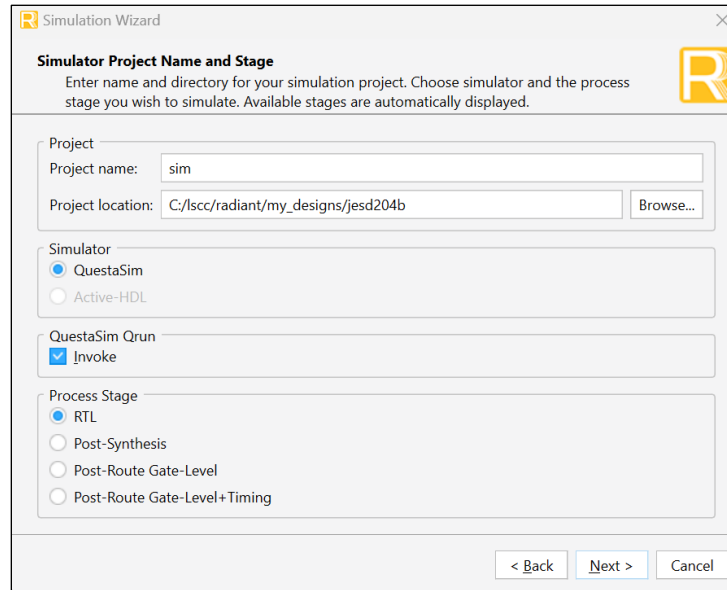


Figure 7.4. Simulation Wizard

2. Click **Next** to open the **Add and Reorder Source** window as shown in Figure 7.5.

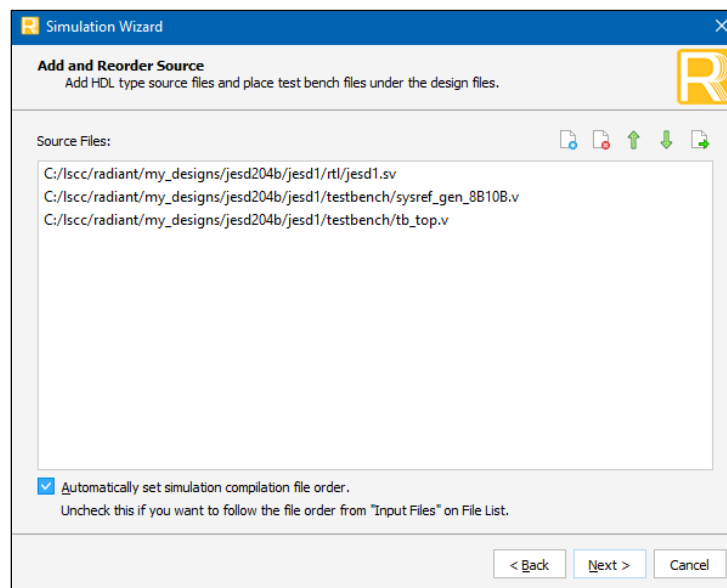


Figure 7.5. Add and Reorder Source

3. Click **Next**. The **Summary** window appears. Change the **Default Run** value to *0* and **Simulator Resolution** to *fs*.
4. Click **Finish** to run the simulation.

The waveform in Figure 7.6 shows an example simulation result.

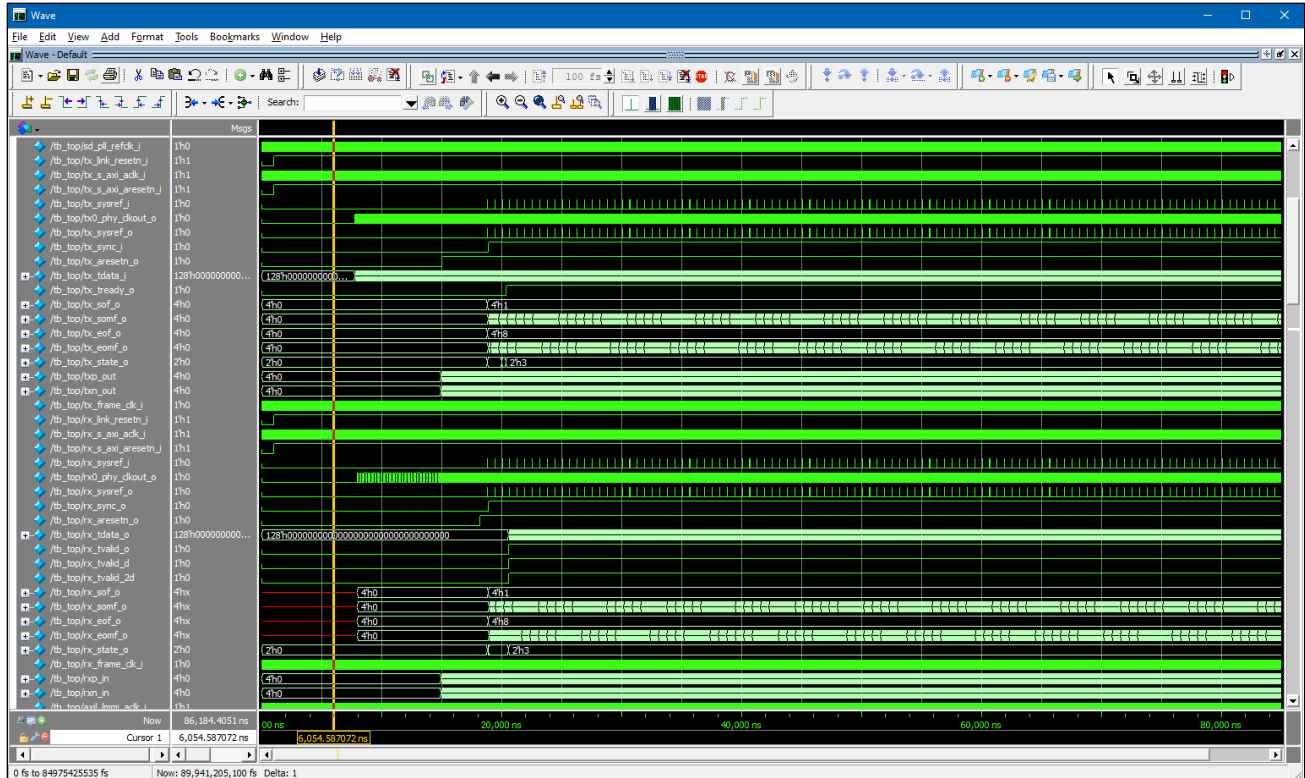


Figure 7.6. Simulation Waveform

7.4.1. Simulation Results

At the end of the test run, the simulation results show whether the simulation passed or failed. Figure 7.7 shows an example simulation result.

```
# =====Incremental Data=====
# 250000 JESD Link-up is done
# Data Passed
#
# *****SIMULATION PASSED*****
#
# ** Note: $finish : C:/lsc/radiant/my_designs/jesd204b/jesd1/testbench/tb_top.v(859)
# Time: 250 us Iteration: 0 Region: /tb_top/genblk2
```

Figure 7.7. Test Transcript Result

The simulation waveform /tb_top/error signals show if any data mismatch was detected. Figure 7.8 shows an example passing simulation waveform.

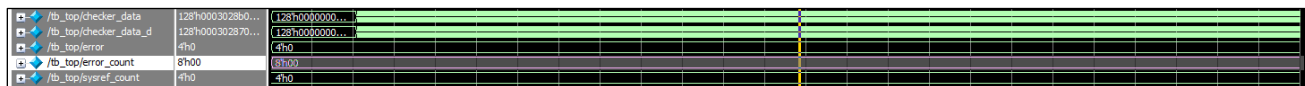


Figure 7.8. Example Passing Simulation Waveform

8. Design Considerations

8.1. Known Issues

8.1.1. Invalid IP Configuration Allowed when HD = 0

The Module/IP Block wizard allows invalid JESD204B IP parameter configurations when *High Density Format (HD)* is disabled. This issue will be fixed in a future Radiant software release.

When *High Density Format (HD)* is disabled, the number of samples across all lanes must be greater than or equal to the required number of converter samples, expressed as follows:

$$L \times \lfloor (F \times 8) / N_t \rfloor \geq M \times S$$

Otherwise, the IP configuration is invalid.

For example, consider an IP configuration with the parameter values HD = 0, L = 2, M = 7, F = 32, S = 3, and N_t = 24:

- $L \times \lfloor (F \times 8) / N_t \rfloor = 2 \times \lfloor (32 \times 8) / 24 \rfloor = 20$
- $M \times S = 7 \times 3 = 21$

Based on the calculations above, this IP parameter configuration is invalid and should not be allowed by the Module/IP Block wizard.

Appendix A. Resource Utilization

Table A.1 and Table A.2 show sample resource utilization of the JESD204B IP core on the LAV-AT-X70 and LFCPNX-100 devices, respectively.

Table A.1. Resource Utilization on LAV-AT-X70 LFG1156 Device

| IP Configuration | JESD204B IP | LUT4 | | PFU Registers | EBR |
|---|-----------------------|-------|--------------|---------------|-----|
| | | Logic | Ripple Logic | | |
| <i>Mode = Rx_and_Tx</i> <i>Number of Lanes = 8</i> <i>Scrambling = Enabled</i> <i>Number of Octets per Frame (F) = 4</i> <i>Number of Frames per Multiframe (K) = 32</i> <i>Transport Layer Enable = Unchecked</i> | Rx Link Wrapper | 4639 | 576 | 5559 | 8 |
| | Tx Link Wrapper | 3062 | 296 | 3759 | 0 |
| | Tx and Rx PHY Wrapper | 282 | 32 | 616 | 0 |
| <i>Mode = Rx_and_Tx</i> <i>Number of Lanes = 8</i> <i>Scrambling = Enabled</i> <i>Number of Octets per Frame (F) = 4</i> <i>Number of Frames per Multiframe (K) = 32</i> <i>Transport Layer Enable = Checked</i> | Rx Link Wrapper | 4707 | 588 | 6104 | 12 |
| | Tx Link Wrapper | 3064 | 308 | 4330 | 4 |
| | Tx and Rx PHY Wrapper | 279 | 32 | 616 | 0 |

Table A.2. Resource Utilization on LFCPNX-100 LFG672 Device

| IP Configuration | JESD204B IP | LUT4 | | PFU Registers | EBR |
|---|-----------------------|-------|--------------|---------------|-----|
| | | Logic | Ripple Logic | | |
| <i>Mode = Rx_and_Tx</i> <i>Number of Lanes = 4</i> <i>Scrambling = Enabled</i> <i>Number of Octets per Frame (F) = 4</i> <i>Number of Frames per Multiframe (K) = 32</i> <i>Transport Layer Enable = Unchecked</i> | Rx Link Wrapper | 2577 | 474 | 3862 | 4 |
| | Tx Link Wrapper | 1828 | 326 | 2683 | 0 |
| | Tx and Rx PHY Wrapper | 375 | 40 | 463 | 0 |
| <i>Mode = Rx_and_Tx</i> <i>Number of Lanes = 4</i> <i>Scrambling = Enabled</i> <i>Number of Octets per Frame (F) = 4</i> <i>Number of Frames per Multiframe (K) = 32</i> <i>Transport Layer Enable = Checked</i> | Rx Link Wrapper | 2900 | 488 | 4547 | 8 |
| | Tx Link Wrapper | 1876 | 340 | 2999 | 4 |
| | Tx and Rx PHY Wrapper | 375 | 40 | 463 | 0 |

References

- [JESD204B IP Release Notes \(FPGA-RN-02006\)](#)
- [JESD204B Driver API Reference \(FPGA-TN-02412\)](#)
- [MPCS Module – Lattice Radiant Software User Guide \(FPGA-IPUG-02118\)](#)
- [CertusPro-NX SerDes/PCS User Guide \(FPGA-TN-02245\)](#)
- [Lattice Avant SERDES/PCS User Guide \(FPGA-TN-02313\)](#)
- [Lattice Nexus 2 SERDES/PCS User Guide \(FPGA-TN-02395\)](#)
- [Lattice Radiant Timing Constraints Methodology \(FPGA-AN-02059\)](#)
- [CertusPro-NX web page](#)
- [Avant-G web page](#)
- [Avant-X web page](#)
- [Certus-N2 web page](#)
- [CertusPro-NX Evaluation Board web page](#)
- [Avant-X Versa Board web page](#)
- [ADI ADRV9009 Dual RF Evaluation Board web page](#)
- [TI ADC32RF45EVM Evaluation Board web page](#)
- [TI DAC39RF10EVM Evaluation Board web page](#)
- [TI DAC39RF10 web page](#)
- [TI DAC39RF10EVM-GUI web page](#)
- [JESD204B IP Core web page](#)
- [Lattice Radiant Software web page](#)
- [Lattice Propel Design Environment web page](#)
- [Lattice Solutions IP Cores web page](#)
- [Lattice Solutions Reference Designs web page](#)
- [Lattice Insights](#) for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Note: In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

Revision 1.4, IP v1.3.0, April 2026

| Section | Change Summary |
|-----------------------|--|
| All | Made minor editorial changes. |
| Introduction | <ul style="list-style-type: none"> In the IP Support Summary section: <ul style="list-style-type: none"> In Table 1.2. JESD204B IP Support Readiness: <ul style="list-style-type: none"> Removed the <i>Hardware Validated</i> column. Added statement on example design and cross reference to the Example Design section. Removed the Hardware Support section. |
| Design Considerations | Added new section. |

Revision 1.3, IP v1.3.0, December 2025

| Section | Change Summary |
|--------------------------------|---|
| All | <ul style="list-style-type: none"> Added a note on the IP version in the Quick Facts and Revision History sections. Made minor editorial changes. |
| Abbreviations in This Document | Added <i>FMC</i> and <i>FTDI</i> . |
| Introduction | <ul style="list-style-type: none"> In Table 1.1. Summary of the JESD204B IP: <ul style="list-style-type: none"> Added Certus-N2 to <i>Supported Devices</i>. Updated IP core version and software version in <i>Lattice Implementation</i>. Also, added <i>Lattice Propel Design Environment</i>. Added <i>Driver Support</i> row. In Table 1.2. JESD204B IP Support Readiness: <ul style="list-style-type: none"> Added Certus-N2. In the Features section: <ul style="list-style-type: none"> Added Certus-N2 to listings for lane rates and configurable lane counts. In Table 1.3. Ordering Part Number: <ul style="list-style-type: none"> Added Certus-N2. In Table 1.4. Minimum Device Requirements for JESD204B IP: <ul style="list-style-type: none"> Updated link speed for Avant-G and Avant-X speed grade 1. Added Certus-N2. |
| Functional Description | In the AXI4-Lite to LMMIAXI4-Lite to LMMI section: <ul style="list-style-type: none"> Added reference to Lattice Nexus 2 SERDES/PCS User Guide (FPGA-TN-02395). |
| IP Parameter Description | <ul style="list-style-type: none"> In Table 3.1. General Attributes: <ul style="list-style-type: none"> Updated data rate range for CertusPro-NX device. Updated data rate selection information for Avant-G/X device and added note on valid ranges. Added Certus-N2 to <i>Data Rate</i> attribute. Updated note on Avant-G/X device data rate support to indicate multiple continuous ranges. Also, added Certus-N2 to note. In Table 3.2. PHY Attributes: <ul style="list-style-type: none"> Added Certus-N2 to <i>Lane ID</i> and <i>Ref Clk Freq</i> attributes. Updated reference clock frequency example values for CertusPro-NX device at < 2.97 Gb/s. Updated reference clock frequency selection information for Avant-G/X device. |
| Signal Description | <ul style="list-style-type: none"> In Table 4.1. Signal Ports: <ul style="list-style-type: none"> Under JESD Rx Embedded Transport Layer Interface [Clock domain = tx_frame_clk_i] |

| Section | Change Summary |
|----------------------|---|
| | <p>section, updated description of tx_frame_clk_i to include reference to the Clock Interface section.</p> <ul style="list-style-type: none"> • Under JESD Tx AXI4 Lite Register Interface section, updated and added frequency range to description of tx_s_axi_aclk_i. • Under JESD Rx Embedded Transport Layer Interface [Clock domain = rx_frame_clk_i] section, updated description of rx_frame_clk_i to include reference to the Clock Interface section. • Under JESD Rx AXI4 Lite Register Interface section, updated and added frequency range to description of rx_s_axi_aclk_i. • Under AXI-Lite to PHY LMMI Interface section: <ul style="list-style-type: none"> • Added clock source information for CertusPro-NX, Avant-G/X, and Certus-N2 devices to description of axil_lmml_aclk_i. • Added reference to Certus-N2 and Lattice Nexus 2 SERDES/PCS User Guide (FPGA-TN-02395) to description for axil_lmml_avalid_N_i through axil_lmml_rresp_N_o. • Added Certus-N2 to Note 1. • In Table 4.2. Clock Ports: <ul style="list-style-type: none"> • Updated section name to <i>PHY Layer for Avant-G/X and Certus-N2</i>. • Under PHY Layer for Avant-G/X and Certus-N2 section, updated reference clock frequency information in description of refclk_p_i. • Under PHY Layer across All Devices section, added clock source information for CertusPro-NX, Avant-G/X, and Certus-N2 devices to description of axil_lmml_aclk_i. • Under Link and Transport Layer section <ul style="list-style-type: none"> • Added frequency range to descriptions of tx_s_axi_aclk_i and rx_s_axi_aclk_i. • Added note on maximum supported frequency for CertusPro-NX devices to descriptions of tx_frame_clk_i and rx_frame_clk_i. |
| Register Description | <ul style="list-style-type: none"> • In Table 5.14. Rx Register Map Overview: <ul style="list-style-type: none"> • Added Buffer Fill Level Register. • In Table 5.17. Rx Error Status Register: <ul style="list-style-type: none"> • Updated description of Unexpected Control Character Flag to include behavior when operating in Subclass 0 mode. • In Table 5.26. Rx Error Counter Register: <ul style="list-style-type: none"> • Updated description of Unexpected Control Character Flag to include behavior when operating in Subclass 0 mode. • Added the Buffer Fill Level Register section. |
| Example Design | <ul style="list-style-type: none"> • In the CertusPro-NX Device Example Design section: <ul style="list-style-type: none"> • Removed note on check and cross symbols in the Example Design Supported Configuration section. • In Table 6.1. JESD204B IP Configuration Supported by the CertusPro-NX Device Example Design: <ul style="list-style-type: none"> • Replaced check symbol with <i>Checked</i> and cross symbol with <i>Unchecked</i> where applicable. Replaced cross symbol with em-dash if not applicable. • In the Running the Hardware without Rebuilding the Design section: <ul style="list-style-type: none"> • Updated description in Step 8 to emphasize setting the serial line and baud rate before programming when using PuTTY to view log messages. • Updated Figure 6.4. Programming Log Messages and Figure 6.5. CertusPro-NX Evaluation Board (Left) with ADI ADRV9009 Dual RF Evaluation Board (Right). • In the Rebuilding the Design section under RISC V Software: <ul style="list-style-type: none"> • Updated file unzipping instructions in Step 1. • Updated Step 5 to include instructions on handling the <i>Cannot Connect to the Device</i> error message. • Updated Step 8 to include reference to Figure 6.7 for JESD204B setup information. • Added Figure 6.7. JESD204B Setup Information. |

| Section | Change Summary |
|-----------------------|--|
| | <ul style="list-style-type: none"> • Updated Step 12 to include note on installing the git client software. • In the Rebuilding the Design section under RTL Design: <ul style="list-style-type: none"> • Updated Step 4 to include instructions for when a newer version of the system memory module is available. • In Step 6, updated IP versions (AHB-Lite to AXI4 Bridge, GPIO, SPI Controller, AHB Lite Interconnect, and APB Interconnect) and added statement on IP version matching in regen_ip_files.tcl. • Updated Figure 6.12. Regenerating the SoC Design RTL. • In the Avant-X Versa Board Rx Example Design section: <ul style="list-style-type: none"> • Removed note on check and cross symbols in the Example Design Supported Configuration section. • In Table 6.3. JESD204B IP Configuration Supported by the Avant-X Versa Board Rx Example Design: <ul style="list-style-type: none"> • Replaced check symbol with <i>Checked</i> and cross symbol with <i>Unchecked</i>. • Updated settings for Converter Resolution, Number of Bits per Sample, Subclass (SUBCLASSV), and SYSREF Always. • In the Generating Bitstream section: <ul style="list-style-type: none"> • Updated file unzipping instructions in Step 1. • In the TI ADC32RF44EVM Setup section: <ul style="list-style-type: none"> • Updated Step 3 to reference mini-USB cable. • Removed Step on unzipping the lav_versa_adc32rf44_8l_9p8g.zip file. • Updated Step 4b to specifically mention clock names. • Updated Step 4c to include additional instructions on configuring the ADC32RFxx_DIGITAL block and corrected reference to JESD_DIG_CHB_0x03. • In the Avant-X Versa Board Setup section: <ul style="list-style-type: none"> • Updated Steps 4 and 5 on locating the generated bitstream file, programming the FPGA, starting the ramp checker with SW13 pushbutton, and master reset through SW12 pushbutton. • In the Avant-X Versa Board Tx Example Design section: <ul style="list-style-type: none"> • Removed note on check and cross symbols in the Example Design Supported Configuration section under . • In Table 6.5. JESD204B IP Configuration Supported by the Avant-X Versa Board Tx Example Design: <ul style="list-style-type: none"> • Replaced check symbol with <i>Checked</i> and cross symbol with <i>Unchecked</i>. • In the Pre-requisites section: <ul style="list-style-type: none"> • Updated version number for TI DAC39RF10EVM-GUI. • Updated clock generator frequency. • In the Generating Bitstream section: <ul style="list-style-type: none"> • Updated file unzipping instructions in Step 1. • Updated Step 4 to cover regenerating all IP instances. • Updated Figure 6.17. Regenerating All IP Instances and title. • In the Hardware Setup section: <ul style="list-style-type: none"> • Updated Step 5 to reference mini-USB cable. • In the Running the Design section: <ul style="list-style-type: none"> • Updated the procedure for DAC39RF10EVM GUI software v3.1.2. • Updated Figure 6.19. DAC39RF10EVM GUI (Select FTDI Device Window) and title. • Added Figure 6.20. DAC39RF10EVM GUI (DAC39RF1xEVM Window) and Figure 6.21. JESD Crossbar Configuration Window. • Updated Figure 6.22. Output Waveform on Oscilloscope. |
| Designing with the IP | Added note on IP version in GUI. |
| References | <ul style="list-style-type: none"> • Added Lattice Nexus 2 SERDES/PCS User Guide (FPGA-TN-02395). • Added Certus-N2 web page. |

| Section | Change Summary |
|----------------------------------|--|
| Appendix A. Resource Utilization | <p>In Table A.1. Resource Utilization on LAV-AT-X70 LFG1156 Device and Table A.2. Resource Utilization on LFCPNX-100 LFG672 Device:</p> <ul style="list-style-type: none"> Reformatted LUT4 headers. Updated LUT4 logic, LUT4 ripple logic, PFU register, and EBR values for various conditions and wrappers. Removed Rx and Tx transport wrappers. |

Revision 1.2, IP v1.2.0, June 2025

| Section | Change Summary |
|--------------------------------|---|
| Abbreviations in This Document | Added <i>CMOS</i> , <i>FPGA</i> , <i>GUI</i> , <i>IQ</i> , <i>RBD</i> , <i>Rx</i> , <i>SERDES</i> , and <i>Tx</i> . |
| Introduction | <ul style="list-style-type: none"> In Table 1.1. Summary of the JESD204B IP: <ul style="list-style-type: none"> Renamed <i>Supported FPGA Family</i> to <i>Supported Devices</i> and incorporated <i>Targeted Devices</i> information into row. Removed <i>Targeted Devices</i> row. Added IP core version to <i>Lattice Implementation</i>. Removed note to Table 1.2. JESD204B IP Support Readiness regarding preliminary hardware validation setup. In Table 1.3. Ordering Part Number: <ul style="list-style-type: none"> Updated header name from <i>Multi-Site Perpetual</i> to <i>Single Seat Perpetual</i>. In Table 1.4. Minimum Device Requirements for JESD204B IP: <ul style="list-style-type: none"> Removed <i>Link Width</i> column. |
| Functional Description | <p>In the Embedded Transport Layer section:</p> <ul style="list-style-type: none"> Removed description of link configuration parameters from the JESD204B specification. Removed the JESD204B Transport Layer Parameter table. Added notes to Figure 2.9. User Data Format for Independent Lane with Oversampling. |
| IP Parameter Description | <ul style="list-style-type: none"> In Table 3.1. General Attributes: <ul style="list-style-type: none"> Added note to <i>Frames per Multiframe</i> attribute regarding requirement for (Octets per Frame + 1) x (Frames per Multiframe + 1) to be a multiple of 4. Made minor editorial change to listing of selectable values for <i>Data Rate</i>. In Table 3.2. PHY Attributes: <ul style="list-style-type: none"> Made minor editorial change to listing of selectable values for <i>Lane ID</i>. |
| Register Description | <ul style="list-style-type: none"> In Table 5.9. Tx Link Config 3 Register: <ul style="list-style-type: none"> Added note to Octets per Multiframe register regarding requirement for register value + 1 to be a multiple of 4. In Table 5.21. Rx Link Config 3 Register: <ul style="list-style-type: none"> Added note to Octets per Multiframe register regarding requirement for register value + 1 to be a multiple of 4. |
| Example Design | <ul style="list-style-type: none"> Updated description. Added Avant-X Versa Board to list of evaluation boards and updated listing name for CertusPro-NX Evaluation Board. Removed the Simulating the Example Design section. In Table 6.1. JESD204B IP Configuration Supported by the CertusPro-NX Device Example Design: <ul style="list-style-type: none"> Updated title. Removed FIFO Depth in Tx attribute. Updated Figure 6.1. JESD204B Example Design Block Diagram. In the RTL Design section under CertusPro-NX Device Example Design: <ul style="list-style-type: none"> Updated Step 6 through Step 10. Removed the Regenerating IP Instances figure. Added the Avant-X Versa Board Rx Example Design and Avant-X Versa Board Tx Example Design sections. |
| Designing with the IP | Updated Figure 7.4. Simulation Wizard. |

| Section | Change Summary |
|------------|---|
| References | <ul style="list-style-type: none"> Added JESD204B Driver API Reference. Updated listing name to Lattice Radiant Software web page. Added Avant-X Versa Board, TI ADC32RF45EVM Evaluation Board, TI DAC39RF10EVM Evaluation Board, TI DAC39RF10, TI DAC39RF10EVM-GUI, and JESD204B IP Core web pages. |

Revision 1.1, IP v1.1.0, March 2025

| Section | Change Summary |
|--------------------------------|--|
| All | Made changes to conform with inclusive language guidelines. |
| Cover | Added IP version. |
| Abbreviations in This Document | <ul style="list-style-type: none"> Updated section title, description, and table header. Added <i>DUT</i> and <i>ES</i>. |
| Introduction | <ul style="list-style-type: none"> In Table 1.1. Summary of the JESD204B IP: <ul style="list-style-type: none"> Added Lattice Avant to Supported FPGA Family. Added IP Changes row. Removed IP Version row. Added Avant-G and Avant-X to Targeted Devices. Added IP core version to Lattice Implementation. Added note on ES devices. Added the IP Support Summary section. In the Features section: <ul style="list-style-type: none"> Added lane rate for Avant-X and -G devices and clarified lane rate for CertusPro-NX devices. Added lane counts for Avant-X and -G devices and clarified lane counts for CertusPro-NX devices. In Table 1.3. Ordering Part Number: <ul style="list-style-type: none"> Added part numbers for Avant-G and Avant-X. Removed the IP Validation Summary section. Added the Hardware Support section. In Table 1.4. Minimum Device Requirements for JESD204B IP: <ul style="list-style-type: none"> Added Device Family column. Added link speeds for Avant-G and Avant-X devices. Updated link speeds for CertusPro-NX device speed grades 7 and 8 (high performance). |
| Functional Description | <ul style="list-style-type: none"> Updated Figure 2.1. JESD204B IP Block Diagram. Updated description in the ILA Detection section. Removed the Link Layer Data Interface Timing Diagram section under the Rx Link Layer section. Removed the Link Layer Data Interface Timing Diagram section under the Tx Link Layer section. Updated Figure 2.14. Timing Diagram with OCTET_PER_FRAME = 3 and TL_FRAME_PER_CLK = 2. Updated Figure 2.15. JESD204B PHY Layer Module. In the PLL Reference Clock for CertusPro-NX Device section: <ul style="list-style-type: none"> Updated section title. Updated description on number of reference clock selections. Updated description and added reference to Lattice Avant SerDes/PCS User Guide in the AXI4-Lite to LMMI section. Updated Figure 2.20. JESD204B IP Clock Domain Block Diagram. In Table 2.5. JESD204B IP Reset Output Overview: <ul style="list-style-type: none"> Updated descriptions for tx_aresetn_o and rx_aresetn_o. |

| Section | Change Summary |
|--------------------------|---|
| IP Parameter Description | <ul style="list-style-type: none"> • In Table 3.1. General Attributes: <ul style="list-style-type: none"> • Added selectable values for data rate for Avant-G/X devices and updated description. • Added supported number of lanes of 8 and updated description. • Added note on Avant-G/X data rate selectable values. • In Table 3.2. PHY Attributes: <ul style="list-style-type: none"> • Added Lane ID values for Avant devices, updated Lane ID values for CertusPro-NX device, and updated Lane ID description. • Updated PMA Reference Clock description. • Updated Ref Clk Freq description. • Updated PLL M Setting description. • In Table 3.3. Transport Layer Setup Attributes: <ul style="list-style-type: none"> • Removed attributes FIFO Depth in Tx and FIFO Depth in Rx. |
| Signal Description | <ul style="list-style-type: none"> • Updated Figure 4.1. JESD204B IP Port Interface Overview. • In Table 4.1. Signal Ports: <ul style="list-style-type: none"> • Updated descriptions for tx_link_clk_i, tx_sysref_i, tx_aresetn_o, tx_frame_clk_i, tx_tl_in_tdata_i, txN_phy_usr_clk_o, txN_phy_clkout_o, txN_phy_usr_clk_i, txN_phy_resetn_i, rx_link_clk_i, rx_sysref_i, rx_sysref_o, rx_aresetn_o, rx_frame_clk_i, rxN_phy_usr_clk_o, rxN_phy_clkout_o, rxN_phy_resetn_i, rxN_phy_usr_clk_i, axil_lmami_aresetn_i, axil_lmami_aclk_i, and axil_lmami_awvalid_N_i through axil_lmami_rresp_N_o. • Updated sections to <i>JESD Tx PHY to or from Link Bus Interface</i> and <i>JESD Rx Link to or from PHY Bus Interface</i>. • Updated note regarding N in port names. • In Table 4.2. Clock Ports: <ul style="list-style-type: none"> • Updated section to <i>PHY Layer for CertusPro-NX</i>. • Updated descriptions for sd_ext_0_refclkp_i, sd_ext_0_refclkn_i, sd_ext_1_refclkp_i, sd_ext_1_refclkn_i, sdq_refclkp_q0_i, sdq_refclkn_q0_i, sdq_refclkp_q1_i, sdq_refclkn_q1_i, pll_0_refclk_i, and pll_1_refclk_i. • Added <i>PHY Layer for Avant-G/X</i> section. • Added <i>PHY Layer across All Devices</i> section, updated descriptions for axil_lmami_aclk_i, txN_phy_clkout_o, txN_phy_usr_clk_i, rxN_phy_clkout_o, and rxN_phy_usr_clk_i under section, and regrouped signals under section. • Updated descriptions for tx_s_axi_aclk_i, rx_s_axi_aclk_i, txN_phy_usr_clk_o, and rxN_phy_usr_clk_o. • Updated note on REFCLK frequency. |
| Register Description | <ul style="list-style-type: none"> • In Table 5.3. Tx Control Register: <ul style="list-style-type: none"> • Updated fields to [31:29] for Reserved and [28:16] for LMFC Buffer Adjust. • Updated default value for SYSREF Always Enable. • In Table 5.6. Tx Link Config 0 Register: <ul style="list-style-type: none"> • Updated default values for ILA_SCR, ILA_L, ILA_ADJDIR, ILA_PHADJ, ILA_ADJCNT, ILA_BID, and ILA_DID. • Updated description for ILA_L. • In Table 5.7. Tx Link Config 1 Register: <ul style="list-style-type: none"> • Updated default values for ILA_CS, ILA_N, ILA_M, ILA_K, and ILA_F. • In Table 5.8. Tx Link Config 2 Register: <ul style="list-style-type: none"> • Updated default values for ILA_HD, ILA_CF, ILA_JESDV, ILA_S, ILA_SUBCLASSV, and ILA_Nt. • In Table 5.9. Tx Link Config 3 Register: <ul style="list-style-type: none"> • Updated default values for Multiframe in ILA Sequence and Octets per Multiframe. • In Table 5.10. Tx Link Config 4 Register: <ul style="list-style-type: none"> • Updated default values for ILA_LID_L3, ILA_LID_L2, ILA_LID_L1, and ILA_LID_L0. • In Table 5.11. Tx Link Config 5 Register: |

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| | <ul style="list-style-type: none"> • Updated field to [31:29] for Reserved. • Added ILA_LID_L7, [23:21] Reserved, ILA_LID_L6, [15:13] Reserved, ILA_LID_L5, [7:5] Reserved, and ILA_LID_L4. • In Table 5.13. Tx Link Config 7 Register: <ul style="list-style-type: none"> • Added ILA_FCHK_L7, ILA_FCHK_L6, ILA_FCHK_L5, and ILA_FCHK_L4. • In Table 5.15. Rx Control Register: <ul style="list-style-type: none"> • Updated fields to [31:29] for Reserved and [28:16] for LMDC Buffer Adjust. • Updated description for LMFC Buffer Adjust. • Updated default value for SYSREF Always Enable. • In Table 5.18. Rx Link Config 0 Register: <ul style="list-style-type: none"> • Updated default values for ILA_SCR, ILA_L, ILA_ADJDIR, ILA_PHADJ, ILA_ADJCNT, ILA_BID, and ILA_DID. • Updated description for ILA_L. • In Table 5.19. Rx Link Config 1 Register: <ul style="list-style-type: none"> • Updated default values for ILA_CS, ILA_N, ILA_M, ILA_K, and ILA_F. • In Table 5.20. Rx Link Config 2 Register: <ul style="list-style-type: none"> • Updated default values for ILA_HD, ILA_CF, ILA_JESDV, ILA_S, ILA_SUBCLASSV, and ILA_Nt. • In Table 5.21. Rx Link Config 3 Register: <ul style="list-style-type: none"> • Updated default values for Multiframe in ILA Sequence and Octets Per MultiFrame. • In Table 5.22. Rx Link Config 4 Register: <ul style="list-style-type: none"> • Updated default values for ILA_LID_L3, ILA_LID_L2, ILA_LID_L1, and ILA_LID_L0. • In Table 5.23. Rx Link Config 5 Register: <ul style="list-style-type: none"> • Updated field to [31:29] for Reserved. • Added ILA_LID_L7, [23:21] Reserved, ILA_LID_L6, [15:13] Reserved, ILA_LID_L5, [7:5] Reserved, and ILA_LID_L4. • In Table 5.25. Rx Link Config 7 Register: <ul style="list-style-type: none"> • Added ILA_FCHK_L7, ILA_FCHK_L6, ILA_FCHK_L5, and ILA_FCHK_L4. |
| Example Design | <ul style="list-style-type: none"> • Added introductory paragraph to list the evaluation boards used for the example design. • Rearranged the Simulating the Example Design section to under the Example Design section and updated description. • Updated description in the Example Design Test Bench section. • Reorganized content into the CertusPro-NX Device Example Design section. • Updated description in the JESD204B PHY section. • In Table 6.2. Summary of LED Indicators on CPNX Evaluation Board: <ul style="list-style-type: none"> • Updated descriptions of green LEDs LED_0 through LED_6. • Updated descriptions of yellow LEDs LED_8, LED_9, LED_14, and LED_15. • Removed the following figures: <ul style="list-style-type: none"> • ADRV9008/ADRV9009 Evaluation Software GUI • Loading GUI Setup • Setup Loaded Successfully • Creating Script |
| Designing with the IP | <ul style="list-style-type: none"> • Removed the Timing Constraints section. • Updated description in the Specifying the Strategy section. • Updated Step 3 in the Running Functional Simulation section. • Updated Figure 7.8. Example Passing Simulation Waveform title and added introducing sentence. |
| Appendix A. Resource Utilization | <ul style="list-style-type: none"> • Added Table A.1. Resource Utilization on LAV-AT-X70 LFG1156 Device. • Updated LUT4 Logic, LUT4 Ripple Logic, PFU Registers, and EBR values in Table A.2. Resource Utilization on LFCPNX-100 LFG672 Device. |
| References | <ul style="list-style-type: none"> • Rearranged items. • Added Lattice Avant SERDES/PCS User Guide. |

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| | <ul style="list-style-type: none">• Added Avant-X and Avant-G web pages.• Removed Lattice Radiant Software User Guide.• Added CertusPro-NX Evaluation Board, ADI ADRV9009 Dual RF Evaluation Board, and Lattice Solutions Reference Designs web pages. |

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| All | Initial release. |



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