CrossLink MIPI Interface Performance Limitations

Technical Note

FPGA-TN-02054-1.0

November 2019

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
FPGA	Field-Programmable Gate Array
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
MIPI	Mobile Industry Processor Interface
SLVS	Scalable Low Voltage Signaling
WLCSP	Wafer Level Chip Scale Package

1. Introduction

The CrossLink™ field-programmable gate array (FPGA) from Lattice Semiconductor is a programmable video bridging device that supports a variety of protocols and interfaces for mobile image sensors and displays. The key video bridging building blocks in the CrossLink device family are the two hardened MIPI D-PHY blocks (one hard D-PHY block in the WLCSP36 package). CrossLink also includes two programmable I/O banks that can be configured as MIPI D-PHY inputs. As stated in the CrossLink Family Data Sheet (FPGA-DS-02007), the hardened MIPI D-PHY interfaces can transmit and receive up to 1.5 Gbps per lane. The programmable I/O banks, when configured as MIPI D-PHY inputs, can support up to 1.2 Gbps per lane. However, the support for 1.2 Gbps comes with caveats and conditions. This technical note discusses the factors that influences the performance of the programmable I/O when configured as MIPI D-PHY inputs.

2. MIPI Alliance Specification for D-PHY

The following tables list some of the MIPI D-PHY high-speed signals' DC specifications as stipulated in the MIPI Alliance Specification for D-PHY version 1.1.

The differential output voltage V_{OD} is defined as the difference of the voltages V_{DP} and V_{DN} at the Dp and Dn pins, respectively. A MIPI transmitter's measured V_{OD} value must be within the conformance limit specified in Table 2.1.

Table 2.1. Transmitter Characteristics: HS Transmitter DC Specification

Parameter	Description	Min	Nom	Max	Unit
V_{OD}	HS Transmit Differential Voltage	140	200	270	mV

On the MIPI receiver side, V_{IDTH} and V_{IDTL} are defined as differential input high and low threshold voltages of the high-speed receiver. The high-speed receiver detects differential signals at its Dp and Dn input signal pins when both signal voltages, V_{DP} and V_{DN}, are within the common-mode voltage range and if the voltage difference of V_{DP} and V_{DN} exceeds either V_{IDTH} or V_{IDTL}.

Table 2.2. Receiver Characteristics: HS Receiver DC Specification

Parameter	Description	Min	Nom	Max	Unit
V_{IDTH}	Differential Input High Threshold	—	—	70	mV
V_{IDTL}	Differential Input Low Threshold	–70	—	—	mV

A receiver in high-speed mode meets the setup and hold times defined in Table 2.3 as measured between the data and clock signals. $T_{SETUP[RX]}$ is the minimum time that the data remains in its current state before a rising or falling clock edge. $T_{HOLD[RX]}$ is the minimum time that the data remains in its current state after a rising or falling clock edge. The total setup and hold times for data rates ≤1 Gbps is 0.3* UI_{INST}. The total setup and hold times for data rates >1 Gbps is 0.4* UI_{INST}.

Table 2.3. Receiver Data-Clock Timing Specification

Parameter	Description	Min	Max	Unit	Notes
$T_{SETUP[RX]}$	Data to Clock Setup Time (Receiver)	0.15	—	UI_{INST}	3[1]
		0.20	—	UI_{INST}	4[2]
$T_{HOLD[RX]}$	Clock to Hold Time (Receiver)	0.15	—	UI_{INST}	3[1]
		0.20	—	UI_{INST}	4[2]

Notes:

1. Total setup and hold window for receiver of 0.3*UI_{INST} when D-PHY is supporting maximum data rate = 1 Gbps.
2. Total setup and hold window for receiver of 0.4*UI_{INST} when D-PHY is supporting maximum data rate > 1 Gbps.

As a result of the specification, the setup/hold time windows do not decrease linearly as data rates increase (shown in Table 2.4.) Theoretically, it is easier to meet the 1.2 Gbps specification (setup/hold = 167 ps) than the 1.0 Gbps specification (setup/hold = 150 ps).

Table 2.4. MIPI D-PHY Specification Setup and Hold Time Requirements at Different Data Rates

Data Rates	Setup/Hold Spec	Setup Times	Hold Times
600 Mbps	0.15 UI	250 ps	250 ps
700 Mbps	0.15 UI	214 ps	214 ps
800 Mbps	0.15 UI	188 ps	188 ps
900 Mbps	0.15 UI	167 ps	167 ps
1.00 Gbps	0.15 UI	150 ps	150 ps
1.1 Gbps	0.20 UI	182 ps	182 ps
1.2 Gbps	0.20 UI	167 ps	167 ps
1.3 Gbps	0.20 UI	154 ps	154 ps
1.4 Gbps	0.20 UI	143 ps	143 ps
1.5 Gbps	0.20 UI	133 ps	133 ps

3. CrossLink Data Sheet

Section 4.2 of CrossLink Family Data Sheet (FPGA-DS-02007), describes the features of the programmable I/O banks 1 and 2. The following statement at the end of section 4.2 of the data sheet describes the limitations of the programmable I/O banks when configured as SLVS200/MIPI Rx interface.

To ensure the MIPI Rx interface implemented optimally in FPGA fabric with the Programmable I/O, follow the guidelines of assigning I/O to the bank for the MIPI Rx inputs:

- *When an SLVS200/MIPI Rx interface is placed in Bank 1 or 2, do not place both Banks 1 and 2 with LVCMOS outputs in these 2 banks.*

Section 5.13 of CrossLink Family Data Sheet (FPGA-DS-02007), describes the CrossLink external switching characteristics. Table 5.13 - CrossLink External Switching Characteristics of the data sheet includes the general purpose I/O MIPI D-PHY receiver with 1:8 or 1:16 gearing setup and hold times under different conditions, as shown in Table 3.1.

Table 3.1. CrossLink External Switching Characteristics

Parameter	Description	Conditions	–6		Unit
			Min	Max	
General Purpose I/O MIPI D-PHY Rx with 1:8 or 1:16 Gearing					
$t_{SU\_GDDRX\_MP}$	Input Data Set-Up Before CLK	900 Mb/s < Data Rate ≤ 1.2 Gb/s and V_{ID} = 140 mV	0.200	—	UI
		600 Mb/s < Data Rate ≤ 900 Mb/s and V_{ID} = 140 mV	0.150	—	UI
		Data Rate ≤ 600 Mb/s and V_{ID} = 70 mV	0.150	—	UI
$t_{HO\_GDDRX\_MP}$	Input Data Hold After CLK	900 Mb/s < Data Rate ≤ 1.2 Gb/s and V_{ID} = 140 mV	0.200	—	UI
		600 Mb/s < Data Rate ≤ 900 Mb/s and V_{ID} = 140 mV	0.150	—	UI
		Data Rate ≤ 600 Mb/s and V_{ID} = 70 mV	0.150	—	UI

CrossLink is fully conformant with the MIPI D-PHY specification up to 600 Mb/s with the caveat of no LVCMOS outputs on banks 1 and 2. This restriction, as outlined in section 4.2 of the data sheet, is to minimize the noise in banks 1 and 2 to ensure that the MIPI D-PHY configuration operates in an optimal environment. In order for CrossLink to operate above 600 Mbps and up to 1.2 Gbps, V_{ID} needs to be at 140 mV instead of the 70 mV per the MIPI D-PHY specification. Since the MIPI D-PHY setup and hold times are partitioned by data rate frequency, frequencies from >600 Mbps to 900 Mbps and from >900 Mbps to 1.2 Gbps are split into two rows in Table 3.1 to show the different conditions. For 900 Mbps to 1 Gbps, even with V_{ID} = 140 mV, can only meet the 0.2UI setup and hold time requirements, not the 0.15UI setup and hold time requirements of the MIPI D-PHY specification.

4. CrossLink Programmable I/O MIPI D-PHY Performance Conditions

There are three main contributors to the CrossLink programmable I/O MIPI D-PHY performance:

- Number of data lanes
- V_{ID}, differential input voltage
- Number of LVCMOS signals on banks 1 and 2 and their corresponding voltages (VCCIO1 and VCCIO2)

The biggest contributor to programmable I/O MIPI D-PHY performance is the number of data lanes on the MIPI D-PHY channel. As the number of data lanes increases, the more it impacts performance. This applies to the number of data lanes per MIPI interface, not the number of lanes in the system. CrossLink programmable I/O configured for single input with four data lanes may have poorer performance compared to programmable I/O configured for four inputs with single lane on each input. The potential degradation of performance is due to the four data lanes not being perfectly aligned relative to each other.

Table 4.1 shows the performance differences between one data lane vs. four data lanes.

Table 4.1. MIPI D-PHY Speed Performance: Different Data Lanes

Data Lanes	VID	Adjacent Bank Voltage No LVCMOS Outputs	MIPI D-PHY Speed Performance
One Data Lane	70 mV	1.26 V	1200 Mbps
Four Data Lanes	70 mV	1.26 V	600 Mbps

The next factor that contributes to programmable I/O MIPI D-PHY performance is V_{ID}, receiver differential input voltage. As previously mentioned in this technical note, CrossLink is conformant with the MIPI Alliance Specification up to 600 Mbps with V_{ID} = 70 mV. As V_{ID} increases, programmable I/O MIPI D-PHY performance increases. The MIPI D-PHY transmitter specification allows for a maximum high-speed differential voltage of 270 mV with a typical differential voltage of 200 mV. Higher differential input voltage may result in sufficient margin to meet higher speeds depending on the transmitter performance and system environment.

Table 4.2 shows the performance differences between V_{ID} = 70 mV and V_{ID} = 140 mV.

Table 4.2. MIPI D-PHY Speed Performance: Different VID

Data Lanes	VID	Adjacent Bank Voltage No LVCMOS Outputs	MIPI D-PHY Speed Performance
One Data Lane	70 mV	1.26 V	1200 Mbps
	140 mV	1.26 V	1400 Mbps
Four Data Lanes	70 mV	1.26 V	600 Mbps
	140 mV	1.26 V	1300 Mbps

CrossLink sysIO buffers can be configured to be LVCMOS12, LVCMOS18, LVCMOS25 or LVCMOS33. However, as stated in the data sheet, placing any LVCMOS outputs on banks 1 and 2 is NOT allowed. This is one of the restrictions on the implementation of the MIPI D-PHY receiver interface.

The programmable I/O MIPI D-PHY performance may be impacted as VCCIO1 and VCCIO2 voltages increase, as is required to support higher voltage LVCMOS standards, and as the number of LVCMOS outputs increases. Limiting the number of LVCMOS outputs or the rate that these LVCMOS outputs are toggling ensures an optimal environment for maximum programmable I/O MIPI D-PHY performance.

Table 4.3 shows the performance differences at different bank voltages with the maximum number of LVCMOS outputs toggling on the adjacent bank (relative to the MIPI D-PHY bank) at a rate of 48 MHz. The maximum number of LVCMOS outputs is defined as 11 signals on bank 1 and 16 total I/O minus the MIPI D-PHY pairs on bank 2. For four data lanes configuration, there will be 6 LVCMOS signals on bank 2. For one data lane configuration, there will be 12 LVCMOS signals on bank 2.

Table 4.3. MIPI D-PHY Speed Performance: Different LVCMOS Outputs

Data Lanes	VID	Adjacent Bank Voltage Maximum LVCMOS Outputs	MIPI D-PHY Speed Performance
One Data Lane	70 mV	1.26 V	800 Mbps
	70 mV	1.89 V	700 Mbps
Four Data Lanes	70 mV	1.26 V	600 Mbps
	70 mV	1.89 V	400 Mbps

Note: The data in this table do not correspond to the data sheet performance numbers. This data is for the condition wherein the maximum number of LVCMOS outputs are toggling, as opposed to the data sheet condition wherein there are no active LVCMOS outputs.

5. Summary

The CrossLink programmable I/O banks, when configured as MIPI D-PHY inputs, are fully conformant with the MIPI D-PHY specification at 600 Mbps. These inputs can support up to 1.2 Gbps per lane with increased V_{ID} of 140 mV. For 900 Mbps to 1 Gbps, even with V_{ID} = 140 mV, can only meet the 0.2UI setup and hold time requirements. There are other variables that effect the performance including the number of data lanes, number of LVCMOS output signals in the banks and the voltage levels of the banks. All these contribute to the maximum MIPI D-PHY performance achievable by a specific design.

References

For more information, refer to the following documents:

- CrossLink Family Data Sheet (FPGA-DS-02007)
- CrossLink High-Speed I/O Interface (FPGA-TN-02012)
- CrossLink Hardware Checklist (FPGA-TN-02013)
- CrossLink Programming and Configuration Usage Guide (FPGA-TN-02014)
- CrossLink sysCLOCK PLL/DLL Design and Usage Guide (FPGA-TN-02015)
- CrossLink sysI/O Usage Guide (FPGA-TN-02016)
- CrossLink Memory Usage Guide (FPGA-TN-02017)
- Power Management and Calculation for CrossLink Device (FPGA-TN-02018)
- CrossLink I2C Hardened IP Usage Guide (FPGA-TN-02019)
- Advanced CrossLink I2C Hardened IP Reference Guide (FPGA-TN-02020)
- High-Speed PCB Design Considerations (FPGA-TN-02014)
- Power Decoupling and Bypass Filtering for Programmable Devices (TN1068)

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, November 2019

Section	Change Summary
All	Initial release

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