RISC-V SM CPU IP Core – Lattice Propel Builder 2024.1

User Guide

FPGA-IPUG-02253-1.0

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AHB-L	Advanced High-performance Bus – Lite
CPU	Central Processing Unit
CSR	Control and Status Register
DMIPS	Dhrystone MIPS (Million Instructions per Second)
FPGA	Field Programmable Gate Array
GDB	Gnu Debugger
HDL	Hardware Description Language
IP	Intellectual Property
IRQ	Interrupt Request
ISA	Instruction Set Architecture
JTAG	Joint Test Action Group
LUT	Lookup-Table
SM	State Machine (RISC-V for state machine applications)
OpenOCD	Open On-Chip Debugger
PIC	Programmable Interrupt Controller
RISC-V	Reduced Instruction Set Computer-V (Five)
RV32I	RISC-V Integer Instruction Sets
WFI	Wait For Interrupt

1. Introduction

The Lattice Semiconductor RISC-V SM CPU IP contains a 32-bit RISC-V processor core and optional submodules – Timer and Programmable Interrupt Controller (PIC). The CPU core supports the RV32I instruction set, external interrupt, and debug feature, which is JTAG – IEEE 1149.1 compliant. The Timer submodule is a 64-bit real-time counter, which compares a real-time register with another register to assert the timer interrupt. The PIC submodule aggregates up to eight external interrupt inputs into one external interrupt. The submodule registers are accessed by the processor core using a 32-bit Advanced High-performance Bus – Lite (AHB-L) interface.

The design is implemented using Verilog HDL, and it can be configured and generated using the Lattice Propel™ Builder software. It supports ECP5™, ECP5-5G™, Lattice Avant™, MachXO5™-NX, CrossLink™-NX, Certus™-NX, CertusPro™-NX, MachXO3D™, MachXO3™, and MachXO2™ FPGA devices.

1.1. Quick Facts

Table 1.1 presents a summary of the RISC-V SM CPU IP Core.

Table 1.1 RISC-V SM CPU IP Core Quick Facts

IP Requirements	Supported FPGA Family	ECP5, ECP5-5G, Lattice Avant, MachXO5-NX, CrossLink-NX, Certus-NX, CertusPro-NX, MachXO3D, MachXO3L™, MachXO3LF™, MachXO2
Resource Utilization	Targeted Devices	LAE5U, LAE5UM, LFE5U, LFE5UM, LFE5UM5G, LAV-AT, LFMXO5, LIFCL, LFD2NX, LFCPNX, LAMXO3D, LCMXO3D, LCMXO3L, LAMXO3LF, LCMXO3LF, LCMXO2
	Supported User Interfaces	AHB – Lite Interface
	Resources	See Table A.1, Table A.2, Table A.3.
Design Tool Support	Lattice Implementation	IP Core Version 1.6.0 – Lattice Propel Builder 2024.1, Lattice Radiant™ 2024.1
	Simulation	For a list of supported simulators, see the Lattice Radiant and Lattice Diamond™ software user guide.

1.2. Features

The RISC-V SM CPU IP has the following features:

- RV32I instruction set
- Five stage pipeline
- Support the AHB-L bus standard for instruction/data ports
- Optional debug through Gnu Debugger (GDB) and Open On-Chip Debugger (OpenOCD)
- Optional Timer module
- Optional PIC module
- Interrupt and exception handling with Machine mode in RISC-V privileged ISA Specification Revision 1.10
- About 0.5 DMIPS/MHz performance
- Around 40 MHz in MachXO2 devices, 50 MHz in MachXO3D devices, and 100 MHz in CrossLink-NX devices, tested on Hello World templates provided by Lattice Propel design environment.

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.4. Licensing and Ordering Information

The SM CPU IP is provided at no additional cost with the Lattice Propel design environment. The IP can be fully evaluated in hardware without requiring an IP license string.

2. Functional Descriptions

2.1. Overview

The RISC-V SM CPU IP processes data and instructions while monitoring the external interrupts. As shown in Figure 2.1, the CPU IP has a 32-bit processor core and optional submodules. It uses one read-only AHB-L interface for instruction fetch and another AHB-L interface with Read/Write access for data access. See Table 2.5 and Table 2.6 for the AHB-L Instruction Fetch and Data Accessing ports definition. The CPU core, PIC, Timer, and AHB-L multiplexor run in the system clock domain. The Core Debug runs in both the system clock domain and the JTAG clock domain.

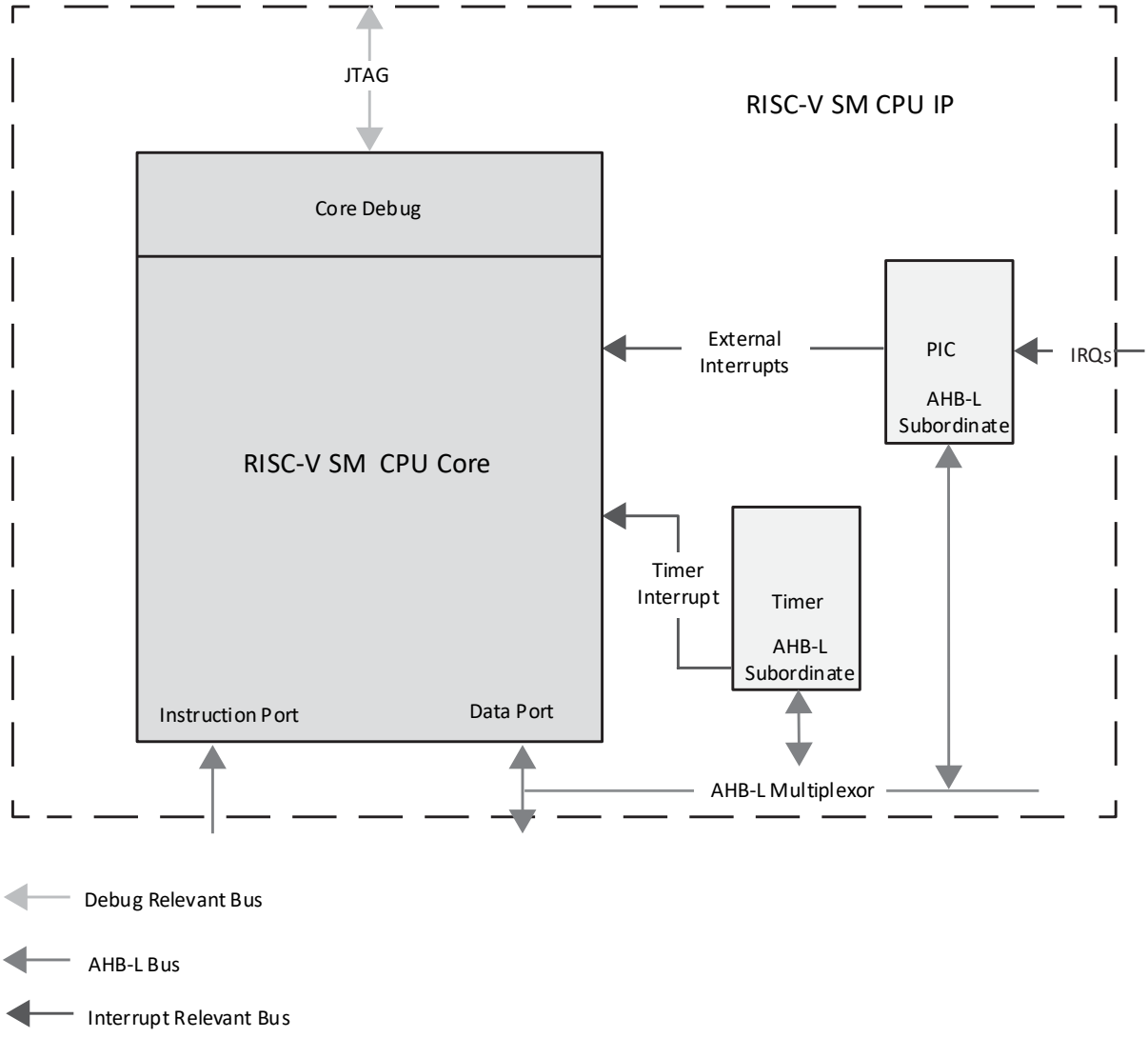


Figure 2.1. RISC-V SM CPU IP Diagram

2.2. Modules Description

2.2.1. RISC-V SM CPU Core

The processor core follows the RV32I instruction set. Figure 2.2 shows the processor core block diagram.

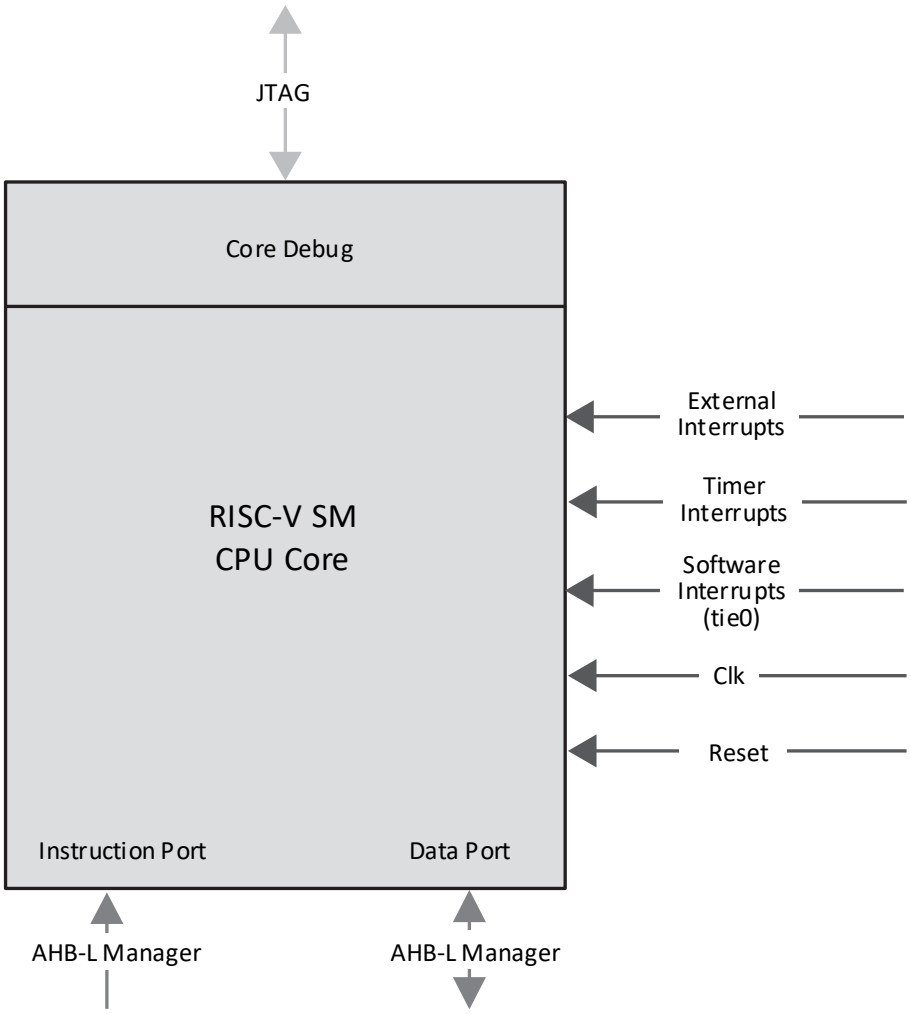


Figure 2.2. RISC-V SM CPU Core Block Diagram

2.2.1.1. Interrupt

The core CPU's interrupts are level sensitive and high active. A given interrupt should remain asserted until cleared by the corresponding interrupt service routine.

If an interrupt occurs, before jumping to the interrupt service routine, the processor core stops the prefetch stage and waits for all instructions in the later pipeline stages to complete their execution.

2.2.1.2. Exception

If an exception occurs, the processor core stops the corresponding instruction, flushes all previous instructions, and waits until the terminated instruction reaches the writeback stage before jumping to the exception service routine.

2.2.1.3. Low Power Mode

The processor core enters into the low power mode with Wait For Interrupt (WFI) instruction. The program counter halts during low power mode, and the processor wakes up if there is external/timer interrupt.

2.2.1.4. Debug

The processor core supports the IEEE-1149.1 JTAG debug logic with two hardware breakpoints. To use the debug module, it is required to allow writes from data port to instruction memory in the SoC. Single-port instruction memory is not allowed to debug.

The soft JTAG is available on Lattice Avant, Certus-NX, CertusPro-NX, CrossLink-NX, and MachXO5-NX devices. For more information, please refer to Appendix B.

2.2.1.5. Reset Vector

The reset vector of processor is 0x0000_0000 and it is fixed.

2.2.1.6. Control and Status Registers

The processor core supports the Control and Status Registers (CSRs) listed in Table 2.1.

Table 2.1. RISC-V SM CPU Core Control and Status Registers

CSR Number	CSR Name	Access	Fields
0x300	Machine Status (mstatus)	read/write	bits[12:11]: mpp, privilege mode before entering a trap. Should always be 2'b11 in machine mode in this CPU core. bit [7]: mpie, mie before entering a trap. Updated to mie value when entering a trap. bit [3]: mie, global interrupt enable.
0x301	Machine ISA (misa)	read-only	bit[31:30]: base, hardwired 0x1, which stands for RV32. bit[25:0]: extension, hardwired 0x100, which stands for RV32I.
0x304	Machine Interrupt Enable (mie)	read/write	bit[11]: meie, machine mode external interrupt enable. bit[7]: mtie, machine mode timer interrupt enable. bit[3]: msie, machine mode software interrupt enable.
0x305	Machine Trap-Vector Base-Address (mtvec)	cannot be accessed, fixed to 0x20	bit[31:2]: trap vector base address, 4-byte aligned. bit[1:0]: trap vector mode. All traps set the program counter to the base address in RISC-V SM CPU core.
0x341	Machine Exception Program Counter (mepc)	cannot be accessed	bits[31:0]: when trap is taken into machine mode, mepc is used to store the address of the instruction that encounters the exception.
0x342	Machine Cause (mcause)	read-only	bit[31]: 1'b1 – interrupt, 1'b0 – exception bit[3:0]: exception code For interrupt: 3 – Machine software interrupt 7 – Machine timer interrupt 11 – Machine external interrupt For exception: 0 – Instruction address misaligned 1 – Instruction access fault 2 – Illegal instruction 4 – Load address misaligned 5 – Load access fault
0x343	Machine Trap Value (mtval)	cannot be accessed	bits[31:0]: When a hardware breakpoint is triggered, or an instruction fetch, load or store address is misaligned or access exception occurs, mtval is written with the fault address. It may also be written with illegal instruction when an illegal instruction occurs.
0x344	Machine Interrupt Pending (mip)	read/write	bit[11]: meip, machine mode external interrupt pending, read only. bit[7] mtip, machine mode timer interrupt pending, read only. bit[3] msip, machine mode software interrupt pending, readable and writable.

2.2.1.7. System Reset Output

The system_resetn_o signal is driven by two ways. When debug is not enabled or if debug reset is not issued, system_resetn_o is the passed value from the input reset signal rst_n_i. It is asynchronous with input clock. When the debugger is enabled and debug reset is issued, the debug reset signal is synchronized to system clock domain and the system_resetn_o is the output of the synchronized signal.

2.2.2. Submodule (PIC/Timer)

The CPU soft IP contains submodules: PIC and Timer. The PIC and Timer share the same start address in memory map and a fixed 2 KB address range is allocated, if either PIC or Timer is enabled.

2.2.2.1. PIC

The PIC aggregates up to eight external interrupt inputs (IRQs) into one interrupt output to the processor core. The PIC's interrupt status register can be used to read the values of IRQs. Individual IRQs can be configured by programming the corresponding PIC_STATUS, PIC_ENABLE, PIC_SET, and PIC_POL registers. All registers can be accessed through the CPU's internal AHB-L interface, as shown in Figure 2.3.

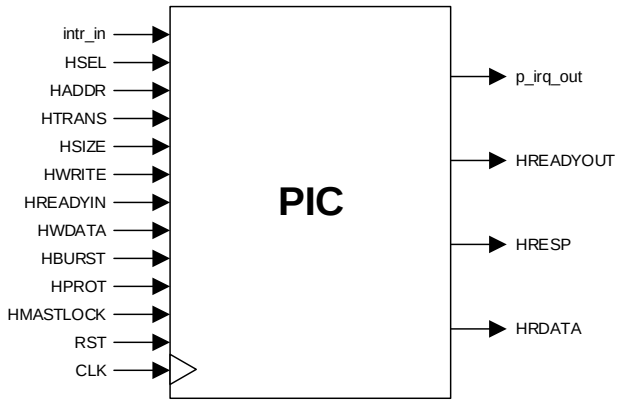


Figure 2.3. PIC Block Diagram

Table 2.2 provides the descriptions of PIC registers.

Table 2.2. PIC Registers

Offset	Name	Description
0x000	PIC_STATUS	Interrupt Status Register Access: read-write Parameterizable width: min=2, max=8 Indicates the pending interrupt at corresponding interrupt request port(irq[i] at top level). **Field / Name / Access / Width / Reset** [N-1] / PIC_STATUS [N-1] / RW / 1 / 0x0 … / … / … / … / … [1] / PIC_STATUS [1] / RW / 1 / 0x0 [0] / PIC_STATUS [0] / RW / 1 / 0x0 PIC_STATUS[i]: Read • 0 – No interrupt at irq[i]. • 1 – Interrupt pending at irq[i]. Write • 0 – No effect. • 1 – Clear interrupt status for irq[i].

<table>
<tr><th>Offset</th><th>Name</th><th>Description</th></tr>
<tr><td>0x004</td><td>PIC_ENABLE</td><td>Interrupt Enable Register
Access: read-write
Parameterizable width: min=2, max=8
Indicates whether the processor responds to the interrupt from the corresponding interrupt request port (irq[i]) or not.

<table>
<tr><th>Field</th><th>Name</th><th>Access</th><th>Width</th><th>Reset</th></tr>
<tr><td>[N-1]</td><td>PIC_ENABLE[N-1]</td><td>RW</td><td>1</td><td>0x0</td></tr>
<tr><td>…</td><td>…</td><td>…</td><td>…</td><td>…</td></tr>
<tr><td>[1]</td><td>PIC_ENABLE[1]</td><td>RW</td><td>1</td><td>0x0</td></tr>
<tr><td>[0]</td><td>PIC_ENABLE[0]</td><td>RW</td><td>1</td><td>0x0</td></tr>
</table>

PIC_ENABLE[i]:
Read
• 0 – irq[i] disabled.
• 1 – irq[i] enabled.
Write
• 0 – Disable irq[i].
• 1 – Enable irq[i].</td></tr>
<tr><td>0x008</td><td>PIC_SET</td><td>Interrupt Set Register
Access: write-only
Parameterizable width: min=2, max=8
Sets the interrupt status for the corresponding interrupt request port(irq[i]).

<table>
<tr><th>Field</th><th>Name</th><th>Access</th><th>Width</th><th>Reset</th></tr>
<tr><td>[N-1]</td><td>PIC_SET [N-1]</td><td>W</td><td>1</td><td>0x0</td></tr>
<tr><td>…</td><td>…</td><td>…</td><td>…</td><td>…</td></tr>
<tr><td>[1]</td><td>PIC_SET [1]</td><td>W</td><td>1</td><td>0x0</td></tr>
<tr><td>[0]</td><td>PIC_SET [0]</td><td>W</td><td>1</td><td>0x0</td></tr>
</table>

PIC_SET[i]:
Read
• Invalid operation. Can get 0.
Write
• 0 – No effect.
• 1 – Set interrupt status for irq[i] (set PIC_STATUS[i]).</td></tr>
<tr><td>0x00C</td><td>PIC_POL</td><td>Interrupt Polarity Register
Access: read-write
Parameterizable width: min=2, max=8
Indicates the polarity of corresponding interrupt request (irq[i]) port.

<table>
<tr><th>Field</th><th>Name</th><th>Access</th><th>Width</th><th>Reset</th></tr>
<tr><td>[N]</td><td>PIC_POL [N]</td><td>RW</td><td>1</td><td>0x0</td></tr>
<tr><td>…</td><td>…</td><td>…</td><td>…</td><td>…</td></tr>
<tr><td>[1]</td><td>PIC_POL l[1]</td><td>RW</td><td>1</td><td>0x0</td></tr>
<tr><td>[0]</td><td>PIC_POL [0]</td><td>RW</td><td>1</td><td>0x0</td></tr>
</table>

PIC_POL[i]:
Read
• 0 – irq[i] is active high.
• 1 – irq[i] is active low.</td></tr>
</table>

Offset	Name	Description
		Write • 0 – Set irq[i] active high. • 1 – Set irq[i] active low.

Note: The register definition of PIC follows Lattice Interrupt Interface (LINTR) Standard, refer to Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039) for more information.

2.2.2.2. Timer

The Timer module provides a 64-bit real-time counter register (mtime) and time compare register (mtimecmp). An output interrupt signal notifies the RISC-V processor core when the value of mtime is greater than or equal to the value of mtimecmp. All registers can be accessed through the CPU's internal AHB-L interface, as shown in Figure 2.4.

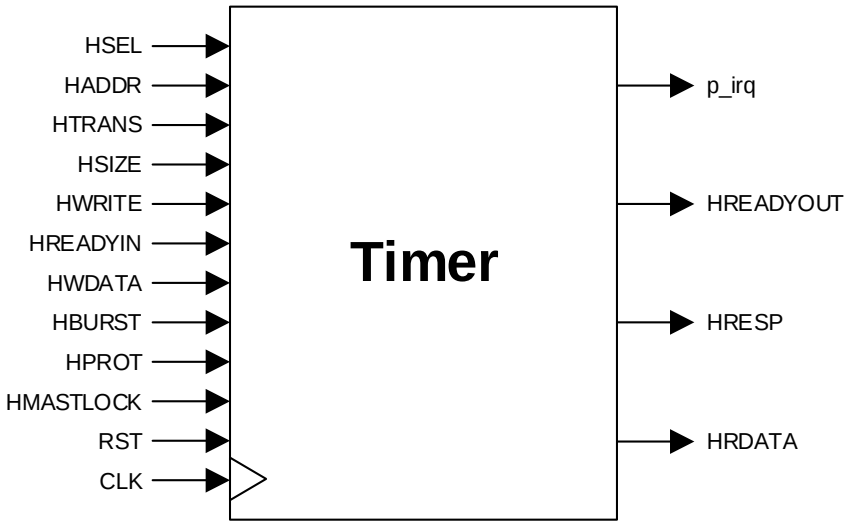


Figure 2.4. Timer Block Diagram

Table 2.3 provides the descriptions of Timer registers.

Table 2.3. Timer Registers

Offset	Name	Description
0x400	TIMER_CNT_L	Lower 32 bits of Timer counter register. **Field** / **Name** / **Access** / **Width** / **Reset** [63:0] / mtime / RW / 64 / 0x0 mtime A 64-bit real-time counter register. You must set the register to a non-zero value to start the counting process.
0x404	TIMER_CNT_H	Higher 32 bits of Timer counter register.
0x410	TIMER_CMP_L	Lower 32 bits for Timer time compare register. **Field** / **Name** / **Access** / **Width** / **Reset** [63:0] / mtimecmp / RW / 64 / 0x0 mtimecmp This register is used to generate or clear the timer interrupt (mtip). When the value of mtime register is greater than or equal to the value of mtimecmp

Offset	Name	Description
		register, the cpu_mtip_o is asserted. The interrupt remains posted until mtimecmp becomes greater than mtime, typically as a result of writing mtimecmp.
0x400	TIMER_CNT_L	Higher 32 bits for Timer time compare register.

2.3. Signal Description

Table 2.4 to Table 2.7 list the ports of the CPU soft IP in different categories.

2.3.1. Clock and Reset

Table 2.4. Clock and Reset Ports

Name	Direction	Width	Description
clk_i	In	1	RISC-V soft IP clock.
rst_n_i	In	1	Global reset, active low.
system_resetn_o	Out	1	Combined Global reset and Debug Reset from JTAG, active low.

2.3.2. Instruction and Data Interface

Table 2.5. Instruction Ports

Name	Direction	Width	Description
AHBL_M0_INSTR - HADDR	Out	32	—
AHBL_M0_INSTR - HWRITE	Out	1	Fixed to 1'b0
AHBL_M0_INSTR - HSIZE	Out	3	Fixed to 3'b010
AHBL_M0_INSTR - HPROT	Out	4	Fixed to 4'b1110
AHBL_M0_INSTR - HTRANS	Out	2	—
AHBL_M0_INSTR - HBURST	Out	3	Fixed to 3'b000
AHBL_M0_INSTR - HMASTLOCK	Out	1	Fixed to 1'b0
AHBL_M0_INSTR - HWDATA	Out	32	—
AHBL_M0_INSTR - HRDATA	In	32	—
AHBL_M0_INSTR - HREADY	In	1	—
AHBL_M0_INSTR - HRESP	In	1	—

Table 2.6. Data Ports

Name	Direction	Width	Description
AHBL_M1_DATA - HADDR	Out	32	—
AHBL_M1_DATA - HWRITE	Out	1	—
AHBL_M1_DATA - HSIZE	Out	3	—
AHBL_M1_DATA - HPROT	Out	4	Fixed to 4'b1111
AHBL_M1_DATA - HTRANS	Out	2	—
AHBL_M1_DATA - HBURST	Out	3	Fixed to 3'b000
AHBL_M1_DATA - HMASTLOCK	Out	1	—
AHBL_M1_DATA - HSEL	Out	1	—
AHBL_M1_DATA - HWDATA	Out	32	—
AHBL_M1_DATA - HRDATA	In	32	—
AHBL_M1_DATA - HREADY	In	1	—

For more information, refer to AMBA 3 AHB-Lite Protocol V1.0.

2.3.3. Interrupt Interface

Table 2.7. Interrupt Ports

Name	Type	Width	Description
IRQ_Sx	In	1~8	Peripheral interrupts.
TIMER_IRQ_M0	Out	1	Timer interrupt output. Exists only when “TIMER_ENABLE” checked.
TIMER_IRQ_S0	In	1	Timer interrupt input. Exists only when “TIMER_ENABLE” unchecked.

2.4. Attribute Summary

The configurable attributes of the RISC-V SM CPU IP are shown in Table 2.8 and are described in Table 2.9.

The attributes can be configured through the Lattice Propel Builder software.

Table 2.8. Configurable Attributes

Attribute	Selectable Values	Default	Dependency on Other Attributes
General			
SIMULATION	Checked, Unchecked	Unchecked	—
DEBUG_ENABLE	Checked, Unchecked	Checked	—
SOFT_JTAG	Checked, Unchecked	Unchecked	—
TIMER_ENABLE	Checked, Unchecked	Checked	—
PIC_ENABLE	Checked, Unchecked	Checked	—
PICTIMER_START_ADDR	0~0xFFFFFC00	0xFFFF0000	Enabled when PIC_ENABLE or TIMER_ENABLE.
IRQ_NUM	2~8	8	Enabled when PIC_ENABLE.
JTAG_CHANNEL	14~16	14	Enabled when DEBUG_ENABLE.

Table 2.9. Attributes Description

Attribute	Description
SIMULATION	1: simulation mode for CPU. 0: synthesis mode for CPU.
DEBUG_ENABLE	1: debug function enable. 0: debug function disable.
SOFT_JTAG	1: debug with hard JTAG. 0: debug with soft JTAG.
TIMER_ENABLE	1: timer enable. 0: timer disable.
PIC_ENABLE	1: pic enable. 0: pic disable.
PICTIMER_START_ADDR	Start address of PIC and Timer.
IRQ_NUM	Number of Peripheral Interrupts.
JTAG_CHANNEL	JTAG channel select.

3. RISC-V SM CPU IP Generation

This section provides information on how to generate the CPU IP module using Lattice Propel Builder software.

To generate the CPU IP module:

1. In Lattice Propel Builder software, create a new design. Select the CPU package.
2. Enter the component name. Click **Next**, as shown in Figure 3.1.

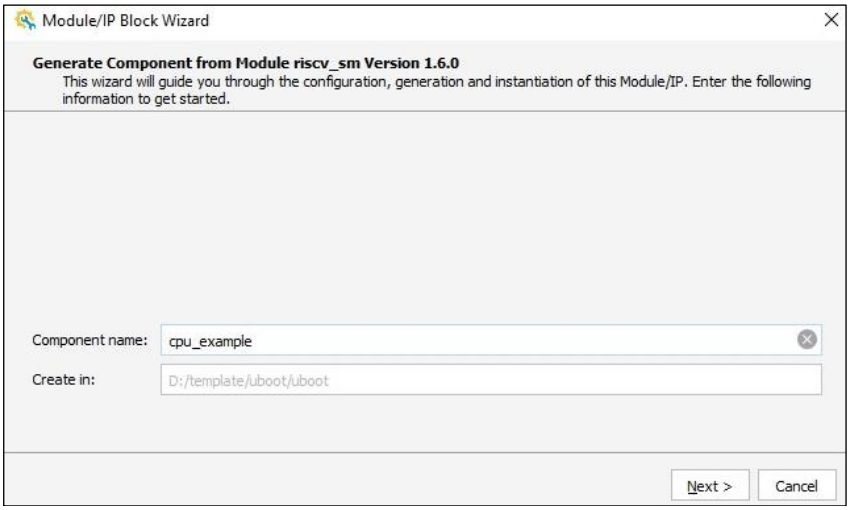


Figure 3.1. Entering Component Name

3. Configure the parameters as needed. Click **Generate**.

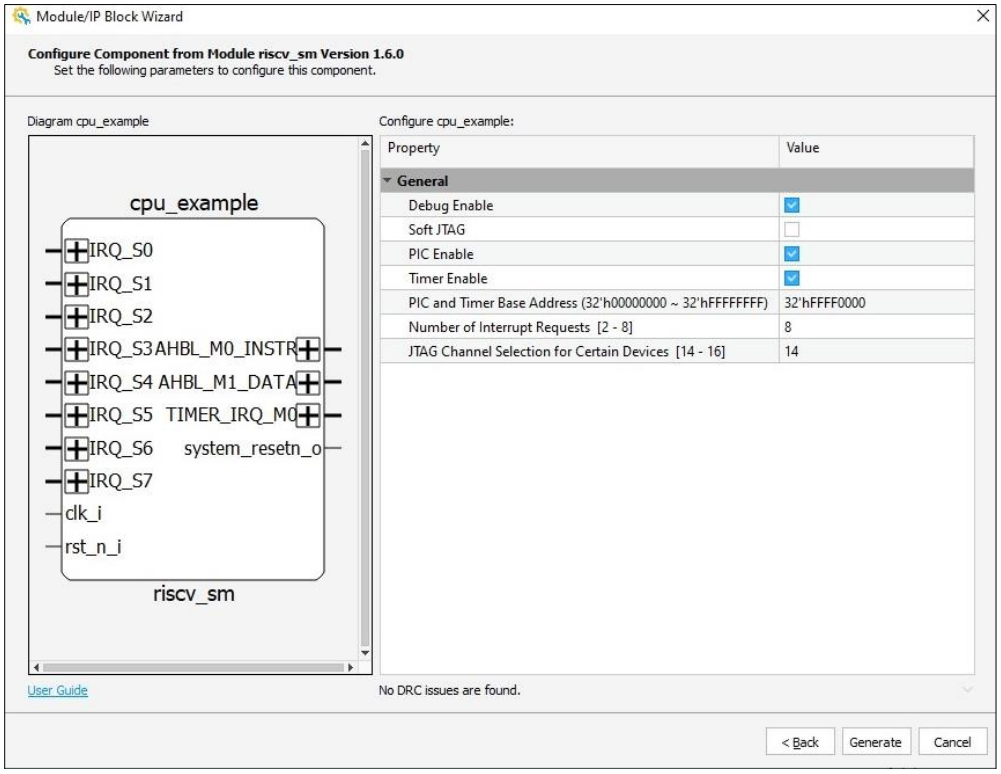


Figure 3.2. Configuring Parameters

4. Verify the information. Click **Finish**.

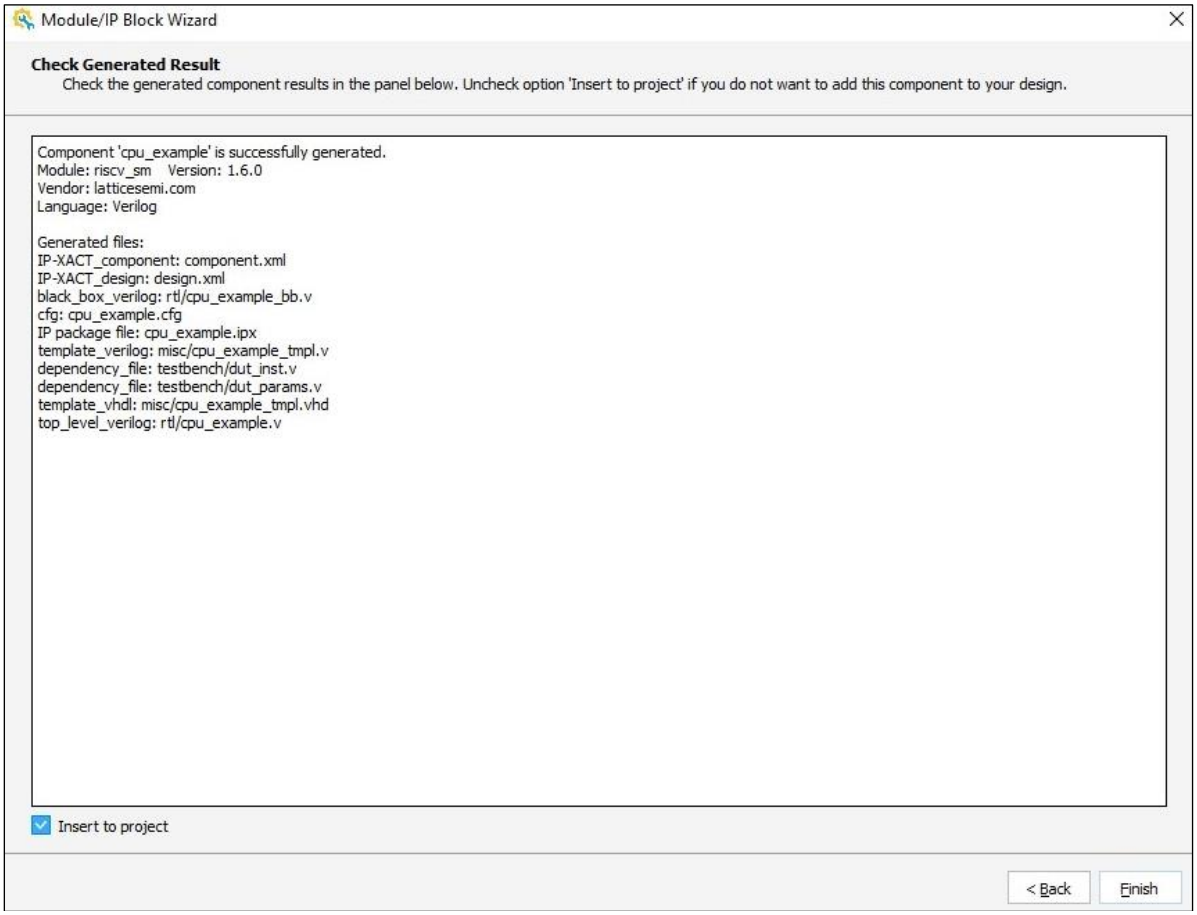


Figure 3.3. Verifying Results

5. Confirm or modify the module instance name. Click **OK**.

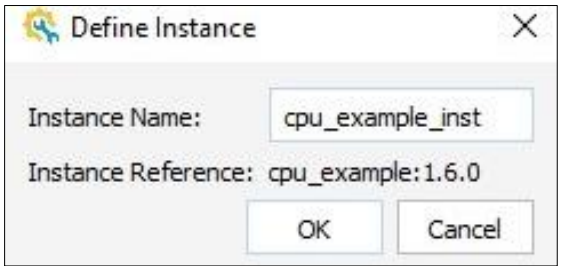


Figure 3.4. Specifying Instance Name

6. The CPU IP instance is successfully generated, as shown in Figure 3.5.

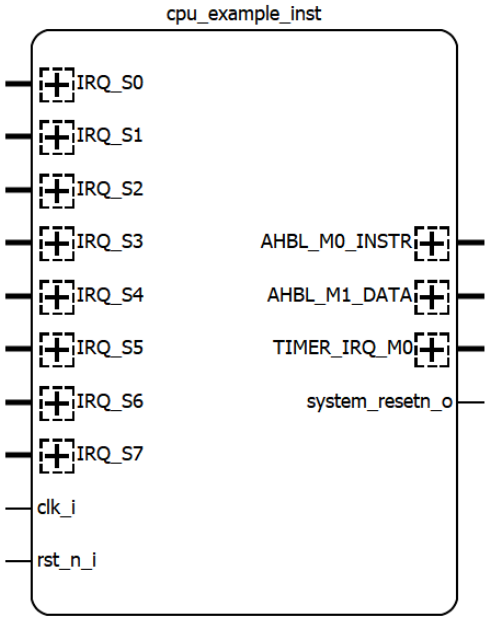


Figure 3.5. Generated Instance

Appendix A. Resource Utilization

Table A.1. Resource Utilization in MachXO2 Device

Configuration	LUTs	Registers	sysMEM EBRs
Processor core only	728	558	4
Processor core + PIC	807	577	4
Processor core + Timer	996	704	4
Processor core + Debug	947	861	4
Processor core + PIC + Timer	1047	713	4
Processor core + PIC + Timer + Debug	1257	1017	4

Note: Resource utilization characteristics are generated using Lattice Diamond software.

Table A.2. Resource Utilization in MachXO3D Device

Configuration	LUTs	Registers	sysMEM EBRs
Processor core only	760	568	4
Processor core + PIC	850	587	4
Processor core + Timer	1135	714	4
Processor core + Debug	1012	871	4
Processor core + PIC + Timer	1186	725	4
Processor core + PIC + Timer + Debug	1402	1026	4

Note: Resource utilization characteristics are generated using Lattice Diamond software.

Table A.3. Resource Utilization in CrossLink-NX Device

Configuration	LUTs	Registers	sysMEM EBRs
Processor core only	899	596	2
Processor core + PIC	980	615	2
Processor core + Timer	1365	715	2
Processor core + Debug	1233	974	2
Processor core + PIC + Timer	1382	724	2
Processor core + PIC + Timer + Debug	1721	1127	2

Note: Resource utilization characteristics are generated using Lattice Radiant software.

Table A.4. Resource Utilization in CertusPro-NX Device

Configuration	LUTs	Registers	sysMEM EBRs
Processor core only	996	570	2
Processor core + PIC	1129	607	2
Processor core + Timer	1369	726	2
Processor core + Debug	1257	947	2
Processor core + PIC + Timer	1466	742	2
Processor core + PIC + Timer + Debug	1652	1119	2

Note: Resource utilization characteristics are generated using Lattice Radiant software.

Table A.5. Resource Utilization in Lattice Avant Device

Configuration	LUTs	Registers	sysMEM EBRs
Processor core only	1045	570	2
Processor core + PIC	1125	607	2
Processor core + Timer	1347	715	2
Processor core + Debug	1352	997	2
Processor core + PIC + Timer	1443	742	2
Processor core + PIC + Timer + Debug	1730	1118	2

Note: Resource utilization characteristics are generated using Lattice Radiant software.

Appendix B. Debug with Soft JTAG

To debug with Soft JTAG:

1. In Lattice Propel Builder software, enable **Soft JTAG** in the IP block Wizard GUI (Figure 3.2) when generating the IP.
2. After the IP is generated, right-click on the **JTAG** port and select **Export** (Figure B.1).

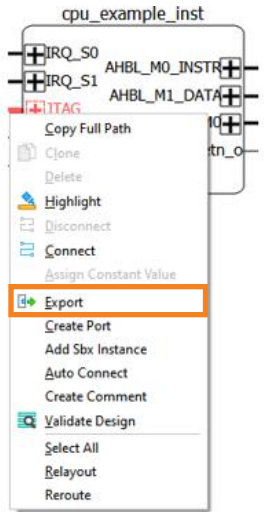
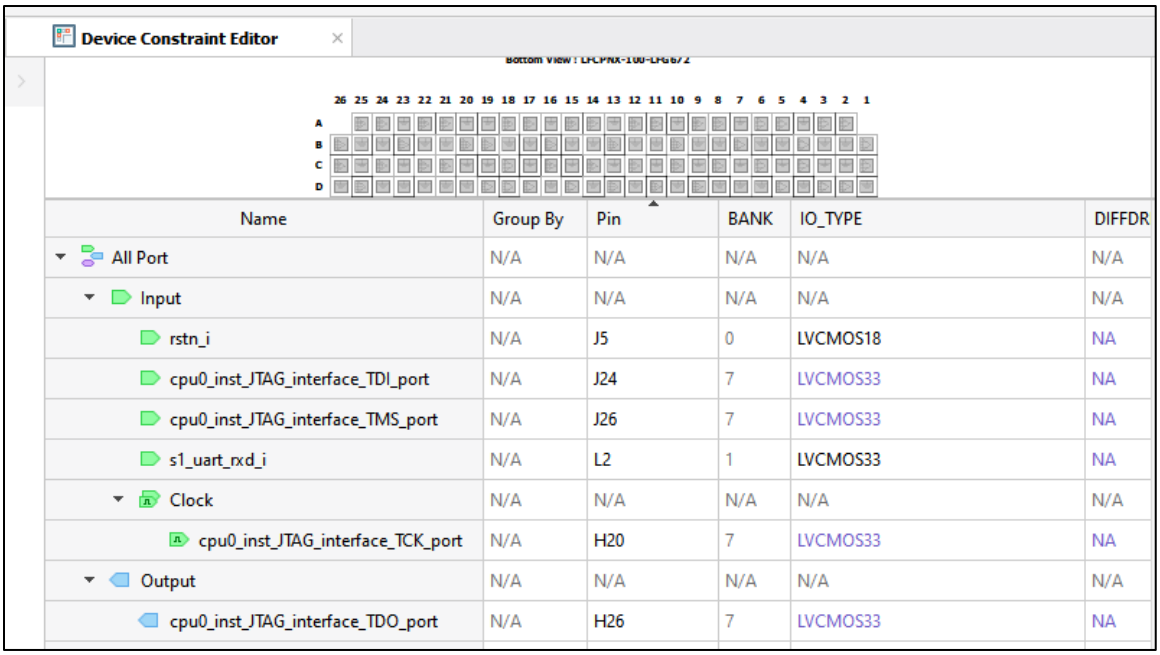


Figure B.1. Exporting Pins

3. Assign the normal I/O as JTAG I/O using the Device Constraint Editor in Lattice Radiant software.
   a. Synthesize the design SoC in Lattice Radiant software by clicking **Synthesis Design** from the process toolbar.
   b. Open **Device Constraint Editor** from the **Tools** tab in Lattice Radiant software and assign the pins. For different devices, refer to the user guide of each board. The following assignment is for LFCPNX-100-9LF672C (Figure B.2).



Name	Group By	Pin	BANK	IO_TYPE	DIFFDR
All Port	N/A	N/A	N/A	N/A	N/A
Input	N/A	N/A	N/A	N/A	N/A
rstn_i	N/A	J5	0	LVCMOS18	NA
cpu0_inst_JTAG_interface_TDI_port	N/A	J24	7	LVCMOS33	NA
cpu0_inst_JTAG_interface_TMS_port	N/A	J26	7	LVCMOS33	NA
s1_uart_rxd_i	N/A	L2	1	LVCMOS33	NA
Clock	N/A	N/A	N/A	N/A	N/A
cpu0_inst_JTAG_interface_TCK_port	N/A	H20	7	LVCMOS33	NA
Output	N/A	N/A	N/A	N/A	N/A
cpu0_inst_JTAG_interface_TDO_port	N/A	H26	7	LVCMOS33	NA

Figure B.2. Assigning Pins

c. Double-click on the targeted strategy in the **File List** view to open the **Strategies** dialog box.

d. In the **Strategies** dialog box, set the environment variable for **Place & Route Design**. Enter `-exp WARNING_ON_PCLKPLC1=1` to the Value of **Command Line Options** if TCK connects to normal I/O (Figure B.3).

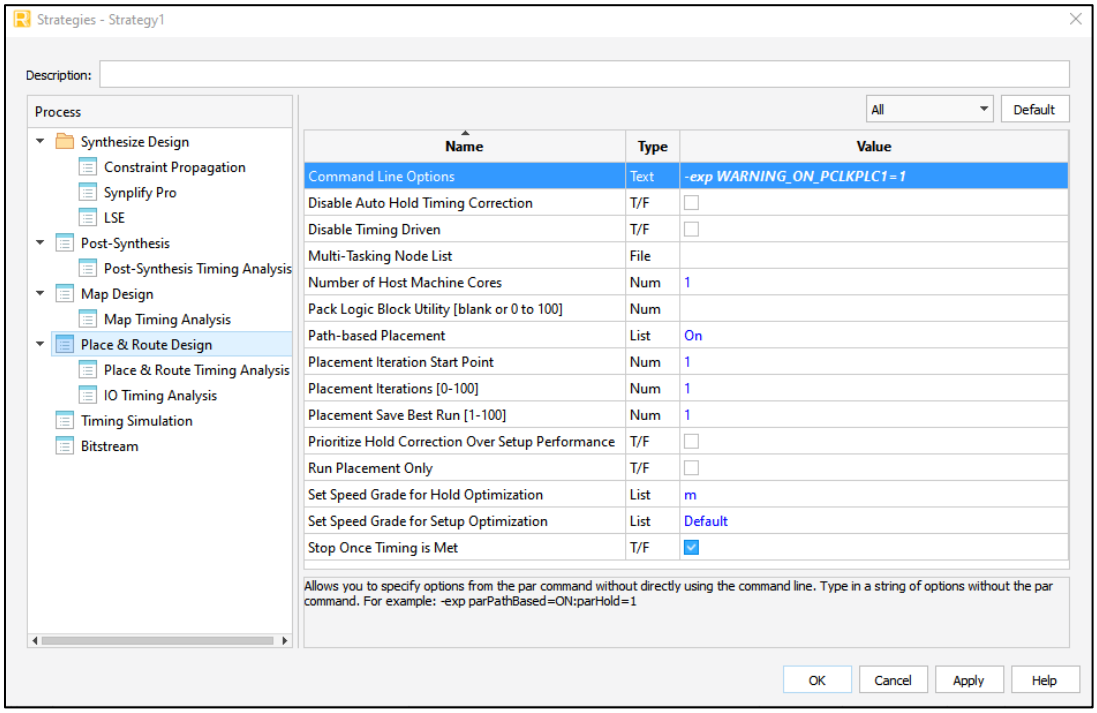


Figure B.3. Setting Environment Variables

e. Generate the bitstream and load it to the board.

f. Connect the pins on cable to the board according to your assignments. Connect VCC and GND. Scan the cable in Propel SDK and ignore the scanning of the device.
Note: C projects generated for Lattice Avant family devices cannot use Soft JTAG to debug on MachXO5-NX, Certus-NX, CertusPro-NX, and CrossLink-NX boards and vice versa.

References

- Lattice Propel Builder 2024.1 User Guide (FPGA-UG-02212)
- AMBA 3 AHB-Lite Protocol V1.0
- RISC-V Privileged Specification (20211203)
- RISC-V Instruction Set Manual (20190608)
- Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039)

For more information, refer to:

- Lattice Propel Web Page
- Lattice Avant-E Family Devices Web Page
- MachXO5-NX Family Devices Web Page
- Certus-NX Family Devices Web Page
- CertusPro-NX Family Devices Web Page
- CrossLink-NX Family Devices Web Page
- MachXO3D Family Devices Web Page
- MachXO3 Family Devices Web Page
- MachXO2 Family Devices Web Page
- ECP5 & ECP5-5G Family Devices Web Page
- Lattice Insights for Training Series and Learning Plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.0, May 2024

Section	Change Summary
All	Production release.

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