

PTP_DAUGHTER_BOARD

REVISION 2.1



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Title		
01_Title_Block		
Size	Project	Schematic Rev
A3	PTP_DAUGHTER_BOARD	v2.1
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		B
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Revision Record

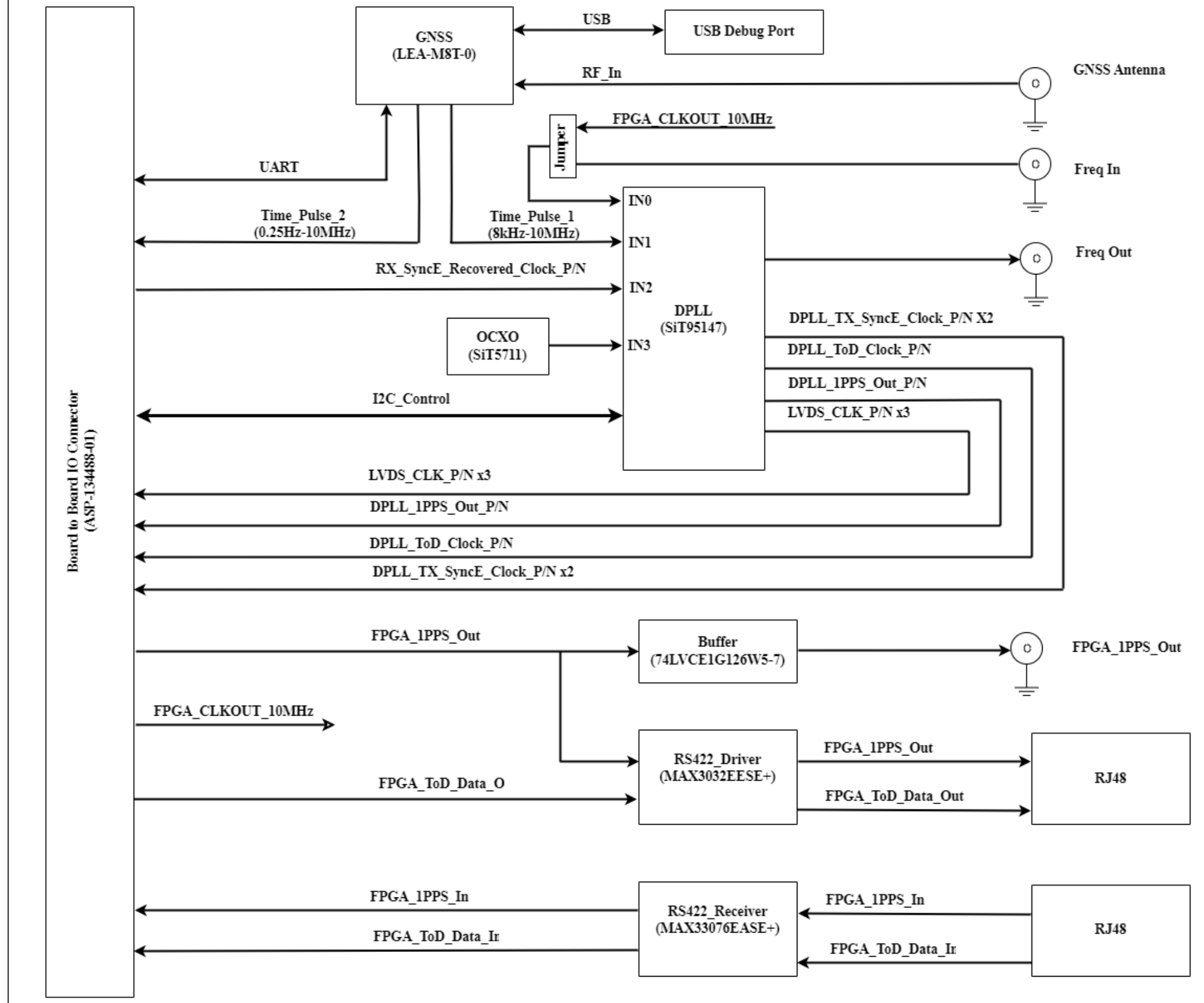
Revision	Date	Description of Change	Author
V1.0	May 1, 2022	Initial Design	
V2.0	Jan 25, 2023	Added DPLL status signals to FMC connector U6 GND pin connected FB6 replaced with 10hm resistor	
V2.1	Jul 25, 2023	Added Jumper on DPLL INO to change the input between external frequency and 10MHz input from FPGA Renamed DPLL Output and Inout signals as per application Reconnected GNSS Reset signal form FPGA to GNSS Reset switch Added DPLL Loss of Lock and FLEXIO signals to FMC connector	



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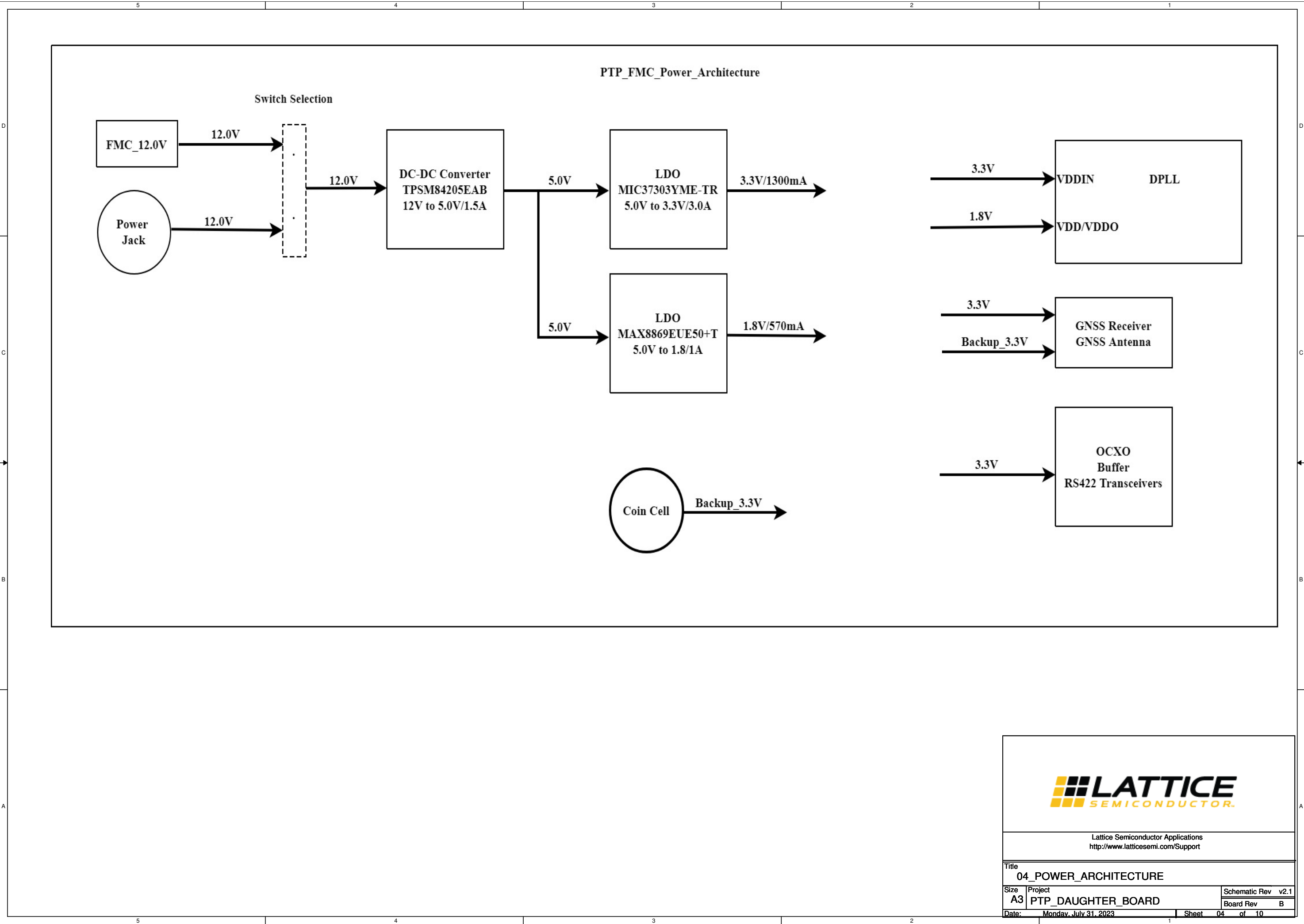
Title		02_INDEX	
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PTP Daughter Board Architecture



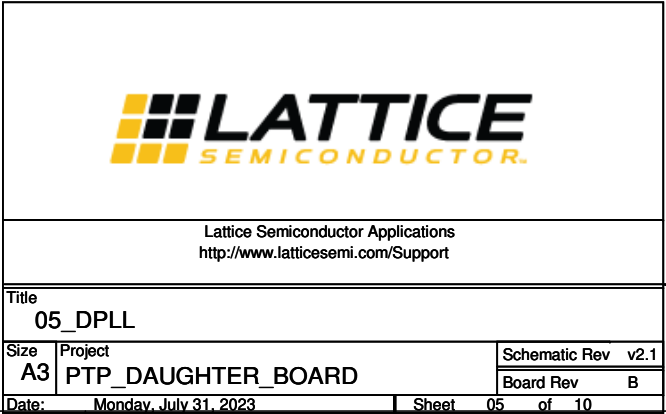
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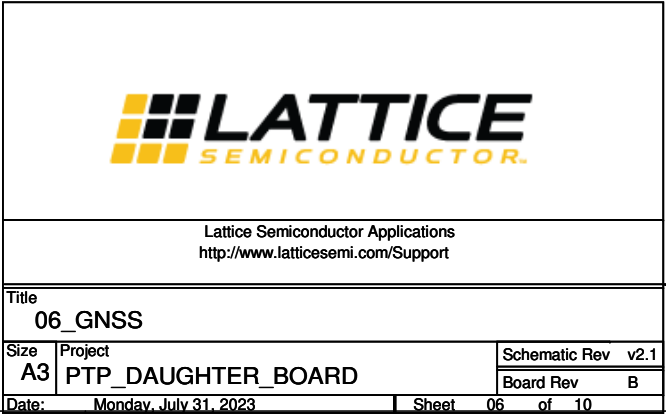
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Size A3	Project PTP_DAUGHTER_BOARD	Schematic Rev v2.1
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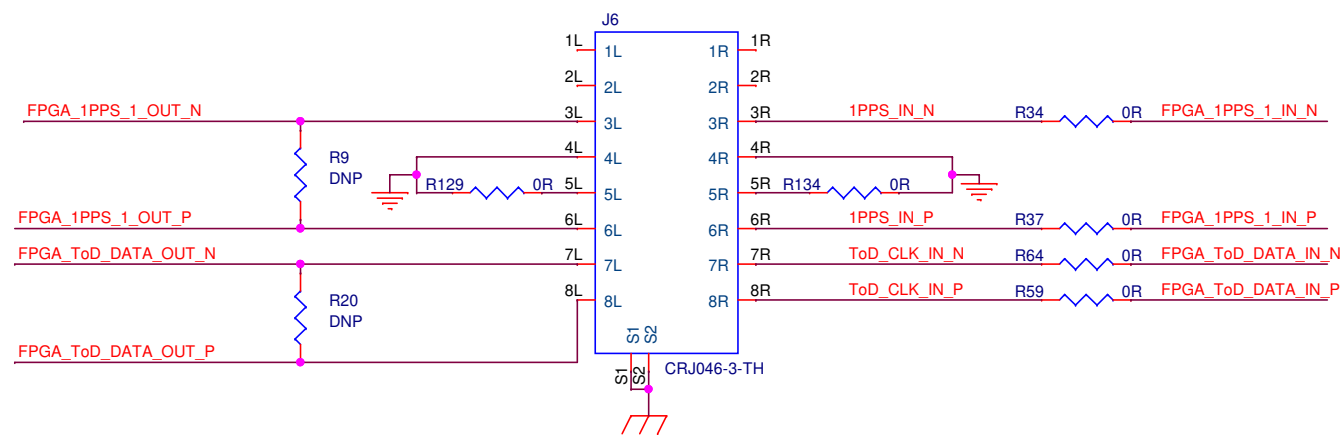
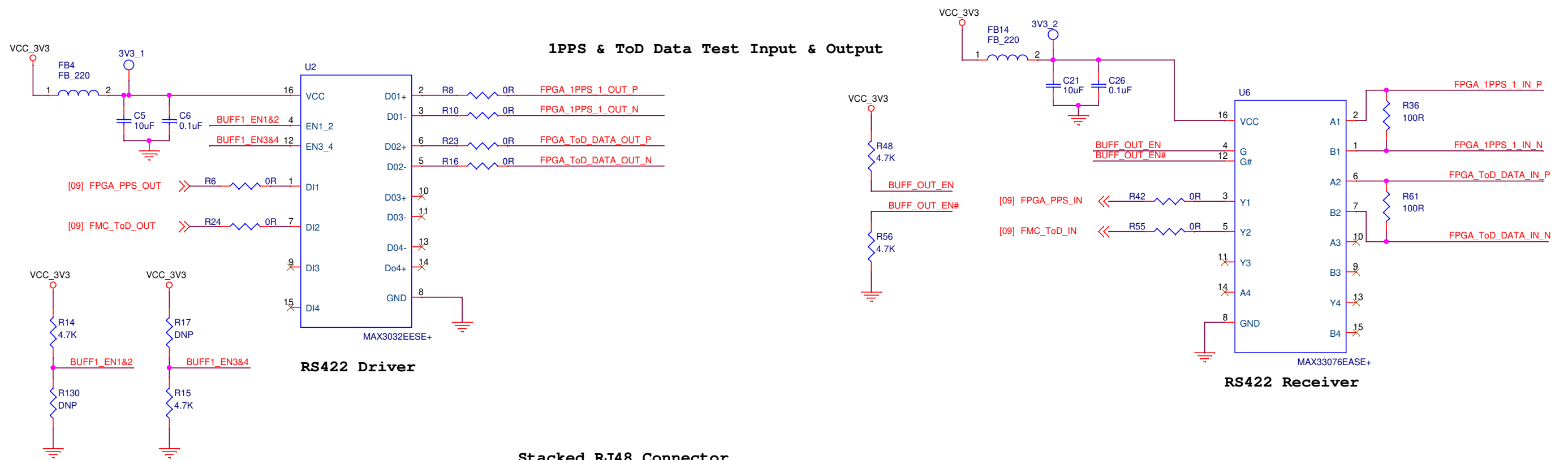
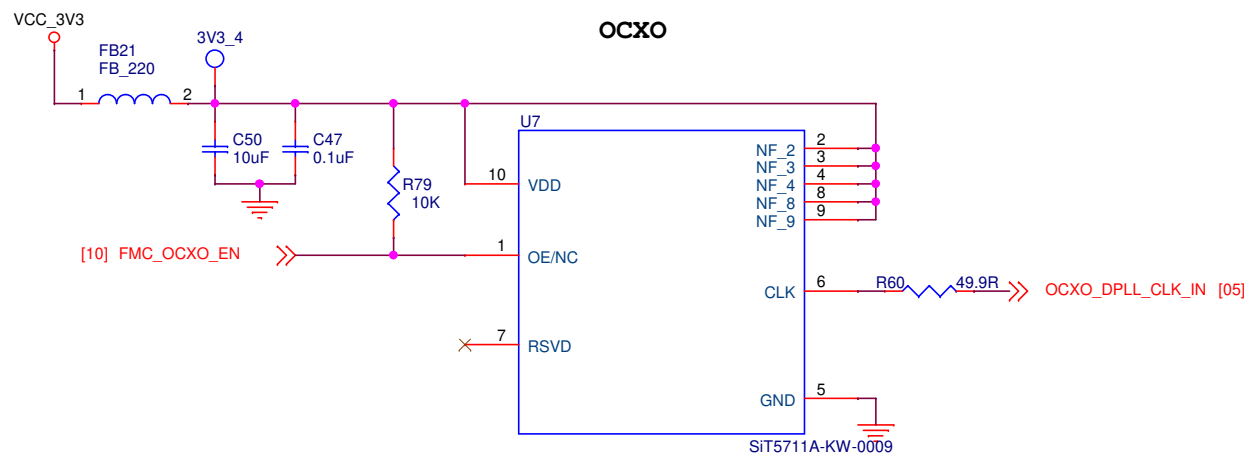


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Title			
04_POWER_ARCHITECTURE			
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Title
07_OCXO_RJ48

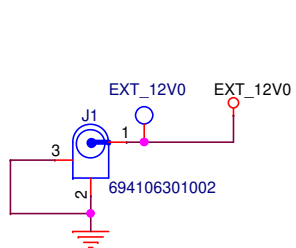
Size Project
A3 PTP_DAUGHTER_BOARD

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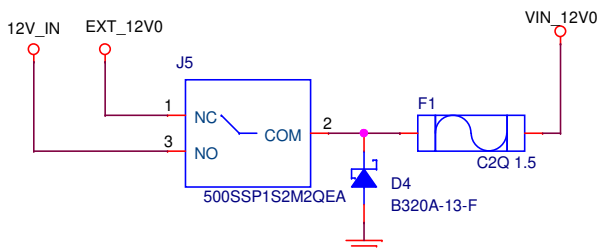
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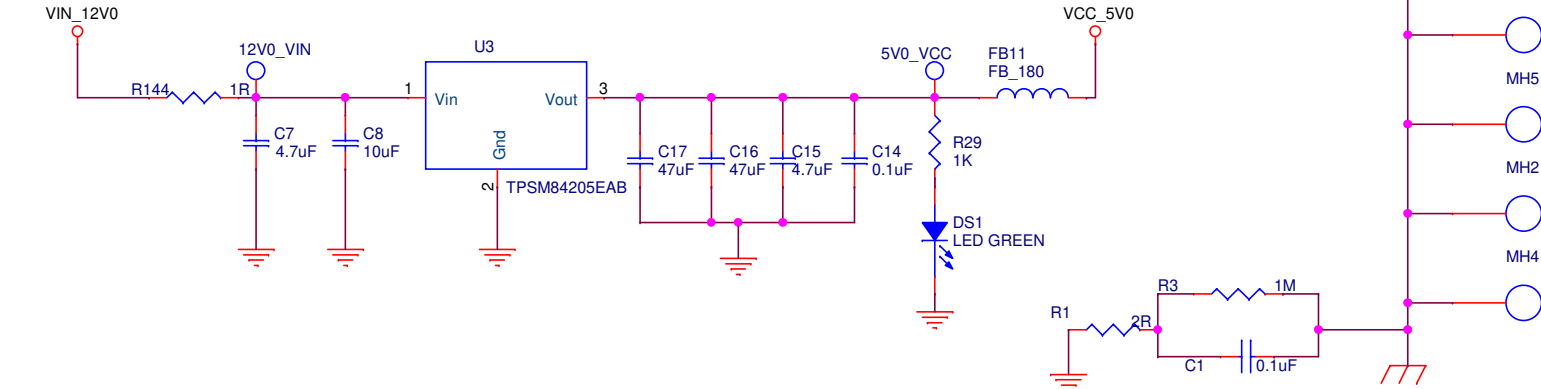
12V POWER JACK



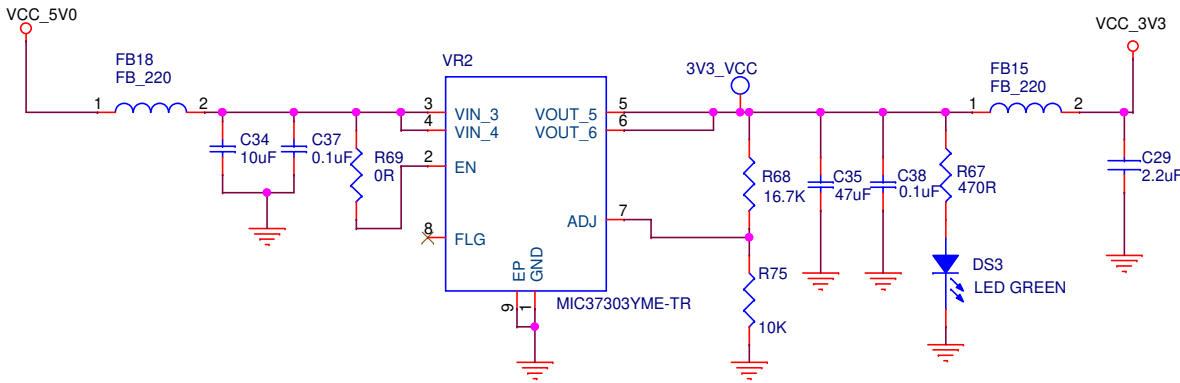
12V SELECTION SWITCH



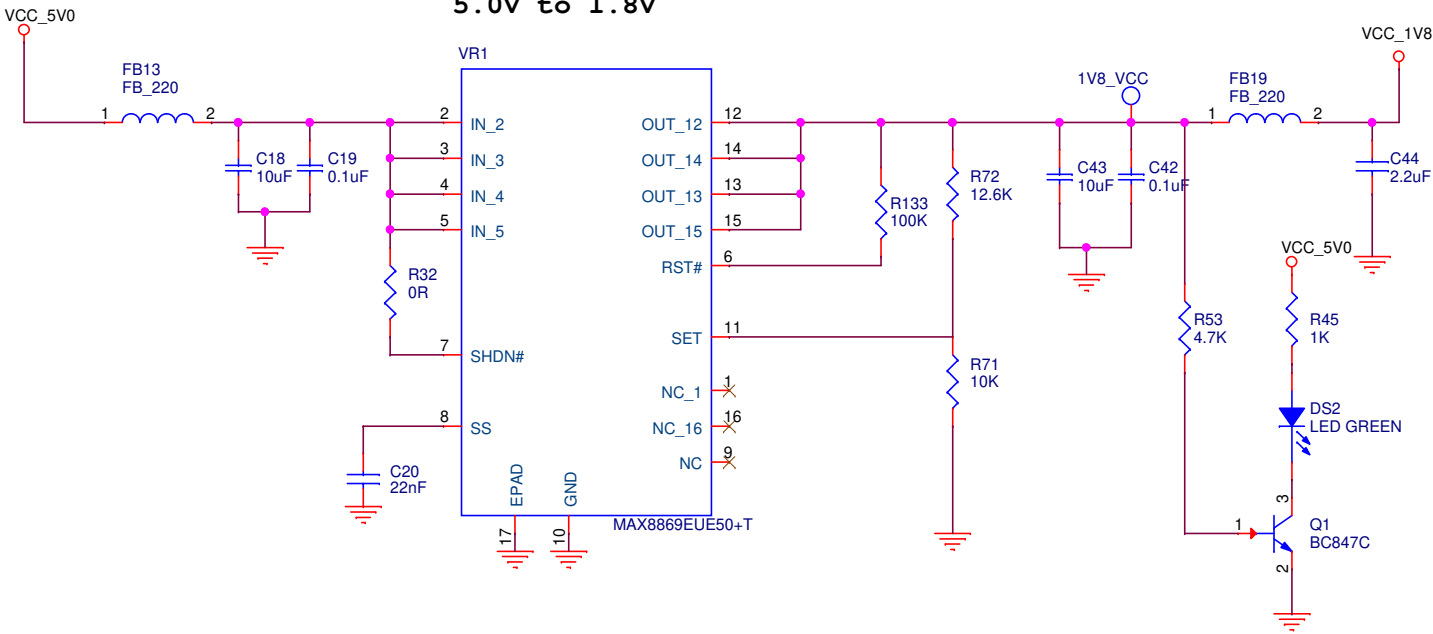
12.0V to 5.0V



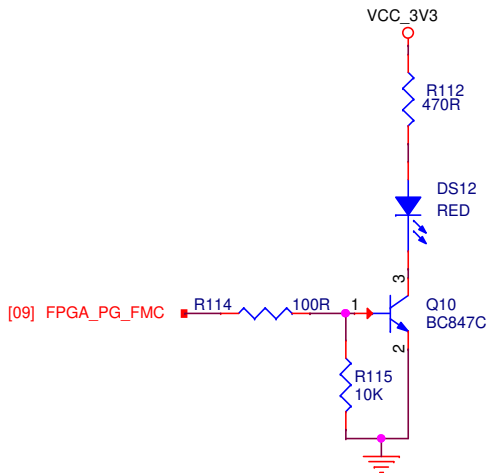
5.0V to 3.3V



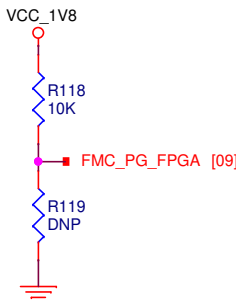
5.0V to 1.8V



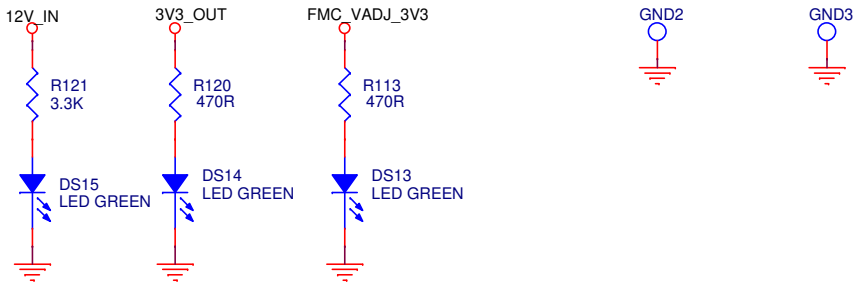
Carrier Card Power Good



FMC Card Power Good



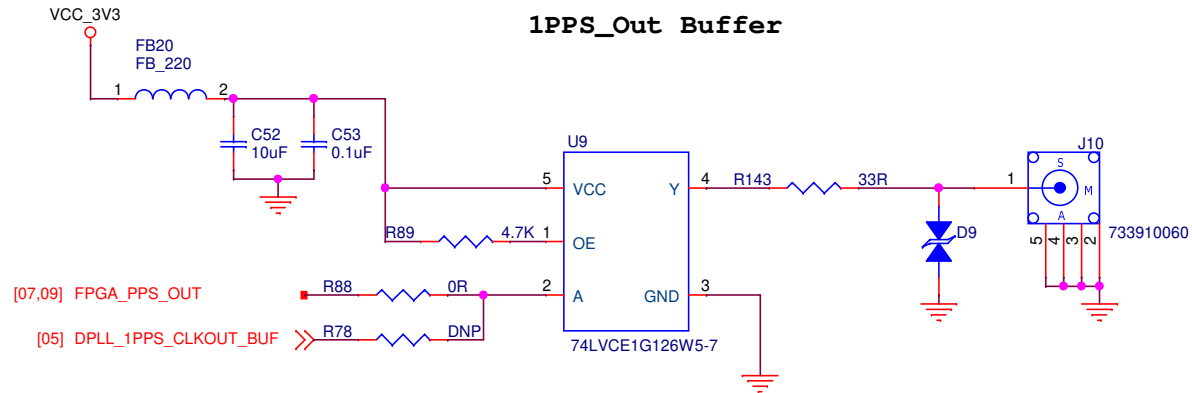
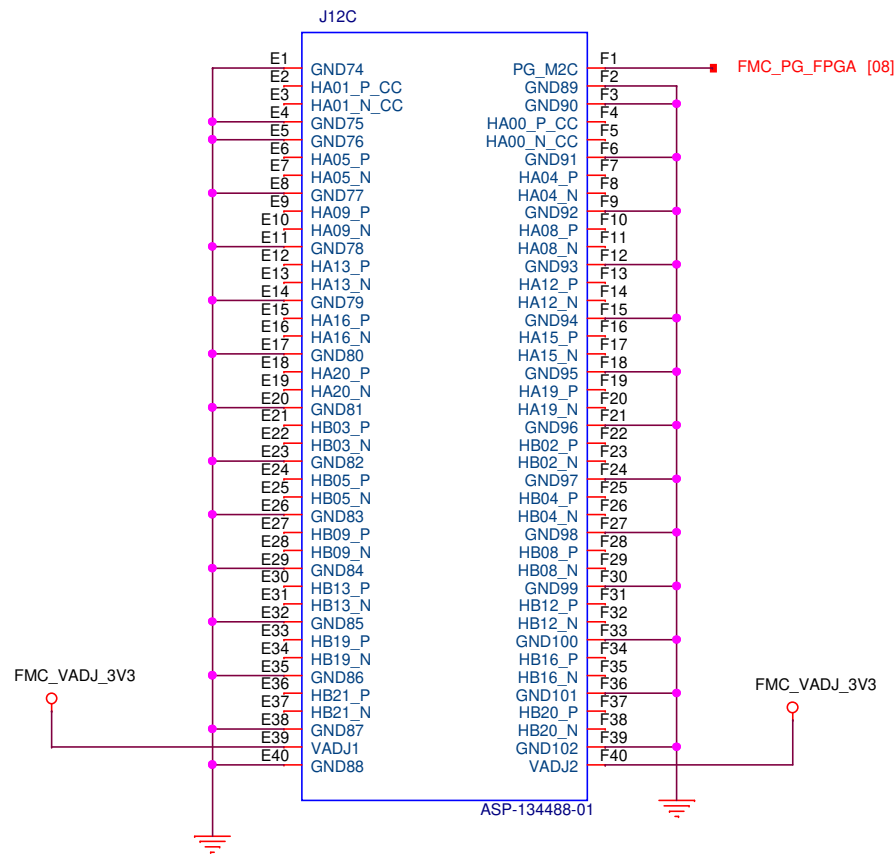
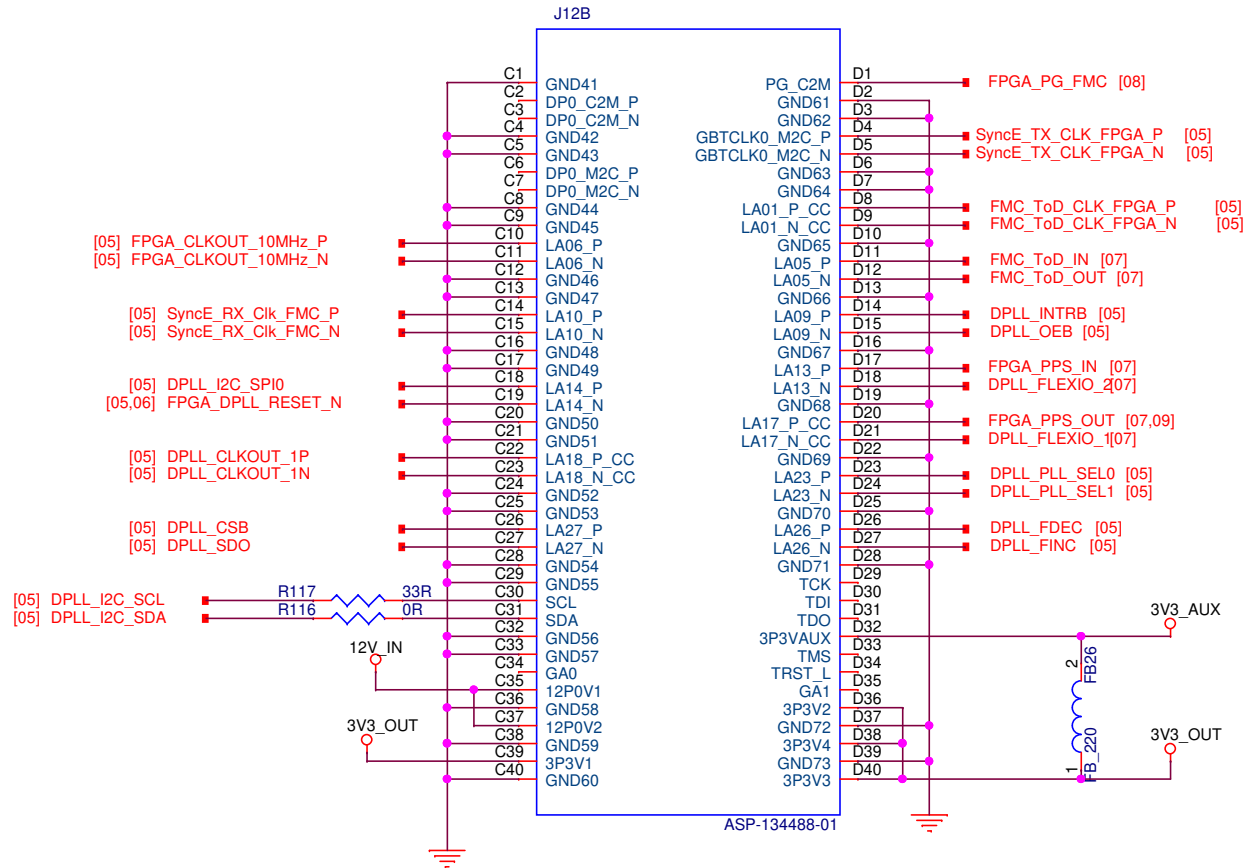
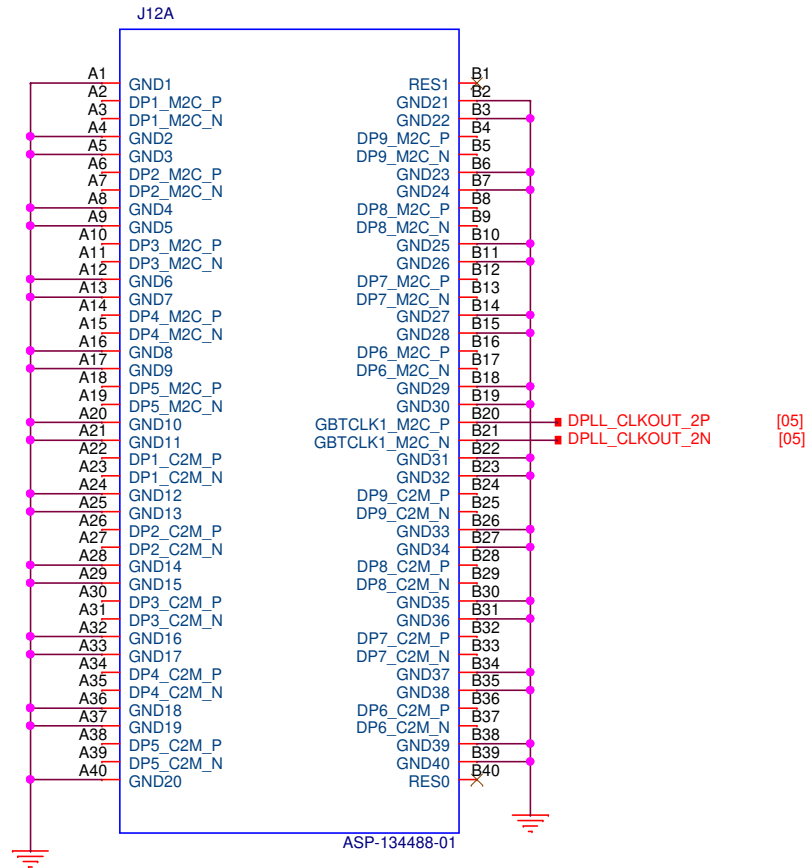
Carrier Card 12.0V & 3.3V PWR Indication Leds



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Title 08_POWER_3V3_1V8		
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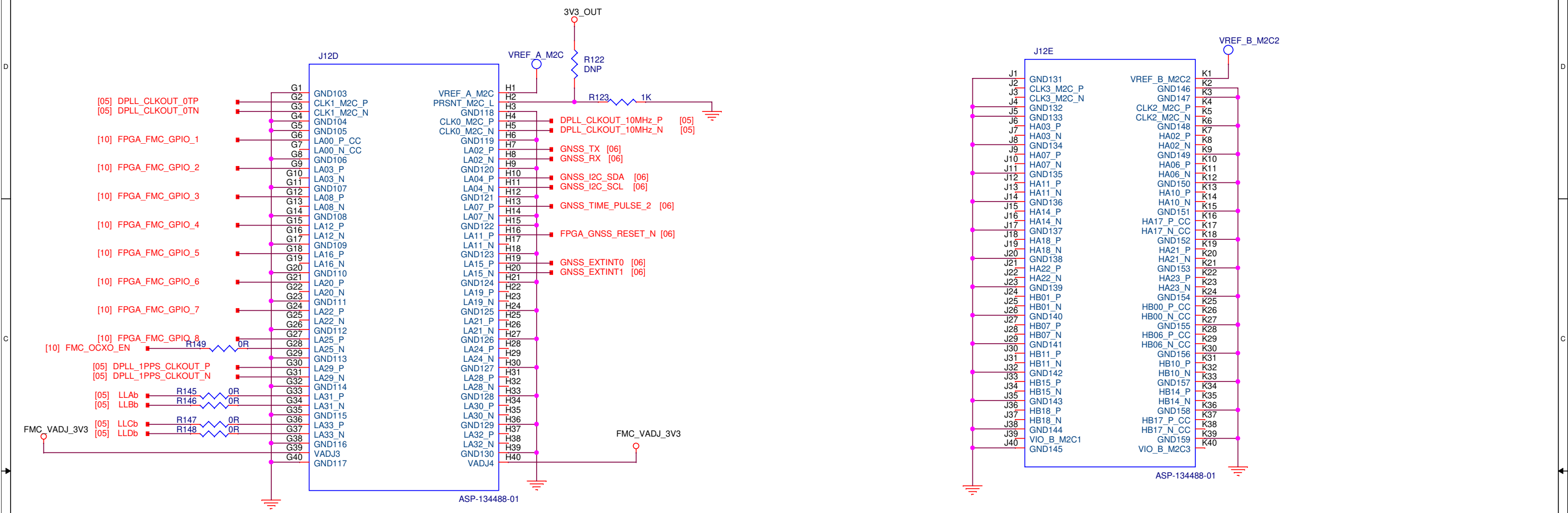
FMC Connector



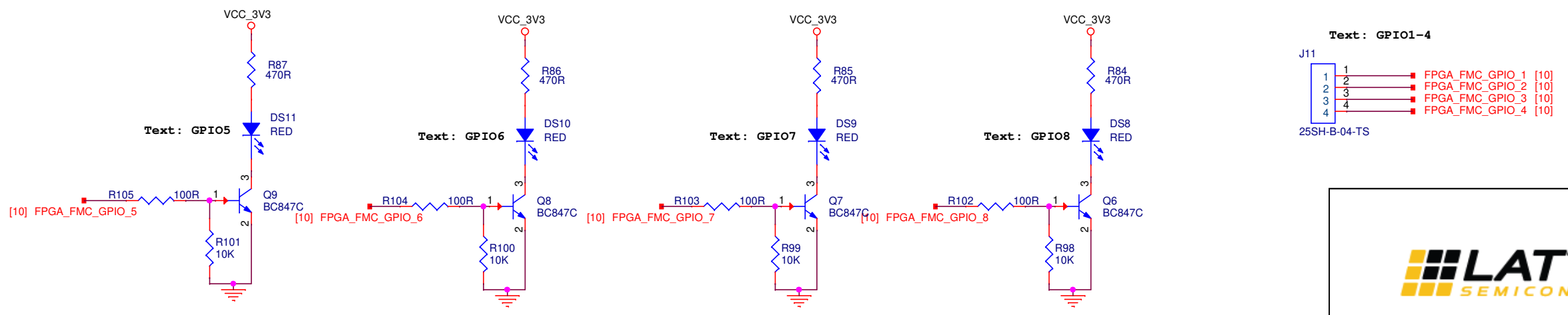
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Title 09_FMC_CONNECTOR_1			
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FMC Connector



GPIO Signals



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10_FMC_CONNECTOR_2			
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