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Title 01_Index		
Size A3	Project PTP_MOTHER_BOARD	Schematic Rev v2.1 Board Rev B
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Revision\_record

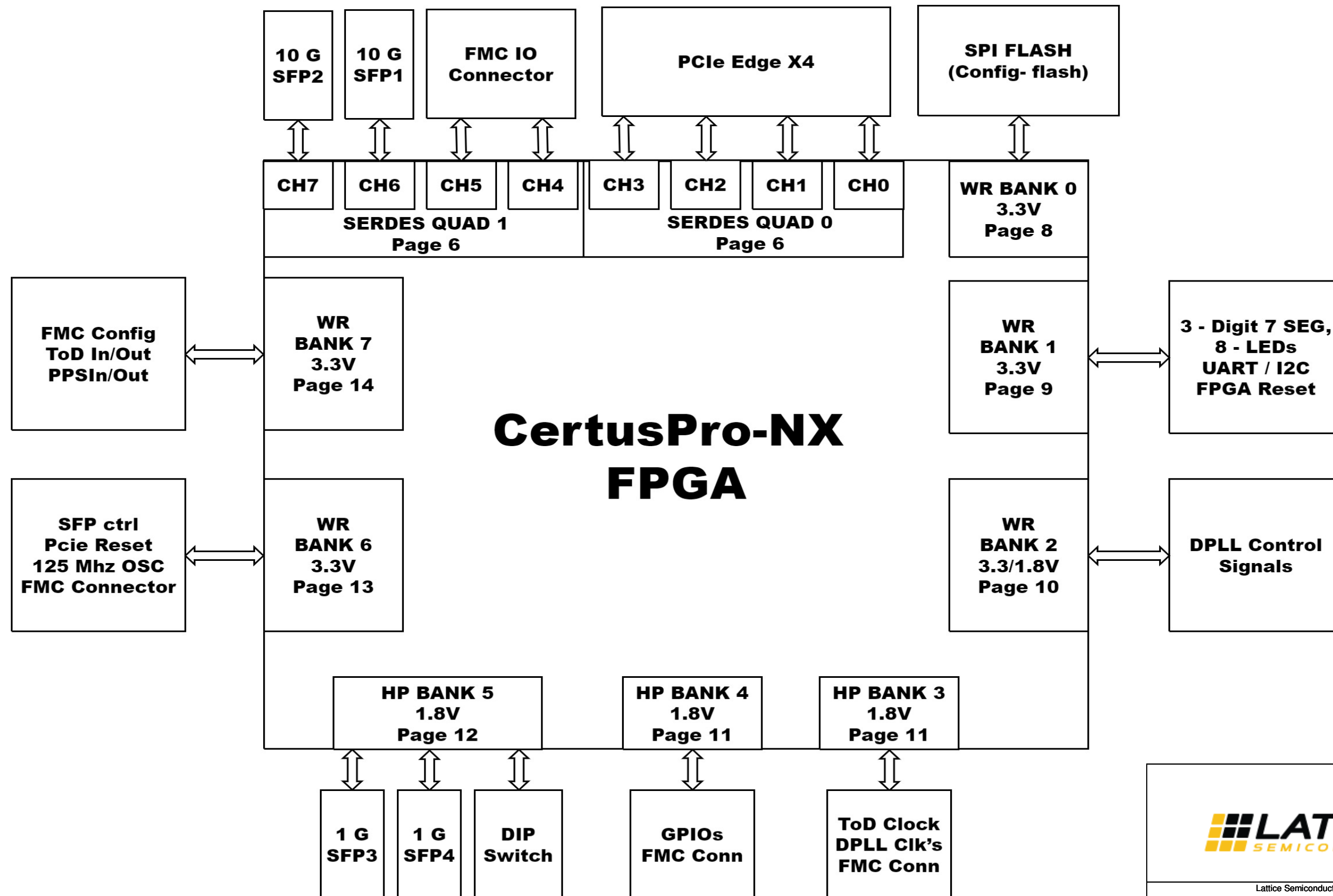
Revision	Date	Description of change	Author
v1.0	June 21, 2022	First Release	
v2.0	Jan 24, 2023	Added control signals for DPLL status  Renamed DPLL output signals (FMC_ToD & OUT7_P/N)  Moved 1G SFP Port0 RX signal to CDR pins	
v2.1	Jul 25, 2023	Renamed DPLL Output and Input signals as per application  Added PROGRAMN pin to FPGA GPIO on Bank7  Added DPLL Loss of Lock and FLEXIO signals to FPGA	



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Title 02_Title_Block			
Size A3	Project PTP_MOTHER_BOARD	Schematic Rev v2.1	Board Rev B
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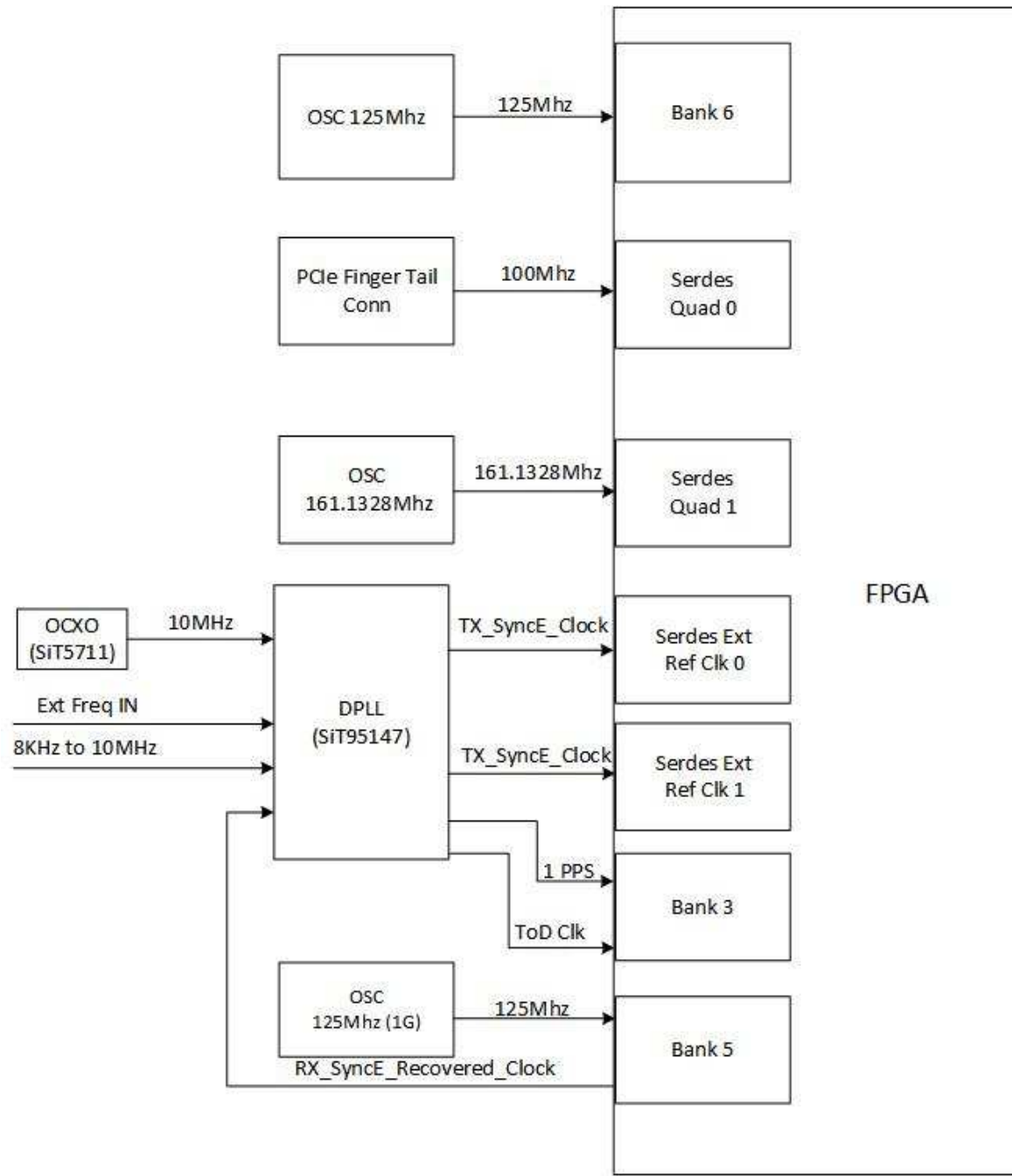
# BLOCK DIAGRAM



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Title 03_Block-Diagram		
Size A3	Project PTP_MOTHER_BOARD	Schematic Rev v2.1
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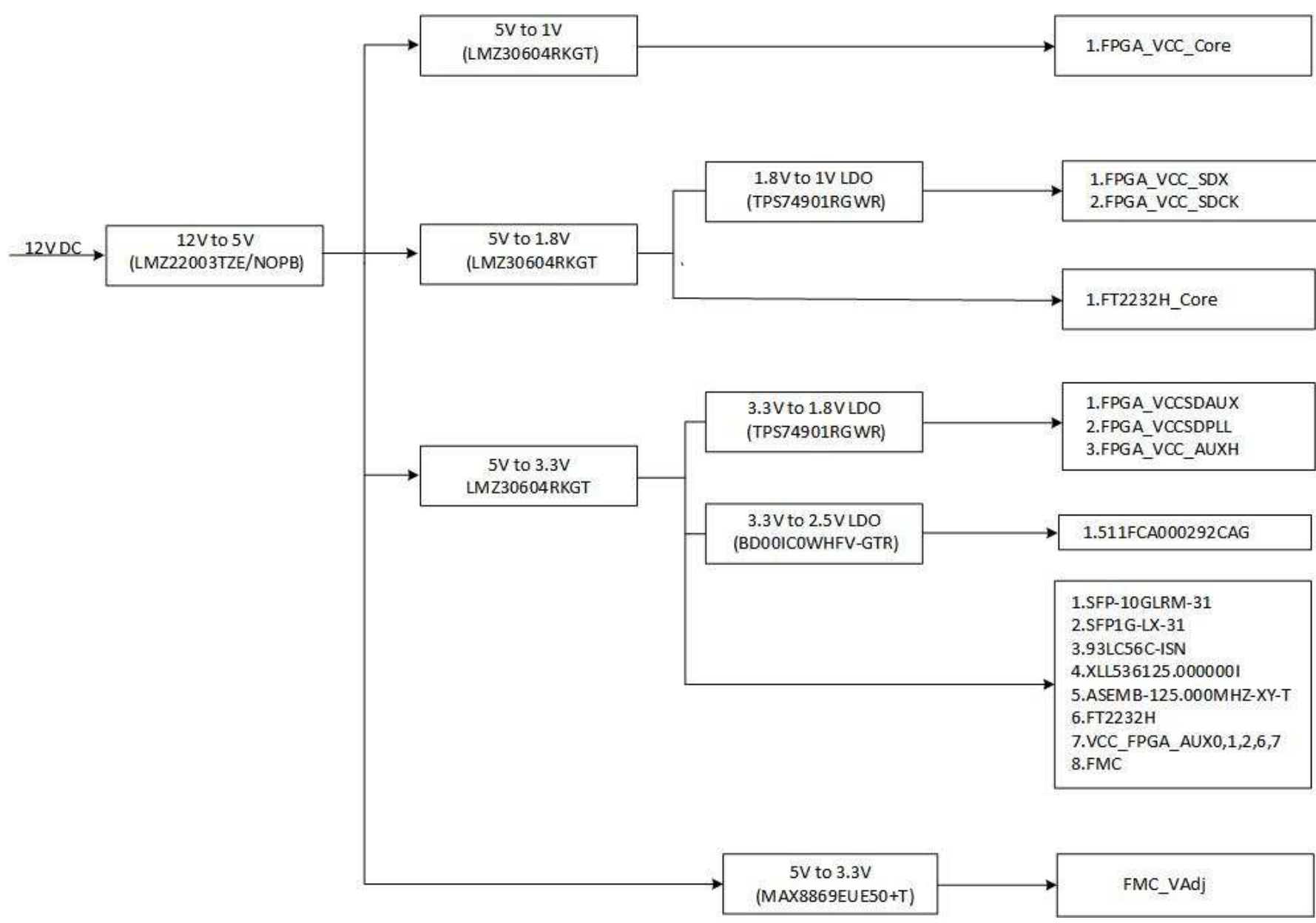
# Clock\_Tree




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Title			
04_Clock_Tree			
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		Board Rev B	
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# PWR Tree

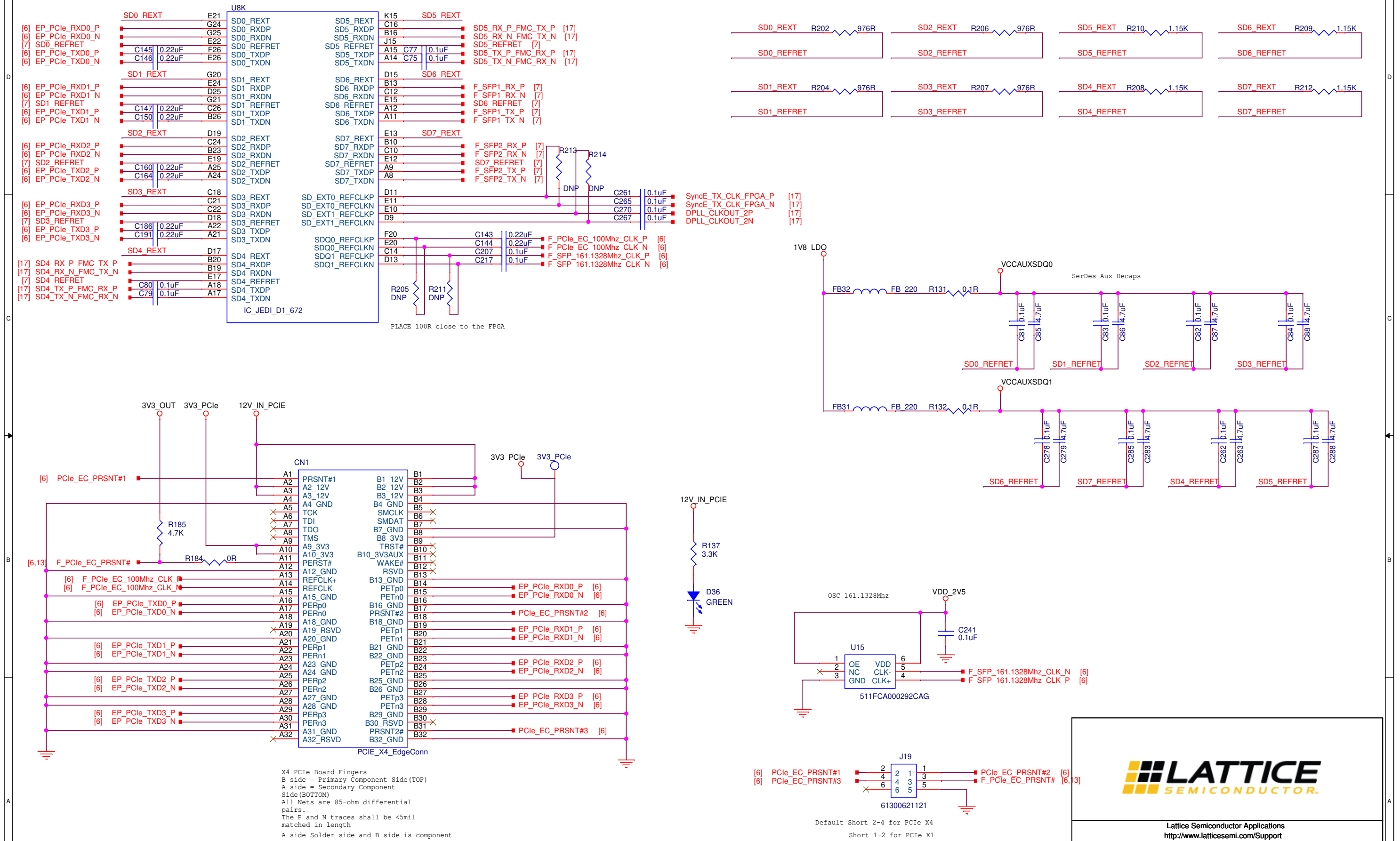




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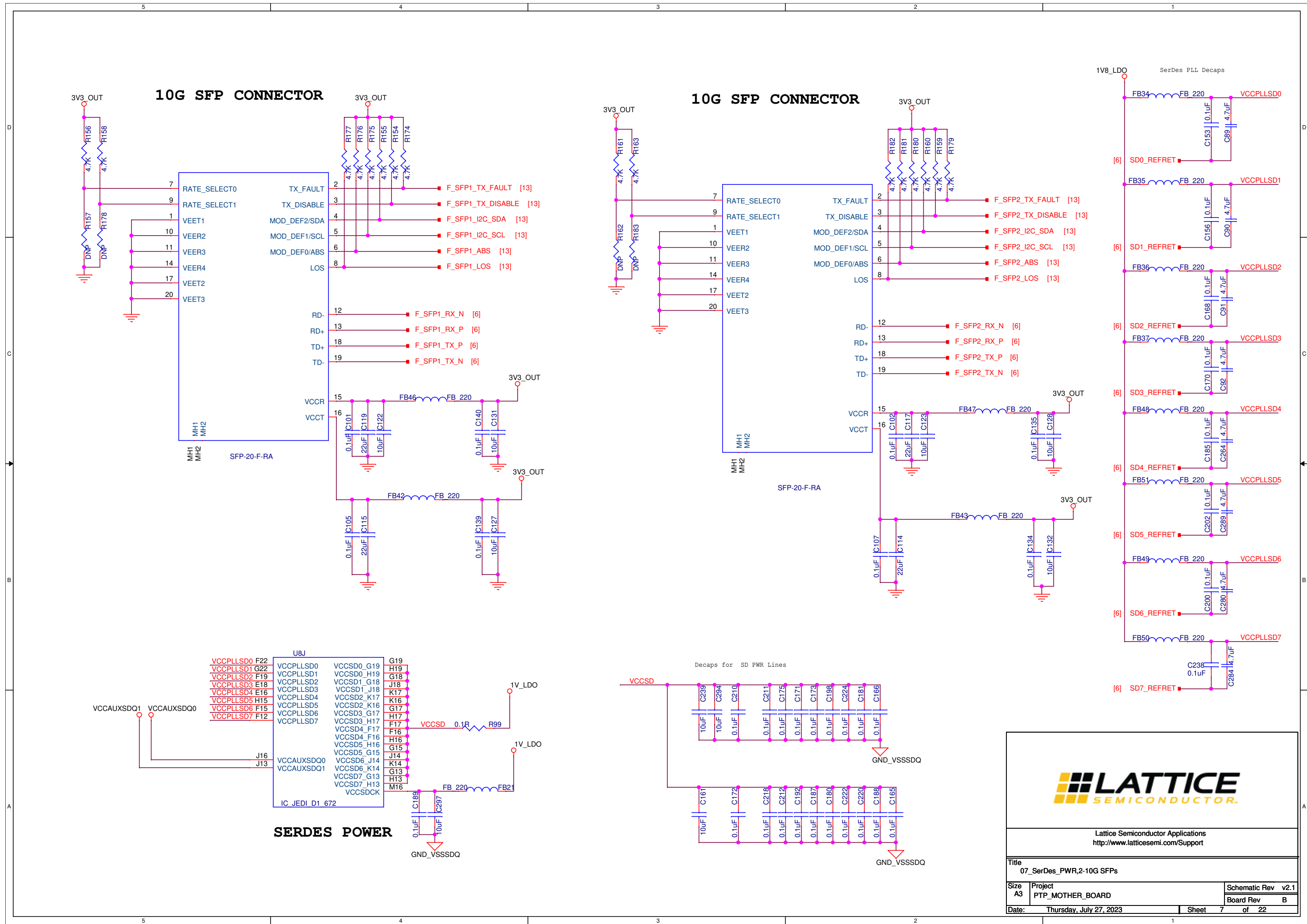
Title 05_PWR_Tree		
Size A3	Project PTP_MOTHER_BOARD	Schematic Rev v2.1
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## SERDES QUADS, PCIe EDGE Connector

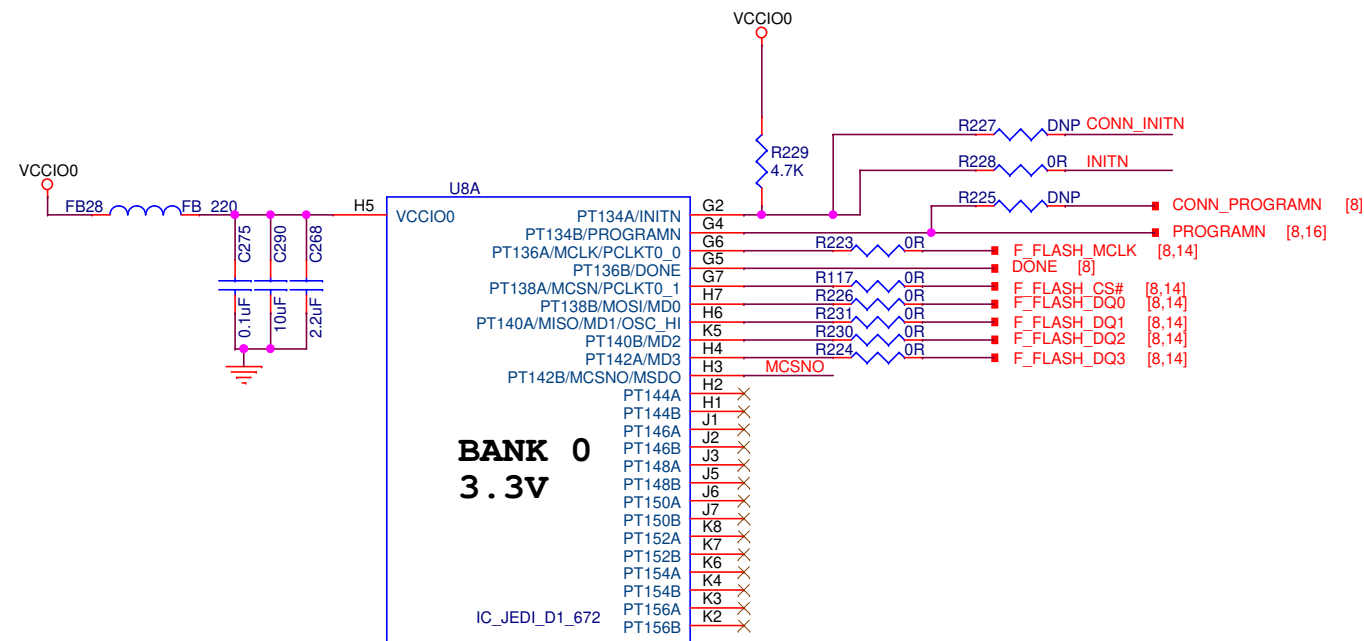


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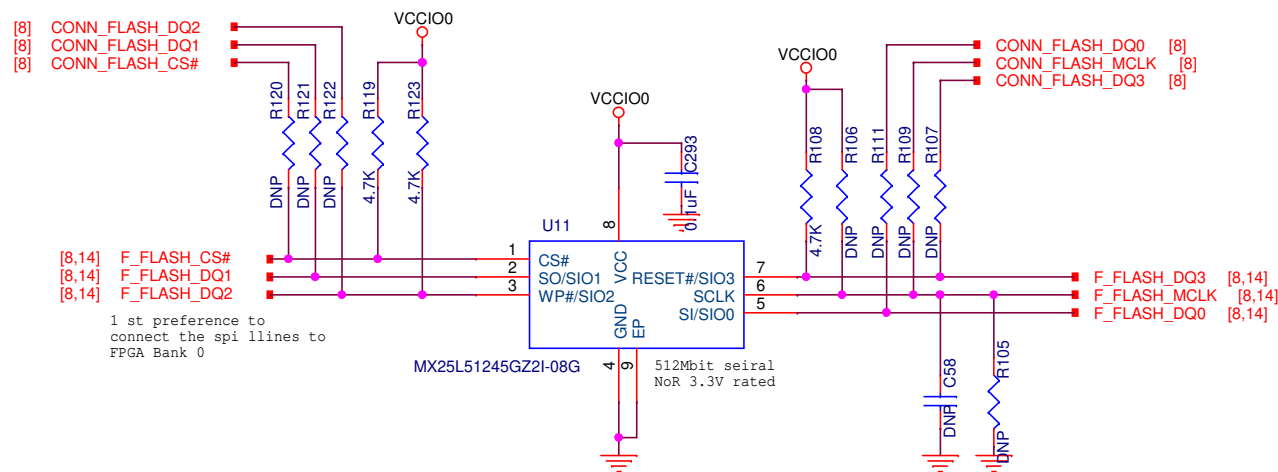
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06_FPGA_SerDes-PCle			
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		Board Rev	B
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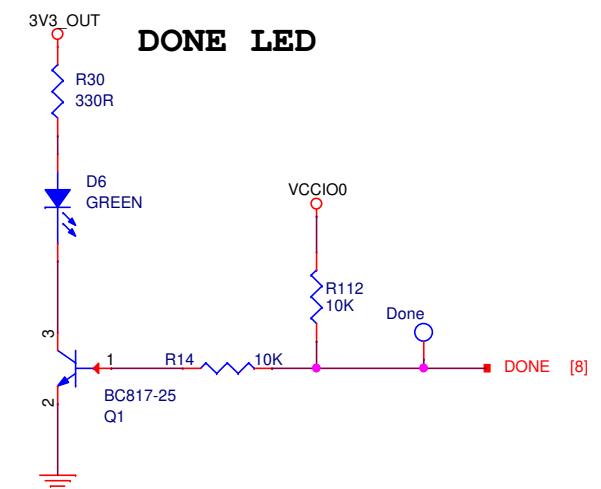
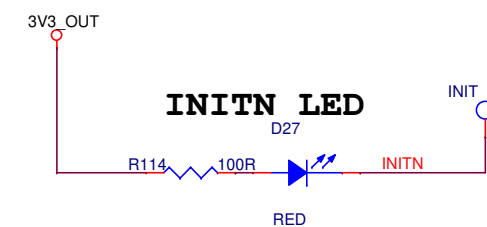
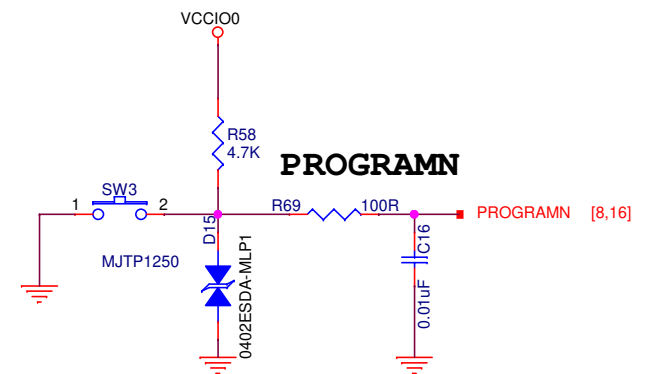
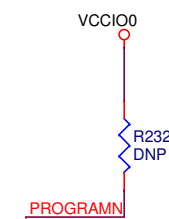
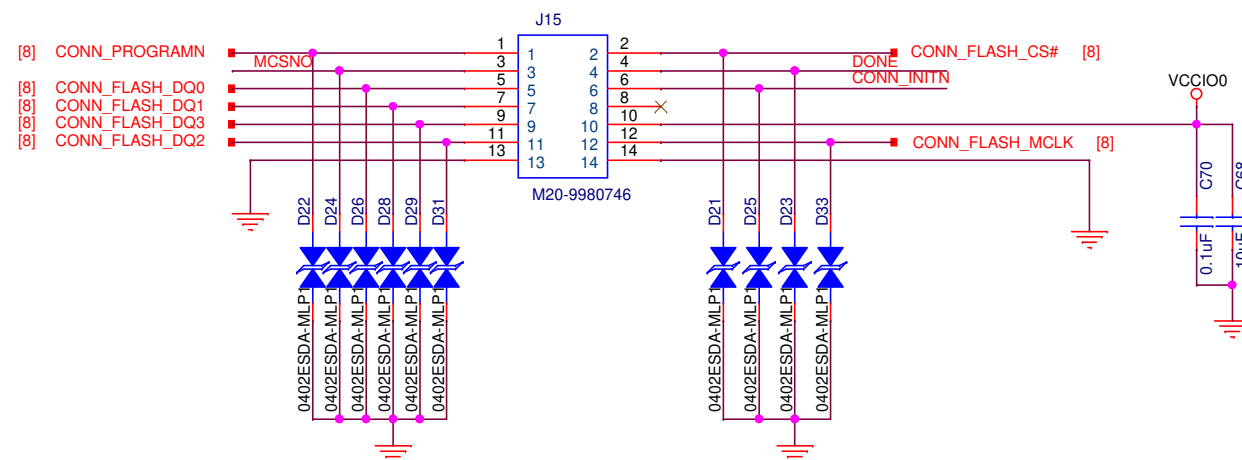




### SPI Boot FLASH



### Parallel / SPI Config Header

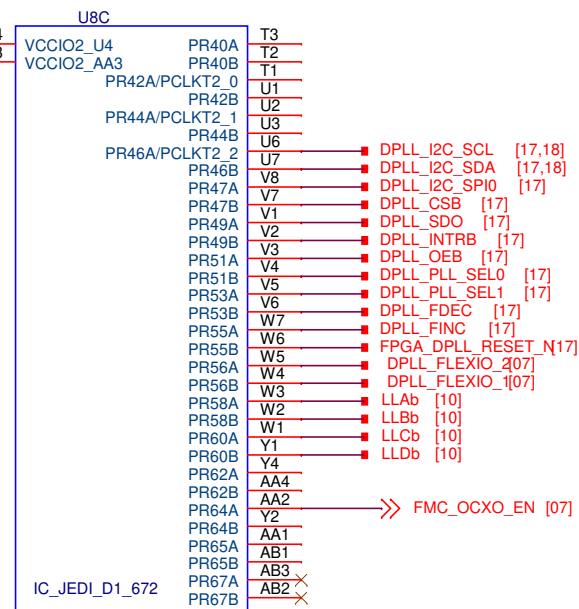
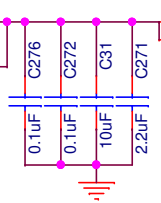
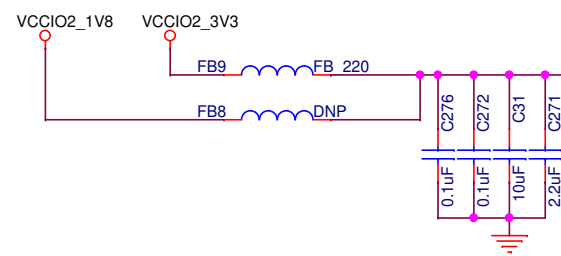
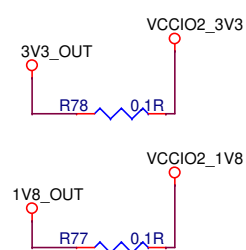


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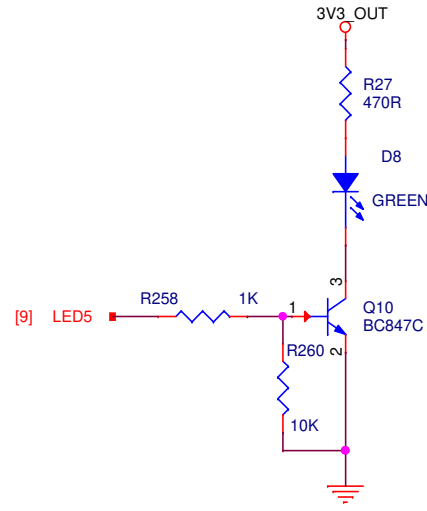
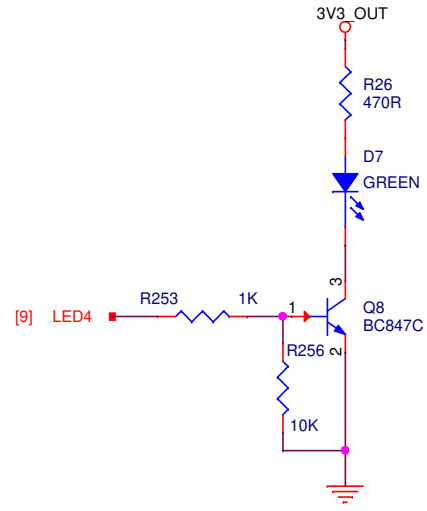
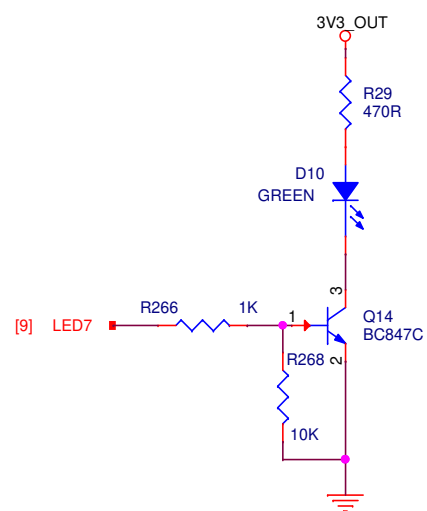
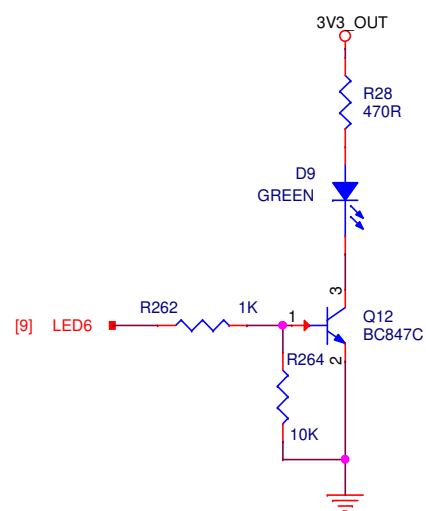
Title 08_FPGA_B0-Config		
Size A3	Project PTP_MOTHER_BOARD	Schematic Rev v2.1
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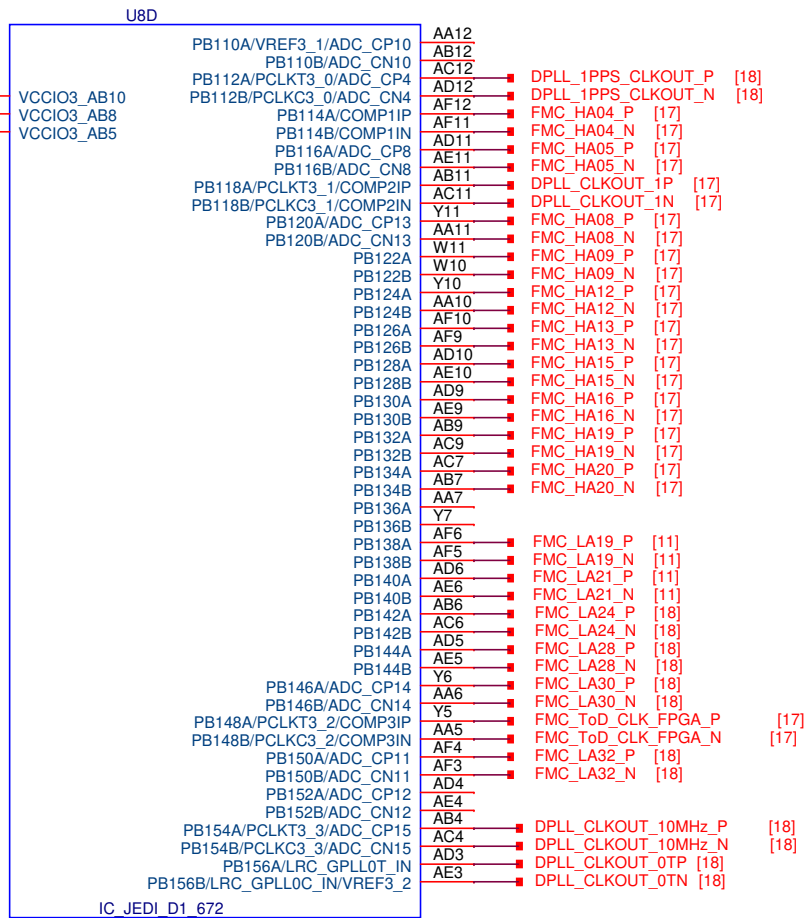
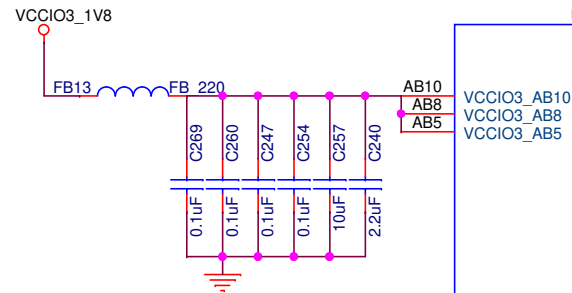


## BANK 2 3.3V/1.8V

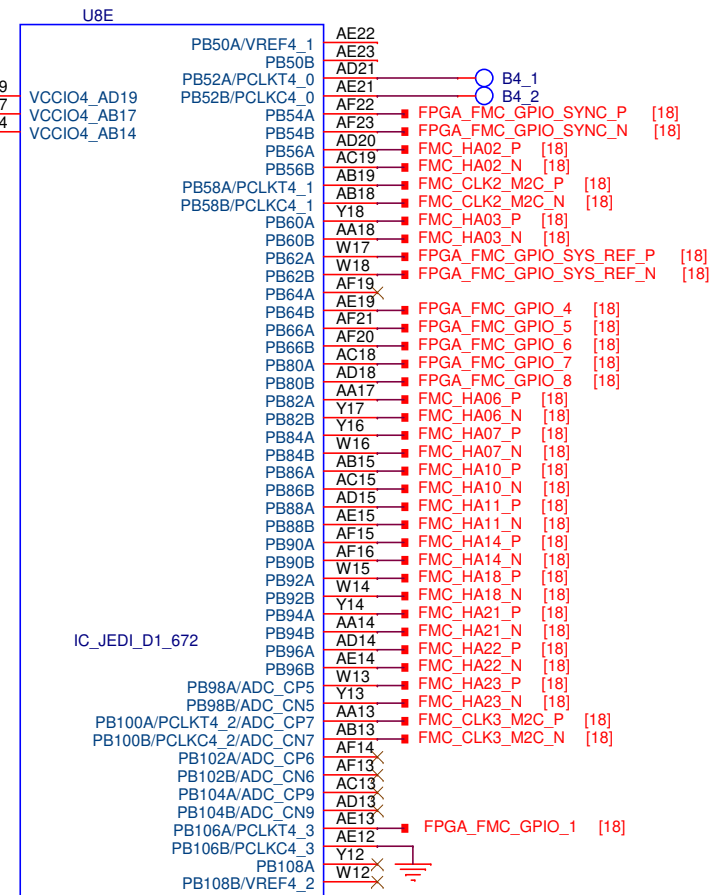
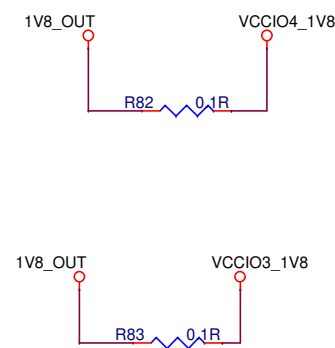
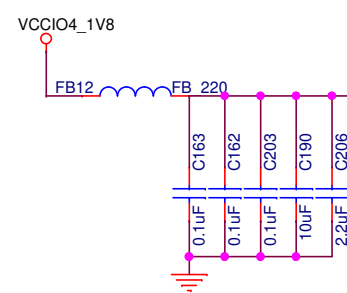


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Title 10_FPGA_B2-WR_Header		
Size A3	Project PTP_MOTHER_BOARD	Schematic Rev v2.1 Board Rev B
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**BANK 3**  
**1.8V**

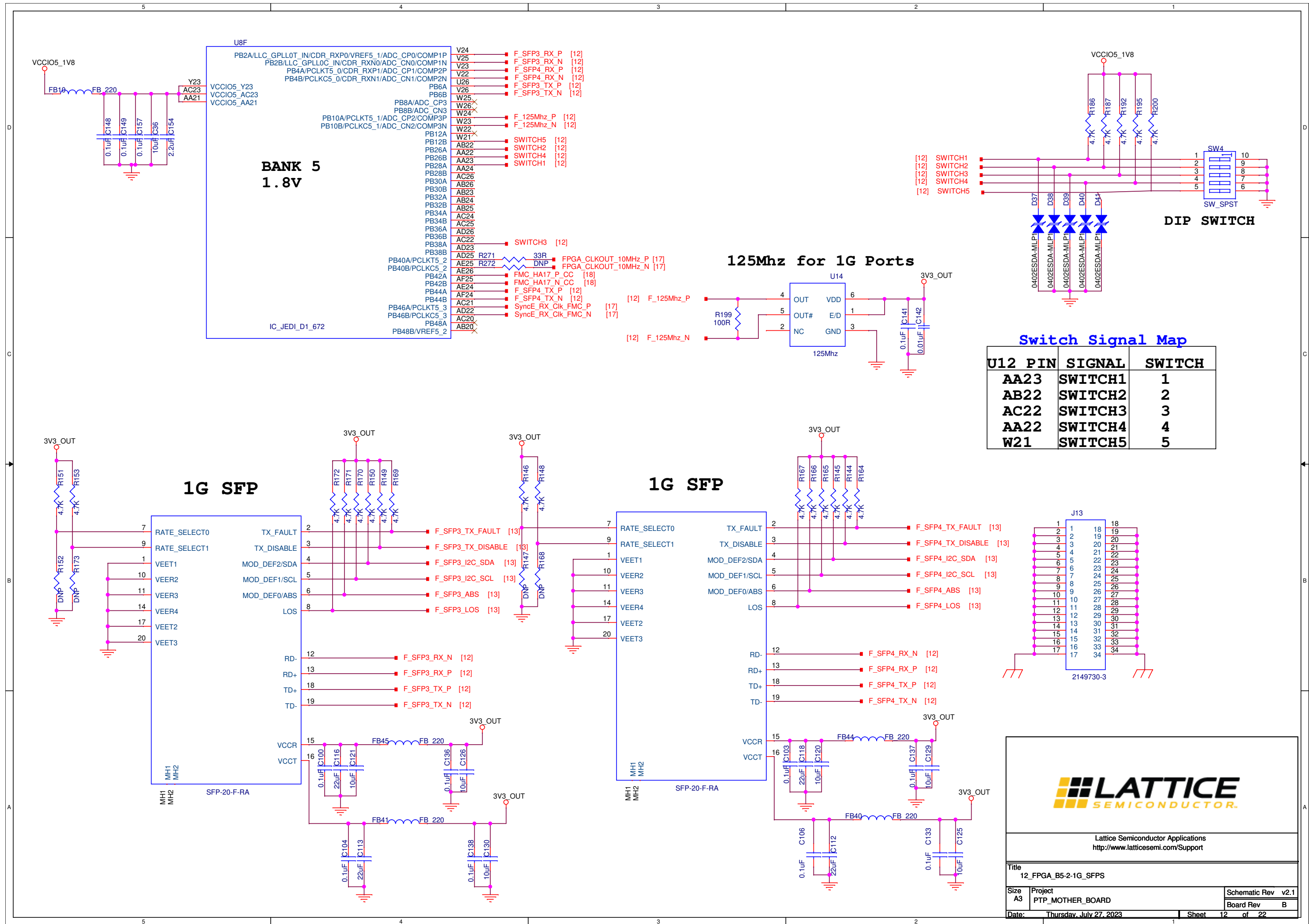


**BANK 4**  
**1.8V**

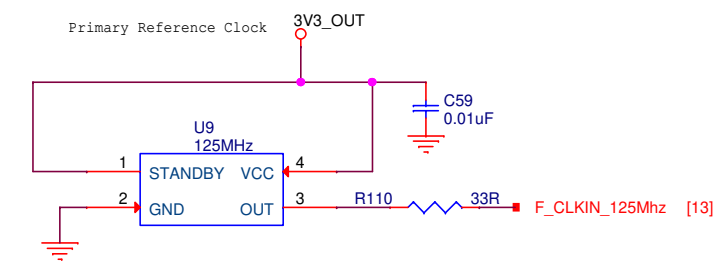
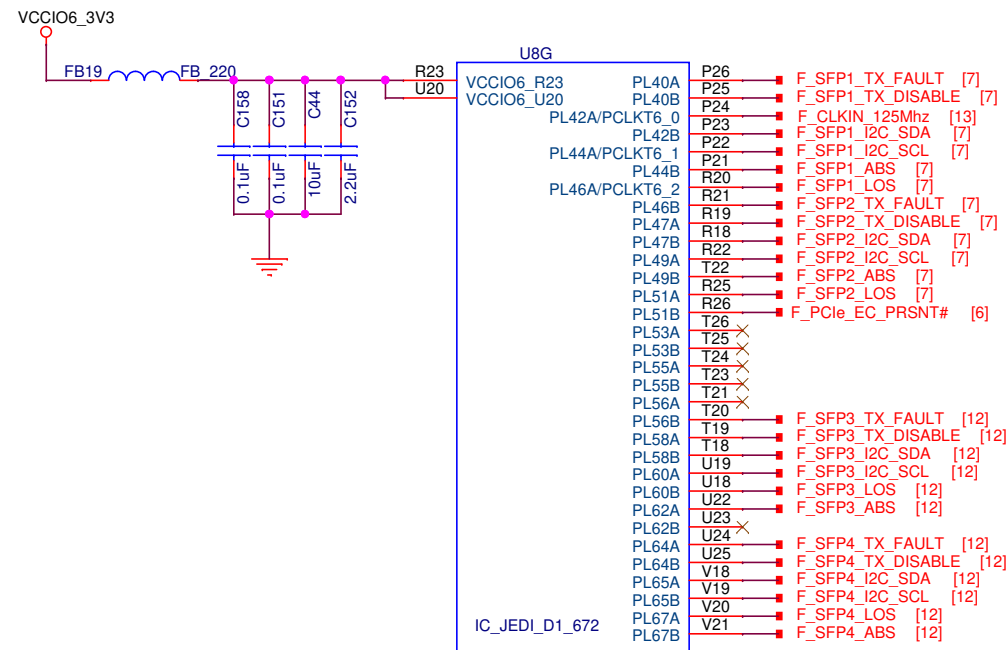


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Title 11_FPGA_B3_B4-FMC		
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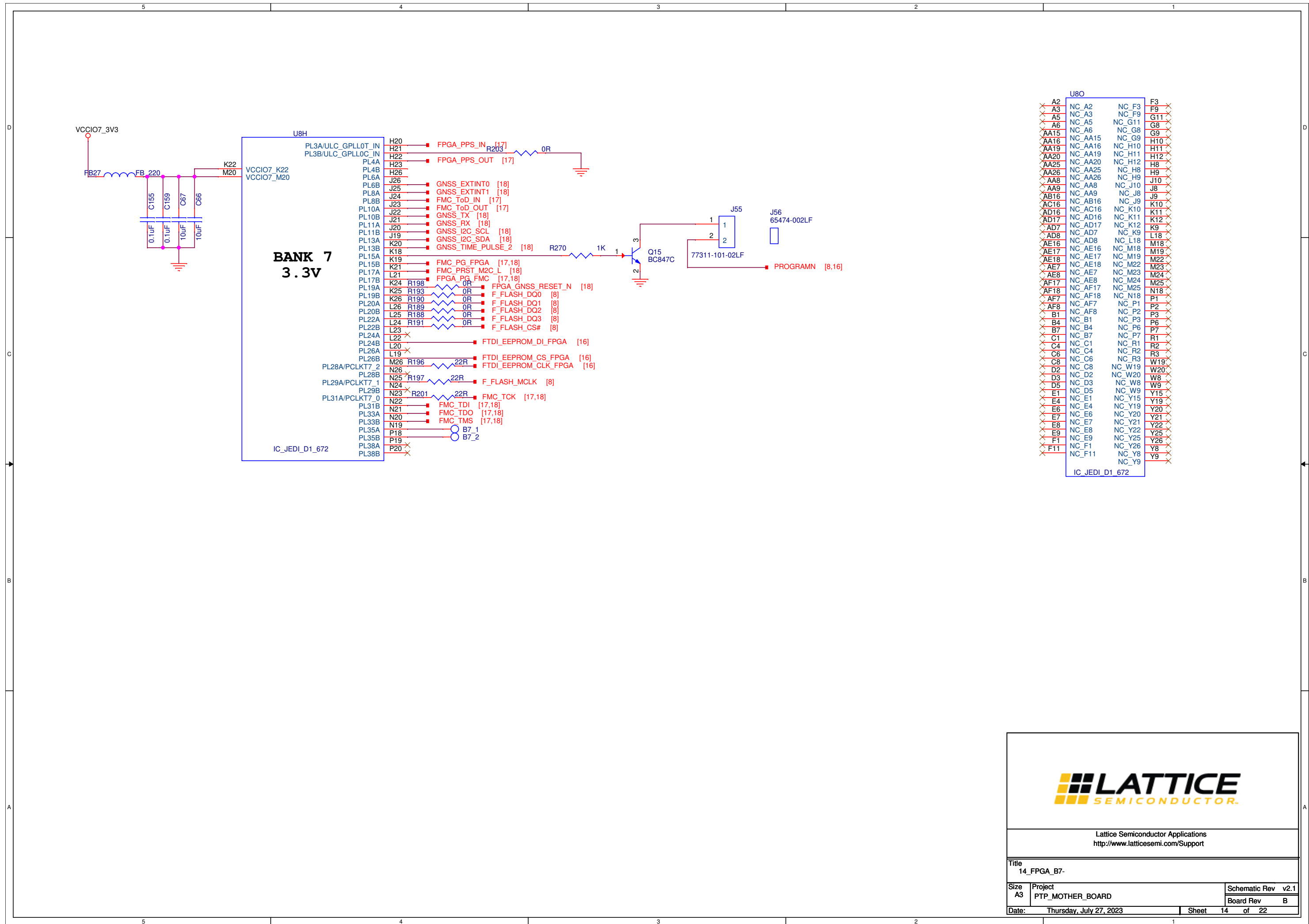


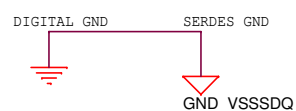
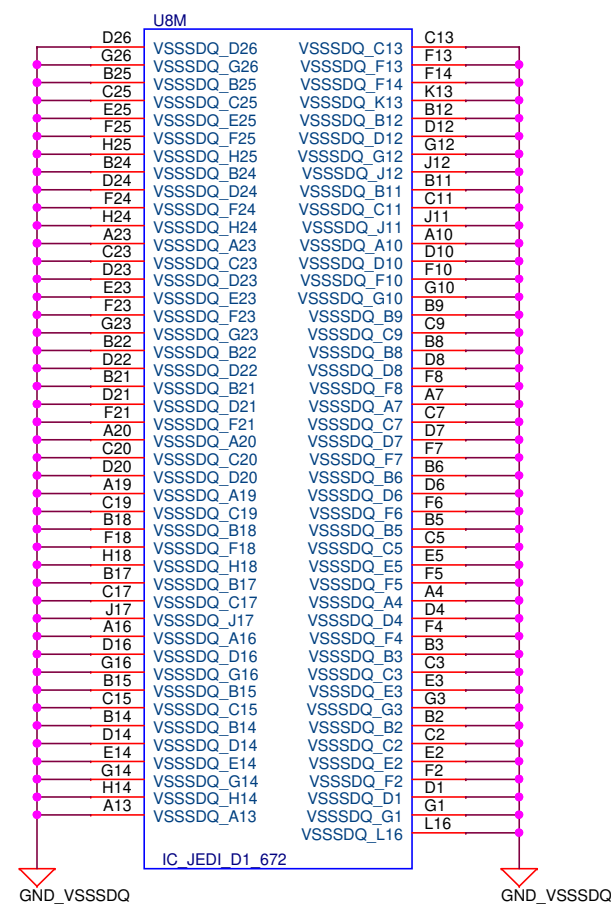
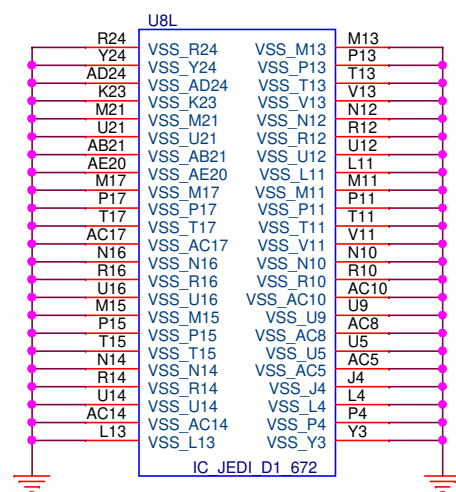
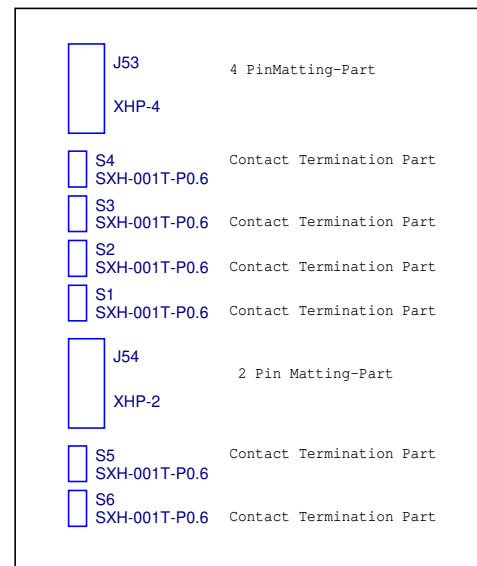
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Title 13_FPGA_B6-SFPS_Ctrl		
Size A3	Project PTP_MOTHER_BOARD	Schematic Rev v2.1
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Title  
15\_FPGA\_ADC

Size  
A3

Project
PTP_MOTHER_BOARD

Schematic Rev	v2.1
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Board Rev	B
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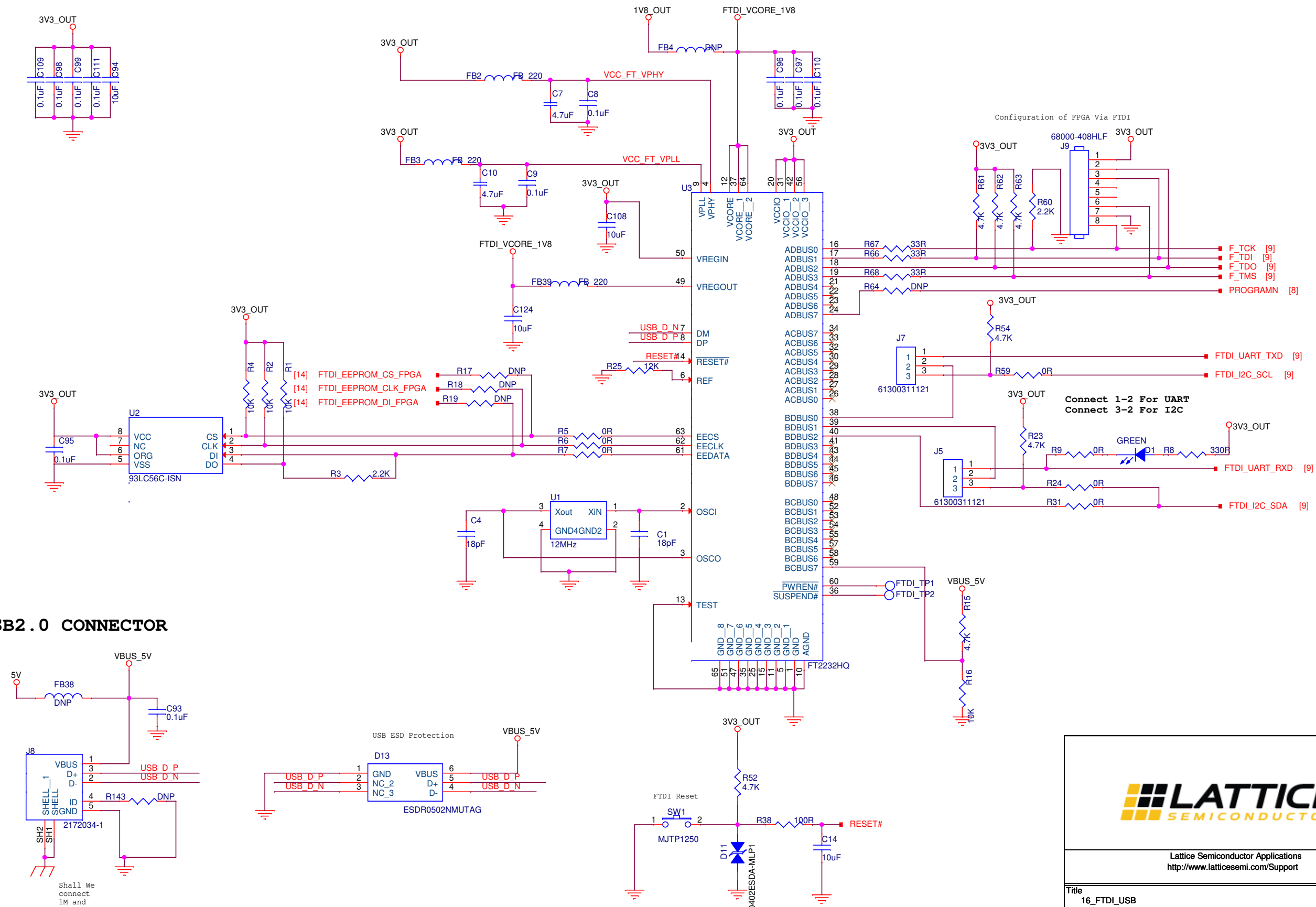
Date: Thursday, July 27, 2023

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# FTDI High-Speed USB

## USB2.0 CONNECTOR

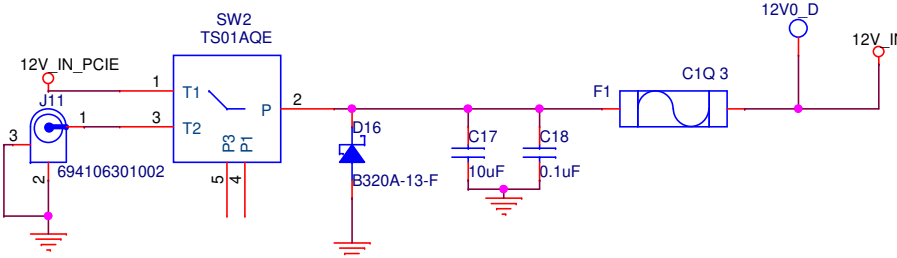




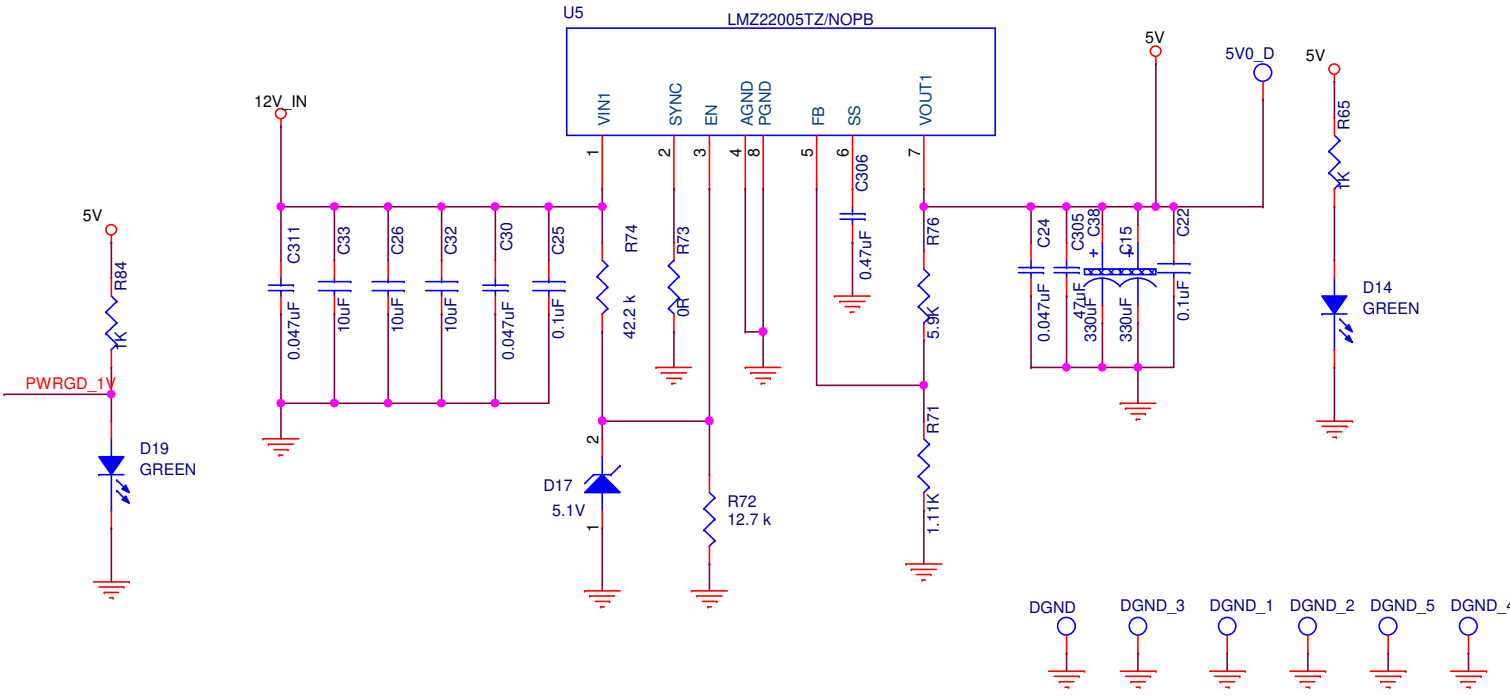


# Power Regulators

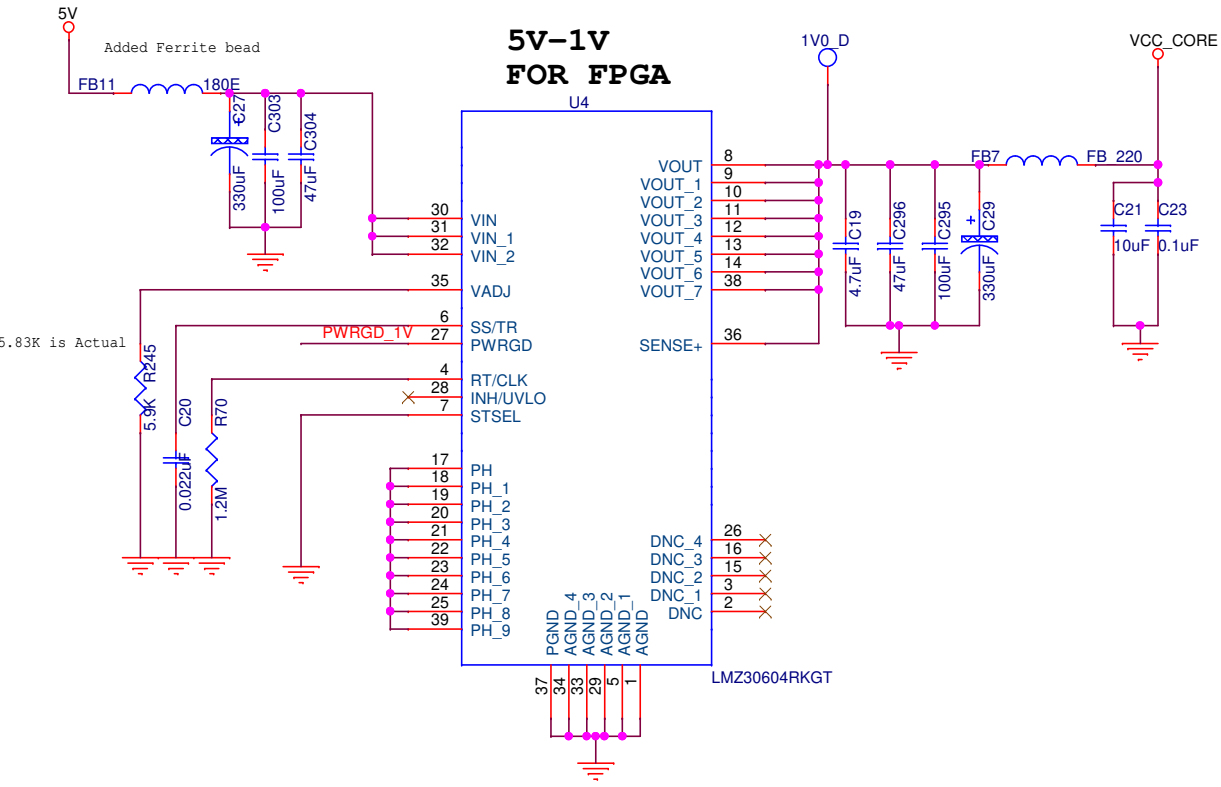
## 12V INPUT



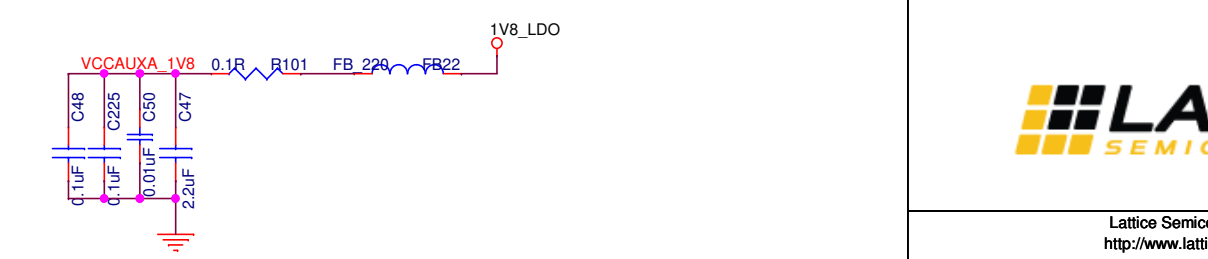
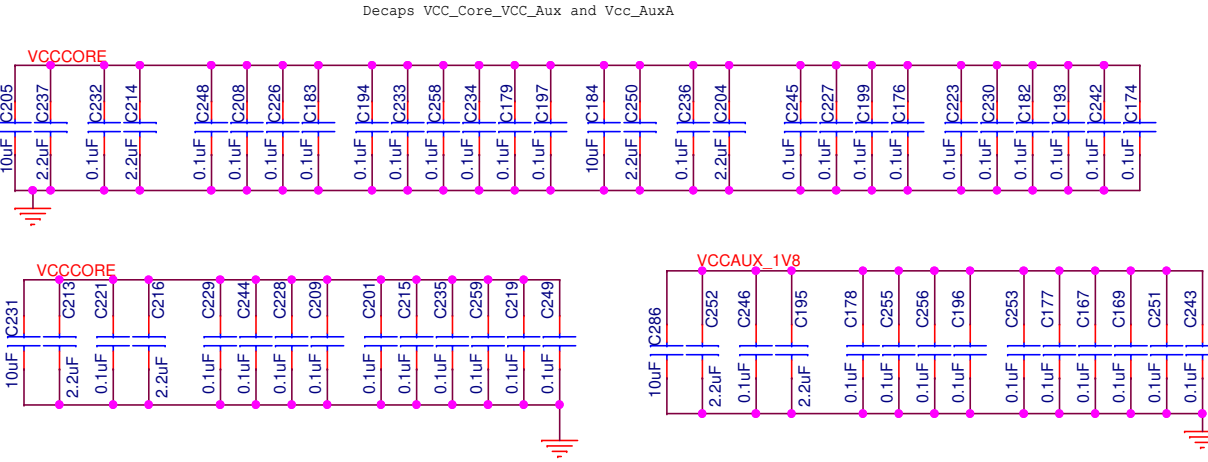
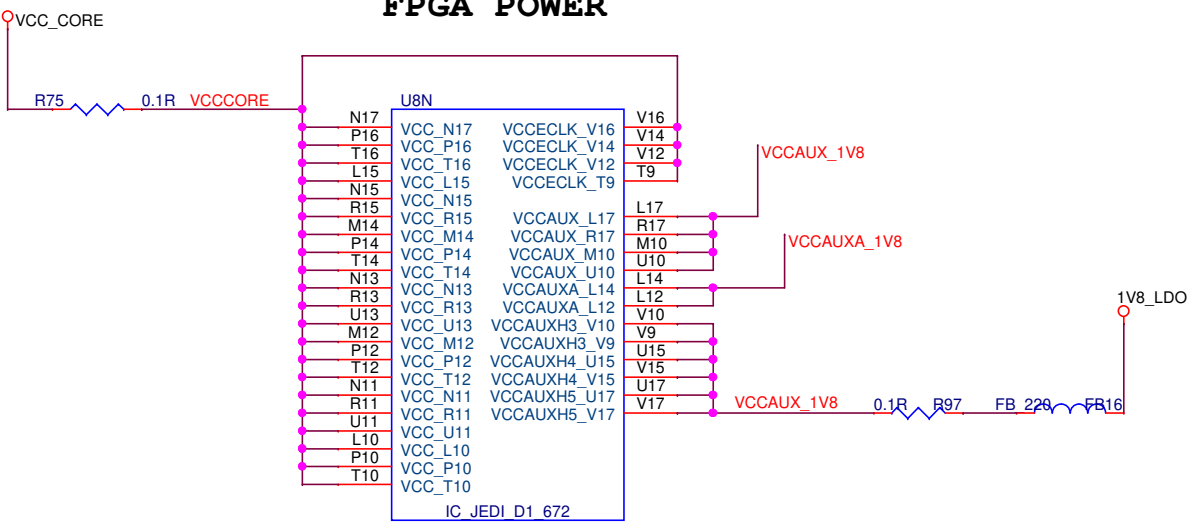
## 12V-5V



## 5V-1V FOR FPGA

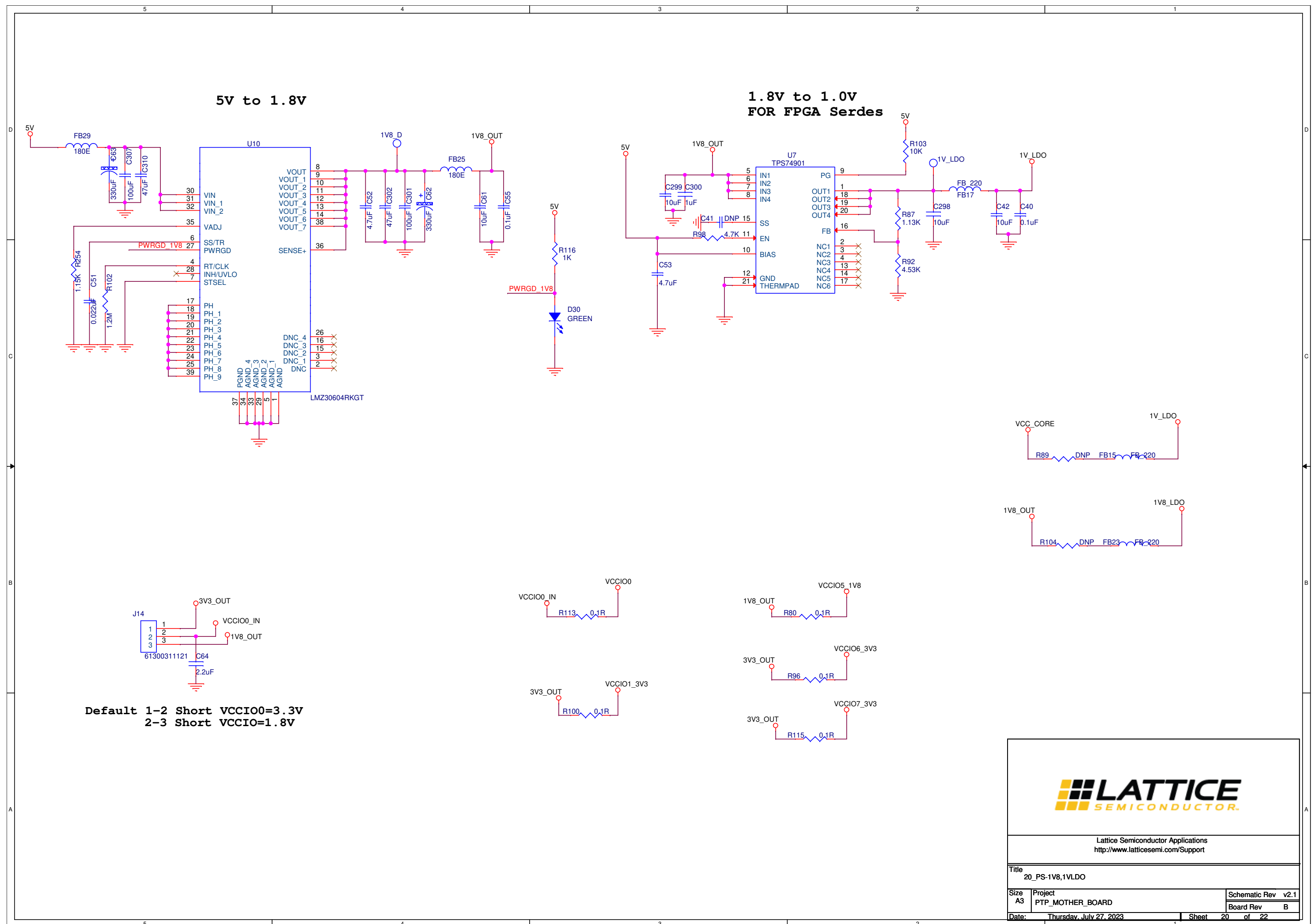


## FPGA POWER



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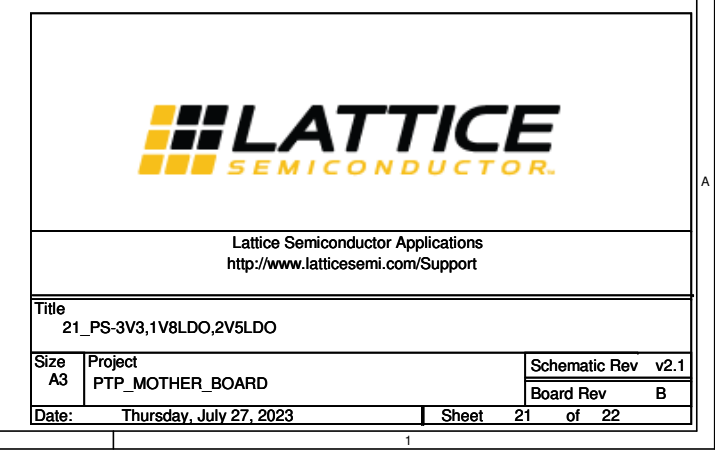
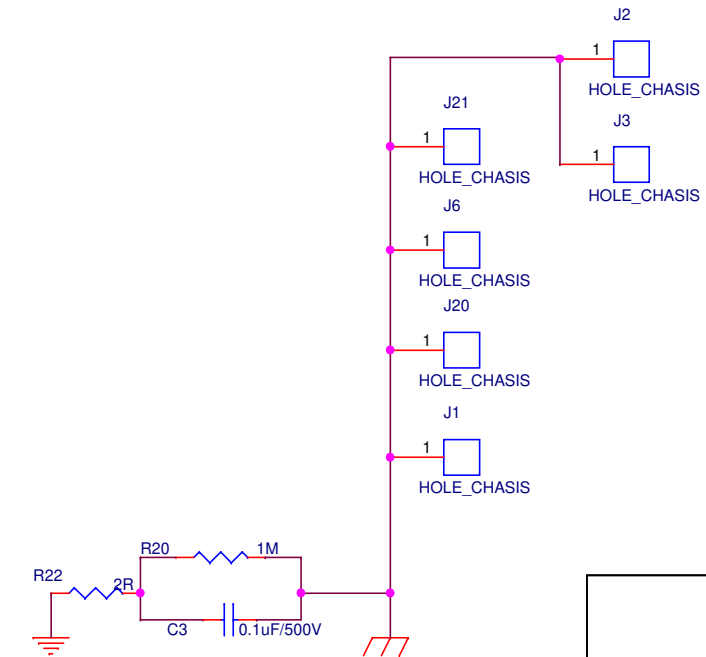
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Size A3	Project PTP_MOTHER_BOARD	Schematic Rev v2.1
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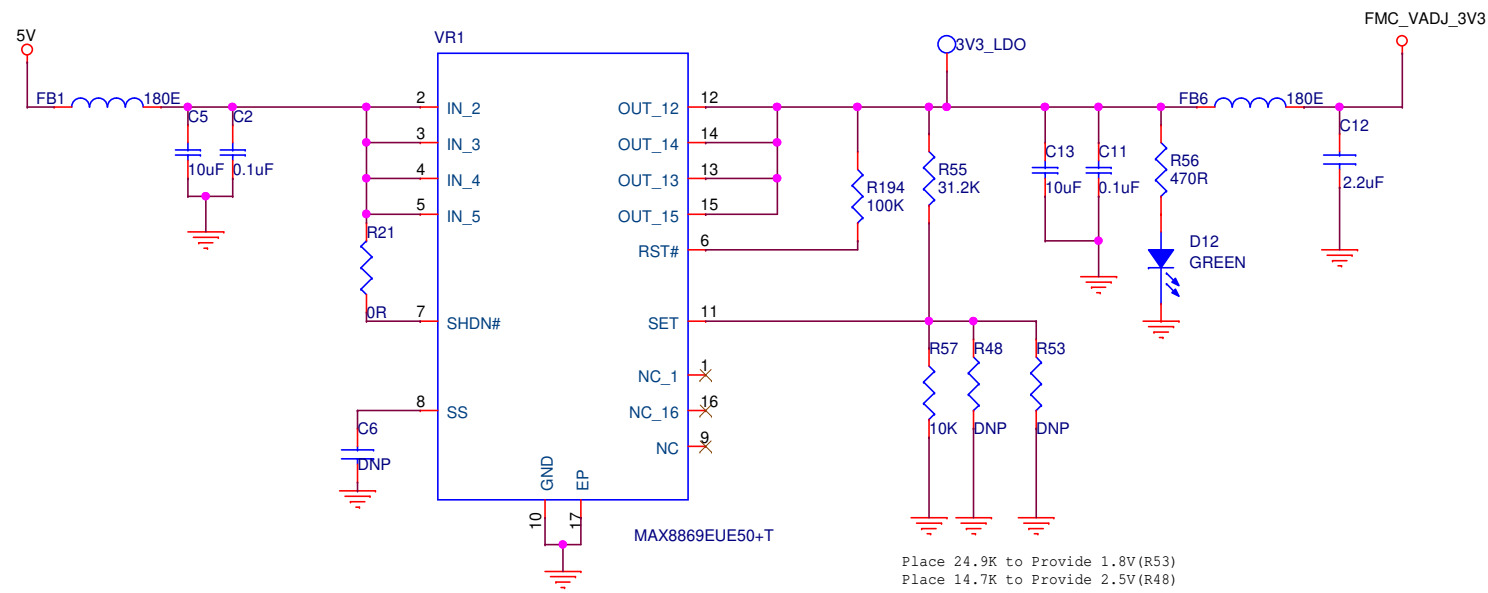


The schematic diagram illustrates the TPS74901 voltage regulator circuit. The input is a 5V supply connected to the IN1 pin of the TPS74901 (U6). The output of the regulator is 3V3\_OUT, which is connected to the 3V3\_LDO output. The 3V3\_OUT is also connected to the 1V8\_LDO output. The circuit includes several components: a 4.7uF capacitor (C35) at the input, a 180E resistor (R85) at the output, a 3.57K resistor (R91) at the feedback, a 10K resistor (R90) at the 1V8\_LDO output, and a 100R resistor (R95) at the 3V3\_OUT output. The TPS74901 is configured with its PG pin to ground, OUT1 to 3V3\_OUT, OUT2 to 1V8\_LDO, OUT3 to 3V3\_OUT, and OUT4 to 1V8\_LDO. The SS pin is connected to ground, and the EN pin is connected to the 3V3\_OUT. The BIAS pin is connected to ground, and the GND THERMPAD pin is connected to ground. The circuit is powered by a 5V source and regulated to 3V3 and 1V8 outputs.

A vertical bar divided into two sections. The top section is labeled 'B' and the bottom section is labeled 'A'.



# 5V to 3.3V



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Title 22_PS-FMC_3V3_LDO		
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