Lattice Radiant 2023.2.1 Software Release Notes

Welcome to Lattice Radiant™ software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs).

What's New in Radiant 2023.2.1 Software

- **Device Support:**
  - CertusPro™-NX (LFCPNX)
    - 50K (-9/-8/-7) 1.0V (AUTO) – ASG256, CBG256, BFG484.

Tool and Other Enhancements:

- **Primitives**
  - OUTDELAYC primitive has been added for CertusPro-NX device.

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- **Device Constraint Editor**
  - 75Mhz selection has been added for MCCLK_FREQ.
- **MAP** – DRC errors regarding shared configuration pin usage for Nexus devices have been resolved.
- **Timing Data** – DPHY timing arcs to fix unconstrained path have been updated for Nexus device.

- **Reveal**
  - JTAGhub feature modules have been enhanced for Nexus and Avant devices.
  - Pooling of data while SEDC is running has been enhanced for Reveal Controller and Reveal Analyzer.
- **Hardware Data File**
  - Minimum pulse width (MPW) has been aligned with datasheet for CrossLink-NX device.
  - Correlation for CertusPro-NX (LFCPNX) IBIS Model has been resolved.

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Radiant software, it may be necessary to re-create some IP, per the procedures described in the following table.

These procedures adapt the project for the changes in Radiant software.

Versions	IP			IP Regeneration Procedures
	Avant (LAV-AT-E)	**CrossLink-NX (LIFCL), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP), MachXO5-NX (LFMXO5)**	**iCE40UP**	
2023.2.1	RAM_DQ	MPCS	N/A	These IP used in designs created in Radiant 2023.2 or earlier must be re-generated in Radiant 2023.2.1
	RAM_DP	RAM_DQ		
	RAM_DP_True	RAM_DP		
	ROM	RAM_DP_True		
	FIFO	ROM		
	FIFO_DC	FIFO		
		FIFO_DC		

The following server IP are not compatible with Radiant 3.0 onwards. Use the latest versions of the IP available on the IP server:

- I2C Master version 1.0.3
- UART 16550 version 1.0.4
- DDR3 SDRAM Controller version 1.1.1
- DDR3 SDRAM Controller version 1.2.1
- LPDDR2 SDRAM Controller Lite version 1.1.1
- LPDDR2 SDRAM Controller Lite version 1.2.1

Supported Devices

Lattice Radiant software can be used with either a free license or a subscription license. The two licenses provide access to different device families.

Device Family	Free License	Subscription License
iCE40 UltraPlus™ (iCE40UP)	◄	
Lattice Avant™ (LAV-AT)		◄
CertusPro-NX (LFCPNX)	Evaluation Mode	◄
Certus-NX (LFD2NX)	◄	
MachXO5-NX (LFMXO5)	Evaluation Mode	◄
CrossLink-NX (LIFCL)	◄	
Certus-NX-RT (UT24C)		RT Subscription
CertusPro-NX-RT (UT24CP)		RT Subscription

Support for Third-Party Synthesis and Simulator Tools

The Synopsys Synplify Pro® for Lattice synthesis tool and Siemens ModelSim® Lattice Edition simulator tools are included in the Radiant software.

- **Synopsys Synplify Pro FPGA synthesis software version U-2023.03LR-SP1**
  - Release Notes for Synplify Pro is located in

    ..\<*install_directory*>\radiant\2023.2\synpbase\doc\. The file name is release_notes.pdf.
  - A full set of documents for Synplify Pro is also located in ..\<*install_directory*>\radiant\2023.2\synpbase\doc\.
- **Siemens ModelSim Lattice Edition 2023.3 revision 2023.07**
  - Release Notes for ModelSim Lattice Edition are located in ...\<*install_directory*>\radiant\2023.2.\modeltech\. The file names are RELEASE_NOTES.html or RELEASE_NOTES.txt.

- A full set of documents for ModelSim Lattice Edition is located in ...\<*install_directory*>\radiant\2023.2\modeltech\doc\.

- **Siemens Questa® 2022.3**
- **Cadence Xcelium®**
  - The devices listed below are compatible with the following versions of Xcelium:
    - **23.03.003** – LAV-AT
    - **20.09.012 or earlier versions** – LFCPNX, LFD2NX, LFMXO5, LIFCL, UT24C, and UT24CP
- **Synopsys VCS® U-2023.03-SP2**

Help Resources

- Online Help updated with CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP), and Lattice Avant (LAV-AT) content.
- To view the Online Help, start the Lattice Radiant software and select the  "Getting Started" icon under Information Center.

  Note: The Firefox Snap install is not supported if you are using Ubuntu 20.04 or 18.04 to access the Radiant Help. This is a result of the snap install's inability to open local HTML pages. You may reinstall the latest version of Firefox using Apt install. For installation instructions, please refer to this guide.

System Requirements

The following shows the basic system requirements for Radiant software:

- Intel x86 64-bit or 64-bit-compatible PC
- OS Support:

64-bit OS	Radiant	Synplify Pro	ModelSim
Windows 10	✓	✓	✓
Windows 11	✓	✓*	✓*
Red Hat Enterprise Linux 7.9	✓	✓	✓
Red Hat Enterprise Linux 8.8	✓	✓	✓
Ubuntu version 18.04 LTS	✓	✓*	✓*
Ubuntu version 20.04 LTS	✓	✓*	✓*

64-bit OS	Radiant	Synplify Pro	ModelSim
CentOS 7.9	✓	✓	✓*
CentOS 8.4	✓	✓	✓*

***Note**: The third-party tools have been tested by Lattice on the listed platforms, but the vendors do not officially support them.

- Approximately 50 GB free disk space
- Computer Memory Requirement:
  - Nexus – 16GB
  - Avant – 32GB Recommended for running a single project. If running multiple projects, the memory requirement will be higher.
- 1024 X 768 graphics display
- Network adapter for license and network connectivity.
- A Web browser with JavaScript capability
- Acrobat Reader

Issues Fixed

The following known issues are fixed in this release. Their workarounds are no longer needed.

Bitstream generation fails when selecting either "Hex File" or "NVCM File" formats in the Bitstream Settings menu.

Devices affected: iCE40 UltraPlus (iCE40UP)

Bug number: DNG-19371

Fixed in Radiant 2023.2.1

“Child Process Exited Abnormally” error occurs when compiling libraries using Xcelium version 23.03.003.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-18594, DNG-19007

Fixed in Radiant 2023.2.1

IBIS generated string for MCLKP/N always sets the PULLMODE value to None.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19472

Fixed in Radiant 2023.2.1

A rev_* folder is generated each time Synthesis is run in a VHDL design.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-19150

Fixed in Radiant 2023.2.1

Common Path skew computation for clock domain crossing paths caused hold timing violation.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-20114

Fixed in Radiant 2023.2.1

Clock drift in long simulation run results in packet corruption.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-19114

Fixed in Radiant 2023.2.1

DDR placement issue of Place and Route not accepting pin constraints used in a previously successful run.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-20456

Fixed in Radiant 2023.2.1

Fixed DRC check for data rate attribute error for MPCS IP.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-20415

Fixed in Radiant 2023.2.1

VHDL 2008 option under Project > Active Strategy > Synplify Pro settings not working after it is set to “TRUE”.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19928

Fixed in Radiant 2023.2.1

VCS issuing “[IND] Identifier not declared” error on cae_library/simulation/verilog/lifcl/lmmis_init_fsm.v when running simulation on LIFCL design in Linux.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-19861

Fixed in Radiant 2023.2.1

FIFO Memory Modules IP for Avant device is not working in FWFT mode.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-20406

Fixed in Radiant 2023.2.1

Long readback time from SRAM through JTAG when using Programmer for Avant family devices.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19817

Fixed in Radiant 2023.2.1

When using SEDC module from the IP Catalog, or when instantiating the SEDCA primitive, the "sedc_busy_o" (IP) or "SEDCBUSY" (primitive) signal will not assert in simulation.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19456

Fixed in Radiant 2023.2.1

Memory initialization for Propel design through ECO Editor is not functional.

Devices affected: All devices

Bug number: DNG-18316, DNG-18383, DNG-18001

Fixed in Radiant 2023.2.1

Synplify Pro crash on specific hardware configurations with Ubuntu 20.04 due to Synplify library issue.

Device affected: All devices

Bug Number: DNG-15909

Fixed in Radiant 2023.2.1

Synplify Pro program error occurs when synthesizing standard_logic_vectors adders of specific width.

Devices affected: Lattice Avant (LAV-AT)

Bug Number: DNG-19556

Fixed in 2023.2.1

Program error occurs for Lattice Radiant while opening the Power Calculator.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-20708

Fixed in 2023.2.1

Synplify Pro Lattice OEM (*.srr and *.srf files) may incorrectly report the number of LRAMs for the target device.

Devices affected: CertusPro-NX (LFCPNX-50)

Bug number: DNG-16362

Fixed in 2023.2.1

The SED block reports an error when a distributed RAM is partially used in the design.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-18424

Fixed in 2023.2.1

Known Issues for Radiant 2023.2.1

The following are known issues for Radiant Software 2023.2.1.

When simulating GDDR 7:1 with RX configuration, and Bandwidth is around 935 Mbps to 945 Mbps, there may be a mismatch in the RTL, Post-Synthesis, and Post-PAR simulation due to a change in the PLL simulation model.

Workaround: On the customer testbench, tb_top.v, where pll_rstn_i signal is asserted and deasserted, increase the pll_rstn_i time. This can be done by increasing the number inside the parentheses after the word “repeat.” The suggested number is 8 or 10 or any greater number.

Device affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink- NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug Number: DNG-20829

LSE mishandles the "syn_black_box=1" attribute on IP generated instance ram_dp_inst_inst.

Workaround: Remove "syn_black_box=1" from the source design to complete synthesis.

Device affected: All Devices

Bug Number: DNG-20764

The value of the 32-bit hardware IDCODE is 0 when running RTL simulation.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CertusPro-NX (LFCPNX), CrossLink-NX (LIFCL-33, LIFCL 33U), MachXO5-NX (LFMXO5)

Bug number: DNG-20754

ModelSim program error occurs when running the RTL simulation of CONFIG_LMMIB.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: MachXO5-NX (LFMXO5-25)

Bug number: DNG-20755

CONFIG_LMMIE RTL simulation error occurs, LMMIRDATA port prompts incorrect data.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: MachXO5-NX (LFMXO5-100T)

Bug number: DNG-20666

Reveal trigger feature error occurs for JTAG merge case.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-20610

An error occurs when using PLL CLKOS4 RCLK due to PLL and CDC registers placement issue.

Workaround: Change from CLKOS4 to CLKOS3 to use GCLK instead of RCLK.

Device Affected: Lattice Avant (LAV-AT)

Bug Number: DNG-20599

Synplify reports an error message for JTAG merge in Reveal Analyzer.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-20598

CONFIG_LMMI RTL simulation error occurs and data missing in output ports.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: Certus-NX (LFD2NX), CrossLink-NX (LIFCL)

Bug number: DNG-20543

Incorrect calculation for LFM airflow when adjusting the Thermal Profile in Power Calculator.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-20485

SEI Editor issues related with different devices.

1. Nexus devices (LIFCL-17K, LFD2NX-17K, and LFMXO5-25K) cannot support SEI 2-bit with Unused strategy for combinations such as EBR-EBR or DSP-DSP.
2. The requirement for SEI 2-bit is that both error bits should be in the same data frame. The data frame corresponds to the FPGA column with reference to the "array" architecture.
3. In Nexus architecture, any device with a density less than 30K has only 1 EBR or 1 DSP per column. Due to this limitation, it cannot support multiple error injection on an EBR or DSP site for these densities.
4. However, those device densities can support SEI 2-bit Random strategy combinations and SEI 2-bit PFU-PFU combination with Unused strategy.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-19715

IBIS reports I/O models of some sysCONFIG pins even if they are used as GPIO.

Workaround: Remove duplicated pins in IBIS file.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19646

AON Case with Cadence Xcelium does not correctly recognize the number of ports on a user defined primitive.

Workaround: Use other simulators for the simulation, such as QuestaSim, VCS.

Devices affected: CrossLink-NX (LIFCL-33U)

Bug number: DNG-19623

Avant input I/O cannot be set as MIPI_DPHY type.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19199

When using LSE, post-synthesis engine may fail with the following error: “ERROR <1025017> - Not user declared module (VERIFIC_AND).”

This error occurs when the MOD operator is used.

Workaround: Replace the MOD operator to avoid this issue.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-16713

The PHASEDIR function of PLL does not work, the phase shift of CLKOS is still delayed when PHASEDIR = 1.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-16440

When using ModelSim to run Post-Route Gate-Level or Post-Route Gate-Level+Timing simulation, Modelsim may crash if you use a large design file, with error message “Fatal: (vsim-4) ****** Memory allocation failure.”

Workaround: Use QuestaSim 64-bit version.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-14945

When simulating Cordic IP using ModelSim, you may encounter an error during simulation.

Workaround: In OEM ModelSim, use the “vsim -voptargs=+acc -L work -L pmi_work -L ovi_lavat tb_top -suppress 8607” command to finish the simulation.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-14888

Reveal Power-on Reset (POR) Debug function does not work when using LSE with only one Trigger Unit (TU).

Workaround: Add another Trigger Unit that can be unrelated to POR Debug.

Devices affected: All devices except iCE40 UltraPlus (iCE40UP)

Bug number: DNG-13901

The CSI-2/DSI D-PHY Transmitter and Receiver Soft IP simulations fail when using Synopsys VCS as simulation tool.

Workaround: Use Modelsim simulation tool.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-13225

When simulating Generic DDR, there may be a mismatch in the RTL and post-route simulation. Silicon is not affected.

Workaround: For Nexus devices, intrinsic delay similar to the delay value on the vo.vo file needs to be added to the IP testbench.

For Avant devices, overwrite the delay parameter values of the primitives used on the GDDR instance with the same value from the generated RTL on the generated post-PAR netlist. This should only be done for simulation purposes.

Devices affected: All devices except iCE40 UltraPlus (iCE40UP)

Bug number: DNG-9639, DNG-18794

MAP incorrectly reports the number of DPHY and PCIE/ADC resources for CrossLink-NX (LIFCL) QFN72 package.

Workaround: Issue relates to DNG-10587 and MAP has been updated using the new API for DPHY.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-8297