AHB-Lite to AXI4 Bridge IP

IP Version: 1.5.0

User Guide

FPGA-IPUG-02242-1.5

June 2026

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ACE	AXI Coherency Extensions
AMBA	Advanced Micro-controller Bus Architecture
AXI	Advanced Extensible Interface Bus
AHB	Advanced High-performance Bus
EBR	Embedded Block RAM
FPGA	Field Programmable Gate Array
GUI	Graphical User Interface
HDL	Hardware Description Language
LUT	Look-Up Table
RTL	Register Transfer Level
QoS	Quality of Service
SoC	System-on-Chip

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1. Introduction

1.1. Overview of the IP

The Lattice Semiconductor AHB-Lite to AXI4 Bridge provides an interface between a single high-speed AHB-Lite manager (compliant to AMBA 3 AHB-Lite Protocol Specification) and an AXI4 or AXI4-Lite subordinate (compliant to AMBA AXI and ACE Protocol Specification Version H.c).

1.2. Quick Facts

The design is implemented in Verilog HDL. The IP can be configured and generated using the Lattice Propel™ Builder and implemented within the Lattice Radiant™ software.

Table 1.1. Summary

IP Requirements	Supported Devices	CrossLink™-NX, Certus™-NX, MachXO5™-NX, CertusPro™-NX, Lattice Avant™, Certus-N2, LatticeECP3™, ECP5™
	IP Changes[1]	For a list of changes to the IP, refer to the AHB-Lite to AXI4 Bridge IP Release Notes (FPGA-RN-02048).
Resource Utilization	Supported User Interface	AHB-Lite, AXI4 and AXI4-Lite
Design Tool Support	IP Configuration and Generation[2]	IP core v1.5.0 – Lattice Propel Builder software 2026.1
	IP Implementation (Synthesis, Map, Place and Route)	LatticeECP3 and ECP5 devices: Lattice Diamond software Other devices: Lattice Radiant software

Notes:

1. In some instances, the IP may be updated without changes to the user guide. This user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.
2. IP Configuration and Generation indicates the IP version release coinciding with the software version release. Check the software for IP version compatibility with earlier or later software versions.

1.3. IP Support Summary

Table 1.2. AHB-Lite to AXI4 IP Support Readiness

Device Family	Radiant/Diamond Timing Model
CrossLink-NX	Final
Certus-NX	Final
Certus-N2	Preliminary
MachXO5-NX	Preliminary
CertusPro-NX	Final
Lattice Avant	Preliminary
LatticeECP3	Final
ECP5	Final

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1.4. Features

The key features of the AHB-Lite to AXI4 Bridge include:

- AHB-Lite to AXI4 conversion supports configurable data bus width: 8, 16, 32, 64, 128, 256, 512, and 1024 bits.
- AHB-Lite to AXI4-Lite conversion supports configurable data bus width: 32, 64 bits.
- Supports configurable address width: 11 to 32 bits.
- Supports configurable AXI4 ID bus width (1 to 11 bits) so that the width can be matched with the subordinate ID bus width, but the ID value for this bridge is always tied to 0 since AHB-Lite does not have the concept of ID.
- Supports basic and burst transfer. Single and indefinite length increment transfer on AHB-Lite are converted to INCR burst with length=0 on AXI4.
- Supports narrow transfer where the requested transfer size can be less than data bus width.
- Supports Secure Access at AXI4 or AXI4-Lite interface.
- Supports optional timeout indicator if there is no response from AXI4 or AXI4-Lite subordinate within certain timeframe.
- Supports write/read data bus pipeline for relaxing timing critical path.

Some limitations of AHB-Lite to AXI4 Bridge are listed below:

- Burst transfer only supports 4, 8 and 16 beats as these are bounded by AHB-Lite specification.
- Fixed burst transfer, out of order transaction, and exclusive accesses on AXI4 interface bus are not supported.
- Does not support AXI4 QOS (Quality of Service), Region identifier, and User Defined signals on AXI4 interface bus.
- AXI4/AXI4-Lite and AHB-Lite interface are expected to have the same address and data bus width, as well as operating at the same clock domain.
- AHB-Lite locked transfer request will be ignored as this feature is not supported on AXI4.

1.5. Licensing and Ordering Information

The AHB-Lite to AXI4 Bridge IP is provided at no additional cost with Lattice Propel Builder.

1.6. Minimum Device Requirements

There is no minimum device requirement for this IP and the IP can be used on any ECP, Nexus, or Avant device family.

1.7. Naming Conventions

1.7.1. Signal Names

- *_n* are active low signals (asserted when value is logic 0)
- *_i* are input signals
- *_o* are output signals

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2. Functional Description

2.1. Overview

The AHB-Lite to AXI4 Bridge is used for interfacing one AHB-Lite Manager and one AXI4 Subordinate or AXI4-Lite Subordinate. The read and write transfers on AHB-Lite side are translated into the equivalent AXI4 or AXI4-Lite transaction to be compatible with the subordinate. Some additional wait states are expected on the AHB-Lite bus because of the translation operation and pipeline in the bridge.

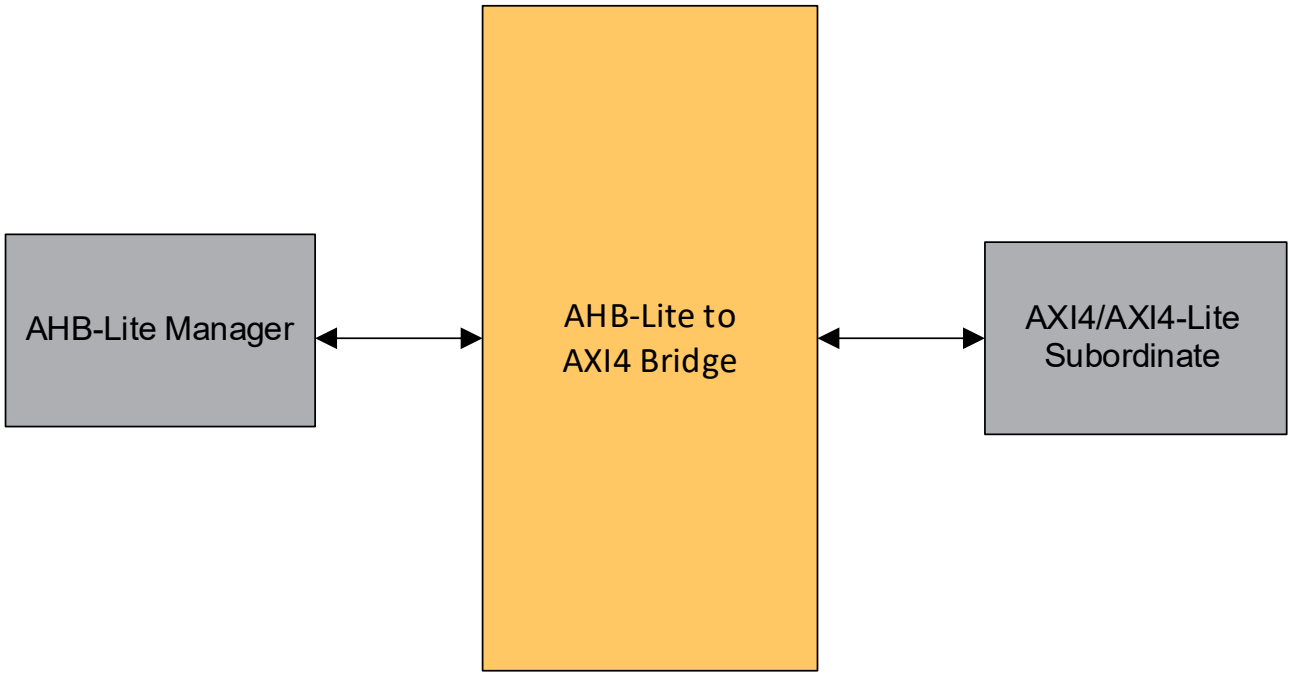


Figure 2.1. AHB-Lite to AXI4 Bridge

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2.2. Interface Description

Figure 2.2 shows the interface diagram of the AHB-Lite to AXI4 Bridge IP. The diagram shows all the available ports on the IP core.

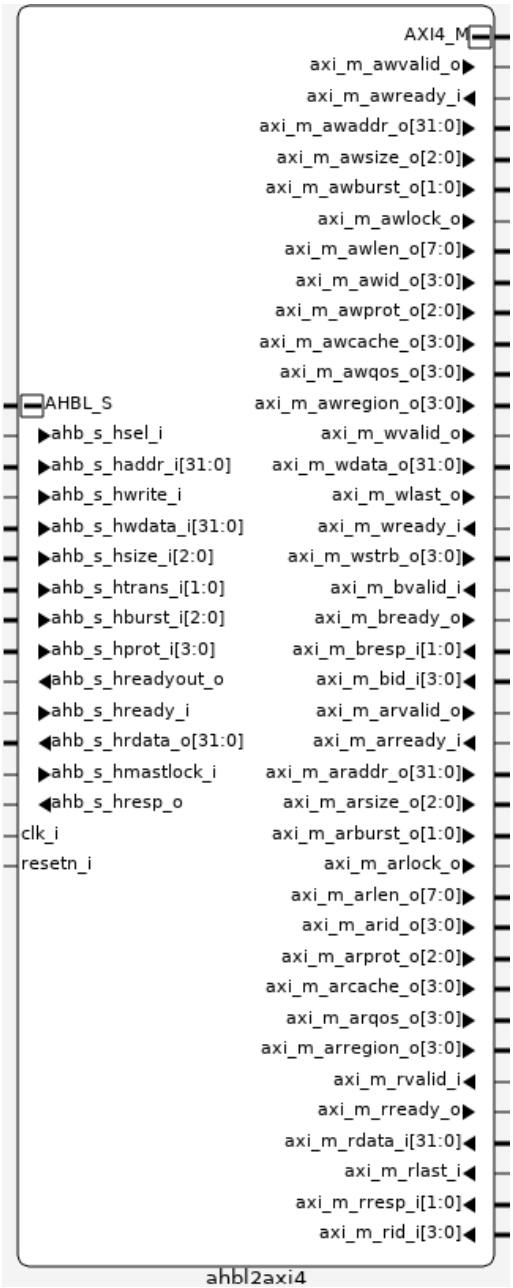


Figure 2.2. AHB-Lite to AXI4 Bridge Interface Diagram

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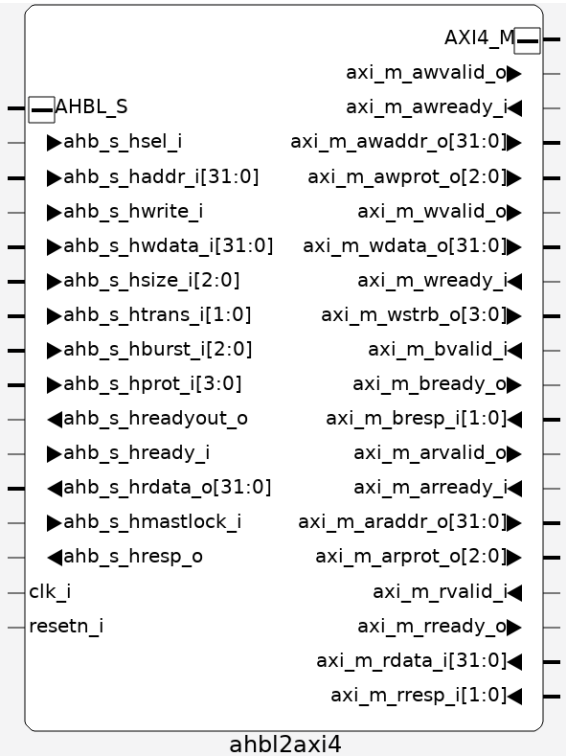


Figure 2.3. AHB-Lite to AXI4-Lite Bridge Interface Diagram

Table 2.1. Signal Description

Pin Name	Direction	Width (Bits)	Description
Clock and Reset			
clk_i	In	1	AHB-Lite to AXI4 bridge clock.
resetn_i	In	1	Active low reset. It is recommended to share the same reset source as the AHB-Lite manager so that HREADY signals are synchronized correctly.
AHB-Lite Interface (AHBL_S)			
ahb_s_hsel_i	In	1	AHB-Lite subordinate select.
ahb_s_haddr_i	In	M_ADDR_WIDTH	AHB-Lite 32-bit system address bus.
ahb_s_hwrite_i	In	1	Indicates the transfer direction. This signal indicates an AHB-Lite write access when High and an AHB-Lite read access when Low.
ahb_s_hwdata_i	In	DATA_WIDTH	Write data. The write data bus transfers data from the manager to the subordinates during write operations. The width of the port is configurable. Refer to Table 2.2.
ahb_s_hsize_i	In	3	Indicates AHB-Lite size of transfer.
ahb_s_htrans_i	In	2	AHB-Lite transfer type, which can be NONSEQ, SEQ, IDLE, or BUSY.
ahb_s_hprot_i	In	4	Protection type. Indicates if it is a data access or instruction access transaction. It also indicates if this is a privileged mode or user mode.
ahb_s_hmastlock_i	In	1	Indicates that it is a locked sequence of transfers. This signal is unused internally.
ahb_s_hburst_i	In	3	AHB-Lite burst type. The burst type indicates if the transfer is a single transfer or forms part of a burst. The burst can be incrementing or wrapping.

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Pin Name	Direction	Width (Bits)	Description
ahb_s_hready_i	In	1	Ready signal from AHB-Lite manager to indicate that the previous transfer is completed. This signal can be connected to *ahb_s_hreadyout_o* if the AHB-Lite manager does not have a HREADY output port.
ahb_s_hreadyout_o	Out	1	Ready signal to AHB-Lite manager to indicate that the previous transfer is completed.
ahb_s_hrdata_o	Out	DATA_WIDTH	AHB-Lite read data to the manager. Width of the port is configurable.
ahb_s_hresp_o	Out	1	Transfer response. When Low, it indicates that the transfer status is OKAY. When High, it indicates that the transfer status is an ERROR. SLVERR and DECERR on AXI4 bus will be translated to error response on AHB-Lite bus. If the returning AXI4 ID does not match with the outgoing AXI4 ID (which is always 0), an error response will be triggered as well.
AXI4 Interface (AXI4_M)			
axi_m_awid_o	Out	AXI_ID_WIDTH	AXI4 write ID. This output signal will always be tied to 0. When the AXI4_LITE parameter is enabled, this signal is not displayed and not supported.
axi_m_awaddr_o	Out	M_ADDR_WIDTH	Write address. In a write burst transaction, this signal holds the address of the first transfer.
axi_m_awlen_o	Out	8	Burst length. This indicates the number of beats per AXI4 burst. When the AXI4_LITE parameter is enabled, this signal is not displayed and not supported.
axi_m_awsize_o	Out	3	Burst size. Indicates the size of each transfer in the burst. When the AXI4_LITE parameter is enabled, this signal is not displayed and not supported.
axi_m_awburst_o	Out	2	Burst type. The burst type and the size information. Determines how the address of each transfer within the burst is calculated. When the AXI4_LITE parameter is enabled, this signal is not displayed and not supported.
axi_m_awlock_o	Out	1	Lock Type. Only normal access type is supported as exclusive access is not supported on AHB-Lite manager. When the AXI4_LITE parameter is enabled, this signal is not displayed and not supported.
axi_m_awcache_o	Out	4	Memory type. Only 4 types of encoding are supported: device non-bufferable, device bufferable, normal non-cacheable non-bufferable, normal non-cacheable bufferable. The rest are not supported as they are not included in AHB-Lite. When the AXI4_LITE parameter is enabled, this signal is not displayed and not supported.
axi_m_awprot_o	Out	3	Access permission signals to protect against illegal transaction. Two protection encodings are supported which are Privileged/Unprivileged access, Data/Instruction access. Secure and non-secure access is based on the *AXI_SECURE_ACCESS* attribute.
axi_m_awqos_o	Out	4	QoS identifier sent for each transaction. Not supported and will always be tied to 0. When the AXI4_LITE parameter is enabled, this signal is not displayed and not supported.

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Pin Name	Direction	Width (Bits)	Description
axi_m_awregion_o	Out	4	Region identifier sent for each transaction. Not supported and will always be tied to 0. When the AXI4_LITE parameter is enabled, this signal is not displayed and not supported.
axi_m_awvalid_o	Out	1	Write address valid. Indicates that the address and control bits on the channel are valid.
axi_m_awready_i	In	1	Write address ready. Indicates the readiness of the subordinate. When asserted, the subordinate is ready for a new address.
axi_m_wdata_o	Out	DATA_WIDTH	Write data.
axi_m_wstrb_o	Out	DATA_WIDTH	Write strobes. This signal indicates which eight bits of the write data bus are valid. This signal will be tied to all 1's as the Write Strobe feature is not supported in AHB-Lite.
axi_m_wlast_o	Out	1	Write last. This signal indicates if the current transfer is the last data transfer in a write transaction. When the AXI4_LITE parameter is enabled, this signal is not displayed and not supported.
axi_m_wvalid_o	Out	1	Write valid. This signal indicates data and strobes on the bus are valid.
axi_m_wready_i	In	1	Write data ready. Indicates the readiness of the subordinate. When asserted, the subordinate is ready for new data.
axi_m_bid_i	In	AXI_ID_WIDTH	Write response ID from subordinate. When the AXI4_LITE parameter is enabled, this signal is not displayed and not supported.
axi_m_bresp_i	In	2	Write response which indicates the status of a write transaction.
axi_m_bvalid_i	In	1	Write response valid. When asserted, the subordinate is signaling a valid write response.
axi_m_bready_o	Out	1	Response ready. Indicates that the manager is now ready to accept a write response.
axi_m_arid_o	Out	AXI_ID_WIDTH	AXI4 read address ID. This output signal will always be tied to 0. When the AXI4_LITE parameter is enabled, this signal is not displayed and not supported.
axi_m_araddr_o	In	M_ADDR_WIDTH	Read address. In a read burst transaction, this signal holds the address of the first transfer.
axi_m_arlen_o	Out	8	AXI4 read burst length. This indicates the number of beats per AXI4 burst. When the AXI4_LITE parameter is enabled, this signal is not displayed and not supported.
axi_m_arsize_o	Out	3	Burst size. This signal indicates the size of each transfer in the burst. When the AXI4_LITE parameter is enabled, this signal is not displayed and not supported.
axi_m_arburst_o	Out	2	Burst type. The burst type and the size information. Determines how the address of each transfer within the burst is calculated. When the AXI4_LITE parameter is enabled, this signal is not displayed and not supported.
axi_m_arlock_o	Out	1	Lock Type. Only normal access type is supported as exclusive access is not supported on AHB-Lite manager. When the AXI4_LITE parameter is enabled, this signal is not displayed and not supported.
axi_m_arcache_o	Out	4	Memory type. Only 4 types of encoding are supported: device non-bufferable, device bufferable, normal non-cacheable non-bufferable, normal non-cacheable bufferable.

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Pin Name	Direction	Width (Bits)	Description
			The rest are not supported as they are not included in AHB-Lite. When the AXI4_LITE parameter is enabled, this signal is not displayed and not supported.
axi_m_arprot_o	Out	3	Access permission signals to protect against illegal transaction. Two protection encodings are supported, which are Privileged/Unprivileged access, Data/Instruction access. Secure and non-secure access is based on the *AXI_SECURE_ACCESS* attribute.
axi_m_arqos_o	Out	4	QoS identifier sent for each transaction. Not supported and will always be tied to 0. When the AXI4_LITE parameter is enabled, this signal is not displayed and not supported.
axi_m_arregion_o	Out	4	Region identifier sent for each transaction. Not supported and will always be tied to 0. When the AXI4_LITE parameter is enabled, this signal is not displayed and not supported.
axi_m_arvalid_o	Out	1	Read address valid. Indicates that the address and control information is valid.
axi_m_arready_i	In	1	Read address ready. Indicates the readiness of the subordinate. When asserted, the subordinate is ready for a new address.
axi_m_rid_i	In	AXI_ID_WIDTH	Identification tag for read data and response. When the AXI4_LITE parameter is enabled, this signal is not displayed and not supported.
axi_m_rdata_i	In	DATA_WIDTH	Read data.
axi_m_rresp_i	In	2	Read response. Indicates the read transaction status.
axi_m_rlast_i	In	1	Read last. This signal indicates if the current transfer is the last data transfer in a read transaction. When the AXI4_LITE parameter is enabled, this signal is not displayed and not supported.
axi_m_rvalid_i	In	1	Read valid. Indicates that the read data channel signals are valid.
axi_m_rready_o	Out	1	Read ready. Indicates the readiness of the manager. When asserted, the manager is ready to receive data.
Optional interface (enabled when AXI4 Timeout counter > 0)			
axi_timeout_o	Out	1	AXI4 timeout signal. Asserted when the AXI4 subordinate does not respond within the threshold set for that option. When this signal is asserted, it is recommended to reset the entire AXI4 and AHB-Lite bus to recover the bus as the AXI4 subordinate is probably hung.

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2.3. Attributes

Table 2.2 provides the list of user-configurable attributes for AHB-Lite to AXI4 Bridge. The attribute values are configured using the IP Core Block Wizard in the Propel Builder software.

Table 2.2. IP Parameters

Attribute Name	Attribute ID	Selectable Values	Default	Dependency on Other Attributes	Description
General Settings Tab					
Address Width	M_ADDR_WIDTH	11-32	32	—	Specifies the bit width of AHB-Lite and AXI4 address bus signals.
Data Bus width	DATA_WIDTH	8, 16, 32, 64, 128, 256, 512, 1024 (AXI4) 32, 64 (AXI4-Lite)	32	AXI4_LITE	Specifies the bit width of AHB-Lite and AXI4 data bus signals.
AXI Transaction ID width	AXI_ID_WIDTH	1-11	4	—	Specifies the bit width of AXI4 Transaction ID signals. The ID value will always be set to 0.
AXI Secure access	AXI_SECURE_ACCESS	0,1	0	—	Specifies the support for secure access at AXI4 side. Enabling this parameter will enable secure access for all AXI4 transactions.
AXI Timeout counter[1]	AXI_TIMEOUT	0,16,32, 64,128	0	—	Specifies the number of clock cycles to wait for the AXI4 subordinate to respond and assert timeout signal if it is not responding. For example: • 0 – no timeout counter will be implemented. • 16 – Timeout if there is no response from bridge within 16 clock cycles.
Read Data bus Pipeline Enable	RDDATA_PIPELINE	0,1	0	—	Enables this parameter to add a pipeline stage to Read Data bus. Useful for relaxing the timing critical path if there is any violated path detected on this bus.
Write Data bus Pipeline Enable	WRDATA_PIPELINE	0,1	0	—	Enables this parameter to add a pipeline stage to Write Data bus. Useful for relaxing the timing critical path if there is any violated path detected on this bus.
Narrow transfers support	NARROW_TRANSFER	0,1	0	DATA_WIDTH > 8	Enables this parameter to support narrow transfer feature where the requested transfer size can be less than the DATA_WIDTH selected.

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Attribute Name	Attribute ID	Selectable Values	Default	Dependency on Other Attributes	Description
AXI4 Lite Support	AXI4_LITE	0,1	0	—	Enables this parameter to support AXI4-Lite on AXI4_M interface, else this parameter supports AXI4.

Note:

1. In cases where the AW (Address Write) and W (Write Data) channels operate concurrently, the timeout counter is reset upon receipt of any valid AW or W response from AXI subordinate.

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3. Timing Diagram

3.1. Write Operation

3.1.1. Write Data Bus Pipeline Disabled

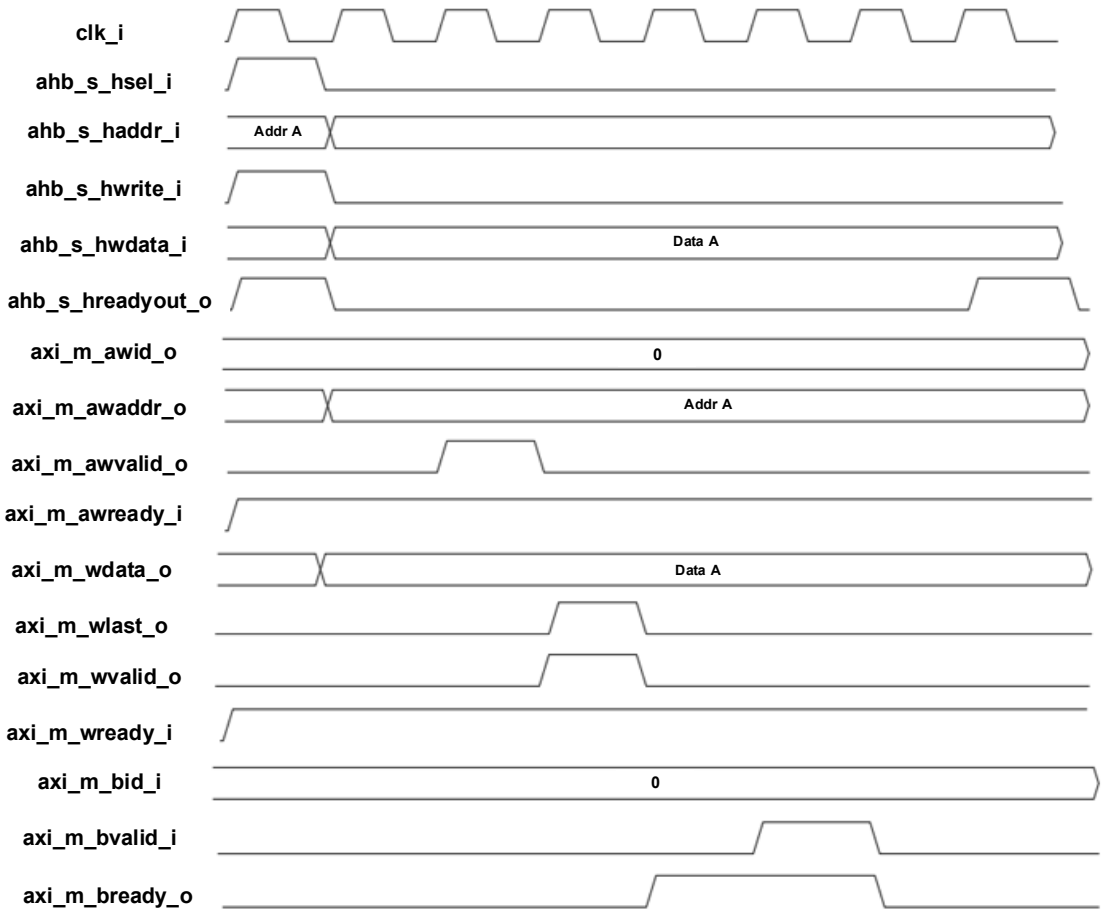


Figure 3.1. Timing Diagram of Write Transfer with Data Bus Pipeline Disabled

Figure 3.1 shows a basic write transfer with write data bus pipeline disabled.

1. At the first clock cycle, the AHB-Lite manager initiates a write transfer by driving the address and control signals. This is the address phase of the AHB-Lite write transfer.
2. At the second clock cycle, the data phase of AHB-Lite starts and the AHB-Lite manager drives the HWDATA bus with a valid data.
3. At the third clock cycle, the bridge is driving the AXI4 write address channels to start the write transfer at the AXI4 bus. The transaction is acknowledged immediately since AWREADY signal is asserted from the beginning. If it is not asserted, the AWVALID signal is held high until the bridge detects the ready signal goes high.
4. At the fourth clock cycle, the write data channel on AXI4 are being asserted to transfer the data. The transaction is immediately being acknowledged, since WREADY signal is asserted from the beginning.

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5. At the fifth clock cycle, the Bready signal at AXI4 Write response channel is asserted and waiting for the Bvalid signal to be asserted.
6. At the sixth clock cycle, the bridge sees a Bvalid signal asserted, indicating that the write transfer is complete. The Bready signal is de-asserted at this point.
7. At the eighth clock cycle, the bridge asserts the HREADYOUT signal on the AHB-Lite bus, indicating to the AHB-Lite manager that the write transfer is complete and ready for the next transfer.

3.1.2. Write Data Bus Pipeline Enabled

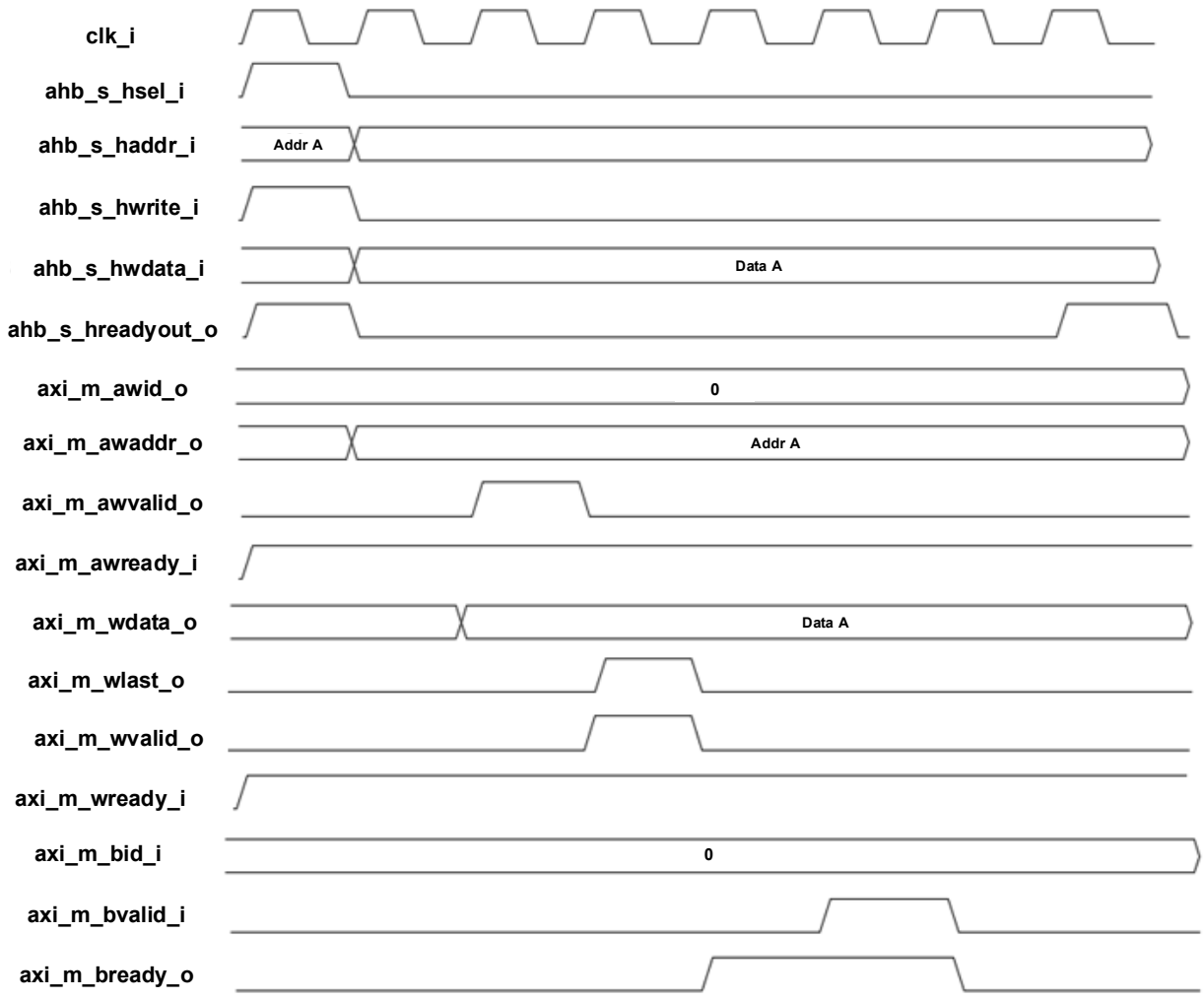


Figure 3.2. Timing Diagram of Write Transfer with Write Data Bus Pipeline Enabled

Figure 3.2 shows a basic write transfer with a write data bus pipeline enabled. Generally, the write operation works similarly to the write transfer with a write data bus pipeline disabled. The only exception is at the 2nd clock cycle, the AXI4 WDATA signal is still not driven by valid data. The data reaches the output at 1 clock cycle later, which is at the 3rd clock cycle.

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3.2. Read Operation

3.2.1. Read Data Bus Pipeline Disabled

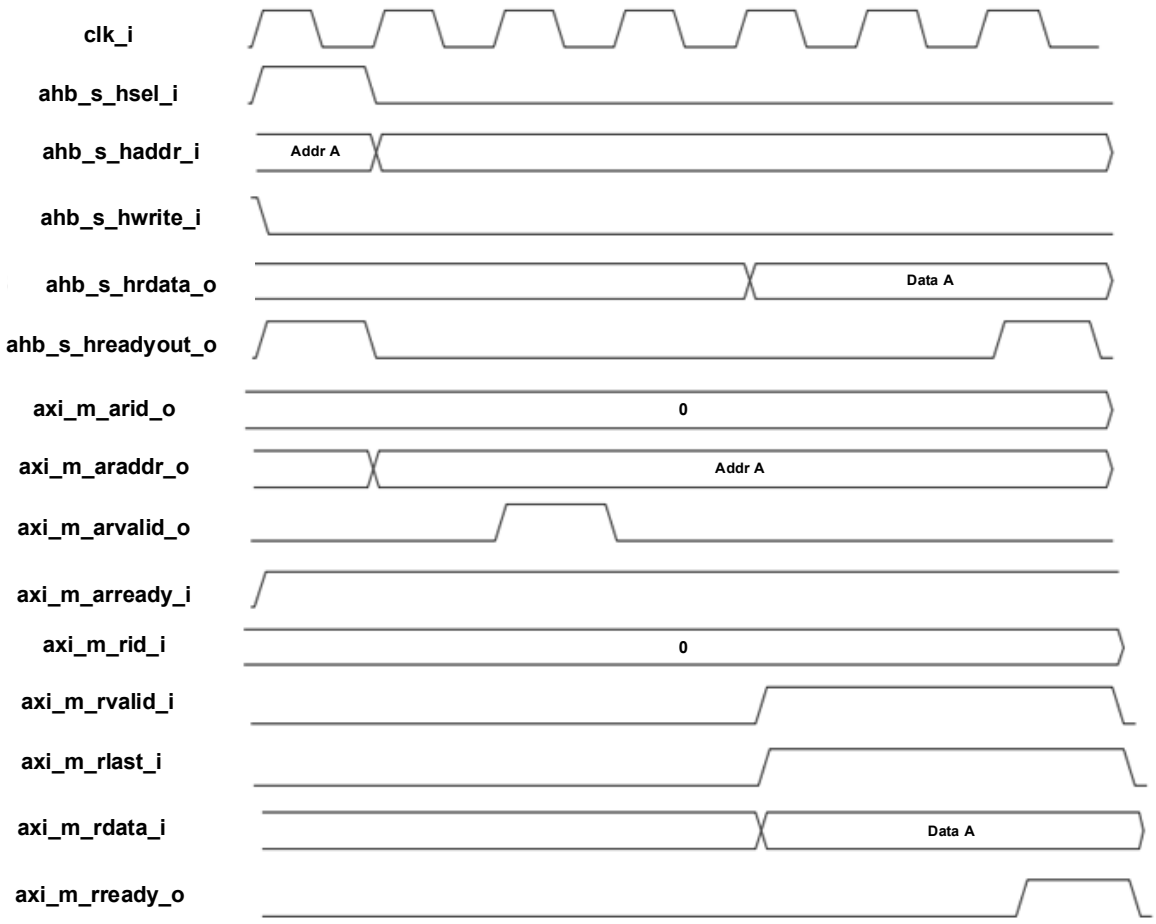


Figure 3.3. Timing Diagram of Read Transfer with Read Data Bus Pipeline Disabled

Figure 3.3 shows a basic read transfer with read data bus pipeline disabled.

1. At the first clock cycle, the AHB-Lite manager initiates a read transfer by driving the address and control signals. This is the address phase of the AHB-Lite read transfer.
2. At the second clock cycle, the data phase of the AHB-Lite transfer starts, and the AHB-Lite manager is waiting for the valid read data.
3. At the third clock cycle, the bridge starts to initiate a read transfer to the AXI4 subordinate by driving the read address channels.
4. The bridge waits for the valid read data after initiating the transfer. The read data channel returns the read data at the fifth clock cycle.
5. The Read data channel holds the valid data until the bridge indicates that the transfer is complete by asserting the Rready at the seventh clock cycle. At the same clock cycle, the HREADYOUT to the AHB-Lite manager is also asserted.

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3.2.2. Read Data Bus Pipeline Enabled

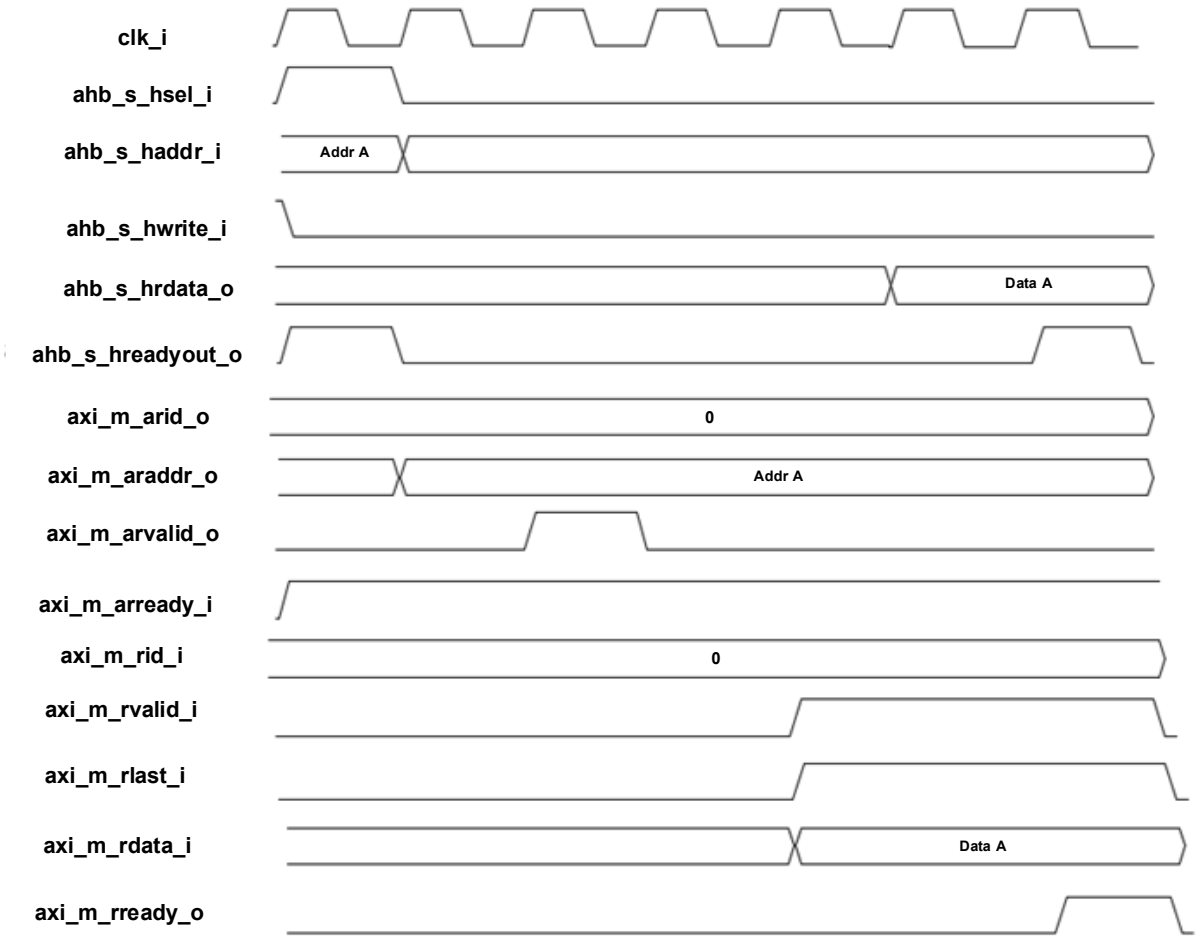


Figure 3.4. Timing Diagram of Read Transfer with Read Data Bus Pipeline Enabled

Figure 3.4 shows the basic read transfer with the read data bus pipeline enabled. Generally, the read operation works similarly to the read transfer with the pipeline disabled. The only exception is the HRDATA on the AHB-Lite interface is outputting the read data at the 6th clock cycle instead of the 5th clock cycle.

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4. Designing with the IP

This section provides information on how to generate the IP core using the Lattice Propel Builder software. For more details on the Lattice Propel software, refer to the Lattice Propel User Guide.

Note: The screenshots provided are for reference only. Details may vary depending on the version of the IP or software being used. If there have been no significant changes to the GUI, a screenshot may reflect an earlier version of the IP.

4.1. Generating and Instantiating the IP

You can use the Lattice Propel software to generate this IP module along with other components required in your System-on-Chip (SoC) design. The steps below describe the procedure for generating the AHB-Lite to AXI4 Bridge IP in the Lattice Propel software.

1. Create a new Lattice Propel software project or open an existing project.
2. In the **IP Catalog** tab, double-click **AHB-Lite to AXI4 Bridge** under **IP > Processors_Controllers_and_Peripherals** category. The Module/IP Block Wizard window opens as shown in Figure 4.1. Enter your desired component name in the **Component Name** field then click **Next**.

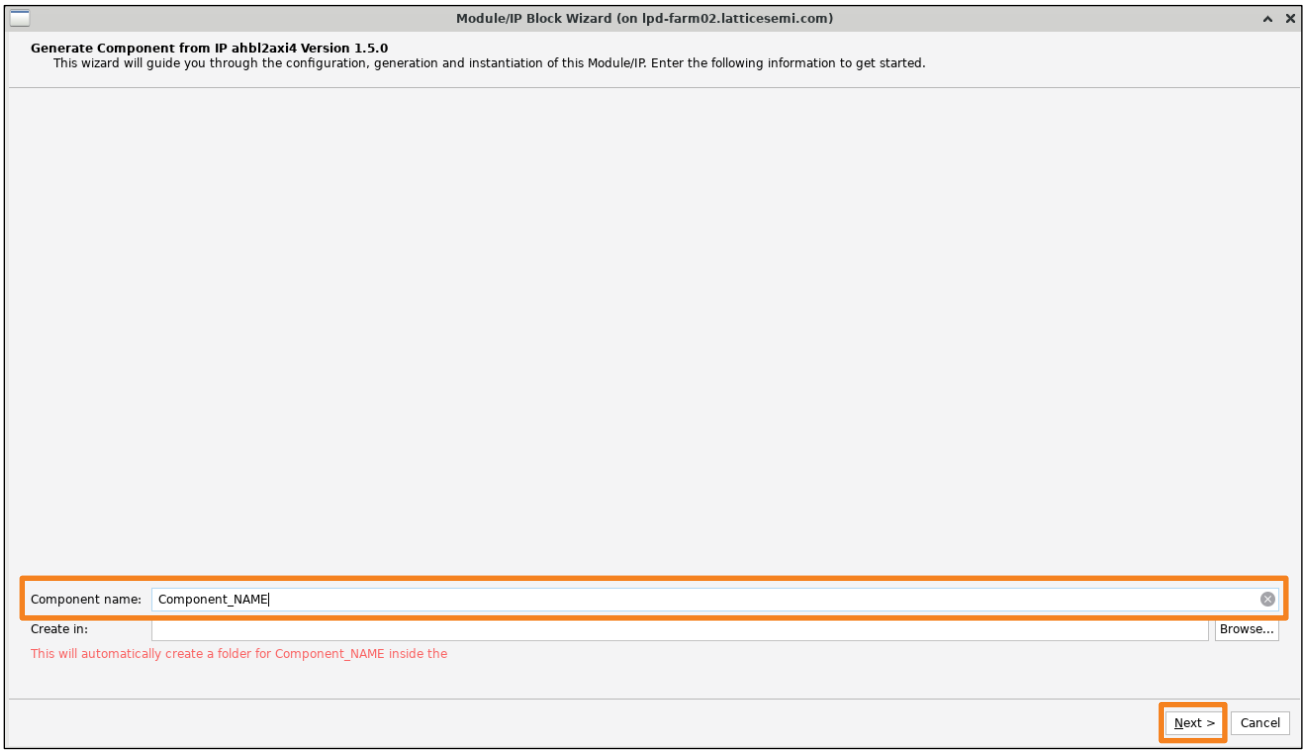


Figure 4.1. Enter Component Name

3. In the next Module/IP Block Wizard window, customize the IP according to your required configuration. Figure 4.2 shows an example configuration. For more details on the configuration options, refer to Section 2.3.

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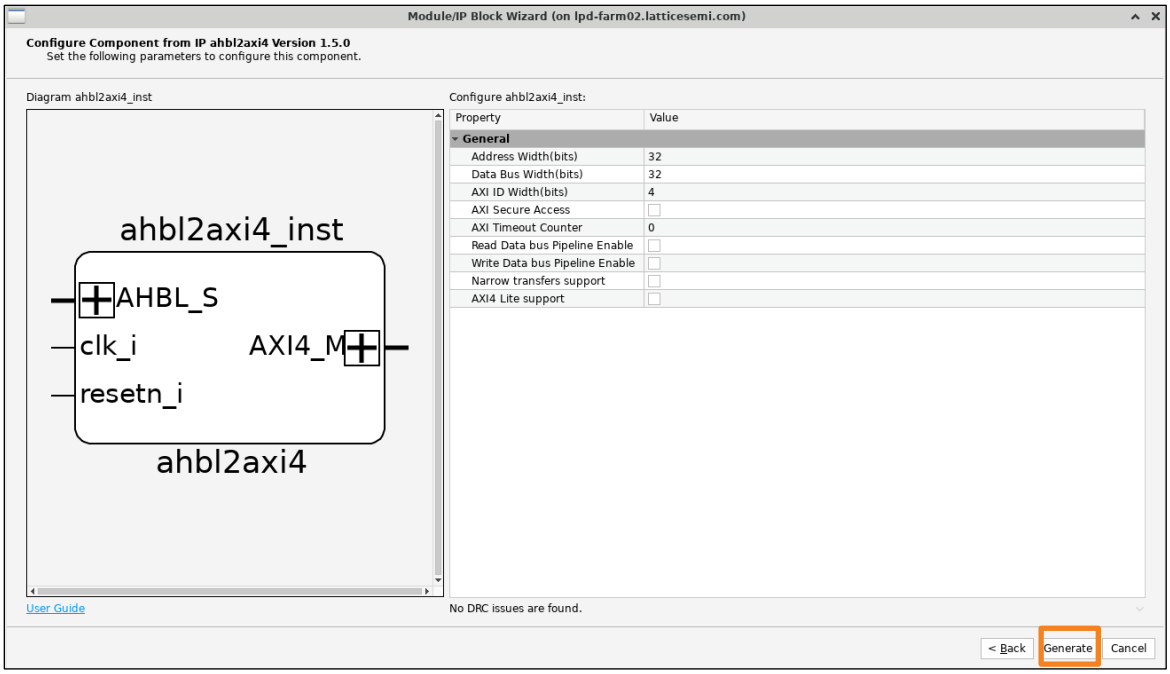


Figure 4.2. IP Configuration

4. Click the **Generate** button. The **Check Generated Result** dialog box opens as shown in Figure 4.3. This dialog box shows the design block messages and results.



Figure 4.3. Check Generated Result

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5. The generated IP will appear as a block diagram in the Schematic window. Connect it to the rest of the components in your system as shown in Figure 4.4.

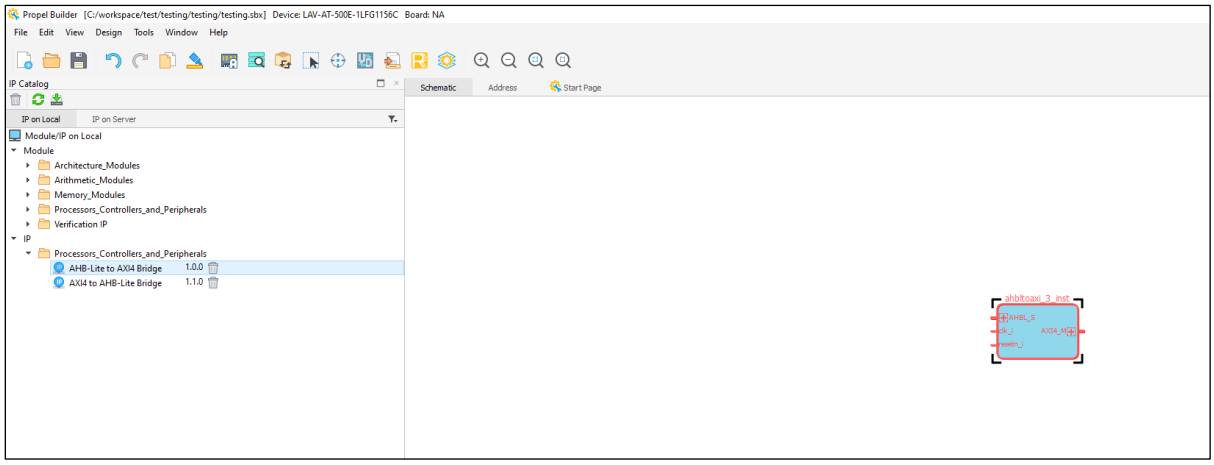


Figure 4.4. Schematic Window

6. Once all the components are connected, click **Design -> Validate Design** to validate your design. If no error is reported, click **Design > Generate** to generate the RTL files for your created system. All the generated files are placed under <directory paths in the **Create in** field as shown in **Step 2>** / lib/ latticesemi.com/ folder.

4.1.1. Generated Files and Structure

The generated AHB-Lite to AXI4 Bridge IP package includes the closed-box (<Component name>_bb.v) and the instance templates (<Component name>_tmpl.v/vhd) that is used to instantiate the core in a top-level design. An example RTL top-level reference source file (<Component name>.v) is given that can be used as an instantiation template for the module. The generated files are listed in Table 4.1.

Table 4.1. Generated Files

Attribute	Description
<Component name>.ipx	This file contains the information on the files associated to the generated IP.
<Component name>.cfg	This file contains the parameter values used in the IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Component name>.v	This file provides an example RTL top file that instantiates the module.
rtl/<Component name>_bb.v	This file provides the synthesis closed-box.
misc/<Component name>_tmpl.v misc /<Component name>_tmpl.vhd	These files provide instance templates for the module.

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Appendix A. Resource Utilization

Note: Resource utilization values in this section are provided for reference only and may change based on the compilation strategy and selected tool options.

Table A.1 shows a sample of the resource utilization of the AHB-Lite to AXI4 Bridge IP on Lattice Avant devices.

Table A.1. Estimated Device Resource Utilization on Lattice Avant Devices

Attribute Values						Clock Fmax (MHz)	LUTs	Register	EBRs
Data Width	AXI4 Timeout Counter	Read Data Bus Pipeline Enable	Write Data Bus Pipeline Enable	Narrow Transfer Support	AXI4 Lite Support				
32	0	0	0	0	0	250	95	82	0
32	0	1	1	0	0	250	89	144	0
32	128	0	0	0	0	250	118	108	0
32	128	1	1	0	0	250	115	170	0
256	0	0	0	0	0	250	95	82	0
256	0	1	1	0	0	250	97	604	0
256	128	0	0	0	0	250	118	108	0
256	128	1	1	0	0	250	122	620	0
32	0	0	0	1	0	250	105	96	0
32	0	1	1	1	0	250	106	161	0
32	128	0	0	1	0	250	128	115	0
32	128	1	1	1	0	250	125	170	0
256	0	0	0	1	0	250	125	116	1
256	0	1	1	1	0	250	128	634	1
256	128	0	0	1	0	250	150	139	1
256	128	1	1	1	0	250	156	652	1
32	0	0	0	0	1	250	68	103	0
32	0	1	1	0	1	250	68	103	0
32	128	0	0	0	1	250	86	125	0
32	128	1	1	0	1	250	86	125	0
32	0	0	0	1	1	250	68	103	0
32	0	1	1	1	1	250	68	103	0
32	128	0	0	1	1	250	86	125	0
32	128	1	1	1	1	250	86	125	0

Notes:

1. Address width is always set to 32 bits in all configurations listed.
2. The resource values are populated using LAV-AT-E70-1LFG676C device compiled in the Lattice Radiant 2023.1 design software with Synplify Pro®. When the IP is combined with other blocks in the FPGA, the value can be expected to vary from the value in the table.

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Table A.2 shows a sample of the resource utilization of AHB-Lite to AXI4 Bridge IP on CertusPro-NX devices.

Table A.2. Estimated Device Resource Utilization on CertusPro-NX Devices

Attributes Values						Clock Fmax (MHz)		LUTs	Register	EBRs
Data Width	AXI4 Timeout Counter	Read Data Bus Pipeline Enable	Write Data Bus Pipeline Enable	Narrow Transfer Support	AXI4 Lite Support	Performance Grade = 7 & 8_Low-Power	Performance Grade = 9_Low-Power and All High-Performance Grade			
32	0	0	0	0	0	160	200	83	87	0
32	0	1	1	0	0	160	200	83	151	0
32	128	0	0	0	0	160	200	109	105	0
32	128	1	1	0	0	160	200	104	169	0
256	0	0	0	0	0	160	200	83	87	0
256	0	1	1	0	0	160	200	86	599	0
256	128	0	0	0	0	160	200	109	105	0
256	128	1	1	0	0	160	200	104	617	0
32	0	0	0	1	0	160	200	94	94	0
32	0	1	1	1	0	160	200	94	158	0
32	128	0	0	1	0	160	200	115	112	0
32	128	1	1	1	0	160	200	115	176	0
256	0	0	0	1	0	160	200	116	118	2
256	0	1	1	1	0	160	200	116	630	2
256	128	0	0	1	0	160	200	137	136	2
256	128	1	1	1	0	160	200	137	648	2
32	0	0	0	0	1	200	200	68	93	0
32	0	1	1	0	1	200	200	68	93	0
32	128	0	0	0	1	200	200	86	114	0
32	128	1	1	0	1	200	200	86	114	0
32	0	0	0	1	1	200	200	68	93	0
32	0	1	1	1	1	200	200	68	93	0
32	128	0	0	1	1	200	200	86	114	0
32	128	1	1	1	1	200	200	86	114	0

Notes:

1. Address width is always set to 32 bits in all configurations listed.
2. The resource values are populated using LFCPNX-50-7ASG256C and LFCPNX-50-9ASG256C device compiled in Lattice Radiant 2023.1 design software with Synplify Pro. When the IP is combined with other blocks in FPGA, the value can be expected to vary from the value in the table.

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References

- AHB-Lite to AXI4 Bridge IP Release Notes (FPGA-RN-02048)
- Lattice Propel 1.0 User Guide (FPGA-UG-02110)
- Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059)
- AMBA AXI and ACE Protocol Specification web page for AMBA AXI and ACE Protocol Specification version H.c
- AMBA 3 AHB-Lite Protocol Specification web page
- LatticeECP3 web page
- ECP5 web page
- CrossLink-NX web page
- CertusPro-NX web page
- Certus-NX web page
- Certus-N2 web page
- MachXO5-NX web page
- Avant-E web page
- Avant-G web page
- Avant-X web page
- Lattice Radiant Software web page
- Lattice Propel Design Environment web page
- Lattice Diamond Software web page
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Revision History

Note: In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

Revision 1.5, IP v1.5.0, June 2026

Section	Change Summary
All	Performed minor formatting and editorial edits.
Acronyms in This Document	Updated list of acronyms.

Introduction	• Added support for AHB-Lite to AXI4-Lite conversion in the Overview of the IP section.
	• Updated Table 1.1. Summary as follows:
	  • Added AXI4-Lite interface.
	  • Updated IP version.
	  • Removed earlier IP versions.
	• Updated the Features section as follows:
	  • Added the AHB-Lite to AXI4-Lite conversion supported configurable data bus width.
	  • Added AXI4-Lite support for secure access and optional timeout indicator.
	  • Added limitation for AXI4-Lite on address, data bus width, and clock domain.

Functional Description	• Added support for AXI4-Lite and updated Figure 2.1. AHB-Lite to AXI4 Bridge in the Overview section.
	• Updated Figure 2.2. AHB-Lite to AXI4 Bridge Interface Diagram.
	• Added Figure 2.3. AHB-Lite to AXI4-Lite Bridge Interface Diagram.
	• Updated Table 2.1. Signal Description as follows:
	  • Added description about the AXI4_LITE parameter.
	  • Updated the description on Secure and non-secure access for the axi_m_awprot_o and axi_m_arprot_o signals.
	• Updated Table 2.2. IP Parameters as follows:
	  • Updated the *Data Bus width* attribute.
	  • Added the *AXI4 Lite Support* attribute.

Designing with the IP	Updated the following figures: • Figure 4.1. Enter Component Name • Figure 4.2. IP Configuration • Figure 4.3. Check Generated Result
Resource Utilization	• Added a note on resource utilization values. • Updated resource utilization for the latest software version.

Revision 1.4, IP v1.4.0, December 2025

Section	Change Summary
Introduction	Updated Quick Facts section: • Added note, *In some instances, the IP may be updated without changes to the user guide. This user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.* • Added note, *IP Configuration and Generation indicates the IP version release coinciding with the software version release. Check the software for IP version compatibility with earlier or later software versions.*
Functional Description	Updated Table 2.2. IP Parameters: • Added note, *In cases where the AW (Address Write) and W (Write Data) channels operate concurrently, the timeout counter is reset upon receipt of any valid AW or W response from AXI subordinate.*

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Section	Change Summary
Designing with the IP	Added note, *The screenshots provided are for reference only. Details may vary depending on the version of the IP or software being used. If there have been no significant changes to the GUI, a screenshot may reflect an earlier version of the IP.*
Revision History	Added note, *In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.*

Revision 1.3, IP v1.3.0, June 2025

Section	Change Summary
Introduction	Updated Table 1.1. Summary as follows: • Renamed *Supported FPGA Family* to *Supported Devices*. • Removed the *Targeted Devices* row. • Added IP version.
References	Updated references.

Revision 1.2, IP v1.2.0, December 2024

Section	Change Summary

Introduction	• Updated Table 1.1 Summary.
	  • Added Certus-N2, LatticeECP3, and ECP5 devices.
	  • Added IP Changes.
	  • Updated Design Tool Support.
	• Added the IP Support Summary section.
	• Removed the *IP Validation Summary* section.
	• Added ECP as one of the minimum device requirements for this IP in the Minimum Device Requirements section.

References	Updated references.

Revision 1.1, June 2024

Section	Change Summary
All	• This release is for version 1.1.0 of the AHB-Lite to AXI4 Bridge IP. • Renamed document from *AHB-Lite to AXI4 Bridge IP Core* to *AHB-Lite to AXI4 Bridge IP*. • Changed *AXI* to *AXI4*. • Changed *AHB* to *AHB-Lite*. • Performed minor formatting and typo edits.
Introduction	• Added CrossLink-NX, Certus-NX, and MachXO5-NX devices in Table 1.1 Summary. • Updated the simulation tool in the IP Validation Summary section. • Added validation status for IP version 1.1.0 in Table 1.2 IP Validation Level. • Updated the minimum device requirements for this IP to Nexus or Avant device family in the Minimum Device Requirements section.
Designing with the IP	Changed *black-box* to *closed-box* in the Generated Files and Structure section.
References	Updated references.

Revision 1.0, December 2023

Section	Change Summary
All	Initial release.

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