Lattice Avant SED/SEC User Guide

Preliminary Technical Note

FPGA-TN-02290-0.82

June 2025

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

© 2025 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Contents

© 2025 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Figures

Tables

© 2025 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
ASCII	American Standard Code for Information Interchange
CRC	Cyclic Redundancy Check
CRAM	Configuration Random Access Memory
DSP	Digital Signal Processing
EBR	Embedded Block RAM
ECC	Error Correction Code
ID	Identification
IP	Intellectual Property
PFU	Programmable Function Unit
PLD	Programmable Logic Device
SEC	Soft Error Correction
SED	Soft Error Detection
SEDC	Soft Error Detection/Correction
SEI	Soft Error Injection
SEU	Single Event Upset
SRAM	Static Random Access Memory

© 2025 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

1. Introduction

This document describes the hard-logic soft error detection (SED) and soft error correction (SEC) implemented in the Lattice Avant™-G and Avant-X device families. When a soft error is detected, Avant-G/X devices provide an easy way to optionally perform SEC without affecting the functionality of the device.

Memory errors can occur when high-energy charged particles alter the stored charge in a memory cell in an electronic circuit. The phenomenon first became an issue in Configuration Random Access Memory (CRAM), requiring error detection and correction for large memory systems in high-reliability applications. As device geometries continue to shrink, the probability of memory errors in Static Random Access Memory (SRAM) becomes significant for some systems.

SRAM-based programmable logic devices (PLDs) store logic configuration data in SRAM cells. As the number and density of SRAM cells in a PLD increase, the probability that a memory error alters the programmed logical behavior of the system increases. Most traditional approaches that are taken to address this issue involve soft intellectual property (IP) cores that you instantiate in your design. Such approaches utilize valuable resources, possibly affecting design performance.

Avant- G/X devices have an improved hardware-implemented SEDC circuit that can be used to detect and correct SRAM errors. There are two layers of SED/SEC, error correction code (ECC) logic to detect and correct single bit error per data frame and detect two-bit errors and cyclic redundancy check (CRC) logic to detect multi-bit errors in the device.

© 2025 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2. Overview of the SEDC IP

The Soft Error Detection/Correction (SEDC) IP offers the following enhanced features:

- Frame-by-frame SED check
- Multiple regions run in parallel for fast SED and SEC performance
- Single-bit and multi-bit error detection
- ECC to correct single bit error at the frame level
- Programmable SEDC clock
- Force error capability for system-level simulation

The SEDC module is part of the sysCONFIG block in Avant-G/X devices. The configuration data is divided into frames in multiple regions. The SED hardware reads data from the FPGA's configuration memory frame-by-frame in the background while the device is in user function mode and performs ECC calculation on every frame of configuration data (see Figure 2.1). When a single-bit error is detected, a single event upset (SEU) notification is generated and the SED resumes operation after the single-bit error is corrected. Single-bit errors are corrected when SEC is enabled. The corrected value is rewritten to the frame using ECC information. If more than one bit errors are detected within one frame of configuration data, an error message is generated. In parallel, CRC is calculated for the entire CRAM contents along with ECC. After the ECC is calculated on all frames of configuration data, CRC is calculated for the configuration data in the entire device. Full-chip CRC and frame-by-frame ECC calculations do not include Embedded Block RAM (EBR). EBRs provide a separate and optional ECC for SED/SEC of the EBR content. Distributed RAM data stored in the CRAM are masked during SED/SEC because RAM content may change during user operation and hence cannot be covered by the SEDC IP without generating false SEDC errors. The distributed RAM enable bit set in CRAM is covered during SED/SEC.

The SEDC IP is part of the sysCONFIG block in Avant-G/X devices. Figure 2.1 shows the system-level view of the SEDC IP.

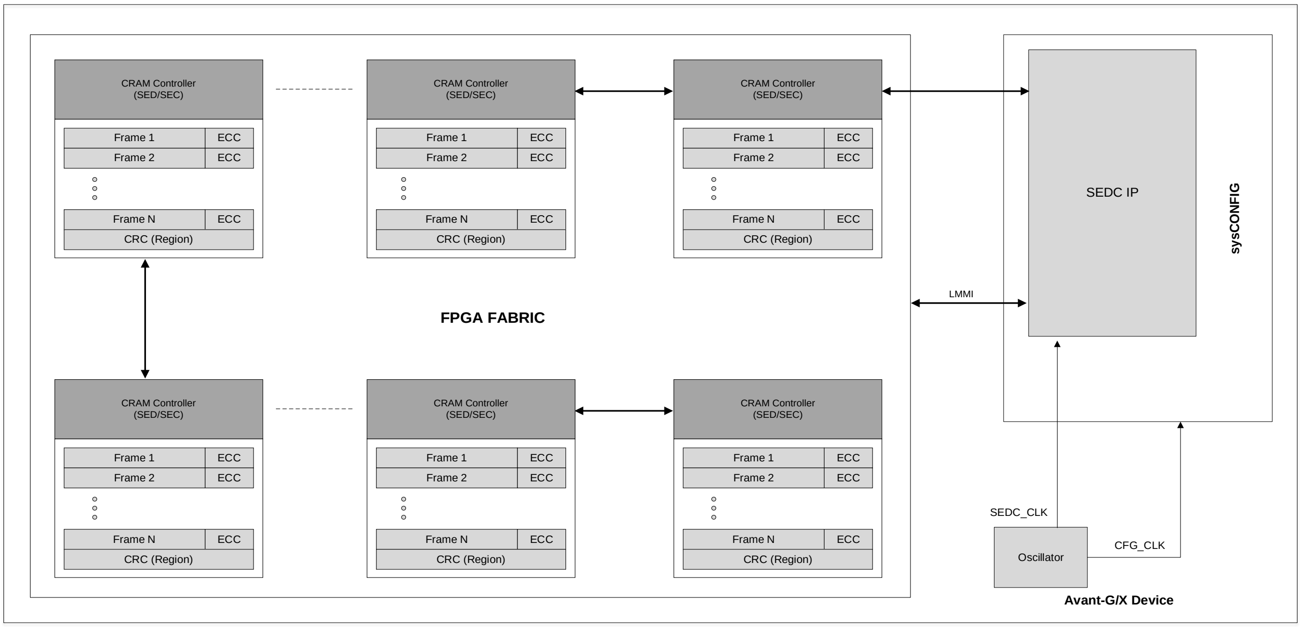


Figure 2.1. SEDC System Block Diagram

© 2025 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2.1. SEDC IP Clock and Reset

The SEDC circuitry is driven by the FPGA's internal oscillator.

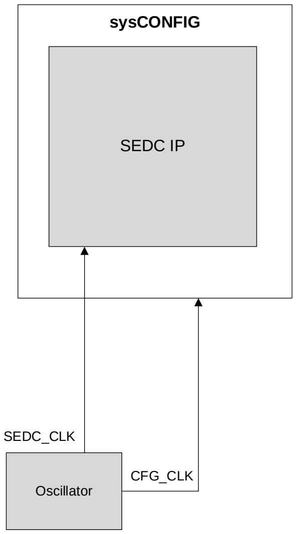


Figure 2.2. SEDC IP Clock and Reset

The default oscillator frequency is 200 MHz. You can set the SEDCLK_divider setting in the SEDC IP from the Lattice Radiant™ software IP catalog anywhere between 2 to 256 in integer increments resulting in a frequency range from 200 MHz to 1.56 MHz (SEDC oscillator frequency = 400 MHz / SEDCLK_divider).

Table 2.1. SEDC Internal Oscillator Divider Settings

Divider Setting	SEDCLK_Divider	SEDC Clock Frequency (MHz)
Divide by 2	2	200
Divide by 3	3	133.33
…	…	…
Divide by 256	256	1.56

© 2025 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

3. SEDC Flow

This section describes the SEDC flow. Once the device enters user mode, the SEDC flow is executed when user logic starts SEDC by engaging the SEDC controller IP.

Avant-G/X devices have an advanced SEDC flow with two levels of SEDC checks. In the first level of SED check, the CRAM content is read one frame at a time and the SED check is performed on a frame-by-frame basis. After all the frames of the device CRAM content are read, the SEDC module performs a CRC of the entire CRAM contents (second-level SED) to check for any multi-bit errors which were not detected by ECC.

Avant-G/X devices are built to support real-time SEC in which a single-bit soft error can be corrected using ECC at the frame level. A multi-bit soft error detected within a frame is non-correctable. Figure 3.1 shows the SEC flow in Avant-G/X devices.

Avant-G/X devices perform a one-time scan of all frames and can detect single-bit (1 bit) and multi-bit (2 bits or more) soft errors. When a single-bit soft error is detected, the hardware halts, notifies the user about the error, and waits for the instruction to proceed. Once the instruction to resume scanning is set, the hardware corrects the 1-bit error, rescans the region where the corrected frame is located, and resumes scanning the remaining frames. When a multi-bit soft error is detected, the hardware notifies the user about the error and continues scanning the remaining frames because a multi-bit soft error is non-correctable.

The following are the bit error reporting schemes:

- When a single-bit soft error is detected, the SEDC IP reports the following:
    - An error indicator with error type of 1-bit error
    - Error bit location
    - Error frame location
    - Error region location
- When a multi-bit soft error is detected, the SEDC IP reports the following:
    - An error indicator with error type of multi-bit (uncorrectable) error
    - Error frame location
    - Error region location
- After a complete scan of the CRAM content, if any soft error was detected, the SEDC IP reports the following:
    - An error indicator with error type of full-chip CRC

© 2025 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

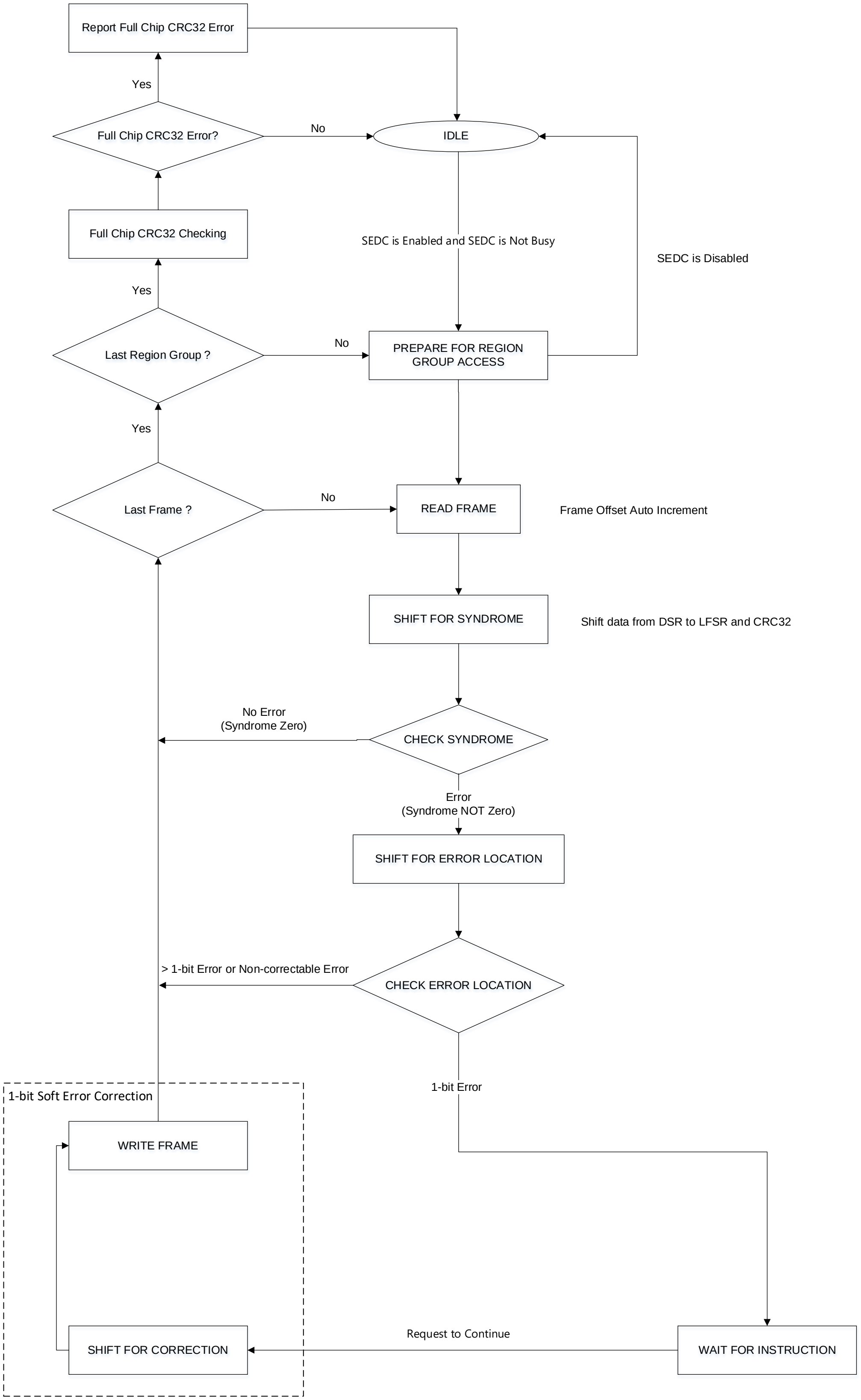


Figure 3.1. SEDC Flow

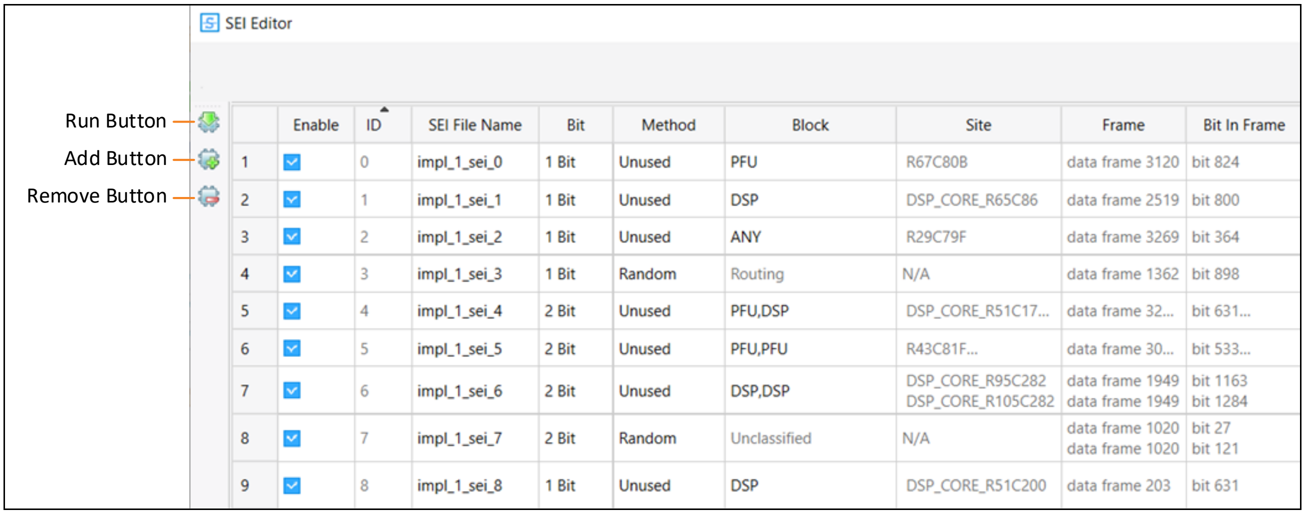
© 2025 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

4. Soft Error Injection

The Radiant soft error injection (SEI) tool offers an easy and economical way to emulate soft error impact on the overall system. This tool allows you to randomly generate and program one or multiple soft errors into the device in background mode without affecting device function. The Radiant SEI tool is supported in the Lattice Radiant software version 24.2.1 and higher.

To use the Radiant SEI tool:

1. Select **Tools** > **SEI Editor**. The SEI editor appears as shown in Figure 4.1. The SEI editor allows you to create a special one-frame bitstream that differs from the original bitstream by one bit or two bits.



	Enable	ID	SEI File Name	Bit	Method	Block	Site	Frame	Bit In Frame
1	☑	0	impl_1_sei_0	1 Bit	Unused	PFU	R67C80B	data frame 3120	bit 824
2	☑	1	impl_1_sei_1	1 Bit	Unused	DSP	DSP_CORE_R65C86	data frame 2519	bit 800
3	☑	2	impl_1_sei_2	1 Bit	Unused	ANY	R29C79F	data frame 3269	bit 364
4	☑	3	impl_1_sei_3	1 Bit	Random	Routing	N/A	data frame 1362	bit 898
5	☑	4	impl_1_sei_4	2 Bit	Unused	PFU,DSP	DSP_CORE_R51C17...	data frame 32...	bit 631...
6	☑	5	impl_1_sei_5	2 Bit	Unused	PFU,PFU	R43C81F...	data frame 30...	bit 533...
7	☑	6	impl_1_sei_6	2 Bit	Unused	DSP,DSP	DSP_CORE_R95C282 DSP_CORE_R105C282	data frame 1949 data frame 1949	bit 1163 bit 1284
8	☑	7	impl_1_sei_7	2 Bit	Random	Unclassified	N/A	data frame 1020 data frame 1020	bit 27 bit 121
9	☑	8	impl_1_sei_8	1 Bit	Unused	DSP	DSP_CORE_R51C200	data frame 203	bit 631

Figure 4.1. SEI Editor

Main features of the SEI editor are as follows:

- **Add** button – Click to add SEI files.
- **Remove** button – Click to remove SEI files.
- **Run** button – Click to generate SEI files. Note that this generates a data frame with flipped random bits, producing a partial bitstream output in binary bit or ASCII raw bit file format.
- **Enable** – Check the checkbox to select the specific bitstream to be generated when you click the **Run** button. Note that the generated bitstream is either a binary bit file or ASCII raw bit file. The bitstream output format setting in Radiant determines the file format. The default file format is binary bit file.
- **ID** – Continuous error ID number assigned by the software. This value is read-only.
- **SEI File Name** – Default filename for the generated bitstream. You may change the filename as desired.
- **Bit**
  - 1 Bit – Error injection of one bit within one data frame
  - 2 Bit – Error injection of two bits within one data frame
- **Method**
  - Unused – Error bit introduced into an unused block which does not affect the customer design logic.
  - Random – Error bit introduced into a random block which might or might not affect the customer design logic.
- **Block**
  - If **Bit** is set to 1 Bit and **Method** is set to Unused, **Block** can be selected as PFU, DSP, or ANY.
  - If **Bit** set to 2 Bit and **Method** is set to Unused, **Block** can be selected as one of the following options:
    - PFU, DSP
    - PFU, PFU
    - DSP, DSP

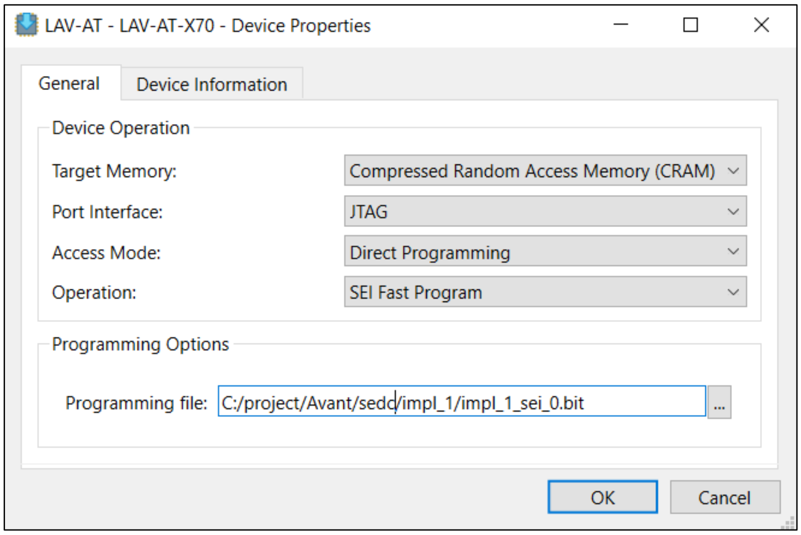
© 2025 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

  - If **Method** is set to Random, any functional block can be used including routing. However, you cannot make this selection. **Block** is read-only when **Method** is Random.
- **Site** — The exact site of the inserted error. Errors inserted into a routing block or unclassified block do not have a site. This field is read-only.
- **Frame** – The data frame of the inserted error. This field is read-only.
- **Bit in Frame** – Displays the address of the SEI frame or the bit location in the frame. This field is read-only.

Notes:

- Grey text in the **Block**, **Site**, **Frame**, or **Bit in Frame** fields indicates read-only. You cannot modify the value.
- Once SEI bitstream generation is complete, the **Site**, **Frame**, and **Bit in Frame** fields display the site name, data frame number, and bit number, respectively, where the soft error is injected.
- There is no site location when SEI is in a routing or unclassified block.

2. To program the SEI bitstream, select the **SEI Fast Program** operation in the Radiant Programmer.



LAV-AT - LAV-AT-X70 - Device Properties

Target Memory: Compressed Random Access Memory (CRAM)

Port Interface: JTAG

Access Mode: Direct Programming

Operation: SEI Fast Program

Programming file: C:/project/Avant/sedc/impl_1/impl_1_sei_0.bit

Figure 4.2. Device Properties

3. Once the SEI bitstream is programmed into the device, you can use the general SED routine to detect the soft error.
   Note: While programming the device with the SEI bitstream, SED checking must stop. You can de-assert sedc_run_i of the SEDC Controller IP.

© 2025 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

5. Important Note

SEDC operation will be interrupted once any PROG_QUALIFY target configuration command is clocked into the device. It is recommended that the SEDC operation be stopped before sending a PROG_QUALIFY target configuration command and restarted after the command is completed.

© 2025 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

References

- Avant-G web page
- Avant-X web page

For more information on Avant-related IP, reference designs, and board documents, refer to the following resources:

- SEDC Controller IP User Guide (FPGA-IPUG-02290)
- IP Cores and Reference Designs for Avant Devices
- Kits, Boards, and Demonstrations for Avant Devices

Other references:

- Lattice Radiant Software web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

© 2025 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

© 2025 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Revision History

Revision 0.82, June 2025

Section	Change Summary
Abbreviations in This Document	• Added *ASCII*, *DSP*, *ID*, and *PFU*. • Removed *CRC32* and *LMMI*.
SEDC Flow	Updated description regarding SEDC flow execution.
Soft Error Injection	Updated Radiant SEI tool support information and added steps to use the SEI tool.
References	• Added SEDC Controller IP User Guide (FPGA-IPUG-02290). • Removed Avant-G/X SEDC Module IP User Guide (FPGA-IPUG-02232). • Removed Lattice Radiant Software User Guide. • Updated listing name to Lattice Radiant Software web page.

Revision 0.81, October 2024

Section	Change Summary
All	• Updated *Avant-AT-G/X* to *Avant-G/X* throughout document. • Updated *SED* to *SEDC* when referencing module, error, clock, oscillator, and circuitry throughout document. • Changed *bitstream* to *CRAM content/s* throughout document.
Abbreviations in This Document	• Updated section title and description. • Removed *SoC*.
Overview of the SEDC IP	• Updated description. • Removed the Bitstream Data Structure figure. • In Figure 2.1. SEDC System Block Diagram: • Removed low-level details. • Removed SED_CLK label from Oscillator block. • Removed the SEDC IP Signal Description and SEDC IP Register Description sections. • In the SEDC IP Clock and Reset section: • Updated description including removing mention of RISC-V block and changing default oscillator frequency and clock frequency range. • In Figure 2.2. SEDC IP Clock and Reset: • Removed RISC-V block. • Removed SED_CLK label from Oscillator block. • Removed *Divide by 1* row and made minor editorial changes in Table 2.1. SEDC Internal Oscillator Divider Settings. • Made minor editorial changes.
SEDC IP Setup	• Moved the SEDC IP Clock and Reset section into the Overview of the SEDC IP section. • Removed section.
SEDC Flow	• Updated description including removing reference to signals (sedc_start_i, sedc_ena_i) and adding information on soft error handling and soft error reporting schemes. • Updated Figure 3.1. SEDC Flow. • Removed the SEDC Modes section.
SEC Flow	Removed section.
Code Examples	Removed section.
Soft Error Injection	Added new section.
Important Note	Added new section.
References	Reorganized, updated, and added links.

© 2025 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Revision 0.80, December 2023

Section	Change Summary
All	Preliminary release.

© 2025 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

LATTICE SEMICONDUCTOR®

www.latticesemi.com