Lattice Radiant 2023.2 Software Release Notes

Welcome to Lattice Radiant® software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs).

What's New in Radiant 2023.2 Software

- **Device Support:**
  - Lattice Avant™ (LAV-AT)
    - E70 (-1/-2/-3) 0.82V (COM/IND) – LFG676, LFG1156
      - 500E has been renamed to E70.
  - CrossLink™-NX (LIFCL)
    - 33U (-7/-8) 1.00V (COM/IND) – FCCSP104
    - 33U (-8) 1.00V (COM/IND) – WLCSP84

- **Tool and Other Enhancements:**

  - **Device Selector** – The device information of the LAV-AT device (E70) has been updated to add 637000 System Logic Cells (LCs).

  - **Lattice Synthesis Engine (LSE)** – LSE now supports the LAV-AT device.

  - **Foundation IP** – LAV-AT-E design needs to be re-generated for the Foundation IP/Soft IP. You also need to re-compile the design and re-generate the bitstream.

  - **Primitives** – The following primitives have been added for the LAV-AT device:

    - DDRPHY64C and DDRPHY72C
    - DDRPHY16D, DDRPHY32D, and DDRPHY64D
    - DDRPHY16E, DDRPHY32E, and DDRPHY64E
    - CONFIG_DONE and CONFIG_LMMIC
    - ECLKDIVA and ECLKSYNCA
    - OSCE

  - **GPIO Pins** – For the LAV-AT device, each HPIO banks now have 1 EXT_RES dedicated pins.

- **IBIS Models** – IBIS has been enhanced to include sysCONFIG pins for the LAV-AT device.
- **Third-Party Simulation Tools** – Cadence Xcelium and Synopsys VCS now support the LAV-AT device.
- **MAP** – For all Nexus devices, mapper issues DRC if ECLKSYNC is missing from the ECLKDIV input.
- **Place & Route Timing Analysis** – Running PAR Timing Analysis is now required for Nexus devices.
- **Static Timing Analyzer (STA)** – The STA introduces automated multi-corner Static Timing Analysis reporting to all Nexus devices which eliminates manual operations.
    - While the PAR report includes multi-corner timing, it is recommended to run STA and analyze the timing results at each corner in the STA timing report.
- **CDC Register** – The CDC_register attribute allows you to constrain CDC (Clock Domain Crossing) synchronization registers for placement and timing analysis.
- **SEI Editor** – The multi-bit (2-bit) error option has been added to the SEI Editor for all Nexus devices.
- **Programmer**
    - To enable a robust Dual Boot and Ping-Pong functionality, the bitstream of LFMXO5-25, LFMXO5-55T, and LFMXO5-100T devices with embedded flash memory needs to be re-generated.
    - Deployment Tool now allows adding user data while generating Dual Boot and Ping-Pong features.
- **Strategies** – The default value of the GSR Infer strategy has been changed to “OFF” for Synplify, LSE, and MAP.
- **Block-Based Design** – The Exclusive option has been added to Physical Designer for reused macros.
- **IP Generator** – The IP Generator has been enhanced to be able to provide VHDL top-level file capability.
- **License File** – The TS_OK option has been enabled for Radiant subscription license. This option allows you to run the Radiant software on a remote connection.
- **File List** – In File List View, you can now manually set top-level modules by right-clicking on an input file.

- **Inclusive Language** – Radiant documentation has been partially updated to follow Lattice's Inclusive Language guidelines.
    - The following terms have been updated:
        - Master SPI has been changed to Controller SPI.
        - Slave SPI has been changed to Target SPI.
- **Simulation Wizard**
    - Simulation Wizard now supports the "-t" option. This option has been added to specify the time resolution of the simulator for VHDL resolution in mixed-language simulations.
    - The "sim_generate_script" Tcl command has been added for Simulation Wizard. You can use this command to generate any file types from your current Radiant project.
- **TCL Enhancement** – New Tcl commands have been added to support project and non-project flows.
    - STA Tcl commands have been added allowing you to query the timing database and generate timing reports or data without having to recompile the design.
- **Test Fixture Template** – The GSR instance has been added to the Test Fixture Template for Avant and Nexus devices.

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Radiant software, it may be necessary to re-create some IP, per the procedures described in the following table.

These procedures adapt the project for the changes in Radiant software.

Versions	IP			IP Regeneration Procedures
	Avant (LAV-AT-E)	**CrossLink-NX (LIFCL), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP), MachXO5-NX (LFMXO5)**	**iCE40UP**	
2023.2	1D Filter	OSC	N/A	These IP used in designs created in Radiant 2023.1 or earlier must be re-generated in Radiant 2023.2.
	Adder Tree	FIFO		
	FIFO	FIFO DC		
	FIFO DC	ADC		
	OSC	DDR Generic		
	DDR Generic	MIPI DPHY		
	GDDR 7:1	MPCS		
	DDRPHY	PLL		
	MIPI DPHY			
	MPPHY			
	PLL			
	RAM DP			
	RAM DP True			
	RAM SP			
	ROM			
	Shift Register			
	SEDC			

The following server IP are not compatible with Radiant 3.0 onwards. Use the latest versions of the IP available on the IP server:

- I2C Master version 1.0.3
- UART 16550 version 1.0.4
- DDR3 SDRAM Controller version 1.1.1
- DDR3 SDRAM Controller version 1.2.1
- LPDDR2 SDRAM Controller Lite version 1.1.1
- LPDDR2 SDRAM Controller Lite version 1.2.1

Supported Devices

Lattice Radiant software can be used with either a free license or a subscription license. The two licenses provide access to different device families.

Device Family	Free License	Subscription License
iCE40 UltraPlus (iCE40UP)	◀	
Lattice Avant (LAV-AT-E)		◀

Device Family	Free License	Subscription License
CertusPro™-NX (LFCPNX)	Evaluation Mode	◄
Certus™-NX (LFD2NX)	◄	
MachXO5™-NX (LFMXO5)	Evaluation Mode	◄
CrossLink-NX (LIFCL)	◄	
Certus™-NX-RT (UT24C)		RT Subscription
CertusPro™-NX-RT (UT24CP)		RT Subscription

Support for Third-Party Synthesis and Simulator Tools

The Synopsys Synplify Pro® for Lattice synthesis tool and the Siemens ModelSim® Lattice Edition simulator tools are included in the Radiant software.

- **Synopsys Synplify Pro FPGA synthesis software version U-2023.03LR-SP1**
  - Release Notes for Synplify Pro are located in ..\<*install_directory*>\radiant\2023.2\synpbase\doc\. The file name is release_notes.pdf.
  - A full set of documents for Synplify Pro are also located in ..\<*install_directory*>\radiant\2023.2\synpbase\doc\.
- **Siemens ModelSim Lattice Edition 2023.3 revision 2023.07**
  - Release Notes for ModelSim Lattice Edition are located in ..\<*install_directory*>\radiant\2023.2\modeltech\. The file names are RELEASE_NOTES.html or RELEASE_NOTES.txt.
  - A full set of documents for ModelSim Lattice Edition are located in ..\<*install_directory*>\radiant\2023.2\modeltech\doc\.
- **Siemens Questa® 2022.3**

- **Cadence Xcelium®**
  - The devices listed below are compatible with the following versions of Xcelium:
    - **23.03.003** – LAV-AT
    - **20.09.012 or earlier versions** – LFCPNX, LFD2NX, LFMXO5, LIFCL, UT24C, and UT24CP
- **Synopsys VCS® U-2023.03-SP2**

Help Resources

- Online Help updated with CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP), and Lattice Avant (LAV-AT) content.
- To view the Online Help, start the Lattice Radiant software and select the  "Getting Started" icon under Information Center.

  Note: The Firefox Snap install is not supported if you are using Ubuntu 20.04 or 18.04 to access the Radiant Help. This is a result of the snap install's inability to open local HTML pages. You may reinstall the latest version of Firefox using Apt install. For installation instructions, please refer to this guide.

System Requirements

The following shows the basic system requirements for Radiant software:

- Intel x86 64-bit or 64-bit-compatible PC
- OS Support:

64-bit OS	Radiant	Synplify Pro	ModelSim
Windows 10	✓	✓	✓
Windows 11	✓	✓*	✓*
Red Hat Enterprise Linux 7.9	✓	✓	✓
Red Hat Enterprise Linux 8.8	✓	✓	✓
Ubuntu version 18.04 LTS	✓	✓*	✓*
Ubuntu version 20.04 LTS	✓	✓*	✓*
CentOS 7.9	✓	✓	✓*
CentOS 8.4	✓	✓	✓*

***Note**: The third-party tools have been tested by Lattice on the listed platforms, but the vendors do not officially support them.

- Approximately 50 GB free disk space
- Computer Memory Requirement:
  - Nexus – 16GB
  - LAV-AT– 32GB Recommended for running a single project. If running multiple projects, the memory requirement will be higher.
- 1024 X 768 graphics display
- Network adapter for license and network connectivity
- A Web browser with JavaScript capability
- Acrobat Reader

Issues Fixed

The following known issues are fixed in this release. Their workarounds are no longer needed.

Synplify Pro Lattice OEM may take large amounts of Memory for designs involving large shift register chains.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-15024

Fixed in Radiant 2023.2

The post route simulation result when using LSE may be incorrect.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-17808

Fixed in Radiant 2023.2

Synthesis using Synplify Pro may output inconsistent netlist causing wrong results on the hardware.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-18907

Fixed in Radiant 2023.2

Memory initialization for Propel design through ECO Editor is not functional.

Devices affected: All devices

Bug number: DNG-18316, DNG-18383, DNG-18001

Fixed in Radiant 2023.2

Synthesis may crash when LSE is used in some cases.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-18634

Fixed in Radiant 2023.2

When MPCS is configured to G8B10B protocol, the Default M counter setting causes PLL to not lock.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-16258

Fixed in Radiant 2023.2

Radiant Programmer has slow operation time when performing operations via JTAG.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-18619

Fixed in Radiant 2023.2

When using Synplify Pro, different timing results are produced for the same design implemented on two different PCs.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-18139

Fixed in Radiant 2023.2

PAR warning - GPLL input pin is not considered as a dedicated clock pin on legal pins.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-17895

Fixed in Radiant 2023.2

State Reset should be added to Reveal TAP controller to solve the DONE pin de-assertion during continuous polling.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-17511

Fixed in Radiant 2023.2

Flash Header File generation in Deployment Tool takes ~330ms configuration time via self-download mode.

Devices affected: MachXO5-NX (LFMXO5)

Bug number: DNG-18165

Fixed in Radiant 2023.2

Incorrect vme file generated in the svf generation for JTAG chain.

Devices affected: All devices

Bug number: DNG-18130

Fixed in Radiant 2023.2

Unable to initialize and write data when setting up the Reveal Controller Memory setting using the pmi_ram_dp_true or the RAM_DP_True soft IP.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-17896

Fixed in Radiant 2023.2

MPCS IP that uses 8 lanes is failing RTL simulation.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-17709

Fixed in Radiant 2023.2

When defining macros for modules that are in plaintext (non-encrypted) and when exporting macros, you may encounter an IP license string issue.

Devices affected: All devices

Bug number: DNG-17878

Fixed in Radiant 2023.2

Timing Analyzer still reports the IO as unconstrainted even if set_input_delay is correctly applied in timing report.

Devices affected: All devices

Bug number: DNG-17559

Fixed in Radiant 2023.2

Set_false_path constraint from clock to cell causes a false path to all clocks in the design.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-17650

Fixed in Radiant 2023.2

When using LFCPNX LPDDR4 IP, synthesis outputs a "No Lattice Encryption Key found for encrypted Module" warning.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-16873

Fixed in Radiant 2023.2

After running Reveal Logic Analyzer/Controller, Programmer may fail to access the cable to detect, scan, or download.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-17592

Fixed in Radiant 2023.2

With the latest version of Synplify Synthesis tool, preaddsub structures and presub structures are not able to be packed into the DSP primitives in inference.

Devices affected: Lattice Avant (LAV-AT-E)

Bug number: DNG-16587

Fixed in Radiant 2023.2

When generating IBIS models for LAV-AT-E, you may encounter warning messages indicating that it is not available for output or bidirectional signals. Even if you can generate IBIS models for input signal, it still produces an error.

Devices affected: Lattice Avant (LAV-AT-E)

Bug number: DNG-15472

Fixed in Radiant 2023.2

Known Issues for Radiant 2023.2

The following are known issues for the Radiant Software 2023.2.

You may encounter the following issues when using SEI Editor on different devices.

1. **Nexus devices (LIFCL-17K, LFD2NX-17K, and LFMXO5-25K) cannot support SEI 2-bit with Unused strategy for combinations such as EBR-EBR or DSP-DSP.**
2. **The requirement for SEI 2-bit is that both error bits should be in the same data frame. The data frame corresponds to the FPGA column with reference to the "array" architecture.**
3. **In Nexus architecture, any device with a density less than 30K has only 1 EBR or 1 DSP per column. Due to this limitation, it cannot support multiple error injection on an EBR or DSP site for these densities.**
4. **However, those device densities can support SEI 2-bit Random strategy combinations and SEI 2-bit PFU-PFU combination with Unused strategy.**

			Nexus	
SEI	**1-bit**	**2-bit**	**Density >= 30K**	**Density < 30K**
Random	Supported	Supported		
Unused	Supported	Supported	EBR-EBR	PFU-PFU
			DSP-DSP	
			PFU-PFU	

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-19715

IBIS reports I/O models of some sysCONFIG pins even if they are used as GPIO.

Workaround: Remove duplicated pins in IBIS file.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19646

Cadence Xcelium does not correctly recognize the number of ports on a user defined primitive.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CrossLink-NX (LIFCL-33U)

Bug number: DNG-19623

IBIS generated string for MCLKP/N always sets the PULLMODE value to None.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19472

When using SEDC module from the IP Catalog, or when instantiating the SEDCA primitive, the "sedc_busy_o" (IP) or "SEDCBUSY" (primitive) signal will not assert in simulation.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19456

Bitstream generation will fail when selecting either "Hex File" or "NVCM File" formats in the Bitstream Settings menu.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: iCE40UP

Bug number: DNG-19371

Avant input I/O cannot be set as MIPI_DPHY type.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19199

An error occurs when compiling libraries using Xcelium version 23.03.003.

Workaround: Use Xcelium 20.09.012 or earlier versions.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-18594, DNG-19007

Place & Route has a repeatability issue when running the same design on the same or different machine.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-16544

When using LSE, post-synthesis engine may fail with the following error: “ERROR <1025017> - Not user declared module (VERIFIC_AND).”

This error occurs when the MOD operator is used.

Workaround: Replace the MOD operator to avoid this issue.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-16713

The PHASEDIR function of PLL does not work, the phase shift of CLKOS is still delayed when PHASEDIR = 1.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-16440

When using ModelSim to run Post-Route Gate-Level or Post-Route Gate-Level+Timing simulation, Modelsim may crash if you use a large design file, with error message “Fatal: (vsim-4) ****** Memory allocation failure.”

Workaround: Use QuestaSim 64-bit version.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-14945

Synplify Pro Lattice OEM (*.srr and *.srf files) may incorrectly report the number of LRAMs for the target device.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CertusPro-NX (LFCPNX-50)

Bug number: DNG-16362

When simulating Cordic IP using ModelSim, you may encounter an RTL compilation error.

Workaround: In OEM ModelSim, use the “vsim -voptargs=+acc -L work -L pmi_work -L ovi_lifcl tb_top -suppress 8607” command to finish the compilation.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-14888

Reveal Power-on Reset (POR) Debug function does not work when using LSE with only one Trigger Unit (TU).

Workaround: Add another Trigger Unit that can be unrelated to POR Debug.

Devices affected: All devices except iCE40UP

Bug number: DNG-13901

The CSI-2/DSI D-PHY Transmitter and Receiver Soft IP simulations fail when using Synopsys VCS as simulation tool.

Workaround: Use Modelsim or QuestaSim simulation tools.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-13225

When simulating Generic DDR, there may be a mismatch in the RTL and post-route simulation. Silicon is not affected.

Workaround:

For Nexus devices, intrinsic delay similar to the delay value on the vo.vo file needs to be added to the IP testbench.

For Avant devices, overwrite the delay parameter values of the primitives used on the GDDR instance with the same value from the generated RTL on the generated post-PAR netlist. This should only be done for simulation purposes.

Devices affected: All devices except iCE40UP

Bug number: DNG-9639, DNG-18794

MAP incorrectly reports number of DPHY and PCIE/ADC resources for CrossLink-NX (LIFCL) QFN72 package.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-8297