DisplayPort IP

IP Version: 2.2.0

User Guide

FPGA-IPUG-02236-1.6

June 2026

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Contents

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Figures

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Tables

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AHB	Advanced High-performance Bus
API	Application Programming Interface
ASSR	Alternate Scrambler Seed Reset
AUX	Auxiliary Transaction
AXI	Advanced Extensible Interface
BE	Blanking End
BER	Bit Error Rate
BPC	Bits per Color Component
BPP	Bits per Pixel
BS	Blanking Start
DP	DisplayPort
DPCD	DisplayPort Configuration Data
DPRX, DP Rx	DisplayPort Receiver
DPTX, DP Tx	DisplayPort Transmitter
DSC	Display Stream Compression
DVI	Digital Visual Interface
EBR	Embedded Block RAM
EDID	Extended Display Identification Data
eDP	Embedded DisplayPort
EOL	End of Line
FIFO	First In First Out
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
FPS	Frames per Second
Gbps	Gigabits per Second
GUI	Graphical User Interface
GUID	Globally Unique Identifier
HDCP	High-bandwidth Digital Content Protection
HDL	Hardware Description Language
HDTV	High-Definition Television
HPD	Hot Plug Detect
I2C	Inter-Integrated Circuit
IP	Intellectual Property
LFSR	Linear Feedback Shift Register
LMMI	Lattice Memory Mapped Interface
LPCM	Linear Pulse Code Modulation
MC	Microcontroller
MSA	Main Stream Attribute
MST	Multi Stream Transport
MTP	Multi Transport Packet
PC	Personal Computer
PCS	Physical Coding Sublayer
PDC	Physical Design Constraints
PHY	Physical Layer
PLL	Phase-Locked Loop

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Abbreviation	Definition
PMA	Physical Medium Attachment
PPC	Pixels per Clock
RBR	Reduced Bit Rate
RGB	Red Green Blue
SDC	Synopsys Design Constraints
SE	Secondary End
SoC	System on Chip
SOF	Start of Frame
SST	Single Stream Transport
SR	Scrambler Reset
SS	Secondary Start
TPS	Training Pattern Sequence
TS	Time Slot
TU	Transfer Unit
UART	Universal Asynchronous Receiver-Transmitter
UVSI	Unified Video Streaming Interface
VB-ID	Vertical Blanking ID
VESA	Video Electronics Standards Association
VGA	Video Graphic Array

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

1. Introduction

1.1. Overview of the IP

The Lattice™ DisplayPort™ IP core is designed for transmission and reception of serial-digital video for consumer and professional displays. This IP helps you to implement a DisplayPort video interface as defined by the Video Electronics Standards Association (VESA) DisplayPort specifications. DisplayPort is a high-speed serial interface standard supported by industry leaders in consumer electronics high-definition television (HDTV), personal computer (PC) laptop, and PC monitors. This protocol is considered as a successor to video graphic array (VGA) and digital visual interface (DVI) standards with support for video resolutions up to 4K video and multi-channel audio.

The Lattice DisplayPort IP core supports scalable main link with 1.62 Gbps, 2.7 Gbps, 5.4 Gbps, and 8.1 Gbps lane rates and number of lane count in 1, 2, or 4 lanes.

1.2. Quick Facts

Table 1.1. Summary of the DisplayPort IP

IP Requirements	Supported Devices	CertusPro™-NX, Lattice Avant™[1] (Avant-G, Avant-X), Certus™-N2 (except LN2-CT-20ES)
	IP Changes[2]	Refer to the DisplayPort IP Release Notes (FPGA-RN-02071).
Resource Utilization	Supported User Interface	AXI4-Lite, AXI4-Stream
	Resources	Refer to Appendix A. Resource Utilization.
Design Tool Support	Lattice Implementation	IP core v2.2.0 – Lattice Radiant™ software 2026.1 IP core v2.2.0 – Lattice Propel™ software 2026.1
	Synthesis	Synopsys® Synplify Pro® for Lattice
	Simulation	QuestaSim™
Driver Support	API Reference	Refer to the DisplayPort Driver API Reference (FPGA-TN-02423).

Notes:

1. Excluding engineering sample (ES) devices.
2. In some instances, the IP may be updated without changes to the user guide. This user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

1.3. IP Support Summary

Table 1.2. DisplayPort IP Support Readiness

Device Family	Simulation	Timing
CertusPro-NX	Yes	Final
Avant-G, Avant-X	Yes	Preliminary
Certus-N2	Yes	Preliminary

Note:

1. Preliminary hardware validation is performed on a setup that is different from the setup in the Example Design section.

The example design for the DisplayPort IP allows for simulation and deployment to development boards for testing. Refer to the Example Design section for more details on how to run the example design on hardware and simulation.

1.4. Features

Key features of the DisplayPort IP are as follows:

- Selectable transmit/receive modes: Tx only, Rx only, and both Tx and Rx
- Static pixels per clock (PPC): 4
- Dynamic lane rates of 1.62, 2.7, 5.4, and 8.1 Gbps
- Dynamic 1, 2, and 4 lanes support

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

- Dynamic bits per color component (BPC): 6, 8, 10, 12, and 16
- Dynamic video resolution
- Dynamic color space format: RGB, YCbCr444, YCbCr422
- Single stream transport (SST)
- Progressive video types
- Embedded DisplayPort (eDP), including enhance framing, alternate scrambler seed reset (ASSR), and reduced auxiliary transaction (AUX) timing
- Bi-directional AUX channel for extended display identification data (EDID) and DisplayPort configuration data (DPCD) registers
- Hot plug detect (HPD) support between source and sink
- AXI4-Stream for video interface
- AXI4-Lite for register interface

1.5. Licensing and Ordering Information

An IP specific license string is required to enable full use of the DisplayPort IP in a complete, top-level design.

The IP can be fully evaluated through functional simulation and implementation (synthesis, map, place and route) without an IP license string. This IP supports Lattice IP hardware evaluation capabilities. You can create versions of the IP to operate in hardware for a limited time (approximately four hours) without requiring an IP license string. A license string is required to enable timing simulation and to generate a bitstream file that does not include the hardware evaluation timeout limitation.

For more information about pricing and availability of the DisplayPort IP, contact your local Lattice Sales Office.

1.5.1. Ordering Part Number

Table 1.3. Ordering Part Number

Device Family	Part Number	
	Single Seat Annual License	Single Seat Perpetual License
CertusPro-NX	DPORT-CPNX-US	DPORT-CPNX-UT
Avant-G	DPORT-AVG-US	DPORT-AVG-UT
Avant-X	DPORT-AVX-US	DPORT-AVX-UT
Certus-N2	DPORT-CN2-US	DPORT-CN2-UT

1.6. Minimum Device Requirements

The table below shows the minimum device requirements for the DisplayPort IP.

Table 1.4. Minimum Device Requirements for DisplayPort IP

Device Family	Link Speed	Speed Grade
CertusPro-NX	8.1 Gbps	9_High-Performance_1.0V
	8.1 Gbps[1]	8_High-Performance_1.0V
	5.4 Gbps	7_High-Performance_1.0V
Avant-X / Avant-G	8.1 Gbps	All speed grades
Certus-N2	8.1 Gbps	All speed grades

Note:

1. Speed grade 8 only supports up to 8 BPC at 8.1 Gbps and supports 10 BPC and above for up to 5.4 Gbps.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

1.7. Naming Conventions

1.7.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.7.2. Signal Names

Signal names that end with:

- _*n* are active low signals (asserted when value is logic 0)
- _*i* are input signals
- _*o* are output signals

1.7.3. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2. Functional Description

2.1. IP Architecture Overview

The Lattice DisplayPort IP includes Physical Layer and Data Link Layer. The IP supports scalable main link with 1, 2, or 4 lanes, and data rates at 1.62 Gbps, 2.7 Gbps, 5.4 Gbps, and 8.1 Gbps. The Lattice DisplayPort IP supports Unified Video® streaming based on AXI-Stream protocol for video data transport and AXI-Lite for IP register access.

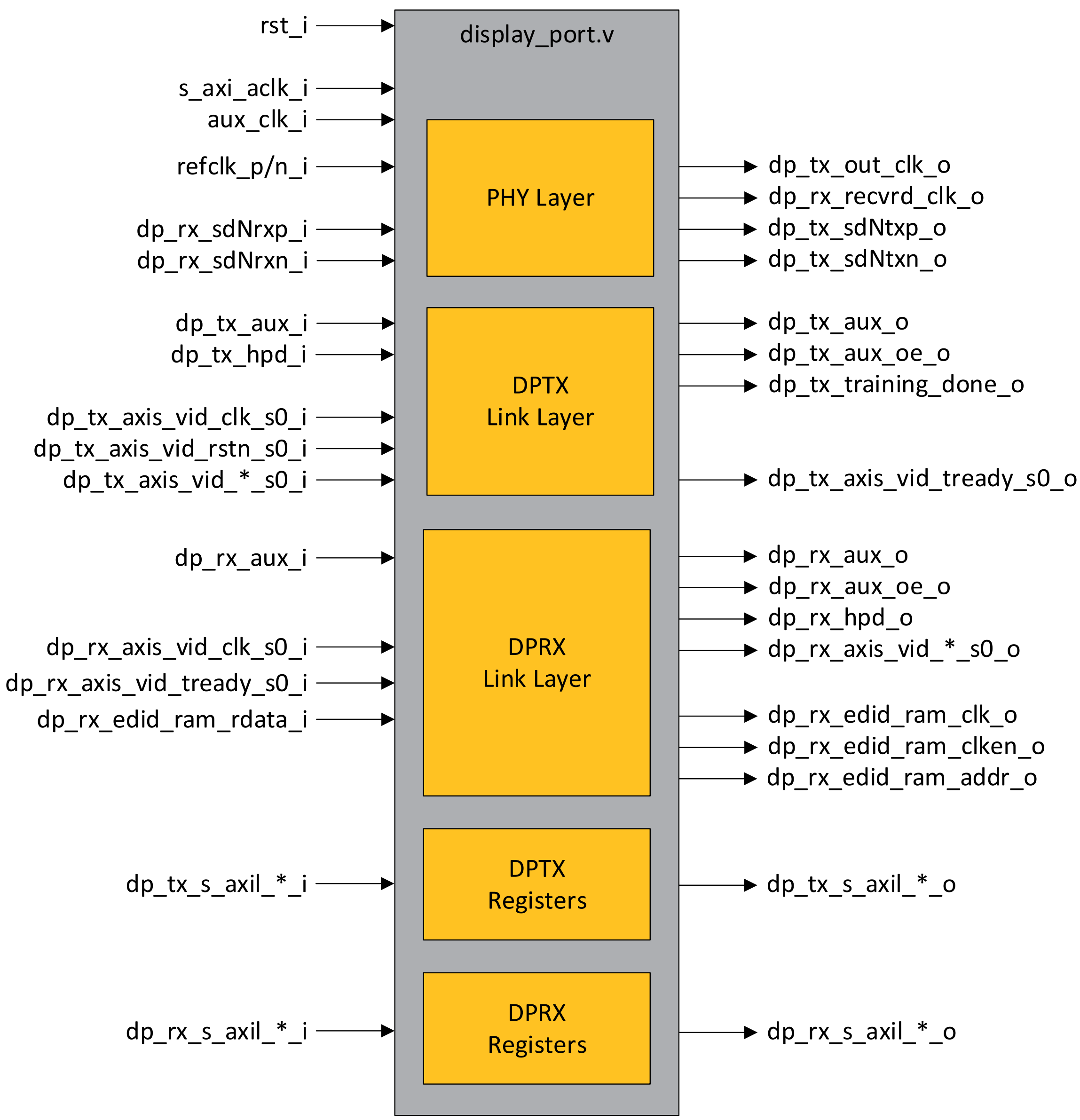


Figure 2.1. Lattice DisplayPort IP Core Block Diagram

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2.2. DisplayPort Source

The DisplayPort source consists of a link training controller for link training handshaking with the downstream DisplayPort sink and video pipeline components to encode the video data into the main link transport.

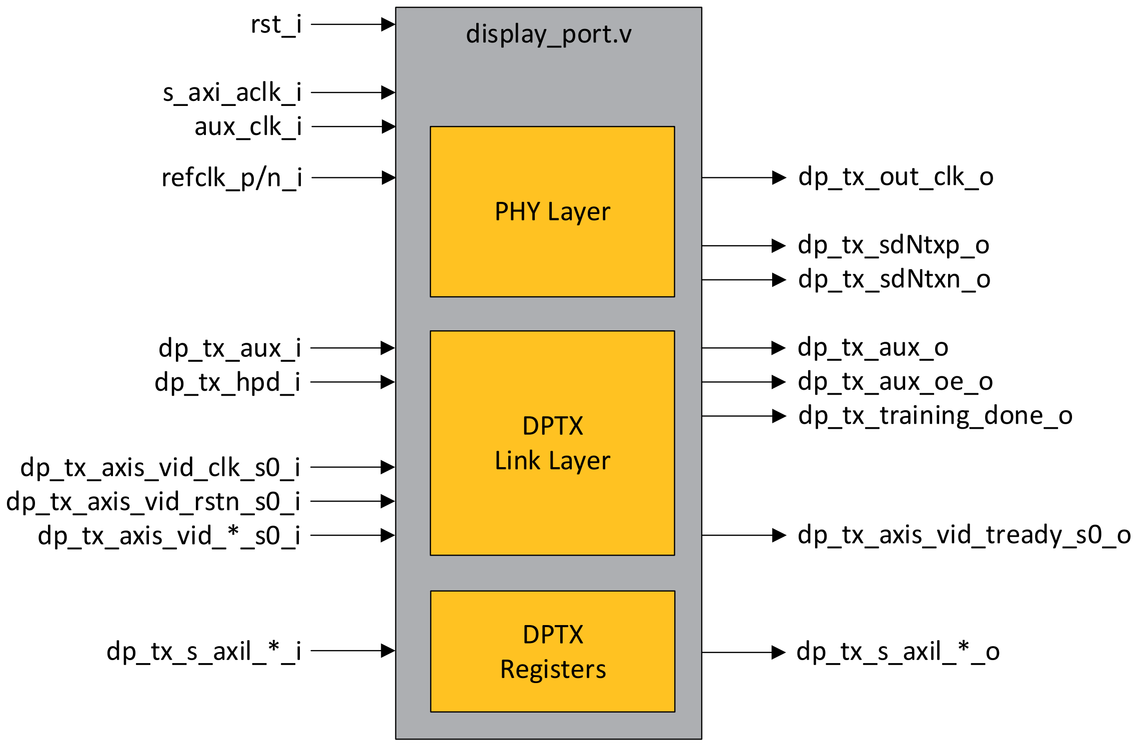


Figure 2.2. Lattice DisplayPort IP Source Interface

DisplayPort source supports the Lattice Unified Video streaming protocol for video streaming transport and encodes video data into the DisplayPort main link transport. Refer to the Unified Video Streaming Interface section for the video streaming protocol.

The main link data path consists of a video streaming interface, video packetizer, and link training pattern generator. The video streaming interface crosses the video data from the video clock domain into the link speed clock domain, and the frequency depends on the link rate trained. The pixel steering and pixel packer components align and remap the video data to the DisplayPort main link data path protocol described in the VESA DisplayPort specifications. The DisplayPort source always packetizes video data into fixed 64 symbols transfer unit (TU) size.

On the link training controller, DisplayPort source autonomously initiates link training based on the following sequence:

1. On HPD detection, DisplayPort source sets downstream sink device power state to D0 (address 0x00600 to value 0x01).
2. DisplayPort source reads downstream sink device DPCD capabilities register (0x00000–0x0000E).
3. DisplayPort source initiates link training sequence by writing to sink device DPCD configuration register (0x00100–0x00106) to configure the link bandwidth, lane count, training pattern sequence of the sink device according to the VESA DisplayPort standard.
4. After waiting for the TRAINING_AUX_RD_INTERVAL period (0x0000E), DisplayPort source polls for the link training status of the sink device.
5. When link training is successful, DisplayPort source ends the link training sequence and switches to video streaming.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2.3. DisplayPort Sink

The DisplayPort sink consists of a link training component for link training handshaking with the upstream DisplayPort source and video pipeline components to decode the video data from the main link transport and output to the video interface.

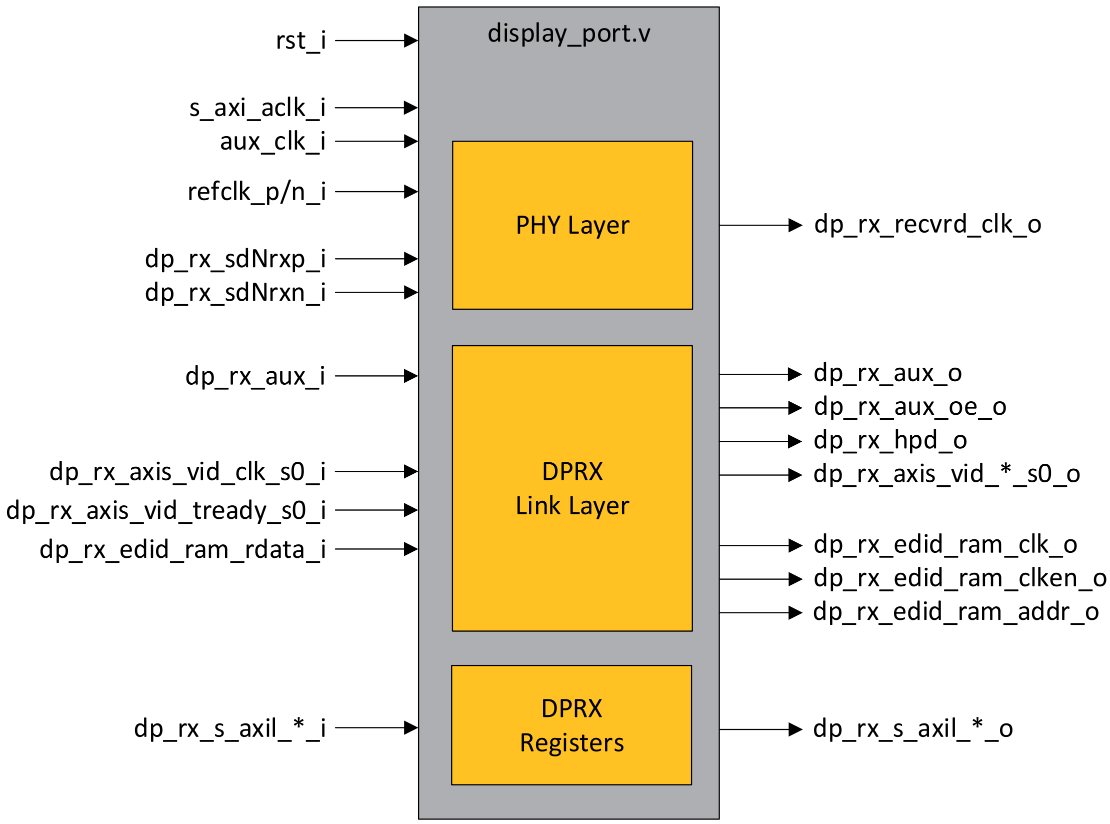


Figure 2.3. Lattice DisplayPort IP Sink Interface

The DisplayPort sink receives main link data from the Physical Layer 8b10b decoder and decodes the main link data according to the DisplayPort stage. During link training period, DisplayPort sink link training module is responsible to detect the training pattern sequence 1, 2, 3, or 4 and perform interlanes deskew to align the main link data across all lanes. In each training pattern sequence, DisplayPort link training module updates the sink device DPCD status registers according to CR_DONE, SYM_LOCKED, and INTERLANE_ALIGN_DONE status. When link training is successful, upstream source reads the status and switches from link training to video streaming. DisplayPort sink decodes the main link data to obtain vertical blanking ID (VB-ID), main stream attribute (MSA), and video streaming data. DisplayPort sink axis interface module crosses decoded video data from the link speed clock domain to the video clock domain.

DisplayPort sink supports Lattice Unified Video streaming protocol for video streaming transport. Refer to the Unified Video Streaming Interface section for the video streaming protocol. DisplayPort sink video stream does not support backpressure when video streaming starts. The downstream TREADY must be asserted until the end of the video streaming.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2.4. Unified Video Streaming Interface

This section describes Lattice Unified Video streaming protocol which is based on the AXI4-Streaming protocol. The DisplayPort IP only supports the Lattice Unified Video streaming protocol. This section explains the video interface pins and video data mapping to TDATA. For more information about the interface signals, refer to the Signal Description section.

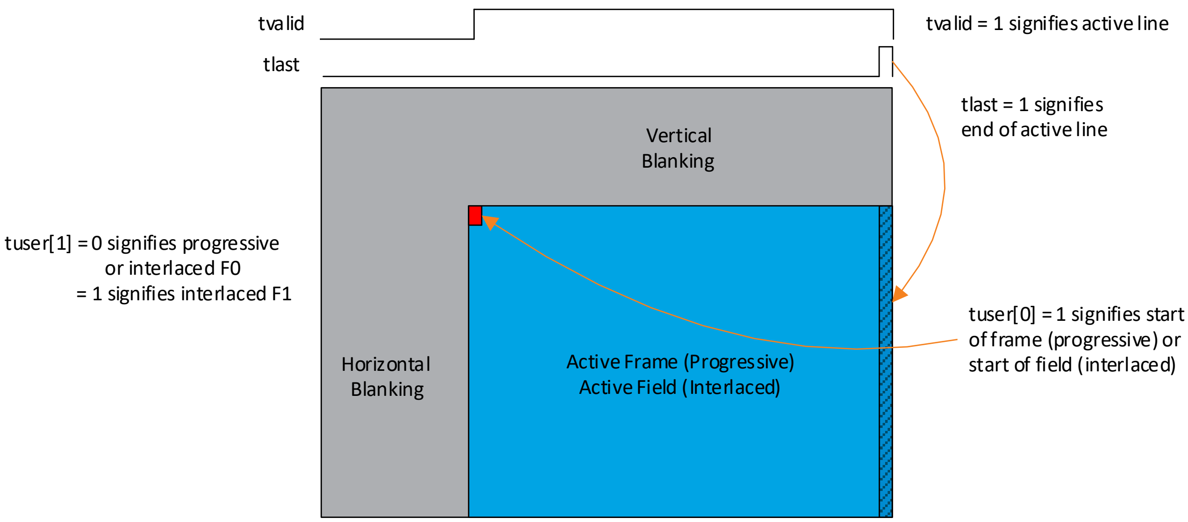


Figure 2.4. Video Timing to Unified Video Streaming Mapping

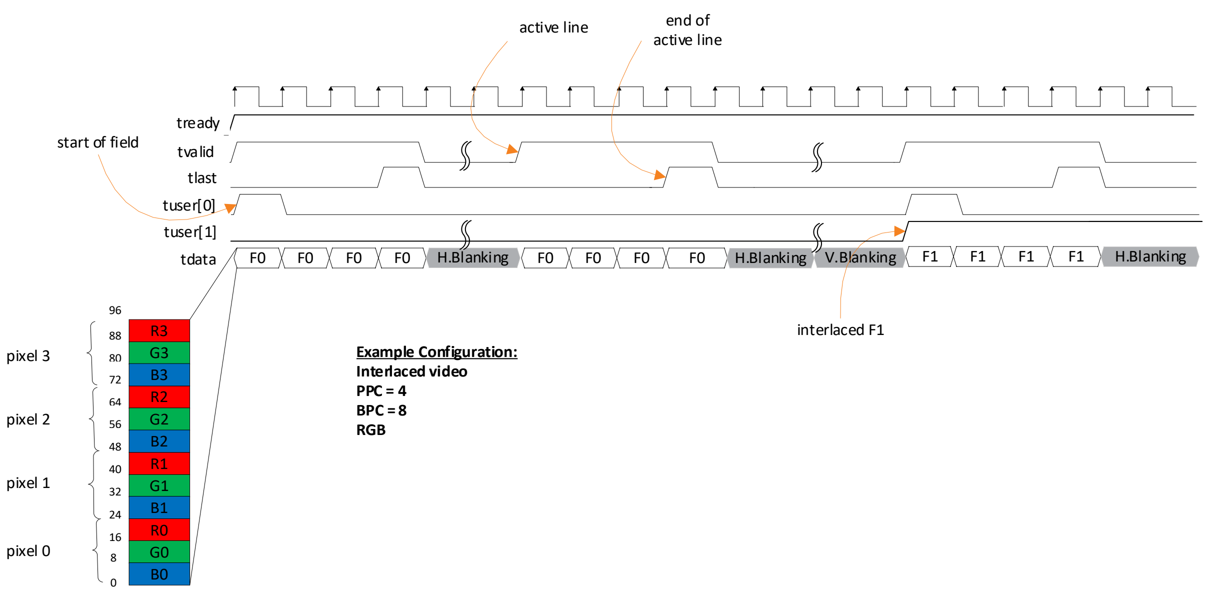


Figure 2.5. Unified Video Streaming Timing Diagram

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2.4.1. TDATA Pixel Mapping

The Unified Video Streaming Interface (UVSI) TDATA is always aligned and TDATA width depends on the MAX_BPC and PPC. The table below summarizes the TDATA_WIDTH.

Table 2.1. Unified Video Streaming TDATA Width Mapping

MAX_BPC	PPC = 1	PPC = 2	PPC = 4
	TDATA_WIDTH		
6	24	48	96
8	24	48	96
10	32	64	128
12	40	80	160
16	48	96	192

The diagrams below show the pixel component mapping to UVSI TDATA with respect to each BPC and color format for each PPC. RGB and YCbCr444 share the same mapping. For YCbCr444, replace R with Cr, G with Y, and B with Cb.

In the figures, the color format is indicated as follows:

- Red = R
- Green = G
- Blue = B
- Yellow = Y
- Blue/red = Cb or Cr
- White = padding

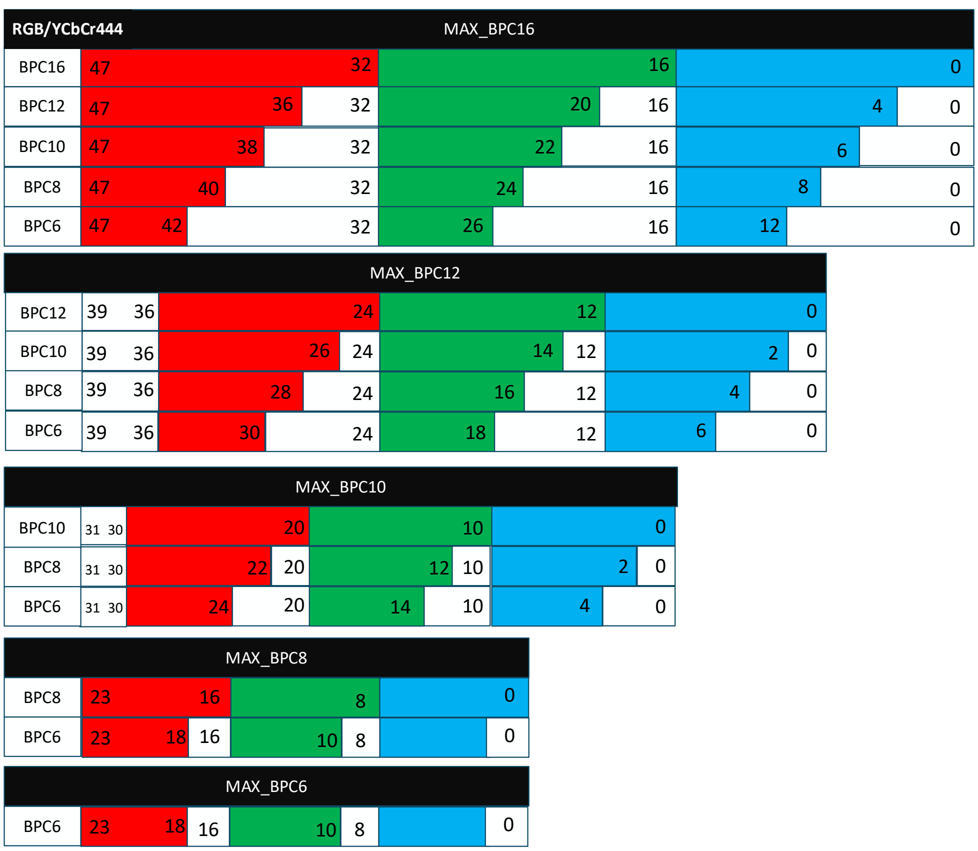


Figure 2.6. RGB/YCbCr444 Mapping

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Figure 2.7. YCbCr422 Mapping

2.5. Clocking Overview

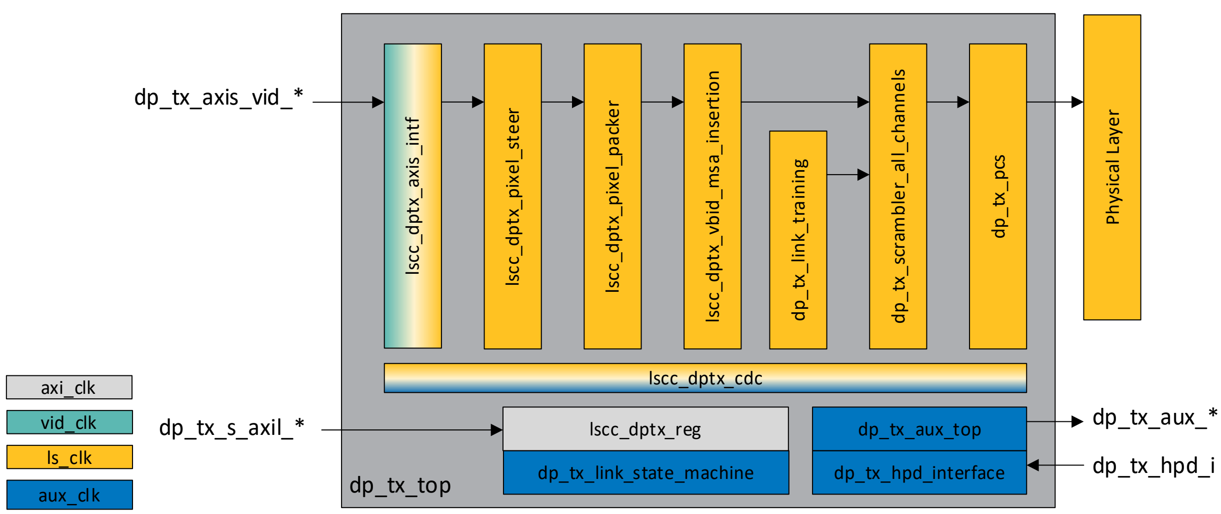


Figure 2.8. Lattice DisplayPort IP Source Block Diagram

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

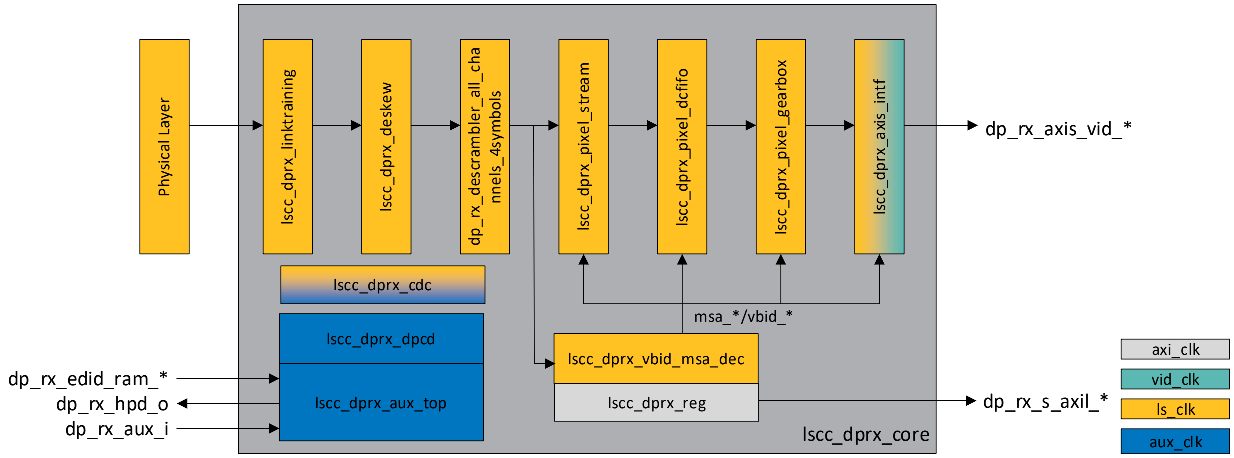


Figure 2.9. Lattice DisplayPort IP Sink Block Diagram

2.6. Reset

DisplayPort IP uses a single reset for all components within the IP.

Table 2.2. Component Reset in DisplayPort IP

Reset	Type	Component To Be Reset				
		axis_intf	aux	CSR (AXI-Lite)	Link Layer	PHY Layer
rst_i	Pin	Tx and Rx	Tx and Rx	Tx and Rx	Tx and Rx	Tx and Rx
dp_tx_axis_vid_rstn_s0_i	Pin	Tx only	No	No	No	No

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

3. IP Parameter Description

The configurable attributes of the DisplayPort IP are shown in the following tables. You can configure the IP by setting the attributes accordingly in the IP Catalog Module/IP Block Wizard of the Lattice Radiant software.

Wherever applicable, default values are in bold.

3.1. General

Table 3.1. General Attributes

Attribute	Selectable Values	Description
General		
Mode	**Tx and Rx** Tx only Rx only	Selects DisplayPort mode in duplex mode, Tx only simplex mode, or Rx only simplex mode.
Lattice Hardware Specific Options		
PHY PCS Lane ID	**0**–7, AUTO	Specifies the location of the first lane of the Physical Coding Sublayer (PCS) instance. Dependency on RX or TX MAX_LANE_COUNT.
PHY Refclk Select	0 or **1**	0: Selects sd_ext_0_refclk. 1: Selects sd_ext_1_refclk. Clock routing is handled by the DisplayPort IP on parameter selection.
Swap lanes 0 and 1 for Tx	Unchecked **Checked**	Enables Tx serial data swap position between lane0 and lane1. This attribute is checked when using the Lattice DisplayPort FPGA mezzanine card (FMC) because of the FMC board design requirement.
Swap lanes 2 and 3 for Tx	Unchecked **Checked**	Enables Tx serial data swap position between lane2 and lane3. This attribute is checked when using the Lattice DisplayPort FMC because of the FMC board design requirement.
Invert lanes 2 and 3 for Tx	Unchecked **Checked**	Inverts Tx serial data lane2 and lane3 polarity. This attribute is checked when using the Lattice DisplayPort FMC because of the FMC board design requirement.
Swap lanes 0,1,2,3 for Rx	Unchecked **Checked**	Reverses Rx serial data lane position from Lane0, 1, 2, 3 to Lane3, 2, 1, 0. This attribute is checked when using the Lattice DisplayPort FMC because of the FMC board design requirement.
Invert all lanes for Rx	Unchecked **Checked**	Inverts all Rx serial data lane polarity. This attribute is checked when using the Lattice DisplayPort FMC because of the FMC board design requirement.
DP RX Settings		
DP RX – IP Capability		
Maximum Lane Count	1, 2, **4**	Selects supported maximum lane count: 1, 2, or 4 lanes.
Maximum Link Rate (Gbps)	1.62, 2.7, 5.4, **8.1**	Selects supported maximum link rate: 1.62, 2.7, 5.4, or 8.1 Gbps.
AXI4-Lite DPRX Register Enable	**Unchecked** Checked	Enables DPRX registers and AXI4-Lite interface.
eDP Enable	**Unchecked** Checked	Enables or disables eDP mode.
Pixels per Clock (PPC)	**4**	Supports only 4 pixels per clock. Not editable. For information only.
DP RX – Video Interface		
Video Interface	**Unified Video Streaming**	Supports only the Lattice Unified Video Streaming (AXI4-Stream) interface. Not editable. For information only.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Attribute	Selectable Values	Description
DP RX – Color Format		
Maximum Bits per Component (BPC)	6, **8**, 10, 12, 16	Selects the maximum BPC support. Allows you to disable in DPRX support BPC parameter.
DPRX Support 6BPC	**Unchecked** Checked	Enables or disables 6 BPC support when maximum BPC is bigger than 6 BPC. YCbCr422 does not support 6 BPC.
DPRX Support 8BPC	Unchecked **Checked**	Enables or disables 8 BPC support when maximum BPC is bigger than 8 BPC.
DPRX Support 10BPC	**Unchecked** Checked	Enables or disables 10 BPC support when maximum BPC is bigger than 10 BPC.
DPRX Support 12BPC	**Unchecked** Checked	Enables or disables 12 BPC support when maximum BPC is bigger than 12 BPC.
DPRX Support 16BPC	**Unchecked** Checked	Enables or disables 16 BPC support.
DPRX Support RGB and YCbCr444	Unchecked **Checked**	Enables support for RGB. YCbCr444 shares the same decoding as RGB.
DPRX Support YCbCr422	**Unchecked** Checked	Enables support for YCbCr422.
DP RX – eDP IP Capability		
eDP Support ASSR	Unchecked **Checked**	Selects eDP sink capability to support eDP ASSR.
eDP Reduced AUX Timing	**Checked**	Always supports reduced AUX timing when eDP mode is enabled. Not editable. For information only.
eDP Fast Link Training	**Unchecked**	eDP fast link training mode is not supported. Not editable. For information only.
DP TX Settings		
DP TX – IP Capability		
Maximum Lane Count	1, 2, **4**	Selects supported maximum lane count: 1, 2, or 4 lanes.
Maximum Link Rate (Gbps)	1.62, 2.7, 5.4, **8.1**	Selects supported maximum link rate: 1.62, 2.7, 5.4, or 8.1 Gbps.
AXI4-Lite DPTX Register Enable	**Unchecked** Checked	Enables DPTX registers and AXI4-Lite interface.
eDP Enable	**Unchecked** Checked	Enables or disables eDP mode.
Pixels per Clock (PPC)	**4**	Supports only 4 pixels per clock. Not editable. For information only.
DP TX – Video Interface		
Video Interface	**Unified Video Streaming**	Supports only the Lattice Unified Video Streaming (AXI4-Stream) interface. Not editable. For information only.
DP TX – Color Format		
Maximum Bits per Component (BPC)	6, **8**, 10, 12, 16	Selects the maximum BPC support. Allows you to disable in DPTX support BPC parameter.
DPTX Support 6BPC	**Unchecked** Checked	Enables or disables 6 BPC support when maximum BPC is bigger than 6 BPC. Enable DPTX registers to support multiple BPCs. YCbCr422 does not support 6 BPC.
DPTX Support 8BPC	Unchecked **Checked**	Enables or disables 8 BPC support when maximum BPC is bigger than 8 BPC. Enable DPTX registers to support multiple BPCs.
DPTX Support 10BPC	**Unchecked** Checked	Enables or disables 10 BPC support when maximum BPC is bigger than 10 BPC. Enable DPTX registers to support multiple BPCs.
DPTX Support 12BPC	**Unchecked** Checked	Enables or disables 12 BPC support when maximum BPC is bigger than 12 BPC. Enable DPTX registers to support multiple BPCs.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Attribute	Selectable Values	Description
DPTX Support 16BPC	**Unchecked** Checked	Enables or disables 16 BPC support. Enable DPTX registers to support multiple BPCs.
DPTX Support RGB and YCbCr444	Unchecked **Checked**	Enables support for RGB. YCbCr444 shares the same encoding as RGB.
DPTX Support YCbCr422	**Unchecked** Checked	Enables support for YCbCr422.
DP TX– eDP IP Capability		
eDP Support ASSR	**Checked**	Always supports ASSR when eDP mode is enabled. Not editable. For information only.
eDP Reduced AUX Timing	**Checked**	Always supports reduced AUX timing when eDP mode is enabled. Not editable. For information only.
eDP Fast Link Training	**Unchecked**	eDP fast link training mode is not supported. Not editable. For information only.
TX Video Settings		
Set MSA based on default resolution	Unchecked **Checked**	Checks to select default resolution based on predefined resolution.
Default Resolution	3840x2160p60,RGB,8BPC, **1920x1080p60,RGB,8BPC**, 1280x720p60,RGB,8BPC	Predefined resolution.
Color Format	RGB, YCbCr444, YCbCr422	Default color format configuration for IP initialization. Selects between RGB(Legacy), YCbCr444(ITU601), or YCbCr422(ITU601). Affects MISC0 MSA and can be overwritten using TX registers.
Video Stream Clock Frequency (MHz)	148.5	Auto calculated actual video stream clock. Not editable. For information only.
Main Stream Attribute		
Total Horizontal Size	2200	Unchecks *Set MSA based on default resolution* to customize default video resolution.
Total Vertical Size	1125	
Horizontal Width	1920	
Vertical Height	1080	
Horizontal Active Start	192	
Vertical Active Start	42	
Horizontal Sync Width	44	
Vertical Sync Width	5	
Frame Rate (Hz)	60	

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

4. Signal Description

This section describes the DisplayPort IP ports.

4.1. Signal Interface

Table 4.1. Signal Ports

Port	Type	Width	Description
rst_i	Input	1	DisplayPort IP global reset pin (active high). Resets the entire DisplayPort IP including the PHY Layer and Link Layer.
s_axi_aresetn_i	Input	1	Resets for the DisplayPort management and FSM logic. **Note**: This port is removed in the DisplayPort IP version 2.2.0 onwards. Any reset must go through the rst_i port.
s_axi_aclk_i	Input	1	DisplayPort management and FSM clock including the AXI4-Lite register interface and PHY LMMI interface. Requires free running at 100 MHz.
refclk_p_i	Input	1	MPCS PHY Physical Medium Attachment (PMA) REFCLK source from external REFCLK. For CertusPro-NX devices: When *PHY Refclk Select* is set 0, refclk is mapped to sd_ext_0_refclk. When *PHY Refclk Select* is set 1, refclk is mapped to sd_ext_1_refclk. Refclk frequency required for HBR3, HBR2, and HBR is 135 MHz. Refclk frequency required for RBR is 81 MHz. For Avant-G/X and Certus-N2 devices: Refclk frequency required is 135 MHz across all bit rates.
refclk_n_i	Input	1	
aux_clk_i	Input	1	DP IP AUX channel clock. Requires free running at 100 MHz. Use the same clock source as s_axi_aclk_i.
dp_rx_axis_vid_clk_s0_i	Input	1	DisplayPort video clock. Frequency must be equal to or higher than the actual video clock calculated by resolution. Recommend fixing video clock at 150 MHz (PPC = 4) to support any resolution equal to or lower than 4K60 without the need to reconfigure the video frequency.
dp_tx_axis_vid_clk_s0_i	Input	1	DisplayPort video clock. Frequency must be equal to or higher than the actual video clock calculated by resolution. Recommend fixing video clock at 150 MHz (PPC = 4) to support any resolution equal to or lower than 4K60 without the need to reconfigure the video frequency.
dp_rx_recvrd_clk_o	Output	1	DisplayPort Rx recovered clock. Also known as Rx link speed clock.
dp_tx_out_clk_o	Output	1	DisplayPort Tx recovered clock. Also known as Tx link speed clock.
dp_tx_sdNtxp_o	Output	1	DisplayPort Tx serial data out (positive pin). N representing number of channel.
dp_tx_sdNtxn_o	Output	1	DisplayPort Tx serial data out (negative pin). N representing number of channel.
dp_rx_sdNrxp_i	Input	1	DisplayPort Rx serial data in (positive pin). N representing number of channel.
dp_rx_sdNrxn_i	Input	1	DisplayPort Rx serial data in (negative pin). N representing number of channel.
dp_tx_aux_o	Output	1	Tx AUX channel data output.
dp_tx_aux_oe_o	Output	1	Tx AUX channel output buffer enable.
dp_tx_aux_i	Input	1	Tx AUX channel data input.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Port	Type	Width	Description
dp_tx_hpd_i	Input	1	Tx hot plug detect input.
dp_tx_training_done_o	Output	1	Tx link training completed. Active high signal.
dp_tx_axis_vid_rstn_s0_i	Input	1	Video stream reset (active low). Resets video stream pipeline.
dp_tx_axis_vid_tvalid_s0_i	Input	1	Indicates TDATA is valid. 0: Indicates TDATA is invalid. 1: Indicates TDATA is valid.
dp_tx_axis_vid_tdata_s0_i	Input	N	Video data width is byte aligned. N = ceil(BPP/8) × 8 × PPC; where BPP = BPC × 3 TKEEP/TSTRB signals are unused, every byte of TDATA is valid (no empty pixels).
dp_tx_axis_vid_tuser_s0_i	Input	2	TUSER[0]: Start of frame, the first beat of a frame (or interlaced field) of video and drives low for subsequent packet beats. TUSER[1]: Currently unused.
dp_tx_axis_vid_tlast_s0_i	Input	1	Strobes high for the last beat of the packet. Always coincides with the last pixel of the line.
dp_tx_axis_vid_tkeep_s0_i	Input	N/8	TKEEP signal is currently unused and this port is ignored by DPTX core.
dp_tx_axis_vid_tstrb_s0_i	Input	N/8	TSTRB signal is currently unused and this port is ignored by DPTX core.
dp_tx_axis_vid_tready_s0_o	Output	1	Indicates downstream is not ready, backpressure is supported. Line buffer FIFO depth is configurable (default to 32).
dp_tx_s_axil_awvalid_i	Input	1	Write address valid input. Indicates that the write address and control information are valid.
dp_tx_s_axil_awready_o	Output	1	Write address ready output. Indicates that the subordinate is ready to accept a write address.
dp_tx_s_axil_awaddr_i	Input	8	Write address input. Specifies the address for write transactions.
dp_tx_s_axil_awprot_i	Input	3	Write address protection type. Indicates the privilege level and security state of the transaction.
dp_tx_s_axil_wvalid_i	Input	1	Write data valid input. Indicates that write data and strobes are valid.
dp_tx_s_axil_wready_o	Output	1	Write data ready output. Indicates that the subordinate is ready to accept write data.
dp_tx_s_axil_wdata_i	Input	32	Write data input. Contains the write data.
dp_tx_s_axil_wstrb_i	Input	4	Write strobes input. Indicates which byte lanes hold valid data (each bit corresponds to one byte).
dp_tx_s_axil_bvalid_o	Output	1	Write response valid output. Indicates that the write response is valid.
dp_tx_s_axil_bready_i	Input	1	Write response ready input. Indicates that the manager is ready to accept a write response.
dp_tx_s_axil_bresp_o	Output	2	Write response output. Indicates the status of the write transaction.
dp_tx_s_axil_arvalid_i	Input	1	Read address valid input. Indicates that the read address and control information are valid.
dp_tx_s_axil_arready_o	Output	1	Read address ready output. Indicates that the subordinate is ready to accept a read address.
dp_tx_s_axil_araddr_i	Input	8	Read address input. Specifies the address for read transactions.
dp_tx_s_axil_arprot_i	Input	3	Read address protection type. Indicates the privilege level and security state of the transaction.
dp_tx_s_axil_rvalid_o	Output	1	Read data valid output. Indicates that the read data and response are valid.
dp_tx_s_axil_rready_i	Input	1	Read data ready input. Indicates that the manager is ready to accept read data.
dp_tx_s_axil_rdata_o	Output	32	Read data output. Contains the read data.
dp_tx_s_axil_rresp_o	Output	2	Read response output. Indicates the status of the read transaction.
dp_rx_hpd_o	Output	1	Rx hot plug detect output.
dp_rx_aux_oe_o	Output	1	Rx AUX channel output buffer enables.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Port	Type	Width	Description
dp_rx_aux_i	Input	1	Rx AUX channel data input.
dp_rx_aux_o	Output	1	Rx AUX channel data output.
dp_rx_axis_vid_tvalid_s0_o	Output	1	Indicates TDATA is valid. 0: Indicates TDATA is invalid. 1: Indicates TDATA is valid.
dp_rx_axis_vid_tready_s0_i	Input	1	Indicates downstream is ready. TREADY can default to low before video streaming starts. When TREADY asserted, DP RX does not support backpressure.
dp_rx_axis_vid_tdata_s0_o	Output	N	Video data width is byte aligned. N = ceil(BPP/8) × 8 × PPC; where BPP = BPC × 3 TKEEP/TSTRB signals are unused, every byte of TDATA is valid (no empty pixels).
dp_rx_axis_vid_tuser_s0_o	Output	2	TUSER[0]: Start of frame, the first beat of a frame (or interlaced field) of video and drives low for subsequent packet beats. TUSER[1]: Interlaced video to indicate fields of type F1 and must remain high for the remainder of the field.
dp_rx_axis_vid_tlast_s0_o	Output	1	Strobes high for the last beat of the packet. Always coincides with the last pixel of the line.
dp_rx_axis_vid_tkeep_s0_o	Output	N/8	TKEEP signal is currently unused, every byte of TDATA is valid.
dp_rx_axis_vid_tstrb_s0_o	Output	N/8	TSTRB signal is currently unused, every byte of TDATA is valid.
dp_rx_s_axil_awvalid_i	Input	1	Write address valid input. Indicates that the write address and control information are valid.
dp_rx_s_axil_awready_o	Output	1	Write address ready output. Indicates that the subordinate is ready to accept a write address.
dp_rx_s_axil_awaddr_i	Input	8	Write address input. Specifies the address for write transactions.
dp_rx_s_axil_awprot_i	Input	3	Write address protection type. Indicates the privilege level and security state of the transaction.
dp_rx_s_axil_wvalid_i	Input	1	Write data valid input. Indicates that write data and strobes are valid.
dp_rx_s_axil_wready_o	Output	1	Write data ready output. Indicates that the subordinate is ready to accept write data.
dp_rx_s_axil_wdata_i	Input	32	Write data input. Contains the write data.
dp_rx_s_axil_wstrb_i	Input	4	Write strobes input. Indicates which byte lanes hold valid data (each bit corresponds to one byte).
dp_rx_s_axil_bvalid_o	Output	1	Write response valid output. Indicates that the write response is valid.
dp_rx_s_axil_bready_i	Input	1	Write response ready input. Indicates that the manager is ready to accept a write response.
dp_rx_s_axil_bresp_o	Output	2	Write response output. Indicates the status of the write transaction.
dp_rx_s_axil_arvalid_i	Input	1	Read address valid input. Indicates that the read address and control information are valid.
dp_rx_s_axil_arready_o	Output	1	Read address ready output. Indicates that the subordinate is ready to accept a read address.
dp_rx_s_axil_araddr_i	Input	8	Read address input. Specifies the address for read transactions.
dp_rx_s_axil_arprot_i	Input	3	Read address protection type. Indicates the privilege level and security state of the transaction.
dp_rx_s_axil_rvalid_o	Output	1	Read data valid output. Indicates that the read data and response are valid.
dp_rx_s_axil_rready_i	Input	1	Read data ready input. Indicates that the manager is ready to accept read data.
dp_rx_s_axil_rdata_o	Output	32	Read data output. Contains the read data.
dp_rx_s_axil_rresp_o	Output	2	Read response output. Indicates the status of the read transaction.
dp_rx_edid_ram_clk_o	Output	1	EDID RAM clock to drive external EDID RAM component. This clock is synchronized with the DisplayPort sink AUX module.
dp_rx_edid_ram_clken_o	Output	1	EDID RAM clock enables to external EDID RAM component.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Port	Type	Width	Description
dp_rx_edid_ram_addr_o	Output	8	EDID RAM address. Increments by the DisplayPort sink during EDID read sequence.
dp_rx_edid_ram_rdata_i	Input	8	EDID RAM read data interface to fetch EDID from external RAM.
dp_rx_edid_ram_rst_o	Output	1	EDID RAM reset to external EDID RAM component.

Table 4.2. DisplayPort Clock Terminology

Clock	Description
Link Symbol Clock	Link symbol clock frequency for different data rates. HBR3: 810 MHz HBR2: 540 MHz HBR: 270 MHz RBR: 162 MHz
Link Speed Clock	Link symbol clock divided by PMA width (40-bit). HBR3: 202.5 MHz HBR2: 135 MHz HBR: 67.5 MHz RBR: 40.5 MHz
Pixel Clock	Actual clock frequency to transfer video data. For example: 4K60 (CTA816G VIC97) runs at 594 MHz.
Video Clock	Pixel clock divided by PPC.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

5. Register Description

All registers are accessed through the AXI4-Lite interface. Access type of each register is defined in the table below.

Table 5.1. Registers Access Type

Access Type	Behavior on Read Access	Behavior on Write Access
RO	Returns register value	Ignores write access
WO	Returns 0	Updates register value
RW	Returns register value	Updates register value
RC	Returns register value	Read to clear/reset the register bit to default value
RSVD	Returns 0	Ignores write access

5.1. DP Source Register Description

AXI4-Lite read and write data are double word (DW) aligned. DisplayPort IP does not support AXI4 unaligned transfer. Refer to the AMBA AXI Protocol Specification.

5.1.1. DP Source Link Register

For DP source link register with RW access, write access is used to set the desired link training value. The read value after successful link training is the actual value of the link established and may differ from the value written.

Table 5.2. DP_SOURCE_LINK

Offset: 0x00 – 0x03

Field	Name	Access	Default	Description
[31:25]	Reserved	RO	0	Reserved.
[24]	Core Reset	WO	0	Writes 1 to reset overall DP source including PHY layer, link layer, and AUX logic. This bit is automatically cleared after write.
[23:20]	Reserved	RO	0	Reserved.
[19:16]	Training Pattern	RO	0	Current training pattern. 8B/10B channel coding as follows: 0000 = Normal video 0001 = Training pattern 1 0010 = Training pattern 2 0011 = Training pattern 3 0100 = Training pattern 4 All other values are reserved.
[15:13]	Reserved	RO	0	Reserved.
[12]	Scrambler Disable	RO	0	0 = DP source scrambles data symbols before transmission. 1 = DP source disables scrambler and transmits all symbols without scrambling.
[11]	Enhanced Frame	RO	0	0 = Standard framing 1 = Enhanced framing
[10:8]	Lane Count	RW	Parameter	Lane Count. 3'd1 = 1 lane 3'd2 = 2 lanes 3'd4 = 4 lanes All other values are reserved.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Field	Name	Access	Default	Description
[7:0]	Lane Rate	RW	Parameter	Link rate. 8'h06 = RBR (1.62 Gbps) 8'h0A = HBR (2.7 Gbps) 8'h14 = HBR2 (5.4 Gbps) 8'h1E = HBR3 (8.1 Gbps) All other values are reserved.

5.1.2. Reserved

Table 5.3. RESERVED

Offset: 0x04 – 0x07

Field	Name	Access	Default	Description
[31:0]	RESERVED	RO	0	Reserved

5.1.3. DP Source PHY Reconfiguration Register

Table 5.4. DP_SOURCE_PHY_RECONFIG

Offset: 0x08 – 0x0B

Field	Name	Access	Default	Description
[31]	PHY_READY	RO	0	Indicates PHY is ready for transaction. 0 = PHY is not ready 1 = PHY is ready
[30:1]	Reserved	RO	0	Reserved.
[0]	RECONFIG_LINKRATE	WO	0	Writes 1 to trigger PHY link rate reconfiguration to link rate configured in DP_SOURCE_LINK. This bit is automatically cleared after write.

5.1.4. DP Source HPD Event Register

Table 5.5. DP_SOURCE_HPD

Offset: 0x0C – 0x0F

Field	Name	Access	Default	Description
[31:3]	Reserved	RO	0	Reserved.
[2]	HPD_STATUS	RO	0	Current HPD logic level. 0 = HPD Unplugged 1 = HPD Plugged
[1:0]	HPD_EVENT	RC	0	Indicates HPD event triggered IRQ. 00 = No event (or HPD_IRQ_EN==0) 01 = HPD plug event (long HPD pulse) 10 = HPD IRQ (short HPD pulse) 11 = Reserved Read to clear the register bits and deassert all Tx IRQ pins.

5.1.5. DP Source MSA Field0 Register

Table 5.6. DP_SOURCE_MSA0

Offset: 0x10 – 0x13

Field	Name	Access	Default	Description
[31:24]	RESERVED	RO	0	Reserved

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Field	Name	Access	Default	Description
[23:0]	MVID	RW	Parameter	MSA MVID

5.1.6. DP Source MSA Field1 Register

Table 5.7. DP_SOURCE_MSA1

Offset: 0x14 – 0x17

Field	Name	Access	Default	Description
[31:24]	RESERVED	RO	0	Reserved
[23:0]	NVID	RW	Parameter	MSA NVID

5.1.7. DP Source MSA Field2 Register

Table 5.8. DP_SOURCE_MSA2

Offset: 0x18 – 0x1B

Field	Name	Access	Default	Description
[31:16]	VTOTAL	RW	Parameter	MSA VTOTAL
[15:0]	HTOTAL	RW	Parameter	MSA HTOTAL

5.1.8. DP Source MSA Field3 Register

Table 5.9. DP_SOURCE_MSA3

Offset: 0x1C – 0x1F

Field	Name	Access	Default	Description
[31:16]	VHEIGHT	RW	Parameter	MSA VHEIGHT
[15:0]	HWIDTH	RW	Parameter	MSA HWIDTH

5.1.9. DP Source MSA Field4 Register

Table 5.10. DP_SOURCE_MSA4

Offset: 0x20 – 0x23

Field	Name	Access	Default	Description
[31:16]	VSTART	RW	Parameter	MSA VSTART (VSTART = Vsync + Vback)
[15:0]	HSTART	RW	Parameter	MSA HSTART (HSTART = Hsync + Hback)

5.1.10. DP Source MSA Field5 Register

Table 5.11. DP_SOURCE_MSA5

Offset: 0x24 – 0x27

Field	Name	Access	Default	Description
[31]	VSP	RW	Parameter	MSA VSP (VSync Polarity) 0 = Active high pulse. VSync signal is high for sync pulse width 1 = Active low pulse. VSync signal is low for sync pulse width
[30:16]	VSW	RW	Parameter	MSA VSW (VSync Width)

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Field	Name	Access	Default	Description
[15]	HSP	RW	Parameter	MSA HSP (HSync Polarity) 0 = Active high pulse. HSync signal is high for sync pulse width 1 = Active low pulse. HSync signal is low for sync pulse width
[14:0]	HSW	RW	Parameter	MSA HSW (HSync Width)

5.1.11. DP Source MSA Field6 Register

Table 5.12. DP_SOURCE_MSA6

Offset: 0x28 – 0x2B

Field	Name	Access	Default	Description
[31:16]	RESERVED	RO	0	Reserved
[15:8]	MISC1	RW	Parameter	MSA MISC1 (refer to the VESA DisplayPort Standard)
[7:0]	MISC0	RW	Parameter	MSA MISC0 (refer to the VESA DisplayPort Standard)

5.1.12. DP Source VBID and MSA Status Register

Table 5.13. DP_SOURCE_VBID_MSA_STATUS

Offset: 0x2C – 0x2F

Field	Name	Access	Default	Description
[31]	MSA_UPDATE	WO	0	Writes 1 to update all MSA field and TU_CALC
[30:4]	RESERVED	RO	0	Reserved
[3:0]	VBID	RO	0	VB-ID flags (refer to the VESA DisplayPort Standard) VB-ID flags are as follows: Bit3 – NoVideoStream Flag Bit2 – Reserved Bit1 – Reserved Bit0 – VerticalBlanking Flag

5.1.13. DP Source TU Calculation Register

Table 5.14. DP_SOURCE_TU_CALC

Offset: 0x30 – 0x33

Field	Name	Access	Default	Description
[31:8]	Valid Bytes per Lane	RW	Parameter	Sets the number of valid bytes per lane for BS symbol insertion period during vertical blanking. The equation is as follows: valid bytes = FLOOR(Per Lane BW / (VTOTAL × FPS × PMA_WIDTH)) where PMA_WIDTH is 40 (always)
[7]	RESERVED	RO	0	Reserved.
[6:0]	Valid Bytes per TU	RW	Parameter	Sets the number of valid bytes per TU per lane. The equation is as follows: valid bytes = CEILING((VIDEO_BW/LINK_BW) × TU_SIZE) where: • LINK_BW = number of active lanes × Per Lane BW • VIDEO_BW = HTOTAL × VTOTAL × FPS × BPP/0.8 • BPP = BPC x COLOR_PLANE

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Field	Name	Access	Default	Description
				• COLOR_PLANE = RGB/YCC44 is 3 and YCC422 is 2 • TU_SIZE is 64 (always)

5.2. DP Sink Register Description

AXI4-Lite read and write data are double word (DW) aligned. DisplayPort IP does not support AXI4 unaligned transfer. Refer to the AMBA AXI Protocol Specification.

5.2.1. DP Sink Control Register

Table 5.15. DP_SINK_CONTROL

Offset: 0x00 – 0x03

Field	Name	Access	Default	Description
[31:25]	RESERVED	RO	0	Reserved.
[24]	Core Reset	WO	0	Writes 1 to reset overall DP sink including PHY layer, link layer, and AUX logic. This bit is automatically cleared after write.
[23:11]	RESERVED	RO	0	Reserved.
[10:8]	Lane Count Capability	RW	Parameter	Configures DP sink maximum lane count capability in DPCD. 3'd1 = 1 lane 3'd2 = 2 lanes 3'd4 = 4 lanes All other values are reserved.
[7:0]	Link Rate Capability	RW	Parameter	Configures DP sink maximum link rate capability in DPCD. 8'h06 = RBR (1.62 Gbps) 8'h0A = HBR (2.7 Gbps) 8'h14 = HBR2 (5.4 Gbps) 8'h1E = HBR3 (8.1 Gbps) All other values are reserved.

5.2.2. DP Sink Link Training Sequence Status Register

Table 5.16. DP_SINK_LT_SEQ_STATUS

Note: Registers in this table reflect the actual link configuration after link training is complete and may defer from the initial settings.

Offset: 0x04 – 0x07

Field	Name	Access	Default	Description
[31]	PHY_READY	RO	0	Indicates that PHY is out of reset and ready for link training 1=Ready 0=Not ready
[30:16]	RESERVED	RO	0	Reserved
[15:8]	LINK_BW	RO	0	Main-Link Bandwidth Setting = Value × 0.27 Gbps / Lane 8'h06 = 1.62 Gbps 8'h0A = 2.7 Gbps 8'h14 = 5.4 Gbps 8'h1E = 8.1 Gbps

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Field	Name	Access	Default	Description
[7]	ENHANCE_FRAME_ENABLE	RO	0	Indicates enhance frame is enabled 1'd0 = Enhance frame is disabled 1'd1 = Enhance frame is enabled
[6:4]	LANE_COUNT	RO	0	Indicates Lane Count selected 3'd4 = 4 lanes 3'd2 = 2 lanes 3'd1 = 1 lane
[3]	SCRAMBLER_DISABLE	RO	0	Indicates data symbol scrambler status 1'd0 = Descrambler is enabled 1'd1 = Descrambler is disabled
[2:0]	LINK_TRAINING_SEQ	RO	0	Indicates Link Training state 3'd0 = Training not in progress (or Normal mode) 3'd1 = Link Training Pattern Sequence 1 (TPS1) 3'd2 = Link Training Pattern Sequence 2 (TPS2) 3'd3 = Link Training Pattern Sequence 3 (TPS3) 3'd4 = Link Training Pattern Sequence 4 (TPS4)

5.2.3. DP Sink Link Status Register

Table 5.17. DP_SINK_LINK_STATUS

Offset: 0x08 – 0x0B

Field	Name	Access	Default	Description
[31:9]	RESERVED	RO	0	Reserved
[8]	LINK_INTERLANE_ALIGN	RO	0	Indicate interlane aligned.
[7:4]	LINK_SYM_LOCK	RO	0	Link Symbol Locked. Bit0 = Lane0 Bit1 = Lane1 Bit2 = Lane2 Bit3 = Lane3
[3:0]	LINK_CR_DONE	RO	0	Link Clock Recovery Done. Bit0 = Lane0 Bit1 = Lane1 Bit2 = Lane2 Bit3 = Lane3

5.2.4. DP Sink HPD Event Register

Table 5.18. DP_SINK_HPD_EVENT

Offset: 0x0C – 0x0F

Field	Name	Access	Default	Description
[31:3]	RESERVED	RO	0	Reserved.
[2]	HPD_IRQ_ENABLE	WO	0	Writes 1 to trigger HPD_IRQ pulse to existing HPD signal. No dependency on HPD_OVERRIDE. This bit is automatically cleared after write.
[1]	HPD_FORCE	RW	0	When HPD_OVERRIDE = 1, • Writes 1 to force HPD signal to high • Writes 0 to force HPD signal to low When HPD_OVERRIDE = 0, writing to this register has no effect to the HPD signal and HPD signal is driven by IP logic.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Field	Name	Access	Default	Description
[0]	HPD_OVERRIDE	RW	0	Writes 1 to enable override HPD signal via bit[1] HPD_FORCE. Writes 0 to release override and HPD signal is driven by IP logic.

5.2.5. DP Sink MSA Field0 Register

Table 5.19. DP_SINK_MSA0

Offset: 0x10 – 0x13

Field	Name	Access	Default	Description
[31:24]	RESERVED	RO	0	Reserved
[23:0]	MVID	RO	0	MSA MVID

5.2.6. DP Sink MSA Field1 Register

Table 5.20. DP_SINK_MSA1

Offset: 0x14 – 0x17

Field	Name	Access	Default	Description
[31:24]	RESERVED	RO	0	Reserved
[23:0]	NVID	RO	0	MSA NVID

5.2.7. DP Sink MSA Field2 Register

Table 5.21. DP_SINK_MSA2

Offset: 0x18 – 0x1B

Field	Name	Access	Default	Description
[31:16]	VTOTAL	RO	0	MSA VTOTAL
[15:0]	HTOTAL	RO	0	MSA HTOTAL

5.2.8. DP Sink MSA Field3 Register

Table 5.22. DP_SINK_MSA3

Offset: 0x1C – 0x1F

Field	Name	Access	Default	Description
[31:16]	VHEIGHT	RO	0	MSA VHEIGHT
[15:0]	HWIDTH	RO	0	MSA HWIDTH

5.2.9. DP Sink MSA Field4 Register

Table 5.23. DP_SINK_MSA4

Offset: 0x20 – 0x23

Field	Name	Access	Default	Description
[31:16]	VSTART	RO	0	MSA VSTART
[15:0]	HSTART	RO	0	MSA HSTART

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

5.2.10. DP Sink MSA Field5 Register

Table 5.24. DP_SINK_MSA5

Offset: 0x24 – 0x27

Field	Name	Access	Default	Description
[31]	VSP	RO	0	MSA VSP (VSync Polarity) 0 = Active high pulse. VSync signal is high for sync pulse width 1 = Active low pulse. VSync signal is low for sync pulse width
[30:16]	VSW	RO	0	MSA VSW (VSync Width)
[15]	HSP	RO	0	MSA HSP (HSync Polarity) 0 = Active high pulse. HSync signal is high for sync pulse width 1 = Active low pulse. HSync signal is low for sync pulse width
[14:0]	HSW	RO	0	MSA HSW (HSync Width)

5.2.11. DP Sink MSA Field6 Register

Table 5.25. DP_SINK_MSA6

Offset: 0x28 – 0x2B

Field	Name	Access	Default	Description
[31:16]	RESERVED	RO	0	Reserved
[15:8]	MISC1	RO	0	MSA MISC1
[7:0]	MISC0	RO	0	MSA MISC0

5.2.12. DP Sink VBID and MSA Status Register

Table 5.26. DP_SINK_VBID_MSA_STATUS

Offset: 0x2C – 0x2F

Field	Name	Access	Default	Description
[31:9]	RESERVED	RO	0	Reserved.
[8]	MSA_UPDATED	RC	0	Indicates MSA is updated after this register last read. Read to clear.
[7]	MSA_LOCK	RO	0	Indicates MSA is locked and valid. 1 = Valid 0 = Invalid
[6:0]	VBID	RO	0	VB-ID flags. Bit6 – DSC (tied off to 0) Bit5 – HDCP Sync Detect (tied off to 0) Bit4 – Audio Mute Flag Bit3 – NoVideoStream Flag Bit2 – Interlace Flag Bit1 – FieldID Flag Bit0 – VerticalBlanking Flag

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

5.3. DPCD Register Description

This section describes DPCD registers supported by the DisplayPort IP and the default value. For more details on the DPCD description, refer to the VESA web page for the DisplayPort Standard version 1.4a.

Table 5.27. DPCD Register

DPCD offset	Name	Default
0x00000/ 0x02200	DPCD_REV	0x14
0x00001/ 0x02201	8b/10b_MAX_LINK_RATE	Parameter: Rx Maximum Link Rate
0x00002/ 0x02202	MAX_LANE_COUNT	Parameter: Rx Maximum Lane Count
0x00003/ 0x02203	MAX_DOWNSPREAD	0x81
0x00004/ 0x02204	NORP and DP_PWR_VOLTAGE_CAP	0x00
0x00005/ 0x02205	DOWN_STREAM_PORT_PRESENT	0x10
0x00006/ 0x02206	MAIN_LINK_CHANNEL_CODING_CAP	0x01
0x00007/ 0x02207	DOWN_STREAM_PORT_COUNT	0x10
0x00008–0x0000B/ 0x02208–0x0220B	RECEIVE_PORTN_CAP_N	0x00
0x0000C/ 0x0220C	I2C Speed Control Capabilities Bit Map	0x08
0x0000D/ 0x0220D	eDP_CONFIGURATION_CAP	0x01 when Parameter: eDP Enable
0x0000E/ 0x0220E	8b/10b_TRAINING_AUX_RD_INTERVAL	0x04
0x00021	MST_CAP	0x00
0x00030–0x0003F	GUID	0x00
0x00100	LINK_BW_SET	Parameter: Rx Maximum Link Rate
0x00101	LANE_COUNT_SET	Parameter: Rx Maximum Lane Count
0x00102	TRAINING_PATTERN_SET	0x00
0x00103	TRAINING_LANE0_SET	0x00
0x00104	TRAINING_LANE1_SET	0x00
0x00105	TRAINING_LANE2_SET	0x00
0x00106	TRAINING_LANE3_SET	0x00
0x0010A	eDP_CONFIGURATION_SET	0x00
0x00200/ 0x02002	SINK_COUNT	0x01
0x00201	DEVICE_SERVICE_IRQ_VECTOR	0x00
0x00202/ 0x0200C	LANE0_1_STATUS	0x00
0x00203/ 0x0200D	LANE2_3_STATUS	0x00

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

DPCD offset	Name	Default
0x00204/ 0x0200E	LANE_ALIGN_STATUS_UPDATED	0x00
0x00205/ 0x0200F	SINK_STATUS	0x00
0x00206	ADJUST_REQUEST_LANE0_1	0x44
0x00207	ADJUST_REQUEST_LANE2_3	0x44
0x00600	SET_POWER and SET_DP_PWR_VOLTAGE	0x01

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

6. Example Design

The DisplayPort example design demonstrates DisplayPort video streaming retransmit within FPGA. The external video source to the example design DisplayPort sink retransmits to the DisplayPort source before transmitting to the external video sink. This example design validates the DisplayPort IP using the following evaluation boards:

- CertusPro-NX Evaluation Board (for CertusPro-NX devices)
- Lattice Avant G/X Versa Evaluation Board (for Avant devices)
- Modular FMC Adapter and DisplayPort Daughter Cards

6.1. Example Design Supported Configuration

Table 6.1. DisplayPort IP Configuration Supported by the Example Design

Attribute	Selectable Values	Description
General		
Mode	**Tx and Rx**	Selects DisplayPort mode in duplex mode, Tx only simplex mode, or Rx only simplex mode.
Lattice Hardware Specific Options		
PHY PCS Lane ID	**0**	Specifies the location of the first lane of the PCS instance. Dependency on RX or TX MAX_LANE_COUNT
PHY Refclk Select	**1**	0: Selects sd_ext_0_refclk. 1: Selects sd_ext_1_refclk. Clock routing is handled by the DisplayPort IP on parameter selection.
Swap lanes 0 and 1 for Tx	**Checked**	Enables Tx serial data swap position between lane0 and lane1. This attribute is checked when using the Lattice DisplayPort FMC because of the FMC board design requirement.
Swap lanes 2 and 3 for Tx	**Checked**	Enables Tx serial data swap position between lane2 and lane3. This attribute is checked when using the Lattice DisplayPort FMC because of the FMC board design requirement.
Invert lanes 2 and 3 for Tx	**Checked**	Inverts Tx serial data lane2 and lane3 polarity. This attribute is checked when using the Lattice DisplayPort FMC because of the FMC board design requirement.
Swap lanes 0,1,2,3 for Rx	**Checked**	Reverses Rx serial data lane position from Lane0, 1, 2, 3 to Lane3, 2, 1, 0. This attribute is checked when using the Lattice DisplayPort FMC because of the FMC board design requirement.
Invert all lanes for Rx	**Checked**	Inverts all Rx serial data lane polarity. This attribute is checked when using the Lattice DisplayPort FMC because of the FMC board design requirement.
DP RX Settings		
DP RX – IP Capability		
Maximum Lane Count	**4**	Selects supported maximum lane count: 1, 2, or 4 lanes.
Maximum Link Rate (Gbps)	**5.4**	Selects supported maximum link rate: 1.62, 2.7, 5.4, or 8.1 Gbps.
AXI4-Lite DPRX Register Enable	**Checked**	Enables DPRX registers and AXI4-Lite interface.
eDP Enable	**Unchecked**	Enables or disables eDP mode.
Pixels per Clock (PPC)	**4**	Supports only 4 pixels per clock. Not editable. For information only.
DP RX – Video Interface		
Video Interface	**Unified Video Streaming**	Supports only the Lattice Unified Video Streaming (AXI4-Stream) interface. Not editable. For information only.
DP RX – Color Format		
Maximum Bits per	**8**	Selects the maximum BPC support. Allows you to disable in DPRX support

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Attribute	Selectable Values	Description
Component (BPC)		BPC parameter.
DPRX Support 6BPC	**Unchecked**	Enables or disables 6 BPC support when maximum BPC is bigger than 6 BPC. YCbCr422 does not support 6 BPC.
DPRX Support 8BPC	**Checked**	Enables or disables 8 BPC support when Max BPC is bigger than 8 BPC.
DPRX Support 10BPC	**Unchecked**	Enables or disables 10 BPC support when Max BPC is bigger than 10 BPC.
DPRX Support 12BPC	**Unchecked**	Enables or disables 12 BPC support when Max BPC is bigger than 12 BPC.
DPRX Support 16BPC	**Unchecked**	Enables or disables 16 BPC support.
DPRX Support RGB and YCbCr444	**Checked**	Enables support for RGB. YCbCr444 shares the same decoding as RGB.
DPRX Support YCbCr422	**Unchecked**	Enables support for YCbCr422.
DP RX – eDP IP Capability		
eDP Support ASSR	**Checked**	Selects eDP sink capability to support eDP ASSR.
eDP Reduced AUX Timing	**Checked**	Always supports reduced AUX timing when eDP mode is enabled. Not editable. For information only.
eDP Fast Link Training	**Unchecked**	eDP fast link training mode is not supported. Not editable. For information only.
DP TX Settings		
DP TX – IP Capability		
Maximum Lane Count	**4**	Selects supported maximum lane count: 1, 2, or 4 lanes.
Maximum Link Rate (Gbps)	**5.4**	Selects supported maximum link rate: 1.62, 2.7, 5.4, or 8.1 Gbps.
AXI4-Lite DPTX Register Enable	**Checked**	Enables DPTX registers and AXI4-Lite interface.
eDP Enable	**Unchecked**	Enables or disables eDP mode.
Pixels per Clock (PPC)	**4**	Supports only 4 pixels per clock. Not editable. For information only.
DP TX – Video Interface		
Video Interface	**Unified Video Streaming**	Supports only the Lattice Unified Video Streaming (AXI4-Stream) interface. Not editable. For information only.
DP TX – Color Format		
Maximum Bits per Component (BPC)	**8**	Selects the maximum BPC support. Allows you to disable in DPTX support BPC parameter.
DPTX Support 6BPC	**Unchecked**	Enables or disables 6 BPC support when maximum BPC is bigger than 6 BPC. YCbCr422 does not support 6 BPC.
DPTX Support 8BPC	**Checked**	Enables or disables 8 BPC support when maximum BPC is bigger than 8 BPC.
DPTX Support 10BPC	**Unchecked**	Enables or disables 10 BPC support when maximum BPC is bigger than 10 BPC.
DPTX Support 12BPC	**Unchecked**	Enables or disables 12 BPC support when maximum BPC is bigger than 12 BPC.
DPTX Support 16BPC	**Unchecked**	Enables or disables 16 BPC support.
DPTX Support RGB and YCbCr444	**Checked**	Enables support for RGB. YCbCr444 shares the same encoding as RGB.
DPTX Support YCbCr422	**Unchecked**	Enables support for YCbCr422.
DP TX – eDP IP Capability		
eDP Support ASSR	**Checked**	Always supports ASSR when eDP mode is enabled. Not editable. For information only.
eDP Reduced AUX Timing	**Checked**	Always supports reduced AUX timing when eDP mode is enabled. Not editable. For information only.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Attribute	Selectable Values	Description
eDP Fast Link Training	**Unchecked**	eDP fast link training mode is not supported. Not editable. For information only.
TX Video Settings		
Set MSA based on default resolution	**Checked**	Checks to select default resolution based on predefined resolution.
Default Resolution	**3840x2160p60, RGB, 8BPC**	Predefined resolution.
Color Format	RGB, YCbCr444, YCbCr422	Default color format configuration for IP initialization. Affects MISC0 MSA and can be overwritten using TX registers. MISC0[4:3] is always defaulted to 2'b00 for RGB and 2'b01 for YCbCr444 and YCbCr422.
Video Stream Clock Frequency (MHz)	148.5	Auto calculated actual video stream clock. Not editable. For information only.

6.2. Overview of the Example Design and Features

Key features of the example design are as follows:

- DisplayPort video retransmit from sink to source.
- Unified Video streaming protocol with static video clock frequency for all video resolution (150 MHz up to 4K60).

6.3. Example Design Components

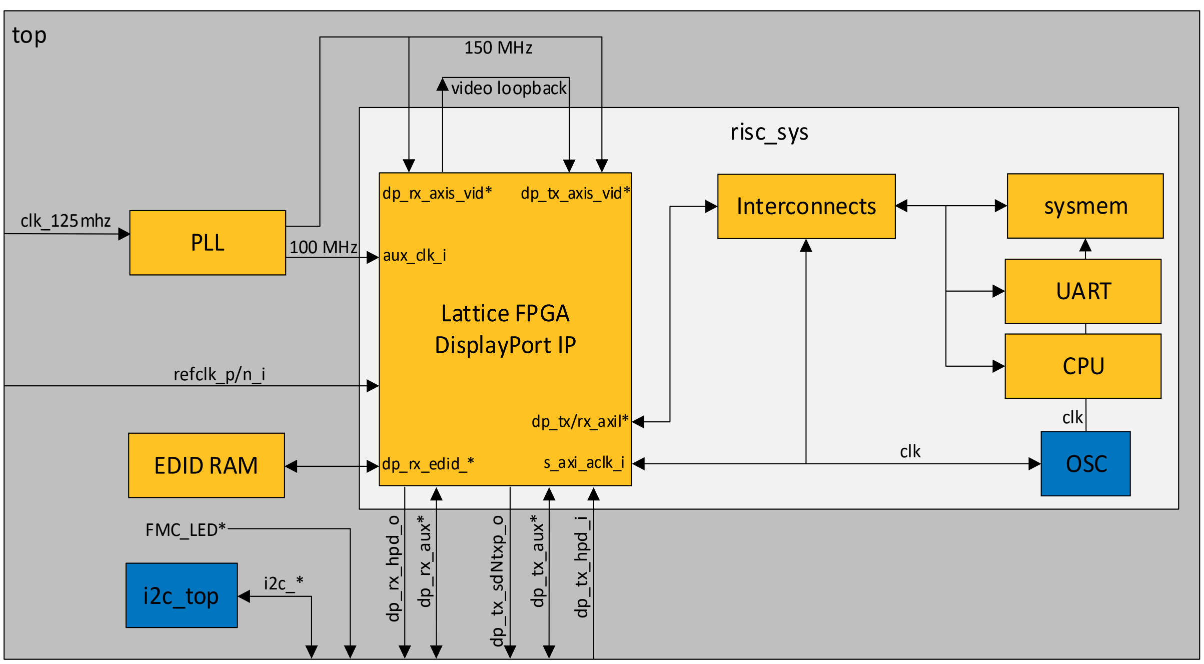


Figure 6.1. DisplayPort Example Design Block Diagram for CertusPro-NX Devices

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

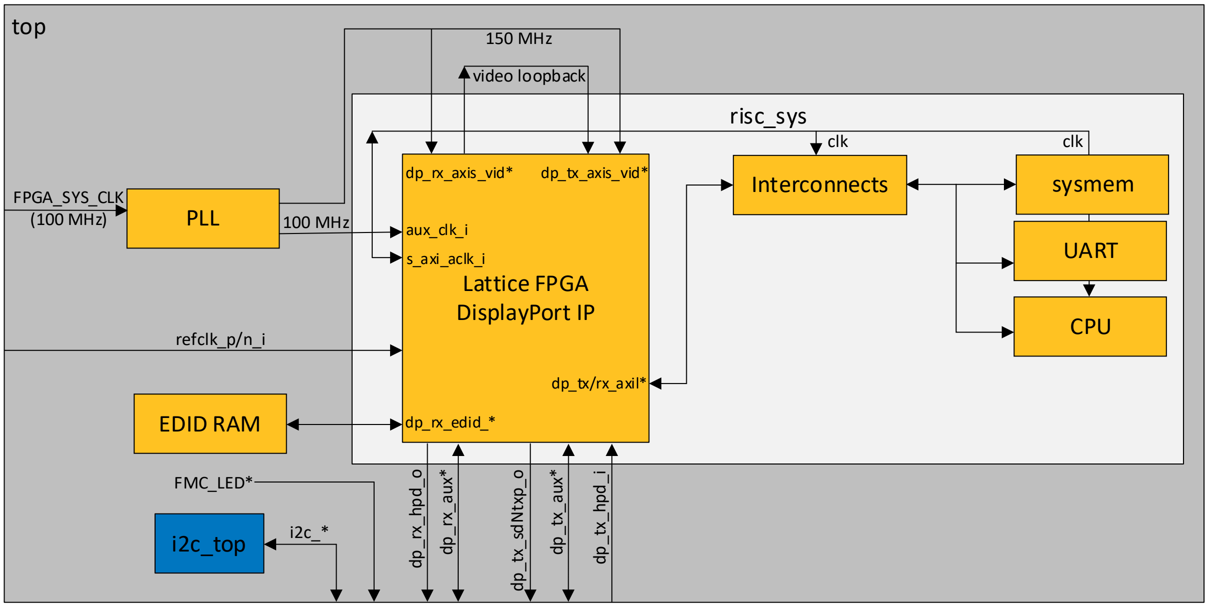


Figure 6.2. DisplayPort Example Design Block Diagram for Avant Devices

The DisplayPort example design includes the following blocks:

- In risc_sys propel project:
  - DisplayPort IP core
  - Interconnects (ahb2axi, axil2axi, ahb2apb)
  - sysmem
  - UART
  - RISC V MC IP
- In top:
  - PLL
  - EDID RAM
  - I2C controller

6.3.1. DisplayPort IP Core

DisplayPort IP with Tx and Rx enabled. For exact configuration, refer to Table 6.1. IP Tx and Rx pixel clocks run at 150 MHz which allow you to drive up to 3840 × 2160 at 60 Hz. The AXI-Lite interface is hooked up to a RISC V MC IP to allow you to read and write IP registers through the RISC V software provided together as part of the IP evaluation kit.

6.3.2. Interconnects

Interconnects convert between protocols to match IP interfaces. Interconnects consist of AHB-Lite to AXI4 Bridge, AHB-Lite Interconnect, AHB-Lite to APB Bridge, APB Interconnect, and AXI to AXI-Lite Bridge.

6.3.3. sysmem

The sysmem block stores the .mem file for RISC.

6.3.4. UART

UART is used for terminal display from RISC.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

6.3.5. RISC V MC IP

RISC V MC IP is a controller for the RISC subsystem.

6.3.6. PLL

The PLL generates 100 MHz for AUX clock and AXI-Lite clock, and 150 MHz for video clock.

6.3.7. EDID RAM

The configuration for the EBR component RAM_DQ is as shown in the figure below.
Customize edid.hex for initialization. Hex file in the example design can be used as a reference.

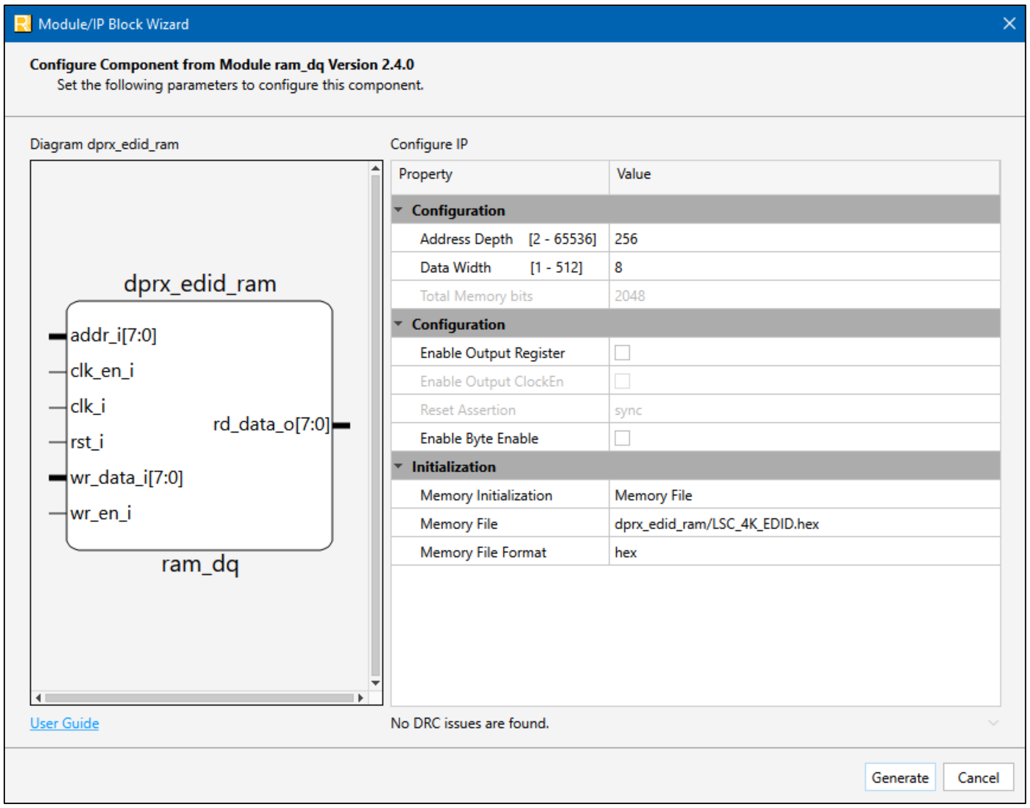


Figure 6.3. DisplayPort Example Design External EDID RAM Configuration

6.3.8. I2C_TOP

Configure the clock chip on the FMC board to generate refclkp/n for Physical Layer. The out-of-box example design configures the refclk to 135 MHz for 2.7 Gbps, 5.4 Gbps, and 8.1 Gbps data rates. For 1.6 Gbps data rate, configure the refclk to 81 MHz for CertusPro-NX devices and 135 MHz for Avant devices. In the top.sv file, the parameter DP_TX_MAX_LANE_RATE is used to switch the refclk frequency between 135 MHz and 81 MHz.

6.3.9. OSC

On-chip clock source for CertusPro-NX. In the Avant example design, OSC is replaced with the 100 MHz FPGA_SYS_CLK on the Lattice Avant G/X Versa Evaluation Board.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

6.4. Running the Example Design on Hardware

The default project supports static resolution of 3840 × 2160 at 60 Hz, RGB, 8 BPC. Ensure that both GPU and monitor support this resolution. You can customize the DisplayPort instance in the Lattice Propel Builder for different configurations.

Note: The screenshots provided are for reference only. Details may vary depending on the version of the IP or software being used. If there have been no significant changes to the GUI, a screenshot may reflect an earlier version of the IP.

Note: The path for CertusPro-NX example design is dp_tx_rx_risc and the path for Avant example design is dp_tx_rx_risc_av.

6.4.1. Precompiled Bitfile

You can use the precompiled bitfile in *dp_tx_rx_risc/impl_1/risc_sys_impl_1.bit* to program to the board.

6.4.2. Recompiling the Project

To generate the bitstream file for the DisplayPort example design, follow these steps:

1. Copy the *dp_tx_rx_risc.zip* file from the eval folder within the IP core directory to your project directory and unzip to extract the example design files.
2. Open the Lattice Propel Builder program and select **Open Design** from the **File** tab.
3. Browse to the *dp_tx_rx_risc /risc_sys* folder and select the *risc_sys.sbx* file to bring up the schematic design of the SoC design.
4. Regenerate all IP instances except axi2axil_M00_inst and axi2axil_M01_inst.
5. If you have a new .mem file, refresh the project software as follows:
   a. Locate the system memory module and select **Reconfig**.

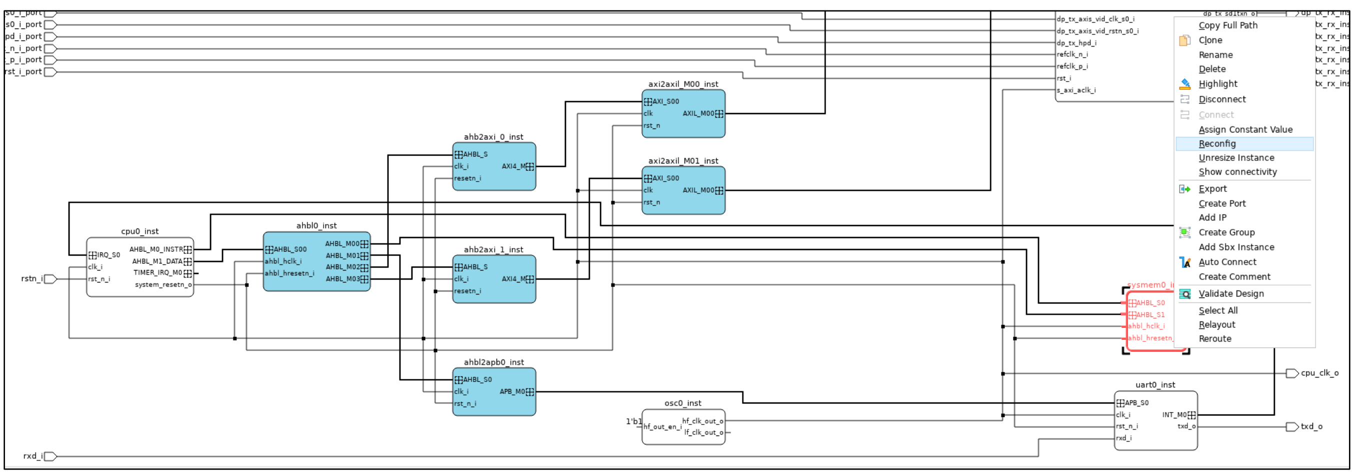


Figure 6.4. Reconfiguring sysmem

   b. Navigate to the .mem file (located in the *<Lattice Propel project dir>/Debug* folder) that you generated in the Lattice Propel project from the Refreshing the Project Software section. Click **Generate**.

   Note: The example design default .mem file is located at *dp_tx_rx_risc/riscv_mc.mem*.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

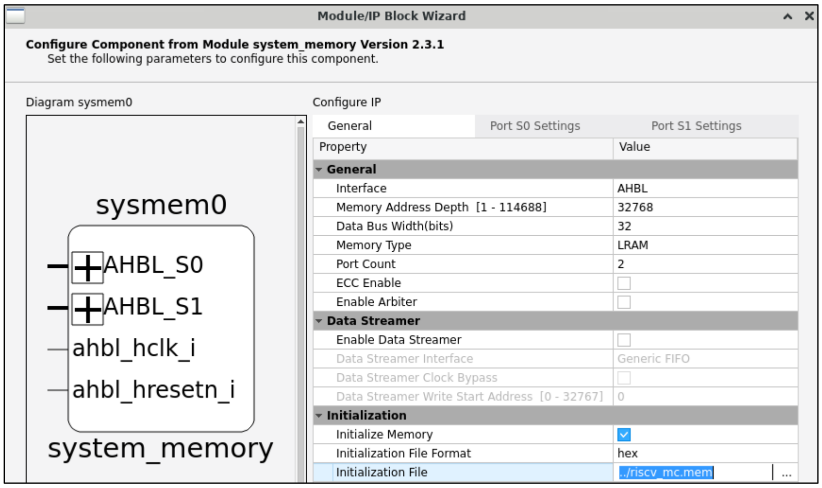


Figure 6.5. Updating the sysmem Initialization File

6. Check the address map to ensure *dp_tx_rx_inst/DP_RX_AXI4L* is mapped to base address of 0x20000 and *dp_tx_rx_inst/DP_TX_AXI4L* is mapped to base address of 0x21000 as shown in the figure below.

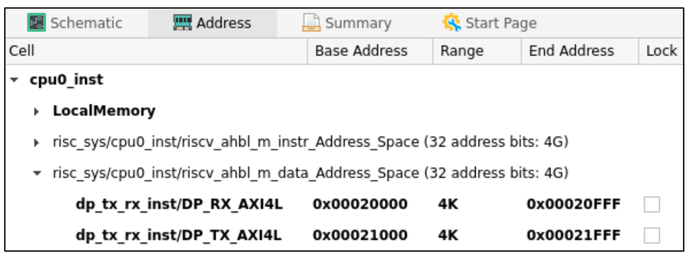


Figure 6.6. Address Mapping for dp_tx_rx_inst

7. To regenerate the wrapper files and software files for the SoC design, select **Design > Generate**.
8. Open the Lattice Radiant software and select **Open Project**.
9. Browse to the *dp_tx_rx_risc* folder for the *risc_sys.rdf* file.
10. Run compilation to generate bitstream.
11. Download the bitstream file to the FPGA board and connect to the DisplayPort source and sink.

6.4.3. Refreshing the Project Software

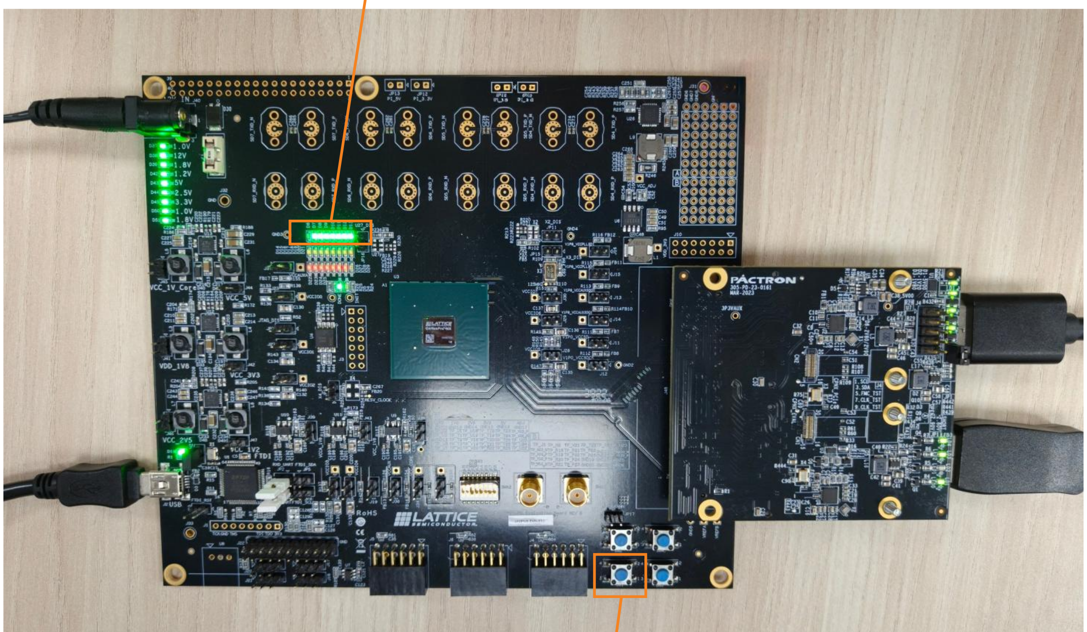
To refresh the project software, follow these steps:

1. Open the Lattice Propel software and point the Workspace to *dp_tx_rx_risc/propel_sw* and click **Launch**.
2. Right-click on the project folder and select **Build Project** to start building the software. This generates a .mem file in a new Debug folder which can be used for initializing the system memory in the design.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

6.4.4. Board Setup

LED Green0 (D6): rst
LED Green1 (D7): gtclk locked
LED Green2 (D8): pll locked
LED Green3 (D9): pixel clock locked
LED Green4 (D10): dp_rx_axis_vid_tvalid (ext)
LED Green5 (D11): tx training_done
LED Green6 (D12): dp_rx_hpd_o
LED Green7 (D13): dp_tx_hpd_i



DIP_SWITCH (SW1): Reset

Figure 6.7. Switches and LED Indicators for CertusPro-NX Evaluation Board

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

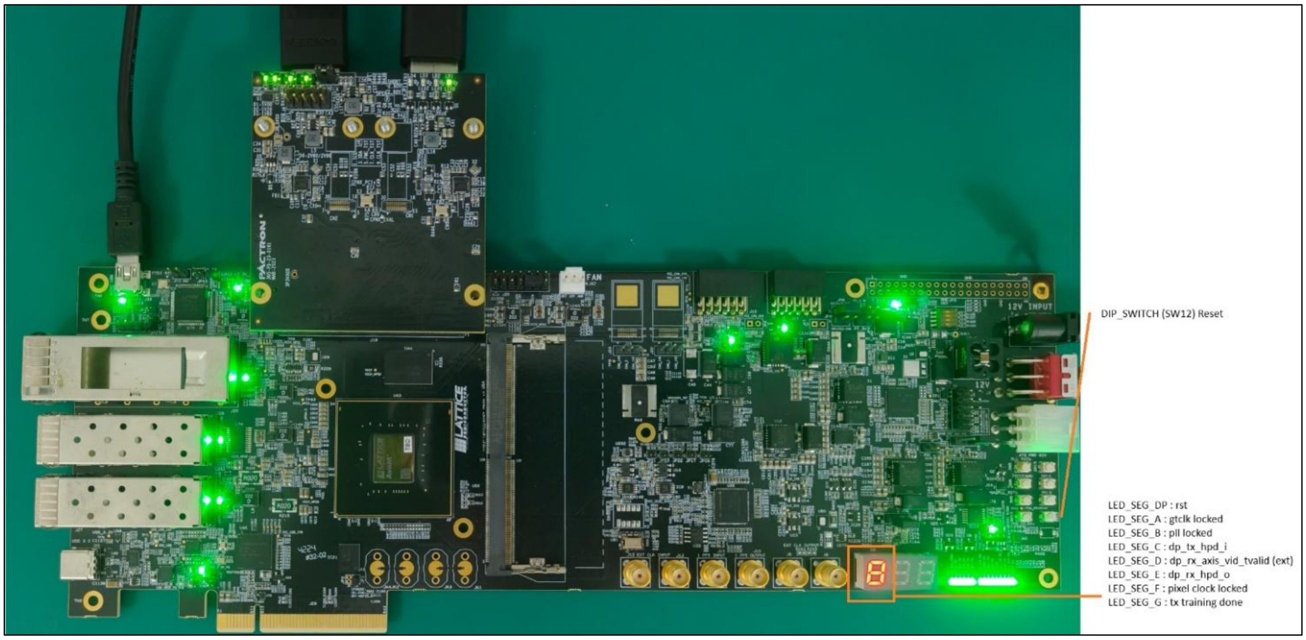


Figure 6.8. Switches and LED Indicators for Lattice Avant G/X Versa Evaluation Board

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

7. Designing with the IP

This section provides information on how to generate the IP core using the Lattice Radiant software and how to run simulation and synthesis. For more details on the Lattice Radiant software, refer to the Lattice Radiant Software User Guide.

Note: The screenshots provided are for reference only. Details may vary depending on the version of the IP or software being used. If there have been no significant changes to the GUI, a screenshot may reflect an earlier version of the IP.

7.1. Generating and Instantiating the IP

You can use the Lattice Radiant software to generate IP modules and integrate them into the device architecture. The following steps describe how to generate the DisplayPort IP in the Lattice Radiant software.

To generate the DisplayPort IP, follow these steps:

1. Create a new Lattice Radiant software project or open an existing project.
2. In the **IP Catalog** tab, double-click **DisplayPort** under **IP, Audio_Video_and_Image_Processing** category. The **Module/IP Block Wizard** opens as shown in the figure below Enter values in the **Component name** and the **Create in** fields and click **Next**.

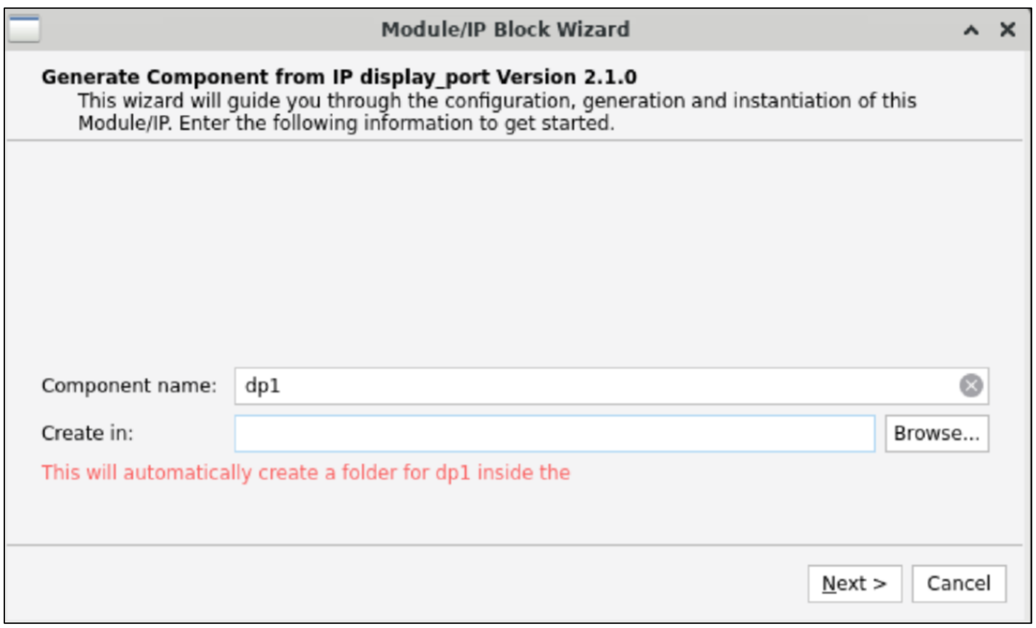


Figure 7.1. Module/IP Block Wizard

3. In the next **Module/IP Block Wizard** window, customize the selected DisplayPort IP using drop-down lists and check boxes. The figure below shows an example configuration of the DisplayPort IP. For details on the configuration options, refer to the IP Parameter Description section.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

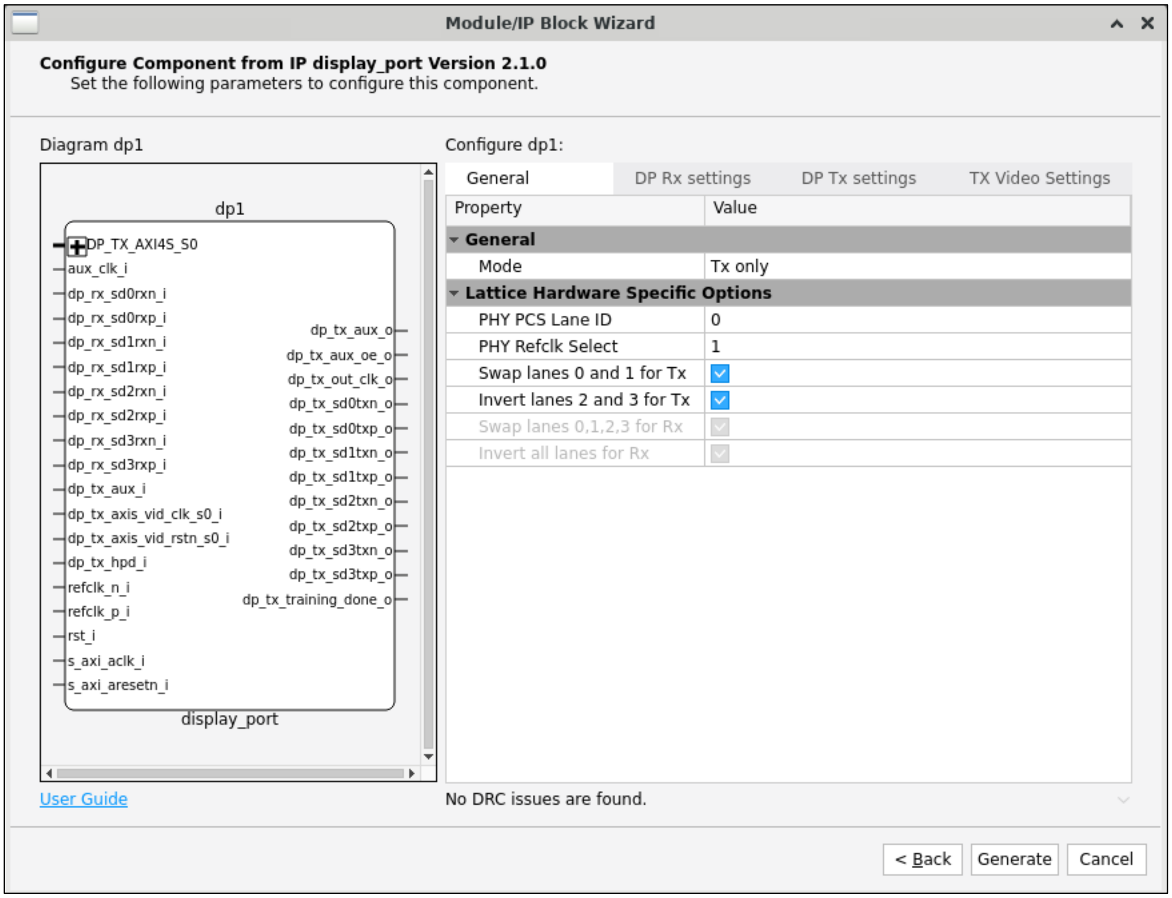


Figure 7.2. IP Configuration

4. Click **Generate**. The **Check Generated Result** dialog box opens, showing design block messages and results as shown in the figure below

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

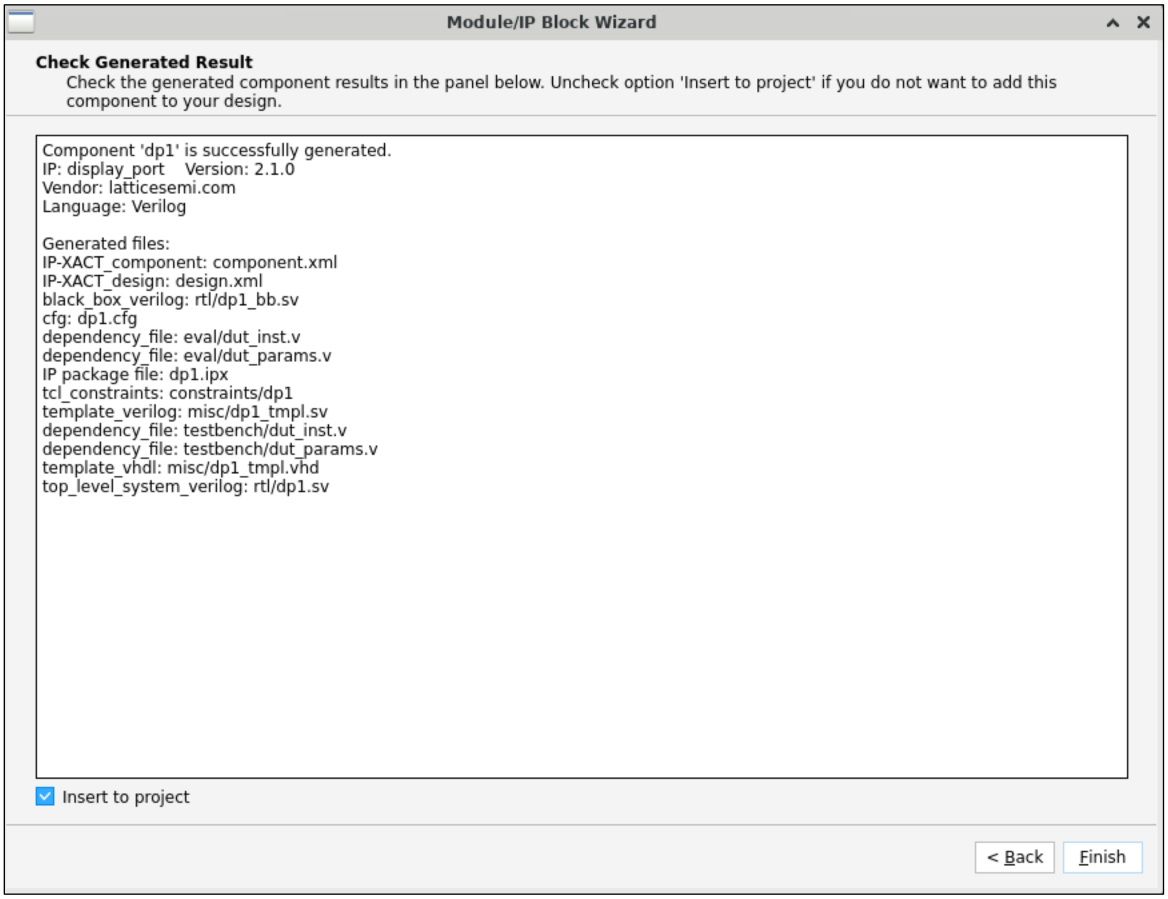


Figure 7.3. Check Generated Result

5. Click **Finish**. All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields shown in Figure 7.1.

7.1.1. Generated Files and File Structure

The generated DisplayPort module package includes the closed-box (*<Component name>_bb.sv*) and instance templates (*<Component name>_tmpl.sv/vhd*) that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file (*<Component name>.sv*) that can be used as an instantiation template for the module is also provided. You may also use this top-level reference as the starting template for the top-level for your complete design. The generated files are listed in Table 7.1.

Table 7.1. Generated File List

Attribute	Description
<Component name>.ipx	This file contains the information on the files associated with the generated IP.
<Component name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Component name>.sv	This file provides an example RTL top file that instantiates the module.
rtl/<Component name>_bb.sv	This file provides the synthesis closed-box.
misc/<Component name>_tmpl.sv misc /<Component name>_tmpl.vhd	These files provide instance templates for the module.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

7.2. Design Implementation

Completing your design includes additional steps to specify analog properties, pin assignments, and timing and physical constraints. You can add and edit the constraints using the Device Constraint Editor or by manually creating a PDC file.

Post-synthesis constraint files (.pdc) contain both timing and non-timing constraint .pdc source files for storing logical timing and physical constraints. Constraints that are added using the Device Constraint Editor are saved to the active .pdc file. The active post-synthesis design constraint file is then used as input for post-synthesis processes.

Refer to the relevant sections in the Lattice Radiant Software User Guide for more information on how to create or edit constraints and how to use the Device Constraint Editor.

7.3. Timing and Physical Constraints

The DisplayPort IP requires you to define clock constraints for the reference clock and link clock of the IP in post-synthesis constraint file.

7.3.1. Clock Constraint for CertusPro-NX Devices

Table 7.2. Link Clock Divider and Multiplier Values for CertusPro-NX Devices

Data Rate	1.62G	2.7G	5.4G	8.1G
ls_clk_div	2	2	1	2
ls_clk_mult	1	1	1	3

Add and edit the following constraints to your PDC file. Use the divider and multiplier values in the table above based on your desired data rate.

```
#Refclk is 81mhz for 1.62G and 135mhz for other datarate
create_clock -name {refclk_p} -period $ref_clk_period [get_ports refclk_p]
create_clock -name {refclk_n} -period $ref_clk_period [get_ports refclk_n]
```

```
#Link Clock 1.62G(40.5Mhz) | 2.7G(67.5MHz) | 5.4G(135MHz) | 8.1G(202.5Mhz)
create_generated_clock -name {tx_ls_clk} -source [get_ports refclk_p] -divide_by $ls_clk_div -
multiply_by $ls_clk_mult [get_pins *display_port_inst*/CH*_PIPE_PCS_TXCLKOUT]
create_generated_clock -name {rx_ls_clk} -source [get_ports refclk_p] -divide_by $ls_clk_div -
multiply_by $ls_clk_mult [get_pins *display_port_inst*/CH*_RXOUTCLK]
```

7.3.2. Clock Constraint for Avant Devices

Table 7.3. Link Clock Divider and Multiplier Values for Avant Devices

Data Rate	1.62G	2.7G	5.4G	8.1G
ls_clk_div	10	2	1	2
ls_clk_mult	3	1	1	3

Add and edit the following constraints to your PDC file. Use the divider and multiplier values in the table above based on your desired data rate.

```
#Refclk is 135mhz for all datarates
create_clock -name {refclk_p} -period 7.407407 [get_ports refclk_p]
create_clock -name {refclk_n} -period 7.407407 [get_ports refclk_n]
```

```
#Link Clock 1.62G(40.5Mhz) | 2.7G(67.5MHz) | 5.4G(135MHz) | 8.1G(202.5Mhz)
create_generated_clock -name {tx_ls_clk} -source [get_ports refclk_p_i] -divide_by $ls_clk_div
-multiply_by $ls_clk_mult [get_pins -hierarchical
display_port_inst/*.mpcs_wrapper_top_inst/*.mpcs_wrapper_inst/*/lscc_mpphy_inst/*/TXOUTCLK_L*]
```

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

```
create_generated_clock -name {rx_ls_clk} -source [get_ports refclk_n_i] -divide_by $ls_clk_div
-multiply_by $ls_clk_mult [get_pins -hierarchical
display_port_inst/*.mpcs_wrapper_top_inst/*.mpcs_wrapper_inst/*/lscc_mpphy_inst/*/RXOUTCLK_L*]
```

7.3.3. Timing Constraint Files

The DisplayPort IP generates the following constraints files:

- A constraint file in SDC format (*<ip_instance_path>/constraints/constraint.sdc*) that contains both pre-synthesis and post-synthesis IP constraints. These constraints are automatically used and propagated by the software tool.
- An evaluation post-synthesis constraint file in PDC format (*<example_design_path>/dp_tx_rx_risc*/risc_sys.pdc*). This constraint file can be used as a reference for your system-level design. You must define the correct clock targets and pin location based on your design.

7.4. Specifying the Strategy

The Lattice Radiant software provides two predefined strategies: Area and Timing. The software also enables you to create customized strategies. For details on how to create a new strategy, refer to the Strategies section of the Lattice Radiant Software user guide.

7.5. Running Functional Simulation

7.5.1. Testbench Structure

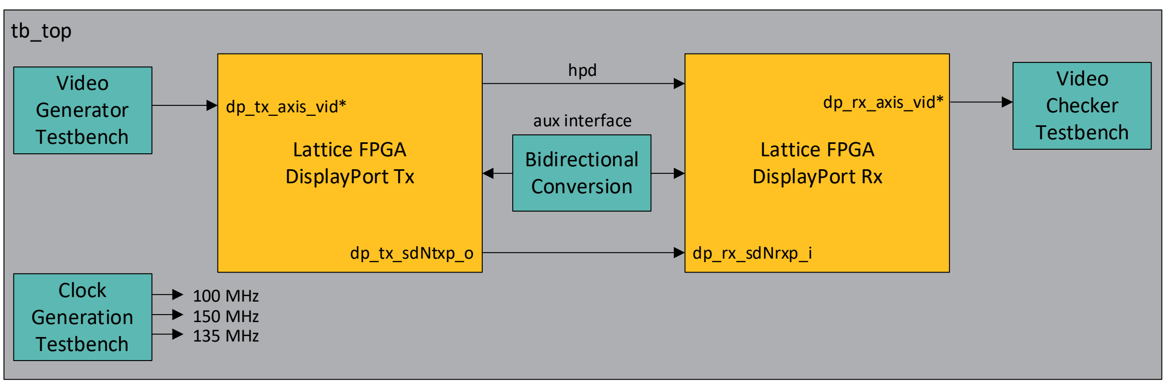


Figure 7.4. DisplayPort Simulation Testbench Block Diagram

The flow of the simulation testbench is as follows:

1. When out of reset, the DisplayPort sink asserts HPD to the DisplayPort source.
2. DisplayPort IP initiates link training to DisplayPort sink.
3. Internally, both DisplayPort source and sink reconfigure the Physical Layer to the desired link rate.
4. DisplayPort source and sink complete the link training sequence.
5. DisplayPort source packetizes video data from the video generator testbench and sends it to DisplayPort sink.
6. DisplayPort sink decodes video data from main link and outputs to video interface.
7. Video checker testbench compares received video data with the video generator testbench.
8. Test passes when the video data matches.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

7.5.2. Simulation Steps

To run functional simulation, follow these steps:

1. Click the  button located on the **Toolbar** to initiate the **Simulation Wizard** shown in the figure below.

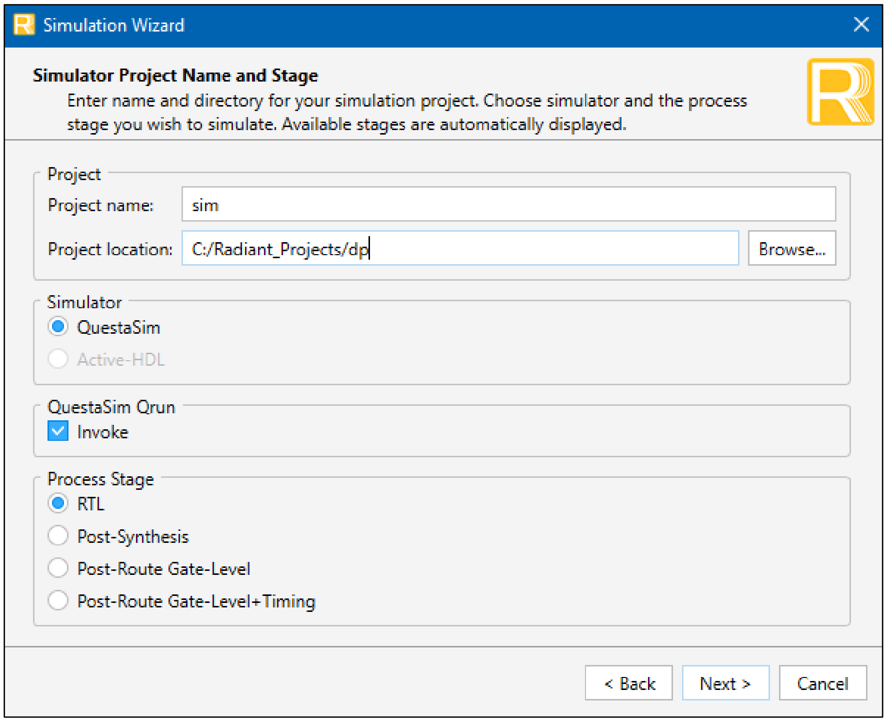


Figure 7.5. Simulation Wizard

2. Click **Next** to open the **Add and Reorder Source** window as shown in the figure below.

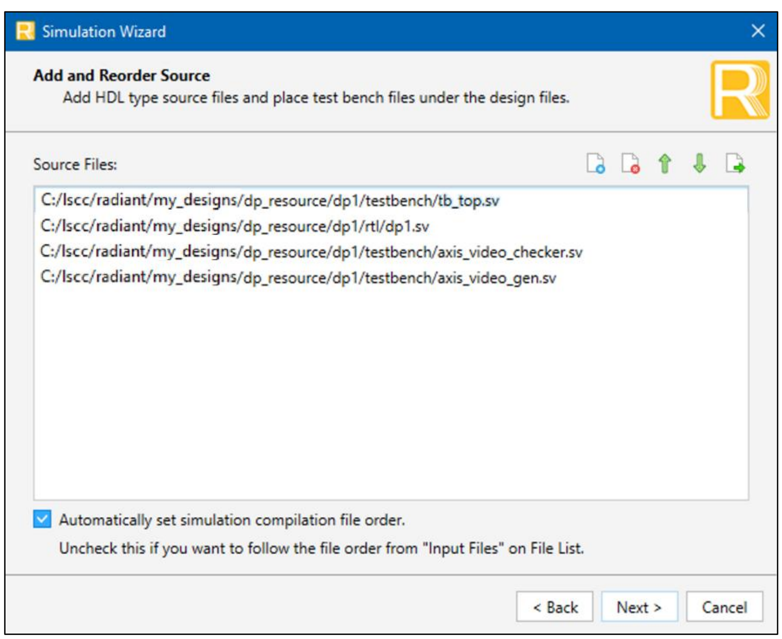


Figure 7.6. Add and Reorder Source

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

3. Select tb_top for **Simulation Top Module**.

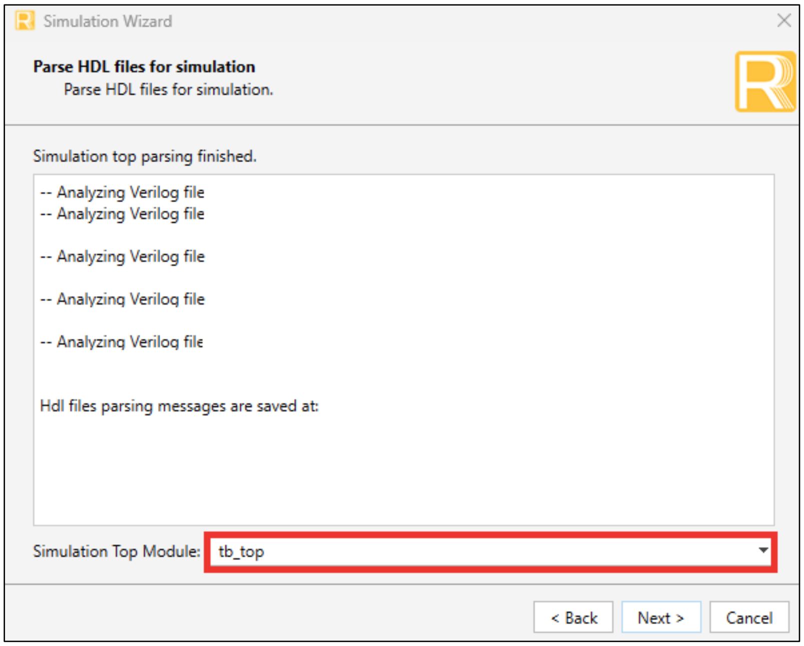


Figure 7.7. Selecting Simulation Top Module

4. Set **Default Run** to 0 for full simulation runtime.

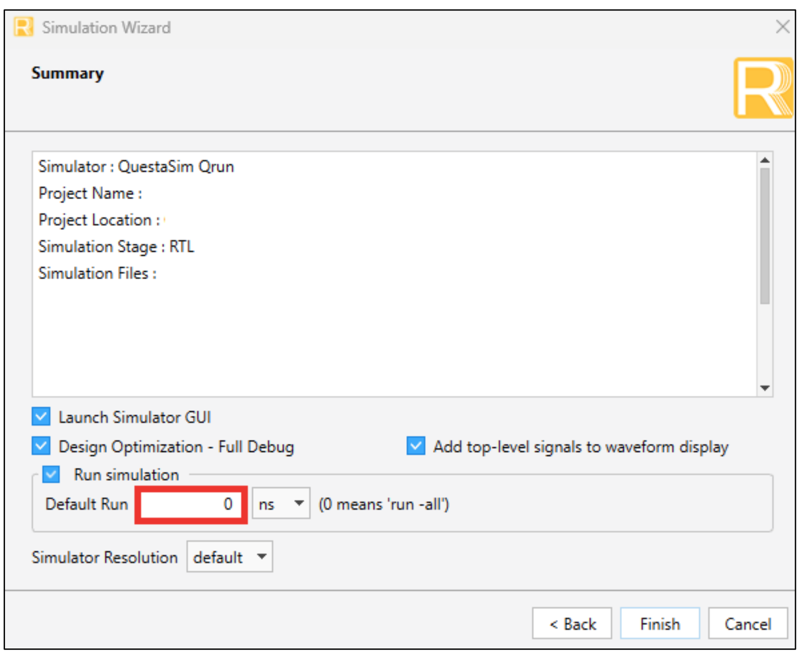


Figure 7.8. Setting Default Run

5. Click **Finish** to run the simulation.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

The figure below shows an example of simulation result. The DisplayPort simulation takes about 1.2 ms to complete the test.

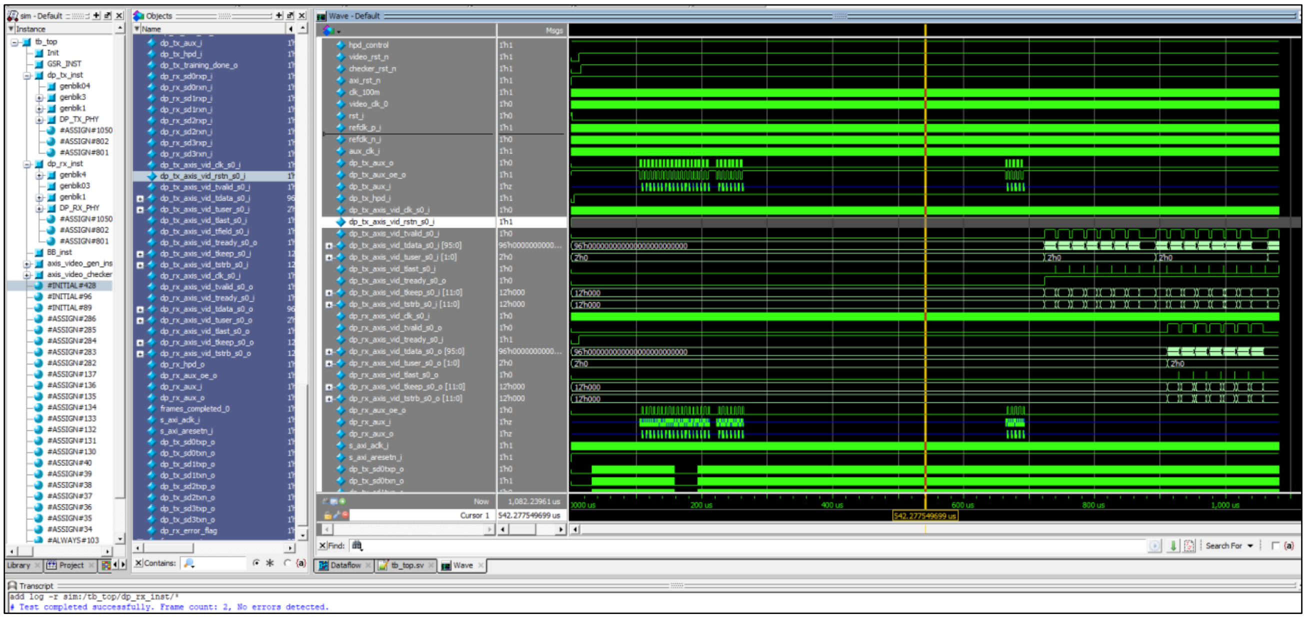


Figure 7.9. Simulation Waveform

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Appendix A. Resource Utilization

Note: Resource utilization values in this section are provided for reference only and may change based on the compilation strategy and selected tool options.

The tables below show the sample resource utilization of the DisplayPort IP.

Table A.1. Resource Utilization Using the LFCPNX-100 LFG672 Device

DisplayPort IP	Colorimetry	AXI-L Register	BPC	LUT4	Registers	EBR
DP Rx	RGB, YCbCr444	Disabled	6	6579	6284	11
			8	6619	6464	11
			10	7479	6759	12
			12	8747	7538	13
			16	9031	7925	14
		Enabled	6, 8	7173	8519	11
	YCbCr422	Disabled	8	6370	6223	11
			10	6524	6398	12
			12	6649	6556	13
			16	6859	6859	14
DP Tx	RGB, YCbCr444	Disabled	6	6969	4901	21
			8	5812	4946	21
			10	7735	4999	21
			12	6876	5053	22
			16	5848	5209	23
		Enabled	6, 8	9482	7213	21
	YCbCr422	Disabled	8	5152	4876	21
			10	6477	4970	21
			12	5780	4945	21
			16	4913	4853	21

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Table A.2. Resource Utilization Using the LAV-AT-X70-3LFG1156C Device

DisplayPort IP	Colorimetry	AXI-L Register	BPC	LUT4	Registers	EBR
DP Rx	RGB, YCbCr444	Disabled	6	6515	6345	9
			8	6576	6523	9
			10	7379	6806	9
			12	8195	7320	10
			16	8438	7756	10
		Enabled	6, 8	7090	8578	9
	YCbCr422	Disabled	8	6329	6224	9
			10	6494	6436	9
			12	6658	6602	10
			16	6707	6922	10
DP Tx	RGB, YCbCr444	Disabled	6	7028	4835	11
			8	5850	4890	11
			10	7815	4946	11
			12	6965	5004	12
			16	5916	5160	12
		Enabled	6, 8	9660	7197	11
	YCbCr422	Disabled	8	5221	4818	11
			10	6535	4915	11
			12	5860	4890	11
			16	4993	4787	11

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

References

- DisplayPort IP Release Notes (FPGA-RN-02071)
- DisplayPort Driver API Reference (FPGA-TN-02423)
- MPCS Module User Guide (FPGA-IPUG-02118)
- Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059)
- Modular FMC Adapter and DisplayPort Daughter Cards web page
- Arm web page for the AMBA AXI Protocol Specification
- VESA web page for the DisplayPort Standard version 1.4a
- CertusPro-NX web page
- Certus-N2 web page
- Avant-G web page
- Avant-X web page
- DisplayPort IP Core web page
- Lattice Radiant Software web page
- Lattice Propel Design Environment web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Revision History

Note: In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

Revision 1.6, IP v2.2.0, June 2026

Section	Change Summary
Abbreviations in This Document	Updated list of abbreviations.

Introduction	• Updated Table 1.1. Summary of the DisplayPort IP as follows:
	  • Added Avant and Certus-N2 devices.
	  • Updated IP version.
	• Updated Table 1.2. DisplayPort IP Support Readiness as follows:
	  • Added Avant and Certus-N2 devices.
	  • Removed the *Hardware* column.
	• Added Avant and Certus-N2 devices in Table 1.3. Ordering Part Number.
	• Added Avant and Certus-N2 devices in Table 1.4. Minimum Device Requirements for DisplayPort IP.

Functional Description	• Removed the *Lattice DisplayPort IP Source Block Diagram* in the DisplayPort Source section.
	• Removed the *Lattice DisplayPort IP Sink Block Diagram* in the DisplayPort Sink section.
	• Updated the following figures:
	  • Figure 2.1. Lattice DisplayPort IP Core Block Diagram
	  • Figure 2.2. Lattice DisplayPort IP Source Interface
	  • Figure 2.3. Lattice DisplayPort IP Sink Interface
	  • Figure 2.6. RGB/YCbCr444 Mapping
	• Added the following sections:
	  • Clocking Overview
	  • Reset

Signal Description	Updated Table 4.1. Signal Ports as follows: • Updated description for the s_axi_aresetn_i, s_axi_aclk_i, refclk_p_i, and refclk_n_i ports. • Updated type for the dp_tx_s_axil_rresp_o and dp_rx_s_axil_rresp_o ports.

Register Description	• Updated default value for field [7:0] in Table 5.2. DP_SOURCE_LINK.
	• Updated description for field [0] in Table 5.4. DP_SOURCE_PHY_RECONFIG.
	• Updated Table 5.14. DP_SOURCE_TU_CALC as follows:
	  • Updated offset values.
	  • Updated description for field [31:8].
	• Updated description for field [31] in Table 5.16. DP_SINK_LT_SEQ_STATUS.
	• Updated offset values in the following tables:
	  • Table 5.19. DP_SINK_MSA0
	  • Table 5.20. DP_SINK_MSA1
	  • Table 5.21. DP_SINK_MSA2
	  • Table 5.22. DP_SINK_MSA3
	  • Table 5.23. DP_SINK_MSA4
	  • Table 5.24. DP_SINK_MSA5
	  • Table 5.25. DP_SINK_MSA6
	  • Table 5.26. DP_SINK_VBID_MSA_STATUS
	• Updated the default value for DPCD offset 0x00002/0x02202 in Table 5.27. DPCD Register.

Example Design	• Added the Lattice Avant G/X Versa Evaluation Board in the Example Design section. • Update figure title from *DisplayPort Example Design Block Diagram* to Figure 6.1. DisplayPort Example Design Block Diagram for CertusPro-NX Devices. • Added Figure 6.2. DisplayPort Example Design Block Diagram for Avant Devices. • Updated the example design blocks in the Example Design Components section. • Removed the *GPIO* section. • Update the I2C_TOP section.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Section	Change Summary
	• Added the OSC section. • Added a note on CertusPro-NX and Avant example design paths in the Running the Example Design on Hardware section. • Updated Figure 6.4. Reconfiguring sysmem. • Updated the Refreshing the Project Software section. • Updated figure title from *Switches and LED Indicators* to Figure 6.7. Switches and LED Indicators for CertusPro-NX Evaluation Board. • Added Figure 6.8. Switches and LED Indicators for Lattice Avant G/X Versa Evaluation Board.
Designing with the IP	• Updated filenames in the Generated Files and File Structure section. • Added the Timing and Physical Constraints section. • Updated the steps in the Simulation Steps section.
Resource Utilization	• Added a note on resource utilization values. • Added Table A.2. Resource Utilization Using the LAV-AT-X70-3LFG1156C Device.
References	Added references to the Certus-N2, Avant-G, and Avant-X web pages.

Revision 1.5, IP v2.1.1, March 2026

Section	Change Summary
Abbreviations in This Document	Updated list of abbreviations.
Introduction	• Updated IP version in Table 1.1. Summary of the DisplayPort IP. • Added description on example design in the IP Support Summary section. • Removed the *Hardware Support* section.
Example Design	• Added a note on IP version in GUI in the Running the Example Design on Hardware section. • Updated the step to regenerate IP instances and added a note on the example design default .mem file in the Recompiling the Project section.
Designing with the IP	Updated Figure 7.4. DisplayPort Simulation Testbench Block Diagram.

Revision 1.4, IP v2.1.0, December 2025

Section	Change Summary
All	• Added a note on IP version in Quick Facts and *Revision History* sections. • Performed minor formatting and editorial edits.
Abbreviations in This Document	Updated list of abbreviations.

Introduction	• Updated Table 1.1. Summary of the DisplayPort IP as follows:
	  ◦ Added LFCPNX-50 devices.
	  ◦ Added AXI4-Lite user interface
	  ◦ Updated IP version.
	  ◦ Added *Resources* and *Driver Support*.
	• Added support for 6 BPC, YCbCr422 color format, and AXI4-Lite for register interface in the Features section.
	• Updated Table 1.4. Minimum Device Requirements for DisplayPort IP.

Functional Description	• Added support for AXI-Lite for IP register access in the IP Architecture Overview section.
	• Updated the address and value for downstream sink device power state for link training in the DisplayPort Source section.
	• Updated the following figures:
	  ◦ Figure 2.1. Lattice DisplayPort IP Core Block Diagram
	  ◦ Figure 2.2. Lattice DisplayPort IP Source Interface
	  ◦ Figure 2.3. Lattice DisplayPort IP Source Block Diagram
	  ◦ Figure 2.4. Lattice DisplayPort IP Sink Interface
	  ◦ Figure 2.5. Lattice DisplayPort IP Sink Block Diagram
	• Updated the description on color format in the TDATA Pixel Mapping section.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Section	Change Summary

	• Added the following figures:
	  • Figure 2.8. RGB/YCbCr444 Mapping
	  • Figure 2.9. YCbCr422 Mapping
	• Removed the following figures:
	  • *RGB/YcbCr444 Mapping of Active BPC When MAX_BPC = 16 and PPC = 1*
	  • *RGB/YcbCr444 Mapping of Active BPC When MAX_BPC = 16 and PPC = 2*
	  • *RGB/YcbCr444 Mapping of Active BPC When MAX_BPC = 12 and PPC = 1*
	  • *RGB/YcbCr444 Mapping of Active BPC When MAX_BPC = 12 and PPC = 2*
	  • *RGB/YcbCr444 Mapping of Active BPC When MAX_BPC = 10 and PPC = 1*
	  • *RGB/YcbCr444 Mapping of Active BPC When MAX_BPC = 8 and PPC = 1*
	  • *RGB/YcbCr444 Mapping of Active BPC When MAX_BPC = 6 and PPC = 1*

IP Parameter Description	Updated Table 3.1. General Attributes as follows: • Added the *AXI4-Lite DPRX Register Enable*, *DPRX Support RGB and YCbCr444*, *DPRX Support YCbCr422*, *AXI4-Lite DPTX Register Enable*, *DPTX Support RGB and YCbCr444*, *DPTX Support YCbCr422*, and *Color Format* attributes. • Updated the *Maximum Bits per Component (BPC)*, *DPRX Support 6BPC*, *DPTX Support 6BPC*, *DPTX Support 8BPC*, *DPTX Support 10BPC*, *DPTX Support 12BPC*, and *DPTX Support 16BPC* attributes. • Corrected the attribute name from *DPRX Support 16BPC* to *DPTX Support 16BPC*.
Signal Description	Updated Table 4.1. Signal Ports as follows: • Updated description for the dp_tx_axis_vid_tuser_s0_i, dp_tx_axis_vid_tlast_s0_i, dp_tx_axis_vid_tkeep_s0_i, dp_tx_axis_vid_tready_s0_o, dp_rx_axis_vid_tkeep_s0_o, dp_rx_axis_vid_tstrb_s0_o signals. • Added the dp_tx_s_axil_* and dp_rx_s_axil_* signals.

Register Description	• Renamed section from *DPCD Register Description* to Register Description.
	• Added the following sections:
	  • DP Source Register Description
	  • DP Sink Register Description
	• Removed the *Access* column in Table 5.27. DPCD Register.

Example Design	• Updated Table 6.1. DisplayPort IP Configuration Supported by the Example Design as follows:
	  • Added the *AXI4-Lite DPRX Register Enable*, *DPRX Support RGB and YCbCr444*, *DPRX Support YCbCr422*, *AXI4-Lite DPTX Register Enable*, *DPTX Support RGB and YCbCr444*, *DPTX Support YCbCr422*, and *Color Format* attributes.
	  • Updated the *DPRX Support 6BPC*, *eDP Support ASSR*, *DPTX Support 6BPC*, and *Default Resolution* attributes.
	• Updated the Example Design Components section.
	• Added the Running the Example Design on Hardware section.
	• Removed the *Simulating the Example Design* section.

Designing with the IP	• Added a note on IP version in GUI in the Designing with the IP section.
	• Updated the following figures:
	  • Figure 7.1. Module/IP Block Wizard
	  • Figure 7.2. IP Configuration
	  • Figure 7.3. Check Generated Result
	• Updated the Running Functional Simulation section.

Resource Utilization	Updated Table A.1. Resource Utilization Using the LFCPNX-100 LFG672 Device.
References	Updated references.

Revision 1.3, IP v2.0.0, June 2025

Section	Change Summary
Disclaimers	Updated disclaimers.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Section	Change Summary
Abbreviations in This Document	Added definition for ASSR, FMC, UVSI, and VB-ID.

Introduction	• Reworked section *1 Introduction* and renamed to subsection 1.1 Introduction.
	• Reworked subsection *1.1 Quick Facts* and moved to subsection 1.2 Quick Facts.
	• Added subsection 1.3 IP Support Summary.
	• Reworked subsection *1.2 Features Supported* and renamed to subsection 1.4 Features.
	• Removed subsection *1.3 Unsupported Features*.
	• Reworked subsection *5.1 Licensing IP* and section *6 Ordering Part Number* and renamed to subsection 1.5 Licensing and Ordering Information.
	• Added the following subsections:
	  • 1.6 Hardware Support
	  • 1.7 Minimum Device Requirements
	• Reworked subsection *1.4 Conventions* and renamed to subsection 1.8 Naming Conventions.

Functional Description	• Reworked subsection *2.1 Overview* and renamed to subsection 2.1 IP Architecture Overview.
	• Reworked subsection *2.2 Transmitter Function* and renamed to subsection 2.2 DisplayPort Source.
	• Reworked subsection *2.3 Receiver Function* and renamed to subsection 2.3 DisplayPort Sink.
	• Reworked subsection *2.4 Interfaces Description* and renamed to subsection 2.4 Unified Video Streaming Interface.
	• Reworked subsection *2.5.5 Pixel Mapping for AXI-Stream* and renamed to subsection 2.4.1 TDATA Pixel Mapping.
	• Removed the following subsections:
	  • *2.5 Architecture and Data Flow of DP Tx*
	  • *2.6 Architecture and Data Flow of DP Rx*
	  • *2.7 Clock Architecture for DP IP*

IP Parameter Description	Reworked subsection *3.8 Attribute Summary* and renamed to section 3 IP Parameter Description.
Signal Description	Reworked the following subsections and renamed to subsection 4 Signal Description: • *3.1. AXI-Lite Interface* • *3.2. Video AXI-Stream Interface for TX Path* • *3.3. Native Video Interface for TX Path* • *3.4. Video AXI-Stream Interface for RX Path* • *3.5. Native Video Interface for Rx Path* • *3.6. Audio AXI-Stream Interface for TX Path* • *3.7. Audio AXI-Stream Interface for RX Path*
DPCD Register Description	Reworked subsection *3.9 Register Description* and renamed to section 5 DPCD Register Description.
Operation Details	Removed this section.
Example Design	Reworked subsection *5.3 Example Designs and Bit File Generation* and renamed to section 6 Example Design.

Designing with the IP	• Reworked section *5 IP Core Generation, Evaluation, and Validation* and renamed to section 7 Designing with the IP.
	• Reworked subsection *5.2 Generation and Synthesis* and renamed to subsection 7.1 Generating and Instantiating the IP.
	• Added the following subsections:
	  • 7.2 Design Implementation
	  • 7.3 Specifying the Strategy
	• Reworked subsection *5.4 Running Functional Simulation* and moved to subsection 7.4 Running Functional Simulation.

Resource Utilization	Reworked section content.
References	Updated references.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Revision 1.2, June 2024

Section	Change Summary
Introduction	• Minor editorial changes. • Updated Lattice Implementation in Table 1.1. DisplayPort IP Quick Facts in Quick Facts section.

Functional Description	• Updated Figure 2.2. DP Tx Path Data Flow in Architecture and Data Flow of DP Tx section.
	• In Pixel Mapping for AXI-Stream section:
	  • Updated discussion on TKEEP and TSTROBE/TSTRB.
	  • Updated Figure 2.3. Pixel Data Mapping for different BPC values for PPC=1 and Max BPC=16.
	• Updated term from *continuous stream of pixel data* to *continuous lane data* in MTP Demultiplexer section.
	• Updated term from *stream of pixel data* to *stream data* in Pixel Demapper section.
	• Minor editorial changes.

Signal Description	• Minor editorial changes.
	• Updated Figure 3.1. DisplayPort IP Interface Diagram.
	• Table 3.1. Signal Description of DP IP Core:
	  • Added dp_tx_out_clk_o signal under DP TX Signals.
	  • Updated description of dp_tx_aux_oe_o under AUX Interface.
	  • Added dp_rx_user_clk_i under DP RX Signals.
	• Table 3.3. Video AXI-Stream Interface Signal Description for TX Path in Video AXI-Stream Interface for TX Path section:
	  • Added dp_tx_axis_vid_tkeep_s[x]_i and dp_tx_axis_vid_tstrb_s[x]_i signals.
	  • Added notes for dp_tx_axis_vid_tkeep_s[x] and dp_tx_axis_vid_tstrb_s[x].
	  • Moved Video Timer Generator module discussion out from table note into Video AXI-Stream Interface for TX Path section.
	• Updated the following figures in Video AXI-Stream Interface for TX Path section:
	  • Figure 3.2. DP Tx AXI-Stream Timing Diagram for PPC=1 and MAX BPC=16
	  • Figure 3.3. DP Tx AXI-Stream Timing Diagram for PPC=2 and MAX BPC=16
	  • Figure 3.4. DP Tx AXI-Stream Timing Diagram for PPC=4 and MAX BPC=16
	• Added Figure 3.5. DP Tx AXI-Stream Timing Diagram PPC=4, Active Pixel not multiple of 4, and MAX BPC=16 in Video AXI-Stream Interface for TX Path section.
	• Table 3.5. Video AXI-Stream Interface Signal Description for RX Path in Video AXI-Stream Interface for RX Path section:
	  • Added dp_rx_axis_vid_tkeep_s[x]_o and dp_rx_axis_vid_tstrb_s[x]_o signals.
	  • Added notes for dp_rx_axis_vid_tkeep_s[x]_o and dp_rx_axis_vid_tstrb_s[x]_o.
	• Updated the following figures in Video AXI-Stream Interface for RX Path section:
	  • Figure 3.9. DP Rx AXI-Stream Signal Diagram for PPC=1 and MAX BPC=16
	  • Figure 3.10. DP Rx AXI-Stream Timing Diagram for PPC=2 and MAX BPC=16
	  • Figure 3.11. DP Rx AXI-Stream Timing Diagram for PPC=4 and MAX BPC=16
	• Added Figure 3.12. DP Rx AXI-Stream Timing Diagram PPC=4, Active Pixel not multiple of 4, and MAX BPC=16 in Video AXI-Stream Interface for RX Path section.
	• Updated the following figures in Attribute Summary section:
	  • Figure 3.18. General Tab
	  • Figure 3.19. DP Tx Settings Tab
	  • Figure 3.20. DP Rx Settings Tab
	  • Figure 3.21. Tx Video Settings Tab
	• Table 3.9. Attributes Table in Attribute Summary section:
	  • Added Lattice Hardware Specific Options attributes.
	  • Added Maximum Bits per component attribute under DP Tx Settings - IP Capability.
	  • Added Maximum Bits per component attribute under DP Rx Settings - IP Capability.
	  • Deleted notes to table.
	• Table 3.10. Attribute Descriptions in Attribute Summary section:

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Section	Change Summary
	• Added Lattice Hardware Specific Options attributes. • Added Maximum Bits per component attribute under DP Tx Settings - IP Capability. • Added Maximum Bits per component attribute under DP Rx Settings - IP Capability. • Updated attribute name to DP TX Activate under TX Video Settings - General. • Added registers FRAME_LOCK_STATUS, PIXEL_CNT_PER_LINE_0/1/2/3, and LINE_CNT_PER_FRAME_0/1/2/3 in Table 3.13. Audio and MST Register Map Description in Tx Audio Interface and MST Register Description section. • Removed VTG Register Space Description section.
Operation Details	• Updated Figure 4.2. DP Rx with Non-CPU Based Mode in DP Rx Activated on Start-up section. • Updated Figure 4.3. DP Rx with CPU Mode in DP Rx not Activated on Start-up section.
IP Core Generation, Evaluation, and Validation	• Updated the following figures in Lattice Propel Builder section: • Figure 5.1. Entering Component Name • Figure 5.2. Configuring Parameters • Figure 5.3. Verifying Results • Figure 5.4. Specifying Instance Name • Figure 5.5. Generated Instance • Updated the following figures in Lattice Radiant section: • Figure 5.6. Module/IP Block Wizard • Figure 5.7. Graphical User Interface of DP IP Module • Figure 5.8. Check Generating Result • For procedure to load and implement the example design in Example Designs and Bit File Generation section, updated the following steps: • Updated step 7 to include Swap lanes 0 and 1 for Tx, Invert lanes 2 and 3 for Tx, and Swap lanes 0,1,2,3 for Rx attributes. • Updated steps 9 and 10 to include Maximum Bits per Component attribute. • Updated the following figures in Example Designs and Bit File Generation section: • Figure 5.16. Generating DP IP for DP Tx TEST • Figure 5.17. Setting up of Interface and IP Capability of DP Tx • Figure 5.18. Setting up of Interface and IP Capability of DP Rx • Figure 5.19. Tx Video Settings Tab
Resource Utilization	• Updated Lattice Radiant software version. • Updated resource utilization information in Table A.1 through Table A.6.

Revision 1.1, December 2023

Section	Change Summary
All	• Minor adjustments to ensure that the document is consistent with Lattice Semiconductor's inclusive language policy. • Renamed the document from *DisplayPort IP Core* to *DisplayPort IP*. • Made editorial fixes.
Disclaimers	Added this section.
Inclusive Language	Added boilerplate.
Introduction	• Updated the *Lattice Implementation* description in Table 1.1. • Updated the Features Supported section.
Functional Description	• Updated the Normal Operation section. • Updated Figure 2.2. • Added the paragraph *For BPCs lower than the selected Maximum BPC, the component data are aligned to the lower part of the slots, leaving the upper bits unused as shown in Figure 2.3. In 4 PPC configurations, if the number of active pixels in a line is not a multiple of 4, the active pixels map to the lower part of the full 4-pixels wide bus. It must be noted that the AXI-Stream byte qualifiers TKEEP and TSTROBE are not used by the DP IP* to the Pixel Mapping for AXI-Stream section.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Section	Change Summary
	• Updated Figure 2.3.
Signal Description	• Updated the *Serial Data Output (Main Channel)* in Table 3.1. • Updated the table note of Table 3.5. • Updated Table 3.7 – Table 3.10. • Updated the first and second paragraphs of the Attribute Summary section. • Added table notes for Table 3.9, and updated the table notes for Table 3.11. • Updated Table 3.12, and Table 3.13. • Updated Table 3.15 – Table 3.17. • Removed item number 13 from the list in DPCD Register Map section. • Renamed *DOWN_REQ Sideband msg* register to *DOWN_REP* in Table 3.18.
Operational Details	• Added steps 15-21 to the list of operational flow in DP Tx Operation Details section. • Updated DP Rx not Activated on Start-up, and Operation Flow sections. • Renamed Figure 4.1.
IP Core Generation, Evaluation, and Validation	• Updated the first sentence and change the IP name from *DP IP Core Module* to *DP IP Core* in the Lattice Radiant section. • Updated the caption for Figure 5.7. • Updated the first paragraph and first step of the Example Designs and Bit File Generation section. • Updated Table 5.2. • Removed steps 14 and 19, and updated steps 17-18 of the Example Designs and Bit File Generation section. • Updated the Running Functional Simulation section. • Added step 22 to the Example Designs and Bit File Generation section. • Updated the description for *DEFAULT*, and *FRAME_COUNT* in Table 5.3. • Updated the description column and added *vc_payload_id_en_3* in Table 5.4.
Resource Utilization	• Removed the phrase *or 8.1 Gbps*, and *SST mode* in the second paragraph of this section. • Updated the Lattice Radiant Software version from *2022.1* to *2023.1*. • Updated Table A.1 – Table A.6.
References	Added references to Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059) document, and Lattice Propel Design Environment web page.

Revision 1.0, August 2023

Section	Change Summary
All	Initial release.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

www.latticesemi.com