Lattice Radiant 2023.1 Software Release Notes

Welcome to Lattice Radiant® software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs).

What's New in Radiant 2023.1 Software

- **Device Support:**
  - MachXO5™-NX (LFMXO5)
    - 55T (-7/-8/-9) 1.00V (COM/IND) – BBG400
    - 100T (-7/-8/-9) 1.00V (COM/IND) – BBG400

- **Tool and Other Enhancements:**

  - **Block-Based Design** – The Block-Based Design feature has been added to the Radiant software. This new feature allows you to implement macros in your project, including the ability to export macros and reuse them in other designs.

  - **Message Classification** – The "Critical Warning" message severity level has been added to the Radiant software. This severity level pertains to issues that could result in a functional problem.

  - **Multi-thread Route** – The multi-thread route has been added to the Radiant software for the Avant device. You can now run PAR in multi-thread mode by using the "-exp maxThreads=n" command. The default number of threads in the Avant device is 4, and the maximum is 8.

  - **Place & Route Timing Analysis** – The Place & Route Timing Analysis process has been updated for Avant and other devices. Running PAR Timing Analysis is required for Avant, while it is optional for other devices.

  - **Programmer** – Support for MachXO3D and LFMNX devices have been added to the Programmer tool.

  - **Reports View** – The Constraint Checker Report section has been added to the Synthesis Reports tab of the Radiant software. This section is only visible when Synplify Pro is used.

  - **Reveal Controller** – The implementation of Reveal Controller for Hard IPs has been updated for Radiant 2023.1.

  - **Revision Control** – Radiant will now output a list of files that are recommended to be placed under revision control for the current project.

- **Strategies** – The Command Line Option strategy has been added to Place & Route Timing Analysis to enable the false_path constraint for timing constraints coverage.
- **sysCONFIG Settings** – With this update, at least one of JTAG_PORT, SLAVE_SPI_PORT, SLAVE_I2C_PORT, or SLAVE_I3C_PORT must be enabled for Nexus devices. Otherwise, Map reports a DRC error.
- **Synthesis Tool** – The default synthesis tool for new projects has been changed to Synplify Pro.
- **Timing Analysis Report** – The Timing Analysis Report has been updated for the Avant device. The DELAYB calculation is now included in the data path.
- **Timing Data** – The IOLOGIC GBB timing data for the CertusPro-NX device has been updated for Radiant 2023.1.

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Radiant software, it may be necessary to re-create some IP, per the procedures described in the following table.

These procedures adapt the project for the changes in Radiant software.

<table>
<tr><th rowspan="2">Versions</th><th colspan="3">IP</th><th rowspan="2">IP Regeneration Procedures</th></tr>
<tr><th>Avant-E (LAV-AT-E)</th><th>CrossLink-NX (LIFCL), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP), MachXO5-NX (LFMXO5)</th><th>iCE40UP</th></tr>
<tr><td rowspan="10">2023.1</td><td>OSC</td><td>ADC Sequencer</td><td rowspan="10">N/A</td><td rowspan="10">These IP used in designs created in Radiant 2022.1.1 or earlier must be re-generated in Radiant 2023.1.</td></tr>
<tr><td>PLL</td><td>RAM_DP</td></tr>
<tr><td>GDDR7:1</td><td>RAM_DP_True</td></tr>
<tr><td>DDRPHY</td><td>RAM_DQ</td></tr>
<tr><td>DDR Generic</td><td rowspan="6">ROM</td></tr>
<tr><td>MIPI DPHY</td></tr>
<tr><td>RAM_DP</td></tr>
<tr><td>RAM_DP_True</td></tr>
<tr><td>RAM_DQ</td></tr>
<tr><td>ROM</td></tr>
</table>

The following server IP are not compatible with Radiant 3.0 onwards. Use the latest versions of the IP available on the IP server:

- I2C Master version 1.0.3
- UART 16550 version 1.0.4
- DDR3 SDRAM Controller version 1.1.1
- DDR3 SDRAM Controller version 1.2.1

- LPDDR2 SDRAM Controller Lite version 1.1.1
- LPDDR2 SDRAM Controller Lite version 1.2.1

Supported Devices

Lattice Radiant software can be used with either a free license or a subscription license. The two licenses provide access to different device families.

Device Family	Free License	Subscription License
iCE40 UltraPlus (iCE40UP)	◀	
Lattice Avant (LAV-AT-E) **Note**: A subscription license is required to access full bitstream for the LAV-AT-E device.		◀
CertusPro™-NX (LFCPNX)	Evaluation Mode	◀
Certus™-NX (LFD2NX)	◀	
MachXO5™-NX (LFMXO5)	Evaluation Mode	◀
CrossLink-NX (LIFCL)	◀	
Certus™-NX-RT (UT24C)		RT Subscription
CertusPro™-NX-RT (UT24CP)		RT Subscription

Support for Third-Party Synthesis and Simulator Tools

The Synopsys Synplify Pro® for Lattice synthesis tool and the Siemens ModelSim® Lattice Edition simulator tools are included in the Radiant software.

- **Synopsys Synplify Pro FPGA synthesis software version U-2023.03LR-1**

- Release Notes for Synplify Pro are located in ..\<*install_directory*>\radiant\2023.1\synpbase\doc\. The file name is release_notes.pdf.
- A full set of documents for Synplify Pro are also located in ..\<*install_directory*>\radiant\2023.1\synpbase\doc\.

- **Siemens ModelSim Lattice Edition 2021.4 revision 2021.10**
  - Release Notes for ModelSim Lattice Edition are located in ..\<*install_directory*>\radiant\2023.1\modeltech\. The file names are RELEASE_NOTES.html or RELEASE_NOTES.txt.
  - A full set of documents for ModelSim Lattice Edition are located in ..\<*install_directory*>\radiant\2023.1\modeltech\doc\.
- **Siemens Questa® 2020.4, Cadence Xcelium® 20.09-s012, Synopsys VCS® T-2022.06**

  Note: Cadence Xcelium and Synopsys VCS do not support Lattice Avant (LAV-AT-E).

Help Resources

- Online Help updated with CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP), and Lattice Avant (LAV-AT-E) content.
- To view the Online Help, start the Lattice Radiant software and select the 

"Getting Started" icon under Information Center.

System Requirements

The following shows the basic system requirements for Radiant software:

- Intel Pentium or Pentium-compatible PC
- OS Support:

64-bit OS	Radiant	Synplify Pro	ModelSim
Windows 10	✓	✓	✓
Windows 11	✓	✓*	✓*
Red Hat Enterprise Linux 7.7	✓	✓	✓
Red Hat Enterprise Linux 8.6	✓	✓	✓

64-bit OS	Radiant	Synplify Pro	ModelSim
Ubuntu version 18.04 LTS	✓	✓*	✓*
Ubuntu version 20.04 LTS	✓	✓*	✓*
CentOS 7.7	✓	✓	✓*
CentOS 8.4	✓	✓	✓*

***Note**: The third-party tools have been tested by Lattice on the listed platforms, but the vendors do not officially support them.

- Approximately 50 GB free disk space
- Computer Memory Requirement:
  - Nexus – 16GB
  - LAV-AT-E – 32GB Recommended for running a single project. If running multiple projects, the memory requirement will be higher.
- 1024 X 768 graphics display
- Network adapter for license and network connectivity
- A Web browser with JavaScript capability
- Acrobat Reader

Issues Fixed

The following known issues are fixed in this release. Their workarounds are no longer needed.

When MAP errors out, it only outputs an error code and not an error message.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-16965

Fixed in Radiant 2023.1

Timing Analyzer reports 25 end points from MULT18X18 to slice register.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-17472

Fixed in Radiant 2023.1

The create_clock constraint in *.fdc file is being ignored during post-synthesis.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-17294

Fixed in Radiant 2023.1

Deployment Tool STAPL causes error in JAM/STAPL file generation.

Devices affected: MachXO5-NX (LFMXO5)

Bug number: DNG-17649

Fixed in Radiant 2023.1

The distributed RAM data output does not match its fixed input value on the board.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-16767

Fixed in Radiant 2023.1

Unable to reproduce the same netlist when recompiling an unmodified design using Synplify Pro as a synthesis tool.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-16168

Fixed in Radiant 2023.1

Radiant proceeds with Process/Flow even if there are errors encountered in Synthesis.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-16873

Fixed in Radiant 2023.1

Timing Analyzer Query does not show the timing paths with hold

analysis even though there are hold analysis shown on the Critical Paths Summary.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-16795

Fixed in Radiant 2023.1

Specifying multiple verilog directives on the Project Properties dialog box is not working.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-16072

Fixed in Radiant 2023.1

JTAG/SPI cannot be used as a GPIO in USESRMODE.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-15961

Fixed in Radiant 2023.1

There should be an option to add ECLK to the port definition of the GDDR7:1 IP.

Devices affected: MachXO5-NX (LFMXO5)

Bug number: DNG-15911

Fixed in Radiant 2023.1

LSE crashes when design is synthesized and generates warning messages.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-16211

Fixed in Radiant 2023.1

Place & Route Design generates the following error message: “ERROR -par: A fatal error occurred. The process will now exit.”

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-16301

Fixed in Radiant 2023.1

When Reveal Controller is used for updating the PCS register (reg80) through the controller, it will cause the PCS Register value to be stuck at a value during successive writes.

Devices affected: CertusPro-NX (LFCPNX), CertusPro-NX-RT (UT24CP)

Bug number: DNG-12235, DNG-13920

Fixed in Radiant 2023.1

Reveal Controller will overwrite the registers of the Hard IP.

Devices affected: All except iCE40UP

Bug number: DNG-12253

Fixed in Radiant 2023.1

Known Issues for Radiant 2023.1

The following are known issues for the Radiant Software 2023.1.

After running Reveal Logic Analyzer/Controller, Programmer may fail to access the cable to detect, scan, or download.

Workaround: Reveal Logic Analyzer/Controller must be closed before Programmer can access the cable to detect, scan, or download.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-17592

When Power Calculator reads from your udb design, it may not recognize the protocol type of MPP.

Workaround: Change to the correct protocol in Power Calculator.

Devices affected: Lattice Avant (LAV-AT-E)

Bug number: DNG-17590

In Power Calculator, Vcclk and Vcchp power multipliers should be merged to Vcc.

Workaround: The voltage of Vccclk and Vcchp must be the same as the voltage of Vcc. And the power of Vccclk and Vcchp will be part of Vcc power.

Devices affected: Lattice Avant (LAV-AT-E)

Bug number: DNG-17478

Incorrect number of dedicated IOs are obtained for MPP in LFG676 package.

There are only 72 Dedicated IO in the Avant device, but 102 are shown in the .mrp report.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: Lattice Avant (LAV-AT-E)

Bug number: DNG-17357

With the latest version of Synplify Synthesis tool, preaddsub structures and presub structures are not able to be packed into the DSP primitives in inference.

Workaround: Implement the Multiplier with preaddsub or presub structures through primitive instantiation.

Devices affected: Lattice Avant (LAV-AT-E)

Bug number: DNG-16587

The PHASEDIR function of PLL does not work, the phase shift of CLKOS is still delayed when PHASEDIR = 1.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: Lattice Avant (LAV-AT-E)

Bug number: DNG-16440

When generating IBIS models for LAV-AT-E, you may encounter warning messages indicating that it is not available for output or bidirectional signals. Even if you can generate IBIS models for input signal, it still produces an error.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: Lattice Avant (LAV-AT-E)

Bug number: DNG-15472

When using ModelSim to run Post-Route Gate-Level or Post-Route Gate-Level+Timing simulation, Modelsim may crash if you use a large design file, with error message “Fatal: (vsim-4) ****** Memory allocation failure.”

Workaround: Use QuestaSim 64bit version.

Devices affected: Lattice Avant (LAV-AT-E)

Bug number: DNG-14945

Synplify Pro Lattice OEM (*.srr and *.srf files) may incorrectly report the number of LRAMs for the target device.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CertusPro-NX (LFCPNX-50)

Bug number: DNG-16362

Synplify Pro Lattice OEM may take large amounts of Memory for designs involving large shift register chains.

Workaround: Run affected designs on machines with enough available memory.

Devices affected: Lattice Avant (LAV-AT-E)

Bug number: DNG-15024

When simulating Cordic IP using ModelSim, you may encounter an RTL compilation error.

Workaround: In OEM ModelSim, use the “vsim -voptargs=+acc -L work -L pmi_work -L ovi_lifcl tb_top -suppress 8607” command to finish the compilation.

Devices affected: Lattice Avant (LAV-AT-E)

Bug number: DNG-14888

Reveal Power-on Reset (POR) Debug function does not work when using LSE.

Workaround: Use Synplify Pro.

Devices affected: All except iCE40UP

Bug number: DNG-12861, DNG-13901

The CSI-2/DSI D-PHY Transmitter and Receiver Soft IP simulations fail when using Synopsys VCS as simulation tool.

Workaround: Use Modelsim or QuestaSim simulation tools.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-13225

When simulating Generic DDR, there may be a mismatch in the RTL and post-route simulation. Silicon is not affected.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: All except iCE40UP

Bug number: DNG-9639

MAP incorrectly reports number of DPHY and PCIE/ADC resources for CrossLink-NX (LIFCL) QFN72 package.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-8297