CORDIC Resource Utilization

IP Configuration for Avant Family

LAV-AT-500E-1LFG1156I

Configuration	Clk Fmax (MHz)*	Registers	LUTs	DSP
Default	201.45	1165	1710	0
Mode: Translation, Others = Default	201.45	1153	1458	0
Mode: Sin/Cos, Others = Default	201.45	1003	1446	0
Mode: Arctan, Others = Default	201.45	1080	1414	0
Compensation: DSP-based, *Rounding Method*: Convergent, *Synchronous Reset*: true, *Clock Enable*: true, Others = Default	201.45	1610	3099	8

***Note:** Fmax is generated when the FPGA design only contains CORDIC IP Core, and the target frequency is 200MHz. These values may bereduced when user logic is added to the FPGA design.

IP Configuration for Nexus Family

LIFCL-40-9BG400I

Configuration	Clk Fmax (MHz)*	Registers	LUTs	DSP
Default	200	1157	1334	0
Mode: Translation, Others = Default	200	1145	1320	0
Mode: Sin/Cos, Others = Default	200	1003	1146	0
Architecture= Word-Serial, Others = Default	200	302	585	0
Compensation: DSP-based, Others = Default	200	1242	1311	8

Note: Fmax is generated when the FPGA design only contains CORDIC IP Core, and the target frequency is 100 MHz. These values may be reduced when user logic is added to the FPGA design

CORDIC Resource Utilization

LFD2NX-40-9BG256I

Configuration	Clk Fmax (MHz)*	Registers	LUTs	DSP
Default	200	1157	1334	0
Mode: Translation, Others = Default	200	1145	1320	0
Mode: Sin/Cos, Others = Default	200	1003	1146	0
Mode: Arctan, Others = Default	200	302	585	0
Compensation: DSP-based, Rounding Method: Convergent, Synchronous Reset: true, Clock Enable: true, Others = Default	200	1242	1311	8

Note: Fmax is generated when the FPGA design only contains CORDIC IP Core, and the target frequency is 100 MHz. These values may be reduced when user logic is added to the FPGA design

LFMXO5-25-9BBG400I

Configuration	Clk Fmax (MHz)*	Registers	LUTs	DSP
Default	200	1157	1334	0
Mode: Translation, Others = Default	200	1145	1320	0
Mode: Sin/Cos, Others = Default	200	1003	1146	0
Mode: Arctan, Others = Default	200	1072	1276	0
Compensation: DSP-based, Rounding Method: Convergent, Synchronous Reset: true, Clock Enable: true, Others = Default	197	1437	2621	8

Note: Fmax is generated when the FPGA design only contains CORDIC IP Core, and the target frequency is 100MHz. These values may be reduced when user logic is added to the FPGA design.

LFMXO5-25-7BBG400I

Configuration	Clk Fmax (MHz)*	Registers	LUTs	DSP
Default	145	1157	1334	0
Mode: Translation, Others = Default	156	1145	1320	0
Mode: Sin/Cos, Others = Default	153	1003	1146	0
Mode: Arctan, Others = Default	158	1072	1276	0
Compensation: DSP-based, Rounding Method: Convergent, Synchronous Reset: true, Clock Enable: true, Others = Default	160.694	1437	2621	8

Note: Fmax is generated when the FPGA design only contains CORDIC IP Core, and the target frequency is 100MHz. These values may be reduced when user logic is added to the FPGA design.

FFT Compiler Resource Utilization

ECP[1]

User Configurable Mode	SLICEs	LUTs	Registers	I/Os	sysMEM EBRs	MULT 18x18	f^{MAX}(MHz)
1	722	1423	1239	85	-	-	305
2	345	686	313	85	-	-	161
3	716	1408	1212	69	-	-	285
4	643	1269	1110	53	-	-	274

1. Performance and utilization data are generated targeting an LFE5UM-45F-8BG554C device using Lattice Diamond 3.10 and Synplify Pro M-2017.03L-SP1-1. Performance may vary when using a different software version or targeting a different device density or speed grade within the ECP5 family.

LatticeECP3[1]

User Configurable Mode	SLICEs	LUTs	Registers	I/Os	sysMEM EBRs	MULT 18x18	f^{MAX}(MHz)
1	647	1280	1207	85	-	-	253
2	318	618	278	85	-	-	176
3	640	1261	1175	69	-	-	320
4	609	1203	1102	53	-	-	298

1. Performance and utilization data are generated targeting an LFE3-70E-8FN484CES device using Lattice Diamond 1.0 and Synplify Pro for Lattice D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP3 family.

1. Performance and utilization data are generated targeting a LFXP2-17E-7F484C device using Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeXP2 family.

FFT Compiler Resource Utilization

LatticeECP2M[1]

User Configurable Mode	SLICEs	LUTs	Registers	I/Os	sysMEM EBRs	MULT 18x18	f^{MAX}(MHz)
1	649	1283	1205	85	-	-	279
2	308	602	278	85	-	-	167
3	644	1268	1182	69	-	-	276
4	624	1232	1104	53	-	-	269

1. Performance and utilization data are generated targeting an LFE2M-20E-7F484C device using Lattice Diamond 1.0 and Synplify Pro for Lattice D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2M family.

LatticeECP2[1]

User Configurable Mode	SLICEs	LUTs	Registers	I/Os	sysMEM EBRs	MULT 18x18	f^{MAX}(MHz)
1	649	1283	1205	85	-	-	278
2	308	602	278	85	-	-	171
3	644	1268	1182	69	-	-	262
4	624	1232	1104	53	-	-	271

1. Performance and utilization data are generated targeting an LFE2-20E-7F484C device using Lattice Diamond 1.0 and Synplify Pro for Lattice D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2 family.

LatticeECP[1]

User Configurable Mode	SLICEs	LUTs	Registers	I/Os	sysMEM EBRs	MULT 18x18	f^{MAX}(MHz)
1	649	1196	1210	85	-	-	183
2	331	605	278	85	-	-	128
3	642	1181	1181	69	-	-	172
4	612	1146	1105	53	-	-	188

1. Performance and utilization data are generated targeting an LFECP20E-5F484C device using Lattice Diamond 1.0 and Synplify Pro for Lattice D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP family.

FFT Compiler Resource Utilization

LatticeEC[1]

User Configurable Mode	SLICEs	LUTs	Registers	I/Os	sysMEM EBRs	MULT 18x18	f^{MAX}(MHz)
1	649	1196	1210	85	-	-	188
2	334	611	271	85	-	-	124
3	640	1179	1178	69	-	-	170
4	611	1146	1105	53	-	-	186

1. Performance and utilization data are generated targeting an LFEC20E-5F484C device using Lattice Diamond 1.0 and Synplify Pro for Lattice D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeEC family.

LatticeSC/M[1]

User Configurable Mode	SLICEs	LUTs	Registers	I/Os	sysMEM EBRs	MULT 18x18	f^{MAX}(MHz)
1	833	1631	1224	85	-	-	389
2	402	739	292	85	-	-	235
3	830	1709	1214	69	-	-	332
4	803	1586	1155	53	-	-	390

1. Performance and utilization data are generated targeting an LFSC3GA25E-7F900C device using Lattice Diamond 1.0 and Synplify Pro for Lattice D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeSC/M family.

LatticeXP2[1]

User Configurable Mode	SLICEs	LUTs	Registers	I/Os	sysMEM EBRs	MULT 18x18	f^{MAX}(MHz)
1	649	1283	1205	85	-	-	275
2	308	602	278	85	-	-	159
3	644	1268	1182	69	-	-	279
4	624	1232	1104	53	-	-	274

1. Performance and utilization data are generated targeting an LFXP2-30E-7F484C device using Lattice Diamond 1.0 and Synplify Pro for Lattice D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeXP2 family.

LatticeXP[1]

User Configurable Mode	SLICEs	LUTs	Registers	I/Os	sysMEM EBRs	MULT 18x18	f^{MAX}(MHz)
1	649	1196	1210	85	-	-	174
2	334	611	271	85	-	-	114
3	640	1179	1178	69	-	-	156
4	611	1146	1105	53	-	-	176

1. Performance and utilization data are generated targeting an LFXP20E-5F484C device using Lattice Diamond 1.0 and Synplify Pro for Lattice D-2009.12L-1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeXP family.