

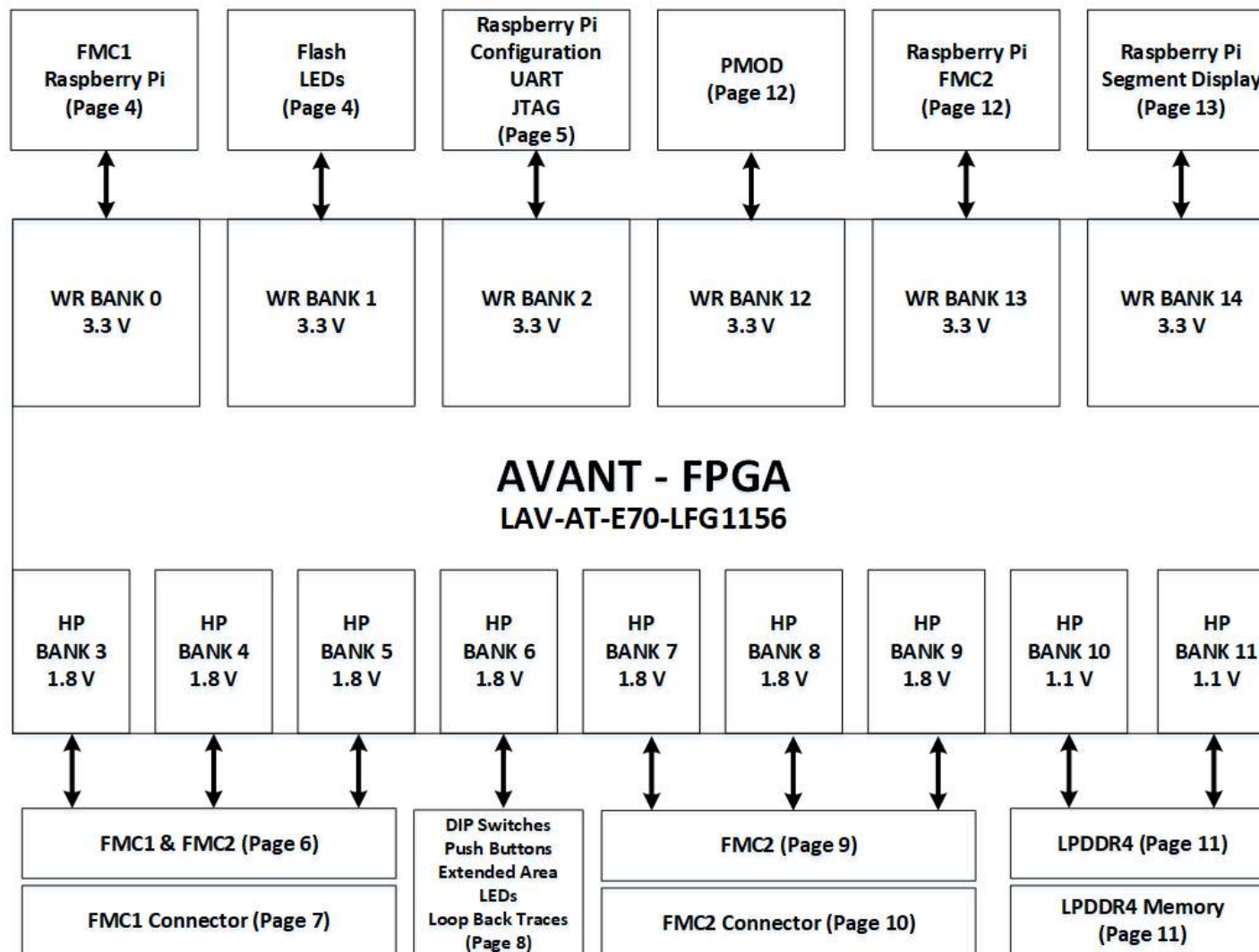
Avant-AT-E Evaluation Board [REV D] (OPN: LAV-E70-EVN)

- 01 - Title Page
- 02 - Block Diagram
- 03 - USB Interface
- 04 - Bank-0/1 Flash, LEDs, FMC1 & Raspberry Pi
- 05 - Bank-2 JTAG, UART, Config & Raspberry Pi
- 06 - Bank-3/4/5 FMC1 & FMC2
- 07 - HPC FMC1
- 08 - Bank-6 Switches, Buttons, LEDs & Extended Bank
- 09 - Bank-7/8/9 FMC2
- 10 - HPC FMC2
- 11 - LPDDR4
- 12 - Bank-12/13 PMODs, FMC2 & Raspberry Pi
- 13 - Bank-14 Segment Display & Raspberry Pi
- 14 - Bank Power
- 15 - Power Decoupling
- 16 - Power Supplies 1
- 17 - Power Supplies 2
- 18 - Ground
- 19 - Platform Manager 2
- 20 - Power Block Diagram



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Title		
Title Page		
Size	Project	Schematic Rev 1.0
B	Avant-AT-E Evaluation Board (LAV-E70-EVN)	Board Rev D
Date:	Tuesday, January 30, 2024	Sheet 1 of 21

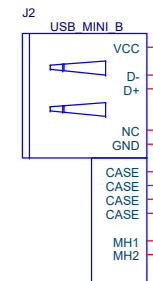


Platform
Manager 2

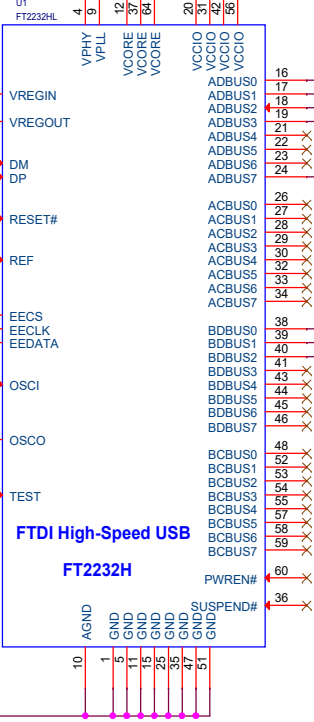
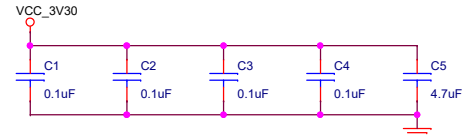
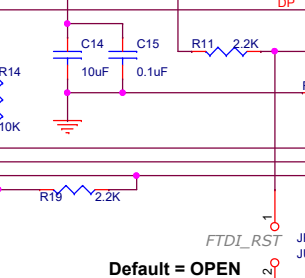
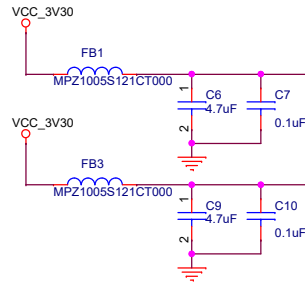
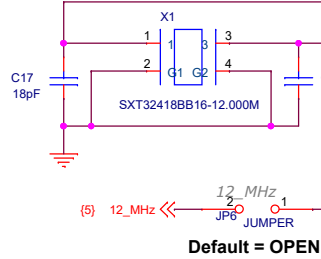
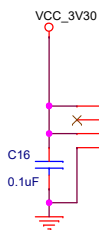
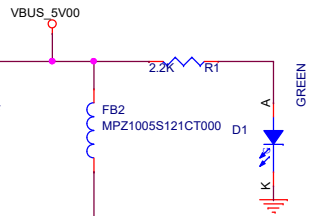
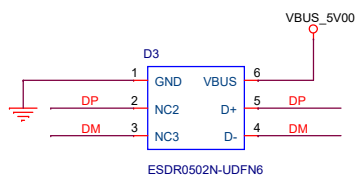


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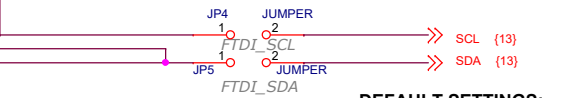
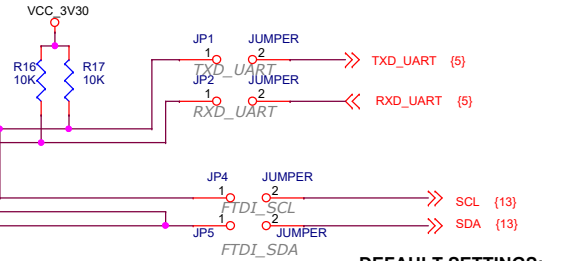
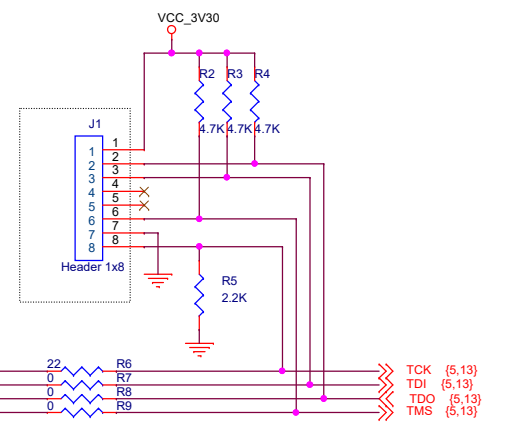
Title			
Block Diagram			
Size	Project	Schematic Rev 1.0	
B	Avant-AT-E Evaluation Board (LAV-E70-EVN)	Board Rev	D
Date:	Tuesday, January 30, 2024	Sheet	2 of 21



Part Number = 1734035-2



FTDI High-Speed USB
FT232H

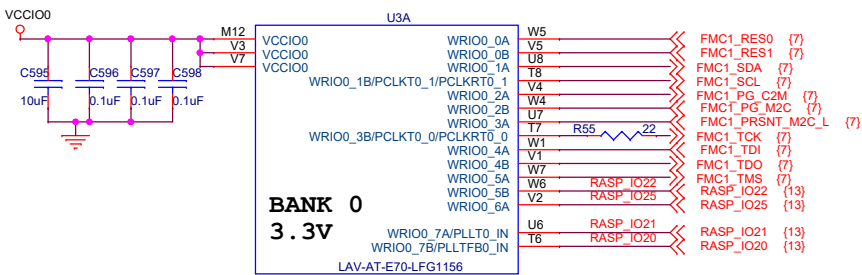


DEFAULT SETTINGS:
JP1 = OPEN
JP2 = OPEN
JP4 = OPEN
JP5 = OPEN



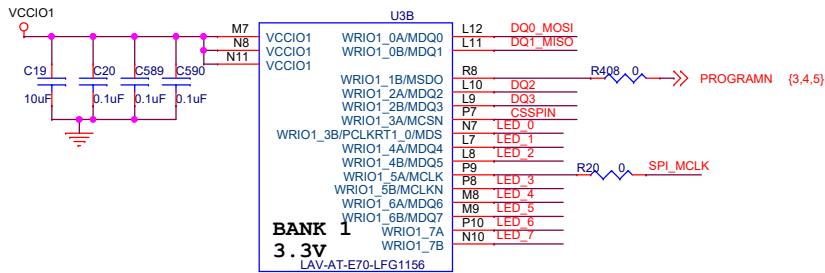
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Title		
USB Interface		
Size	Project	Schematic Rev 1.0
B	Avant-AT-E Evaluation Board (LAV-E70-EVN)	Board Rev D
Date:	Tuesday, January 30, 2024	Sheet 3 of 21

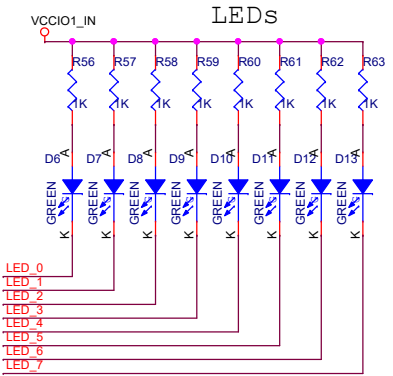
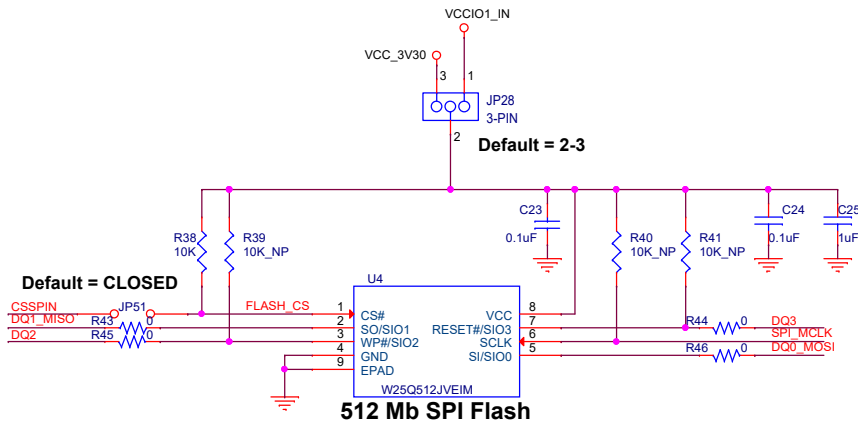
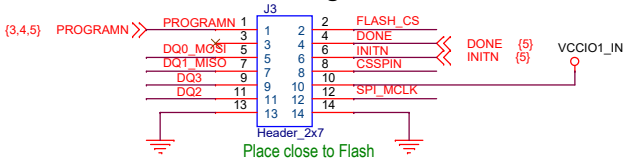


LEDs Signal Map

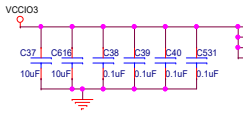
U3 pin	Signal	LED
N7	LED_0	D6
L7	LED_1	D7
L8	LED_2	D8
P8	LED_3	D9
M8	LED_4	D10
M9	LED_5	D11
P10	LED_6	D12
N10	LED_7	D13



Parallel / SPI Config Header

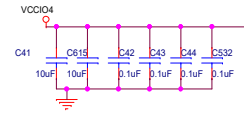


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Title Bank-0/1 Flash, LEDs, FMC & Raspberry Pi			
Size B	Project Avant-AT-E Evaluation Board (LAV-E70-EVN)	Schematic Rev 1.0	Board Rev D
Date: Tuesday, January 30, 2024	Sheet 4		of 21



USD	
VCCIO3	HPI03_0A/DPO_DQ43
VCCIO3	HPI03_0B/DPO_DQ42
VCCIO3	HPI03_1A/DPO_DQ51
VCCIO3	HPI03_1B/DPO_DQ50
VCCIO3	HPI03_2A/DPO_DQ47
VCCIO3	HPI03_2B/DPO_DQ46
VCCIO3	HPI03_3A/DPO_DQ55
VCCIO3	HPI03_3B/DPO_DQ54
VCCIO3	HPI03_4A/DPO_DQ58
VCCIO3	HPI03_4B/DPO_DQ59
VCCIO3	HPI03_5A/DPO_DQ56
VCCIO3	HPI03_5B/DPO_DQ57
VCCIO3	HPI03_6A/DPO_DQ41
VCCIO3	HPI03_6B/DPO_DQ40
VCCIO3	HPI03_7A/DPO_DQ48
VCCIO3	HPI03_7B/DPO_DQ49
VCCIO3	HPI03_8A/DPO_DQ45
VCCIO3	HPI03_8B/DPO_DQ44
VCCIO3	HPI03_9A/DPO_DQ53
VCCIO3	HPI03_9B/DPO_DQ52
HPI03_10A/PCLKT3_0/PCLKRT3_0/DPO_DM0	HPI03_10B/PCLKT3_0/PCLKRT3_0/DPO_DM0
HPI03_11A/PCLKT3_1/PCLKRT3_1/DPO_DM1	HPI03_11B/PCLKT3_1/PCLKRT3_1/DPO_DM1
HPI03_12A/VREF3/DPO_VREF3	HPI03_12B/VREF3/DPO_VREF3
EXT_RES3/DPO_EXT_RES3	
HPI03_13A/PLLT3_IN	HPI03_13B/PLLT3_IN
HPI03_14A/DPO_DQ59	HPI03_14B/DPO_DQ58
HPI03_15A/DPO_DQ67	HPI03_15B/DPO_DQ66
HPI03_16A/DPO_DQ65	HPI03_16B/DPO_DQ64
HPI03_17A/DPO_DQ71	HPI03_17B/DPO_DQ70
HPI03_18A/DPO_DQ68	HPI03_18B/DPO_DQ67
HPI03_19A/DPO_DQ57	HPI03_19B/DPO_DQ56
HPI03_20A/DPO_DQ57	HPI03_20B/DPO_DQ56
HPI03_21A/DPO_DQ65	HPI03_21B/DPO_DQ64
HPI03_22A/DPO_DQ61	HPI03_22B/DPO_DQ60
HPI03_23A/DPO_DQ69	HPI03_23B/DPO_DQ68
HPI03_24A/PCLKRT3_2/DPO_DM7	HPI03_24B/PCLKRT3_2/DPO_DM7
HPI03_25A/PCLKRT3_3/DPO_DM8	HPI03_25B/PCLKRT3_3/DPO_DM8
LAV-AT-E70-LFG1156	

BANK 3
1.8V

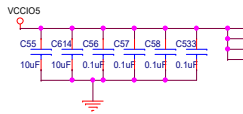


USE	
VCCIO4	HPI04_0A/DPO_MCLKT0
VCCIO4	HPI04_0B/DPO_MCLKT0
VCCIO4	HPI04_1A/DPO_MCLKT1
VCCIO4	HPI04_1B/DPO_MCLKT1
VCCIO4	HPI04_2A/DPO_CKE0
VCCIO4	HPI04_2B/DPO_MA0
VCCIO4	HPI04_3A/DPO_CKE1
VCCIO4	HPI04_3B/DPO_COT1
VCCIO4	HPI04_4A/DPO_MA1
VCCIO4	HPI04_4B/DPO_MA2
VCCIO4	HPI04_5A/DPO_DQ070
VCCIO4	HPI04_5B/DPO_CS_N1
VCCIO4	HPI04_6A/DPO_MA3
VCCIO4	HPI04_6B/DPO_MA4
VCCIO4	HPI04_7A/DPO_CS_N0
VCCIO4	HPI04_7B/DPO_MA8
VCCIO4	HPI04_8A/DPO_MA5
VCCIO4	HPI04_8B/DPO_MA6
VCCIO4	HPI04_9A/DPO_MA10
VCCIO4	HPI04_9B/DPO_MA11
HPI04_10A/PCLKT4_0/PCLKRT4_0/DPO_DM7	HPI04_10B/PCLKT4_0/PCLKRT4_0/DPO_DM7
HPI04_11A/PCLKT4_1/PCLKRT4_1/DPO_DM8	HPI04_11B/PCLKT4_1/PCLKRT4_1/DPO_DM8
HPI04_12A/VREF4/DPO_VREF4	HPI04_12B/VREF4/DPO_VREF4
EXT_RES4/DPO_EXT_RES4	
HPI04_13A/PLLT4_IN	HPI04_13B/PLLT4_IN
HPI04_14A/DPO_DQ03	HPI04_14B/DPO_DQ02
HPI04_15A/DPO_DQ11	HPI04_15B/DPO_DQ10
HPI04_16A/DPO_DQ07	HPI04_16B/DPO_DQ06
HPI04_17A/DPO_DQ15	HPI04_17B/DPO_DQ14
HPI04_18A/DPO_DQ05	HPI04_18B/DPO_DQ04
HPI04_19A/DPO_DQ01	HPI04_19B/DPO_DQ00
HPI04_20A/DPO_DQ09	HPI04_20B/DPO_DQ08
HPI04_21A/DPO_DQ08	HPI04_22A/DPO_DQ05
HPI04_22B/DPO_DQ04	HPI04_23A/DPO_DQ13
HPI04_23B/DPO_DQ12	
HPI04_24A/PCLKRT4_2/DPO_DM0	HPI04_24B/PCLKRT4_2/DPO_DM0
HPI04_25A/PCLKRT4_3/DPO_DM1	HPI04_25B/PCLKRT4_3/DPO_DM1
LAV-AT-E70-LFG1156	

BANK 4
1.8V

Default = OPEN

Default = OPEN



USF	
VCCIO5	HPI05_0A/DPO_DQ36
VCCIO5	HPI05_0B/DPO_DQ37
VCCIO5	HPI05_1A/DPO_DQ20
VCCIO5	HPI05_1B/DPO_DQ21
VCCIO5	HPI05_2A/DPO_DQ32
VCCIO5	HPI05_2B/DPO_DQ33
VCCIO5	HPI05_3A/DPO_DQ16
VCCIO5	HPI05_3B/DPO_DQ17
VCCIO5	HPI05_4A/DPO_DQ34
VCCIO5	HPI05_4B/DPO_DQ35
VCCIO5	HPI05_5A/DPO_DQ32
VCCIO5	HPI05_5B/DPO_DQ31
VCCIO5	HPI05_6A/DPO_DQ38
VCCIO5	HPI05_6B/DPO_DQ39
VCCIO5	HPI05_7A/DPO_DQ22
VCCIO5	HPI05_7B/DPO_DQ23
VCCIO5	HPI05_8A/DPO_DQ34
VCCIO5	HPI05_8B/DPO_DQ35
VCCIO5	HPI05_9A/DPO_DQ18
VCCIO5	HPI05_9B/DPO_DQ19
HPI05_10A/PCLKT5_0/PCLKRT5_0/DPO_DM4	HPI05_10B/PCLKT5_0/PCLKRT5_0/DPO_DM4
HPI05_11A/PCLKT5_1/PCLKRT5_1/DPO_DM2	HPI05_11B/PCLKT5_1/PCLKRT5_1/DPO_DM2
HPI05_12A/VREF5/DPO_VREF5	HPI05_12B/VREF5/DPO_VREF5
EXT_RES5/DPO_EXT_RES5	
HPI05_13A/PLLT5_IN	HPI05_13B/PLLT5_IN
HPI05_14A/DPO_DQ28	HPI05_14B/DPO_DQ29
HPI05_15A/DPO_MCLKT3	HPI05_15B/DPO_MCLKT3
HPI05_16A/DPO_DQ24	HPI05_16B/DPO_DQ25
HPI05_17A/DPO_MCLKT2	HPI05_17B/DPO_MCLKT2
HPI05_18A/DPO_DQ53	HPI05_18B/DPO_DQ54
HPI05_19A/DPO_MA16	HPI05_19B/DPO_MA15
HPI05_20A/DPO_DQ30	HPI05_20B/DPO_DQ31
HPI05_21A/DPO_MA14	HPI05_21B/DPO_MA13
HPI05_22A/DPO_DQ28	HPI05_22B/DPO_DQ27
HPI05_23A/DPO_BA2	HPI05_23B/DPO_BA1
HPI05_24A/PCLKRT5_2/DPO_DM3	HPI05_24B/PCLKRT5_2/DPO_DM3
HPI05_25A/PCLKRT5_3/DPO_DM0	HPI05_25B/PCLKRT5_3/DPO_DM0
LAV-AT-E70-LFG1156	

BANK 5
1.8V

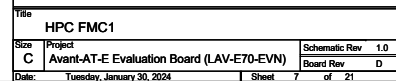
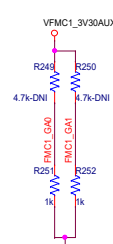
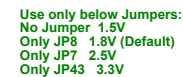
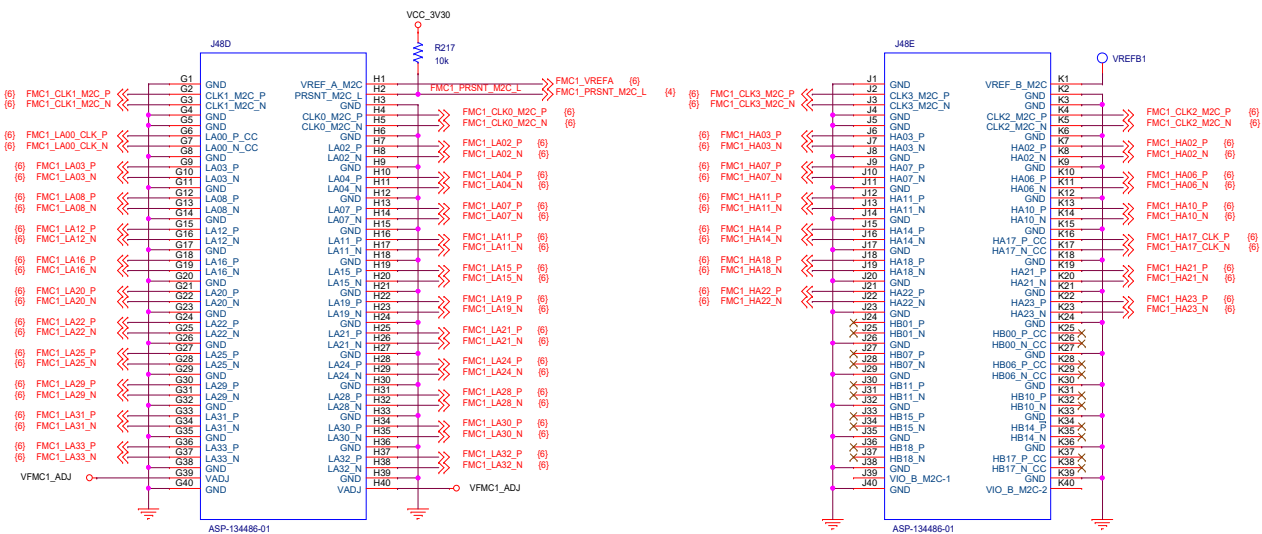
Default = OPEN

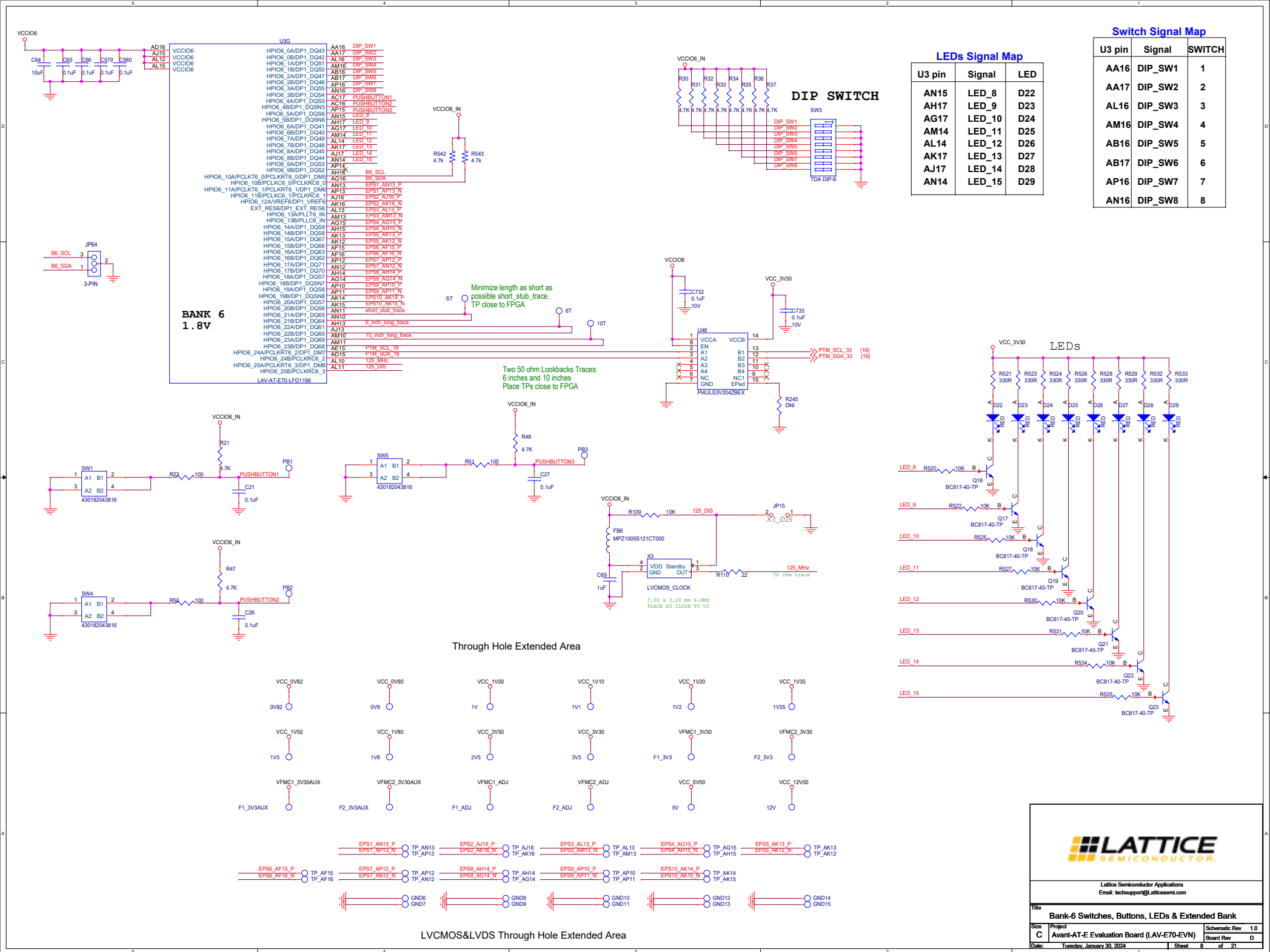
Default = OPEN

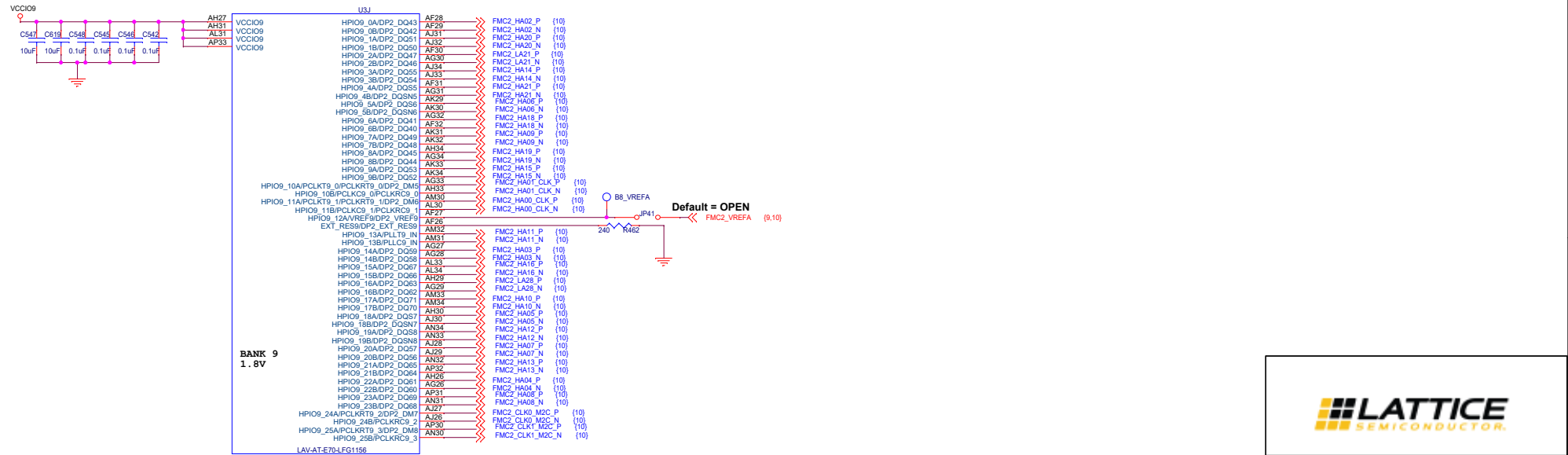


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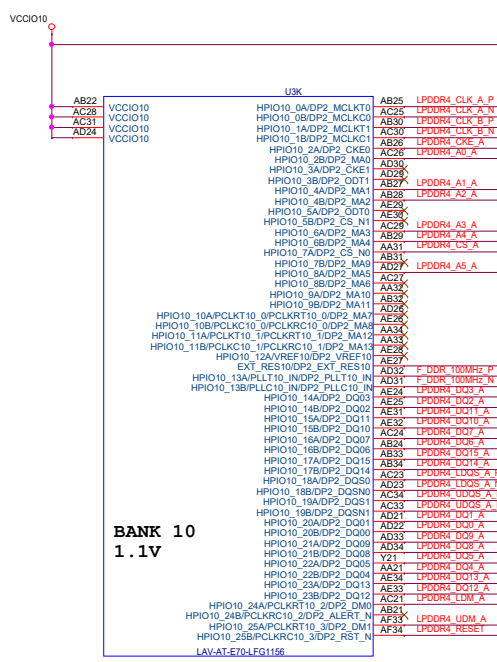
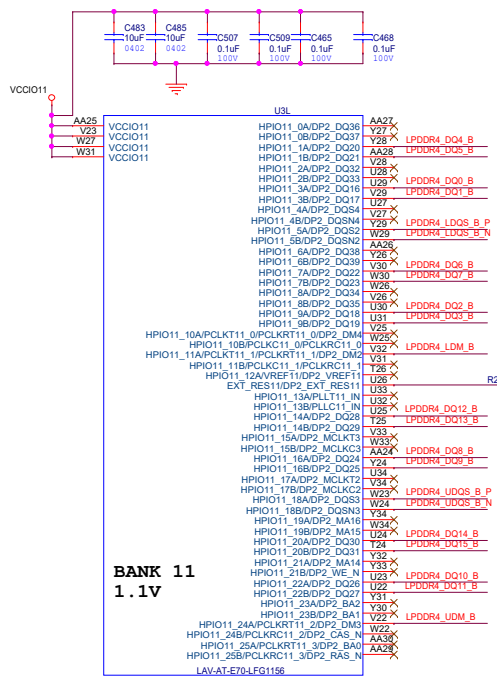
Title Bank 3/4/5 FMC1 & FMC2			
Size C	Project Avant-AT-E Evaluation Board (LAV-E70-EVN)	Schematic Rev 1.0	Board Rev D
Date Tuesday, January 30, 2024	Sheet 6	of 21	





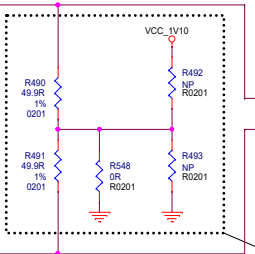


Title Bank-7/8/9 FMC2			
Size C	Project Avant-AT-E Evaluation Board (LAV-E70-EVN)	Schematic Rev 1.0	
		Board Rev D	
Date: Tuesday, January 30, 2024	Sheet 9	of 21	

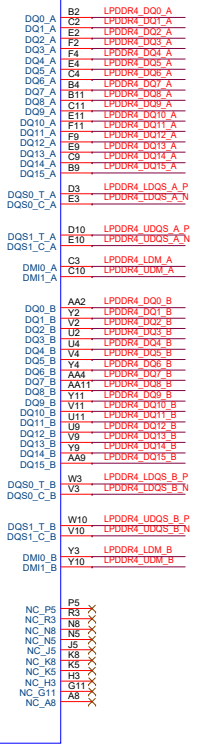
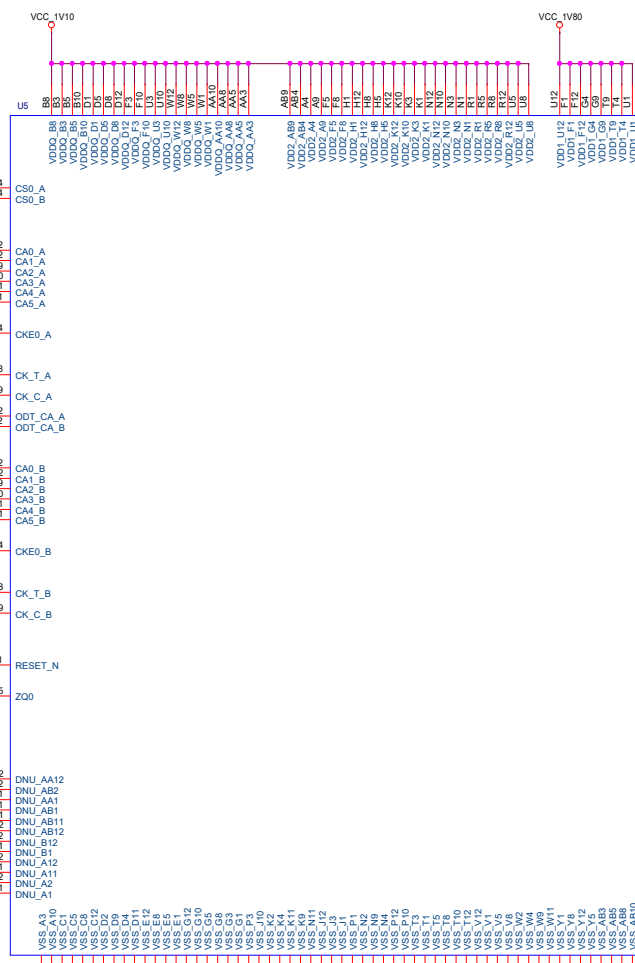


	HCSSL (Default)	LVDS
R490	49.9 Ohms	49.9 Ohms
R491	49.9 Ohms	49.9 Ohms
R492	DNP	2K Ohms
R493	DNP	2K Ohms
R537	0 Ohm	0.1 uF
R538	0 Ohm	0.1 uF
R548	0 Ohm	0.1 uF

Place R490, R491 & R548 close to FPGA

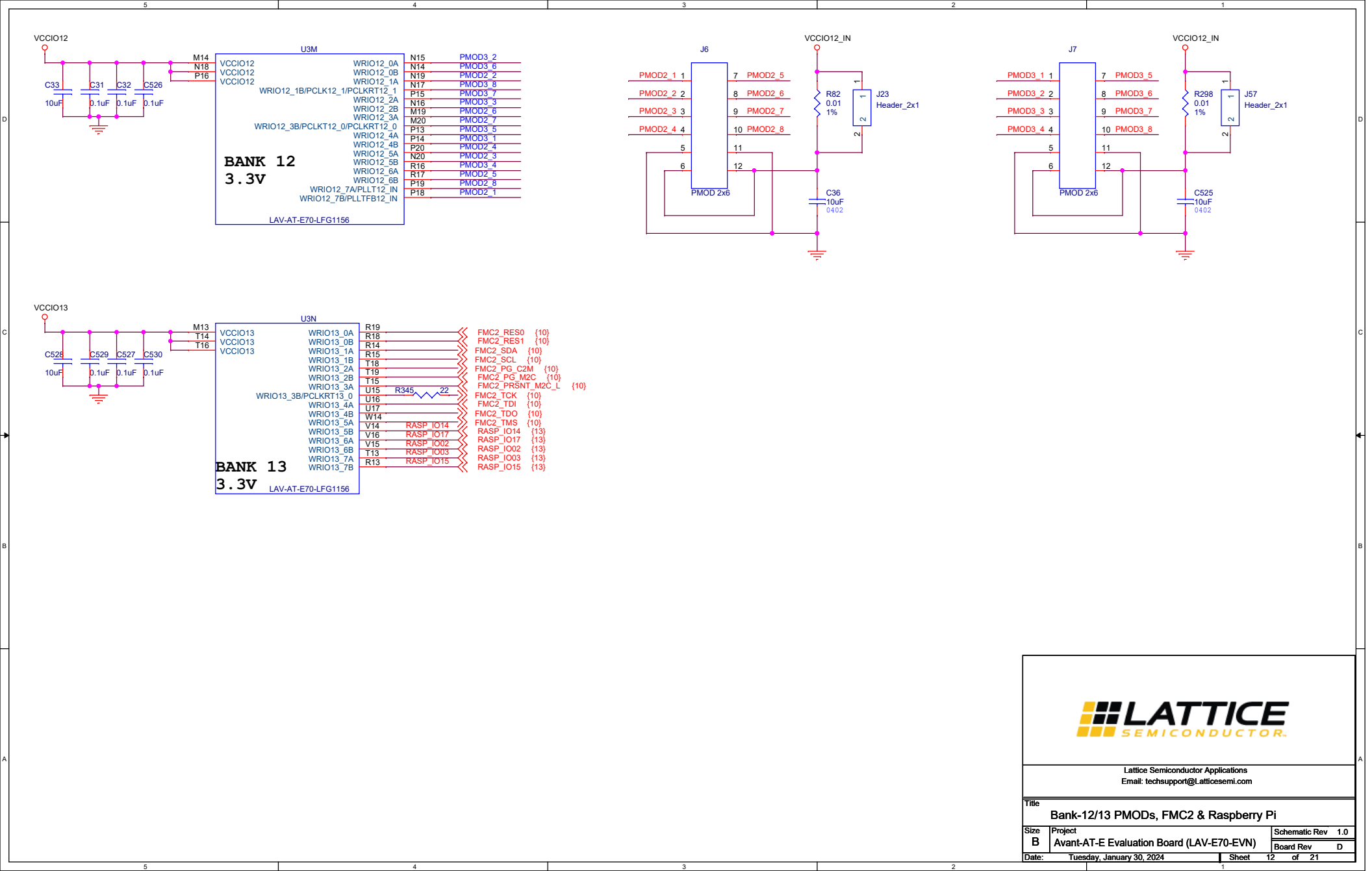


Place this termination circuit to back side of board close to FPGA (not close to Y1)



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Title		LPDDR4	
Size	Project	Schematic Rev 1.0	
C	Avant-AT-E Evaluation Board (LAV-E70-EVN)	Board Rev D	
Date:	Tuesday, January 30, 2024	Sheet	11 of 21

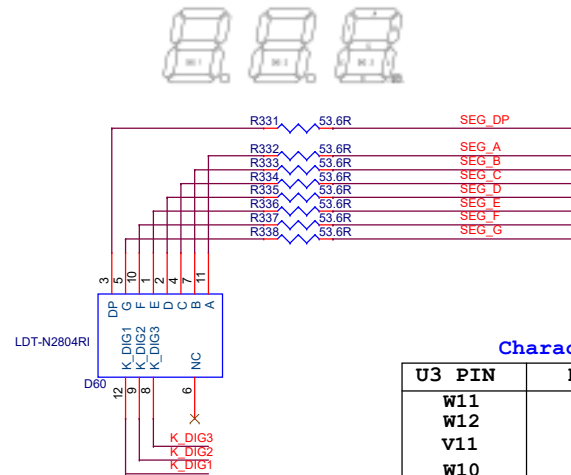
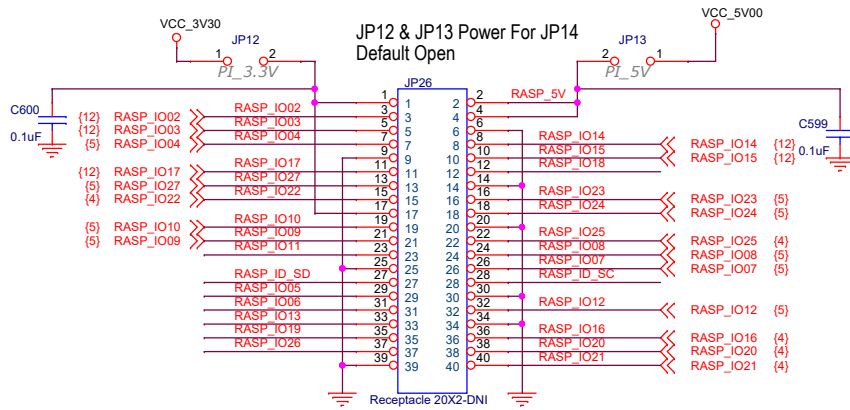


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Title			
Bank-12/13 PMODs, FMC2 & Raspberry Pi			
Size	Project	Schematic Rev 1.0	
B	Avant-AT-E Evaluation Board (LAV-E70-EVN)	Board Rev D	
Date:	Tuesday, January 30, 2024	Sheet	12 of 21

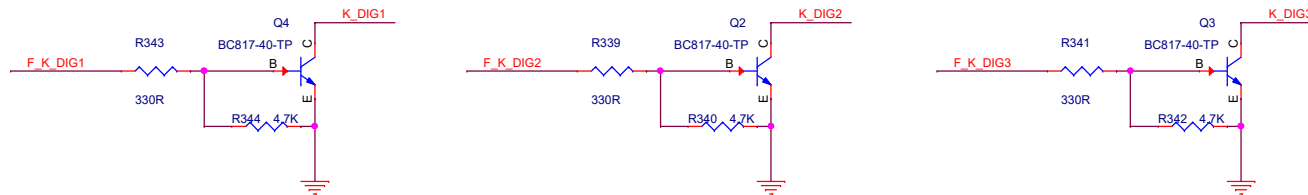
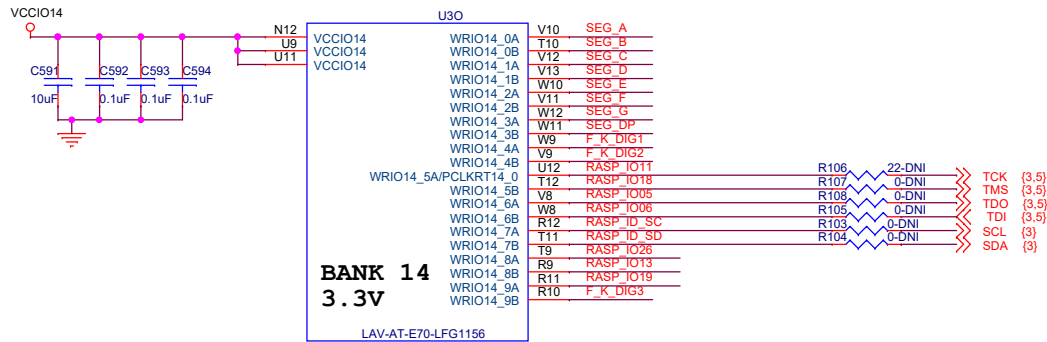
7_SEGMENT_DISPLAY_SECTION

Raspberry PI and User I/O Connector



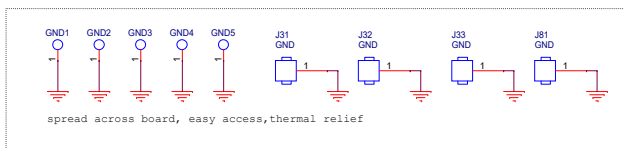
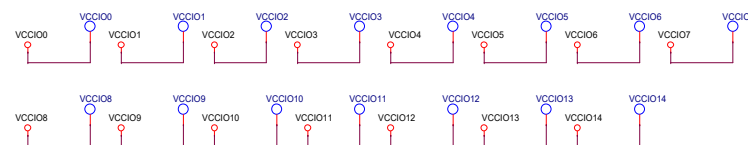
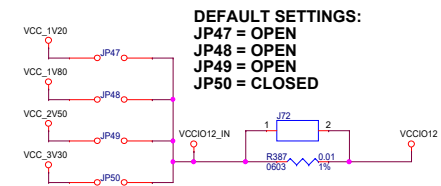
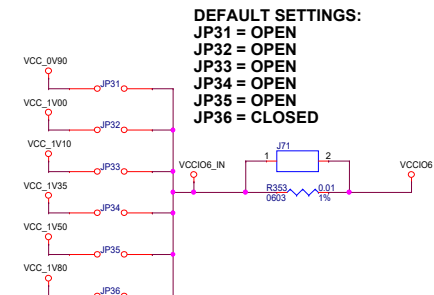
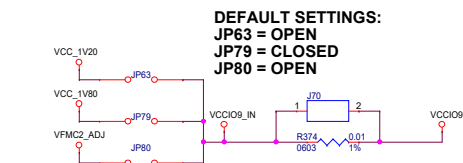
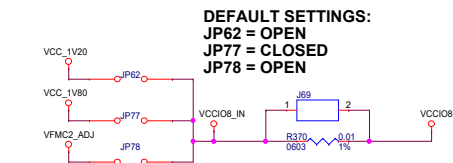
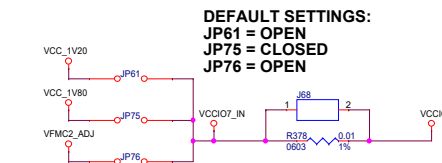
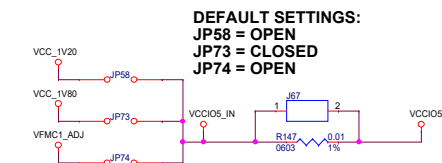
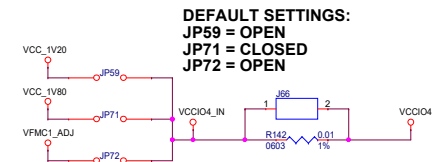
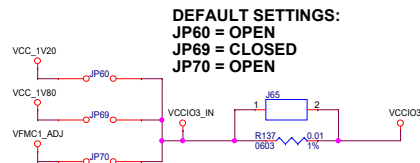
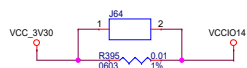
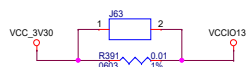
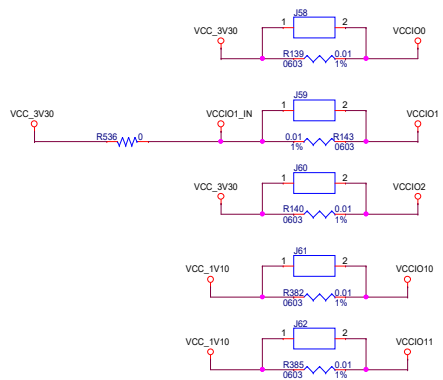
Character Signal Map

U3 PIN	D60 PIN	SEGMENT
W11	3	DP
W12	5	G
V11	10	F
W10	1	E
V13	2	D
V12	4	C
T10	7	B
V10	11	A



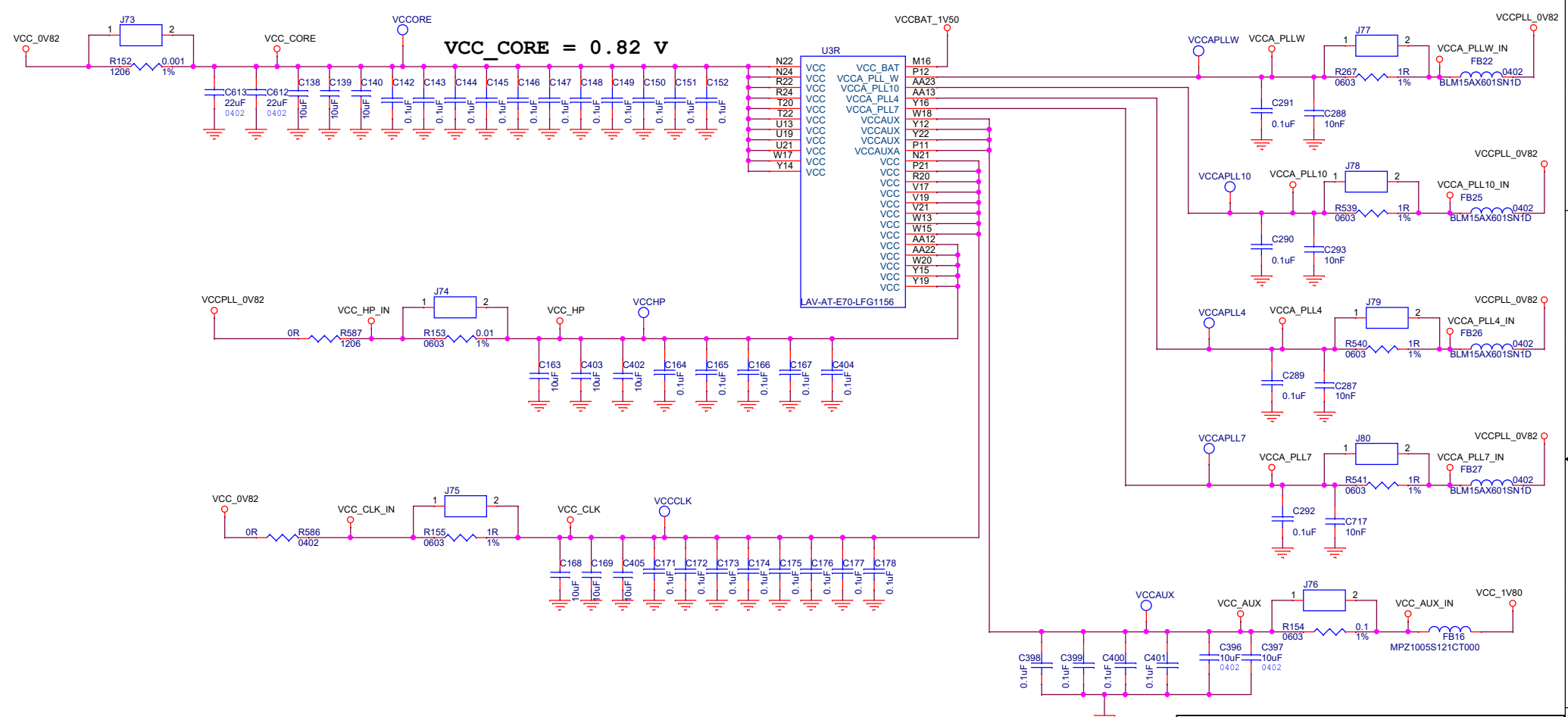
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Title Bank-14 Segment Display & Raspberry Pi			
Size B	Project Avant-AT-E Evaluation Board (LAV-E70-EVN)	Schematic Rev 1.0	
Date: Tuesday, January 30, 2024	Sheet 13	of 21	



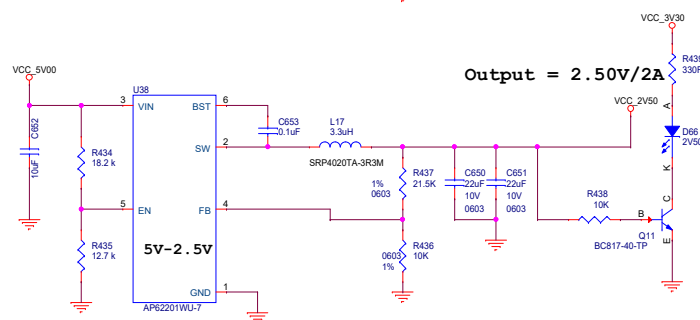
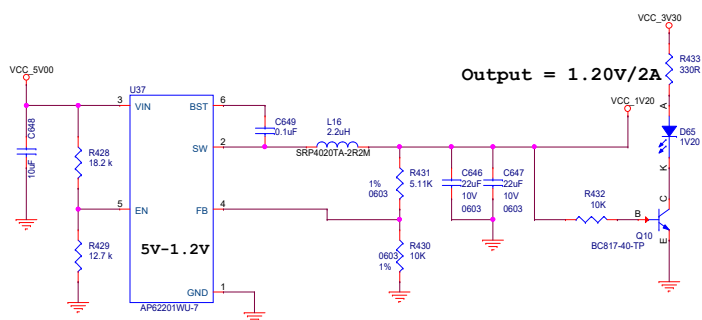
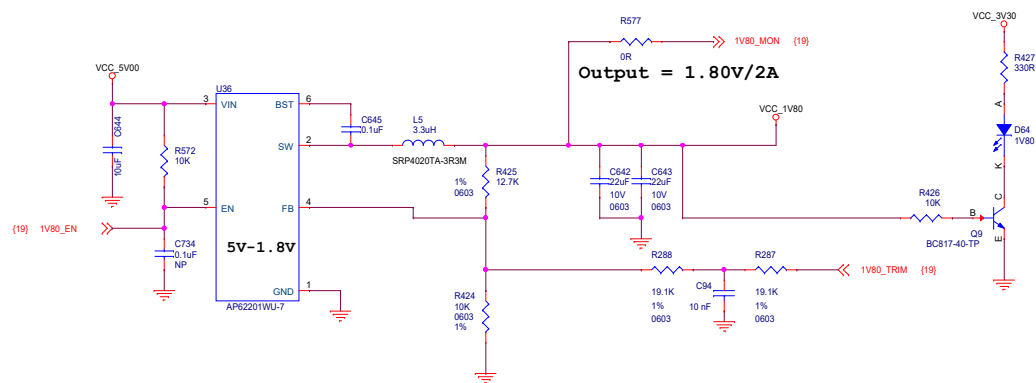
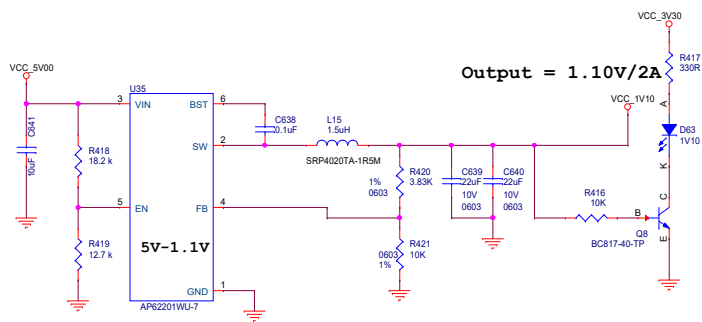
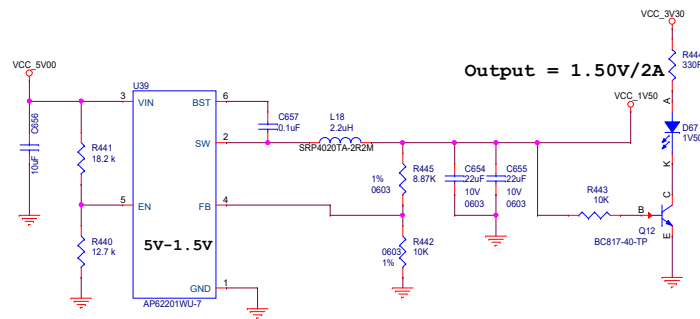
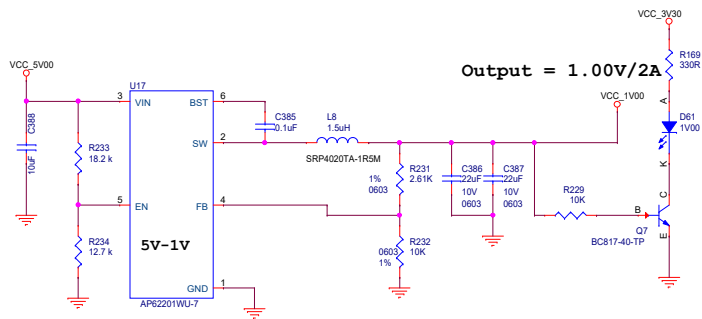
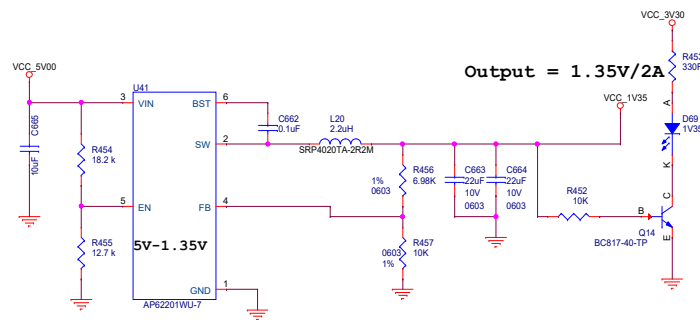
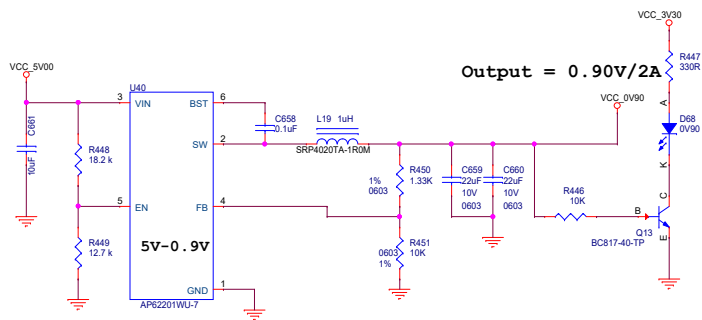
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Title			Bank Power	
Size	Project			Schematic Rev
C	Avant-AT-E Evaluation Board (LAV-E70-EVN)			1.0
Date:	Tuesday, January 30, 2024	Sheet	14	of 21



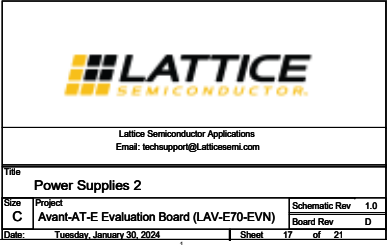
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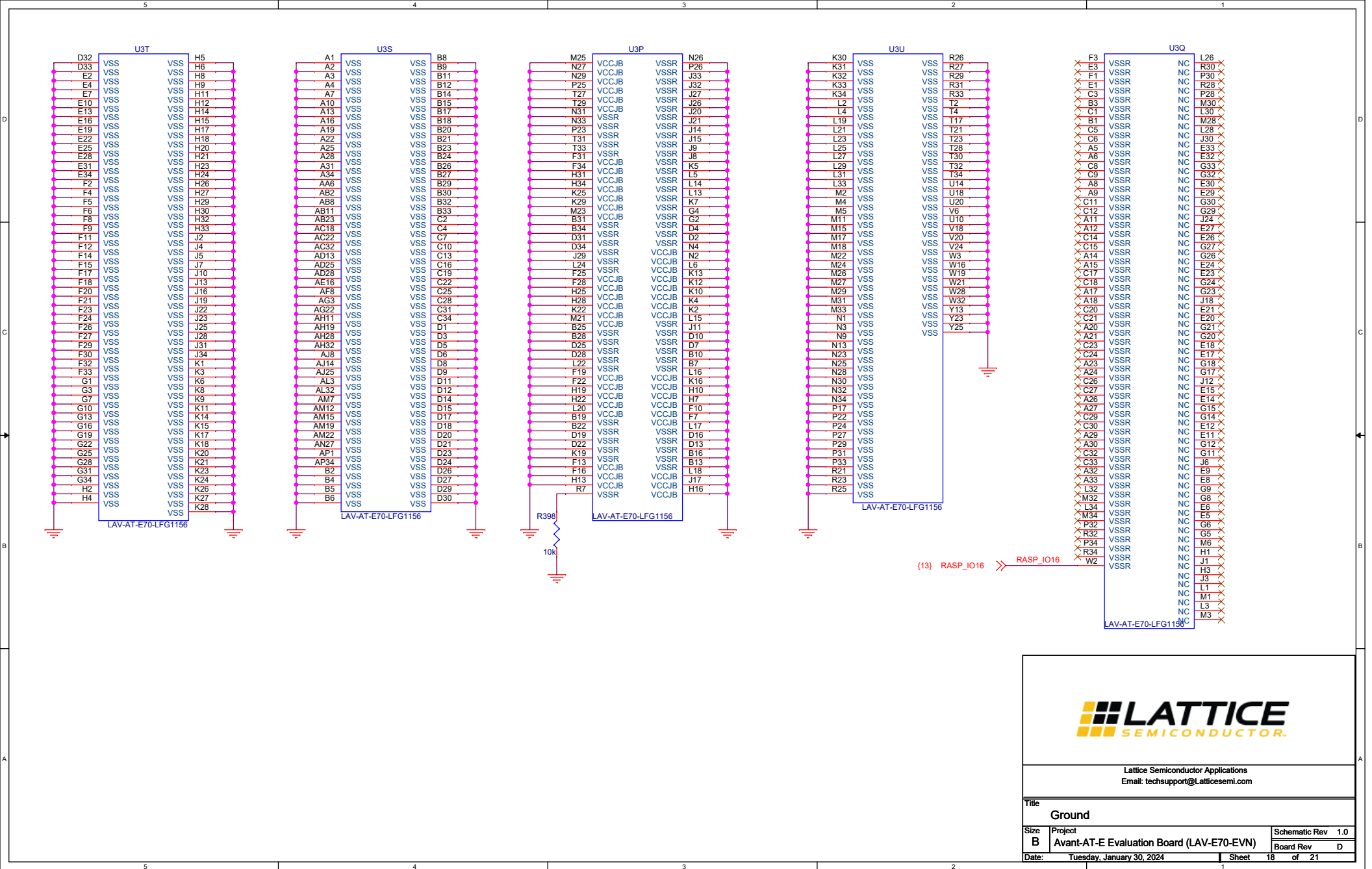
Title				
Power Decoupling				
Size	Project			Schematic Rev 1.0
B	Avant-AT-E Evaluation Board (LAV-E70-EVN)			Board Rev D
Date:	Tuesday, January 30, 2024		Sheet	15 of 21



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Title			Power Supplies 1
Size	Project	Schematic Rev	1.0
C	Avant-AT-E Evaluation Board (LAV-E70-EVN)	Board Rev	D
Date:	Tuesday, January 30, 2024	Sheet	16 of 21

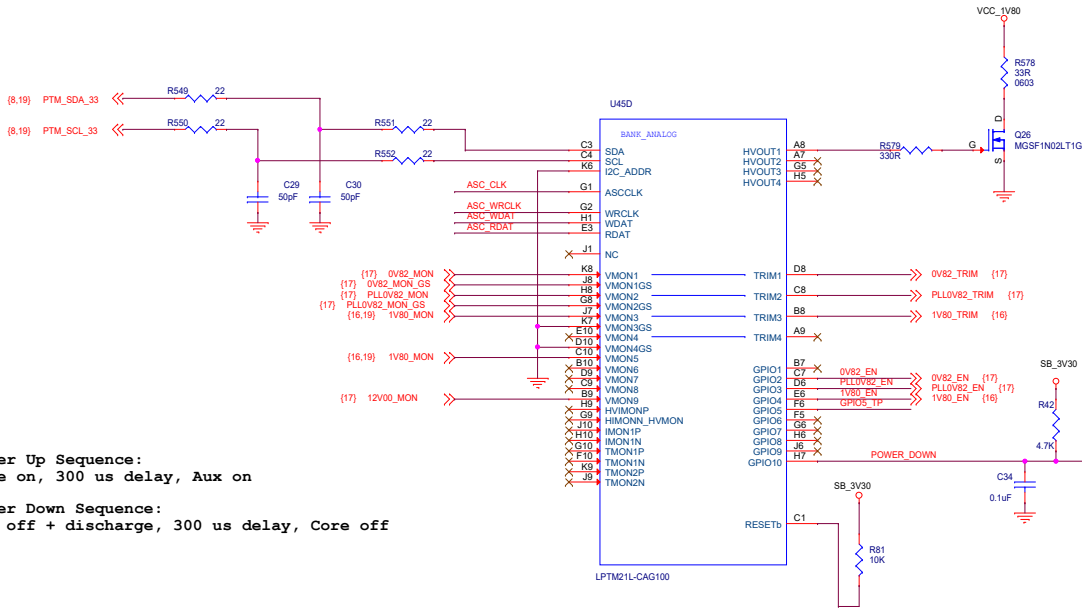
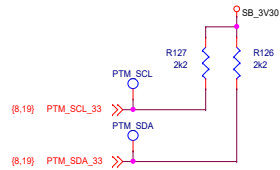




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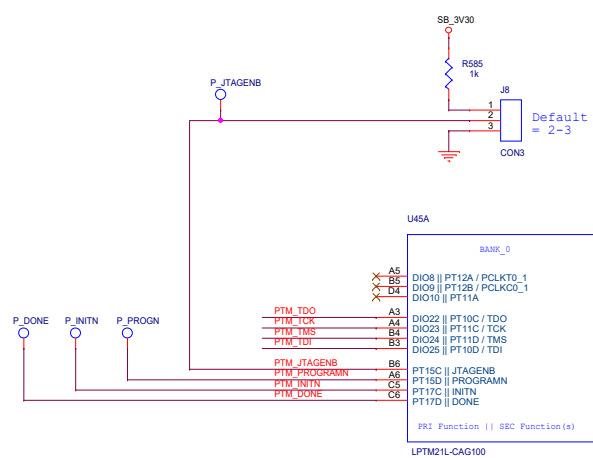
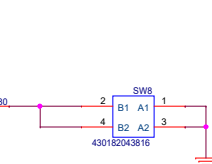
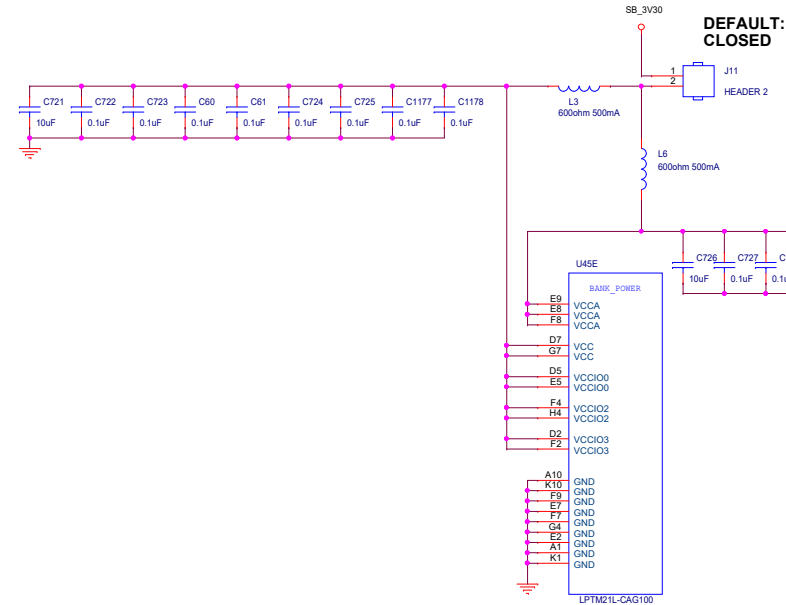
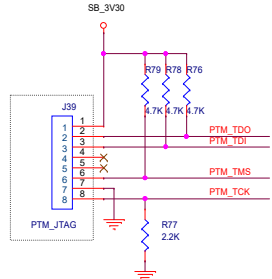
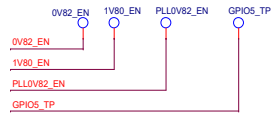
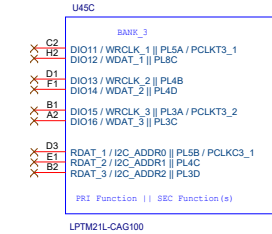
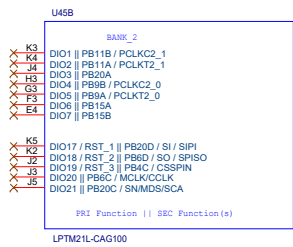
Title		Ground	
Size	Project	Schematic Rev 1.0	
B	Avant-AT-E Evaluation Board (LAV-E70-EVN)	Board Rev D	
Date:	Tuesday, January 30, 2024	Sheet	18 of 21

ASC_CLK ○ ASC_CLK
WRCLK ○ ASC_WRCLK
WDAT ○ ASC_WDAT
RDAT ○ ASC_RDAT



Power Up Sequence:
Core on, 300 us delay, Aux on

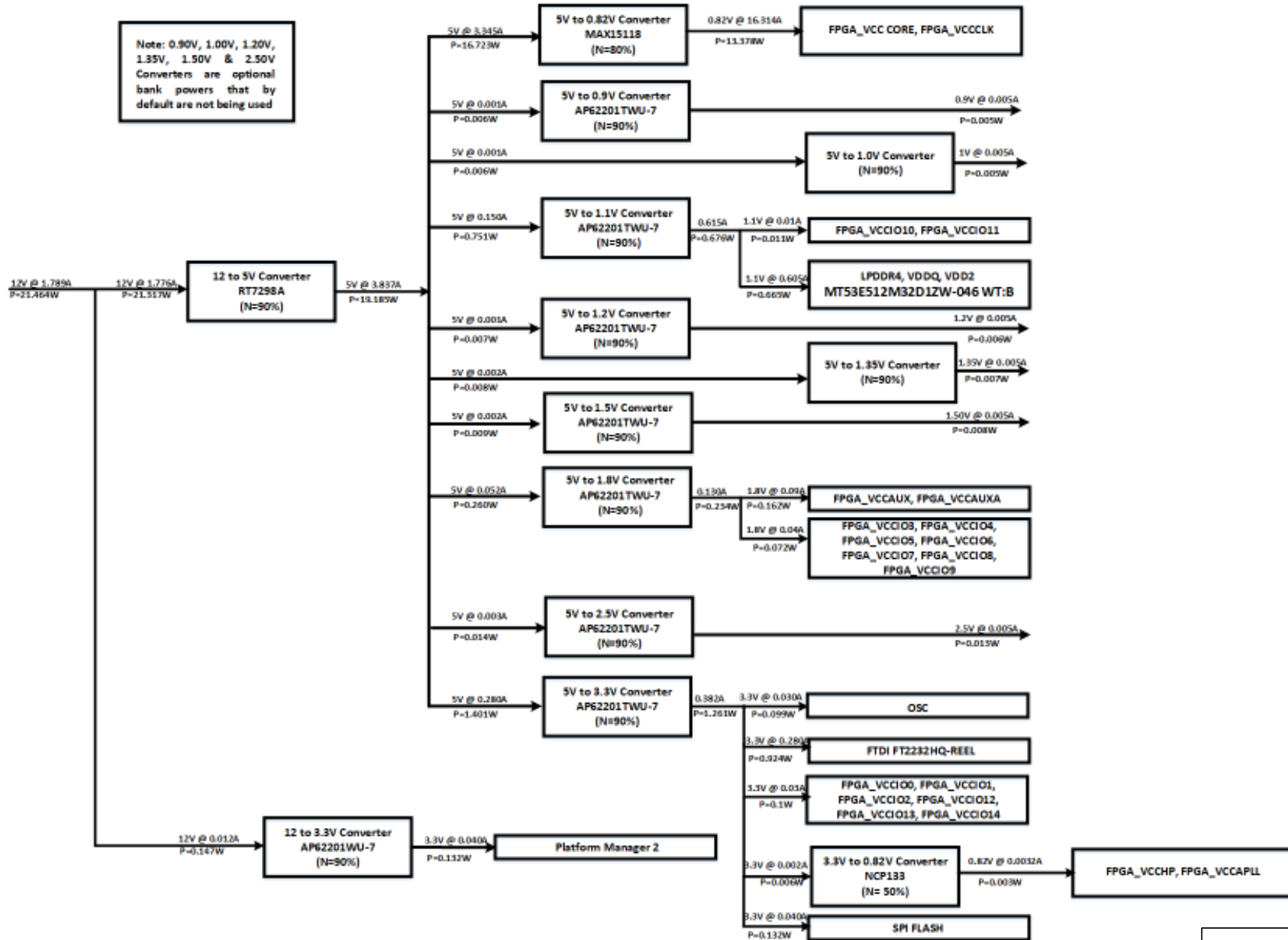
Power Down Sequence:
Aux off + discharge, 300 us delay, Core off



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Platform Manager 2			
Size	Project	Schematic Rev 1.0	
C	Avant-AT-E Evaluation Board (LAV-E70-EVN)	Board Rev D	
Date:	Tuesday, January 30, 2024	Sheet	19 of 21

Note: 0.90V, 1.00V, 1.20V, 1.35V, 1.50V & 2.50V Converters are optional bank powers that by default are not being used



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Title			
Power Block Diagram			
Size	Project	Schematic Rev	
C	Avant-AT-E Evaluation Board (LAV-E70-EVN)	1.0	
Date:	Tuesday, January 30, 2024	Sheet	20 of 21

Avant-AT-E Evaluation Board Revision History

Revision B

--- Initial Release

Revision C

--- Updated LPDDR4 connection to Avant FPGA

--- Added Platform Manager 2 for Avant power sequencing

--- Added 125 MHz Oscillator connected to BANK 6

--- Swapped FMC2_LA16_P/N on BANK 7

--- Swapped FMC2_HB05_P/N on BANK 8

--- Change to Switch (SW7) to control CFGMODE on BANK 2

--- Added VFMx_ADJ option to power FMC BANKs

Revision D

--- VCC_1V80 global power net is fixed on Platform Manager circuit & Regulator U36

--- Change R565 value to delay power down sequence

--- Add jumper option to disable JTAG for Platform Manager 2

--- Replaced FB15 & FB17 with 0 Ohm Resistors

--- Added J81, GND Pin

--- Added various Test Points

--- Added R588 & R589 (NPs) for U43 EN control



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Title		
Revision History		
Size	Project	Schematic Rev
B	Avant-AT-E Evaluation Board (LAV-E70-EVN)	1.0
Date:	Tuesday, January 30, 2024	Board Rev
		D
		Sheet 21 of 21