Lattice Radiant 2022.1.1 Software Release Notes

Welcome to Lattice Radiant® software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs).

What's New in Radiant 2022.1.1 Software

- **Device Support:**
  - CertusPro™-NX (LFCPNX)
    - 50K (-7/-8/-9) 1.00V (COM/IND) – ASG256
    - 50K (-7/-8/-9) 1.00V (COM/IND) – BBG484
    - 50K (-7/-8/-9) 1.00V (COM/IND) – BFG484
    - 50K (-7/-8/-9) 1.00V (COM/IND) – CBG256

- **Tool and Other Enhancements:**

  - **Power Calculator** – The Power Calculator for CertusPro-NX (LFCPNX) has been updated to reflect a roughly 10% improvement (lower power consumption) for designs using PCIe over previous versions due to improved silicon correlation data.

  - **Reveal Logic Controller/Analyzer** – The Reveal User Status and User Control Register features have been updated to expand the values of the control and status signals to 32-address locations with a maximum data-width of 8 bits.

  - **Simulation Library** – The Simulation Library has been updated to include compilation of PMI and source libraries.

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Radiant software, it may be necessary to re-create some IP, per the procedures described in the following table.

These procedures adapt the project for the changes in Radiant software.

Versions	IP			IP Regeneration Procedures
	Avant-E (LAV-AT-E)	**CrossLink-NX (LIFCL), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP), MachXO5-NX (LFMXO5)**	**iCE40UP**	
2022.1.1	DDRPHY (DDR PHY Interface Module)	ADC_Sequencer (Analog to Digital Converter with Sequencer)	N/A	These IP used in designs created in Radiant 2022.1 or earlier must be re-generated in Radiant 2022.1.1.
	PLL (Phase Locked Loop)	OSC (Oscillator)		
	ROM (Read-Only Memory)	ROM (Read-Only Memory)		
	FIFO	FIFO		
	FIFO_DC (Dual Clock FIFO)	FIFO_DC (Dual Clock FIFO)		
2022.1	N/A	ADC_Sequencer (Analog to Digital Converter with Sequencer)	N/A	These IP used in designs created in Radiant 3.2.1 or earlier must be re-generated in Radiant 2022.1.
		ADC (Analog to Digital Converter)		
		DDR_Generic (DDR Generic Interfaces)		
		DDR_MEM (DDR Memory Interfaces)		
		FIFO		
		FIFO_DC (Dual Clock FIFO)		
		GDDR7:1 (LVDS Interface)		
		Large_RAM_SP (Single Port Large RAM)		
		Large_ROM (Read-only Large Memory)		
		LPDDR4_MEM (LPDDR4 Memory Interface)		
		MIPI_DPHY (MIPI D-PHY Interface)		
		MPCS (Multi-Protocol PCS)		
		OSC (Oscillator)		
		PLL (Phase Locked Loop)		
3.2.1	N/A	MPCS (Multi-Protocol PCS)	N/A	These IP used in designs created in Radiant 3.2 or earlier must be re-generated in Radiant 3.2.1.
3.2	N/A	ADC_Sequencer (Analog to Digital Converter with Sequencer)	N/A	These IP used in designs created in Radiant 3.1.1 or earlier must be re-generated in Radiant 3.2.
		MPCS (Multi-Protocol PCS)		
		FIFO		
		FIFO_DC (Dual Clock FIFO)		
		RAM_DP (Dual Port RAM)		
3.1.1	N/A	PLL (Phase Locked Loop)	N/A	These IP used in designs created in Radiant 3.1 or earlier must be re-generated in Radiant 3.1.1.
		ADC (Analog to Digital Converter)		
		ROM (Read-only Memory)		
		MPCS (Multi-Protocol PCS)		
		DDR_Generic (DDR Generic Interfaces)		
		GDDR7:1 (LVDS Interface)		
		DDR_MEM (DDR Memory Interfaces)		

Versions	IP			IP Regeneration Procedures
	Avant-E (LAV-AT-E)	**CrossLink-NX (LIFCL), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP), MachXO5-NX (LFMXO5)**	**iCE40UP**	
		LPDDR4_MEM (LPDDR4 Memory Interface)		
		MIPI_DPHY (MIPI D-PHY Interface)		
		ADC_Sequencer (Analog to Digital Converter with Sequencer)		
3.1	N/A	PLL (Phase Locked Loop)	N/A	These IP used in designs created in Radiant 3.0 or earlier must be re-generated in Radiant 3.1.
		DDR_Generic (DDR Generic Interfaces)		
		GDDR7:1 (LVDS Interface)		
		DDR_MEM (DDR Memory Interfaces)		
		LPDDR4_MEM (LPDDR4 Memory Interface)		
		MIPI_DPHY (MIPI D-PHY Interface)		
		ADC_Sequencer (Analog to Digital Converter)		
		Large_RAM_DP (Dual Port Large RAM)		
		Large_RAM_DP_True (True Dual Port Large RAM)		
		Large_RAM_SP (Single Port Large RAM)		
		Large_ROM (Read-only Large Memory)		
		FIFO_DC (Dual Clock FIFO)		
		Complex Mult		
		MPCS (Multi-Protocol PCS)		
3.0	N/A	PLL (Phase Locked Loop)	N/A	These IP used in designs created in Radiant 2.2.1 or earlier must be re-generated in Radiant 3.0.
		DDR_Generic (DDR Generic Interfaces)		
		GDDR7:1 (LVDS Interface)		
		DDR_MEM (DDR Memory Interfaces)		
		MIPI_DPHY (MIPI D-PHY Interface)		
		LFSR (Linear Feedback Shift Register)		
		ADC_Sequencer (Analog to Digital Converter)		
		RAM_DP_True (True Dual Port RAM)		
		RAM_DQ (Single Port RAM)		
		ROM (Read-only Memory)		
		FIFO		
		FIFO_DC		
		Shift Register		
		Sine-Cosine Table		
		Convert		
2.2.1	N/A	PLL (Phase Locked Loop)	N/A	These IP used in designs created in Radiant 2.2 or earlier must be
		DDR_Generic (DDR Generic Interfaces)		
		GDDR7:1 (LVDS Interface)		

Versions	IP			IP Regeneration Procedures
	Avant-E (LAV-AT-E)	**CrossLink-NX (LIFCL), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP), MachXO5-NX (LFMXO5)**	**iCE40UP**	
		DDR_MEM (DDR Memory Interfaces)		re-generated in Radiant 2.2.1.
		MIPI_DPHY (MIPI D-PHY Interface)		
		LFSR (Linear Feedback Shift Register)		
		ADC_Sequencer (Analog to Digital Converter)		
		RAM_DP (Pseudo Dual Port RAM)		
2.2	N/A	PLL (Phase Locked Loop)	PLL (Phase Locked Loop)	These IP used in designs created in Radiant 2.1 or earlier must be re-generated in Radiant 2.2.
		DDR_Generic (DDR Generic Interfaces)		
		GDDR7:1 (7:1 LVDS Interface)		
		SDR (Single Data Rate)		
		DDR_MEM (DDR Memory Interfaces)		
		ADC (Analog to Digital Converter)		
		SEDC (Soft Error Detection/Correction)		
		Sin_Cos_Table (Sine Cosine Table)		
		OSC (Oscillator)		
		RAM_DQ (Single Port RAM)		
		RAM_DP_True (True Dual Port RAM)		
		FIFO		
		FIFO_DC (FIFO Dual Clock)		
2.1	N/A	PLL (Phase Locked Loop)	N/A	These IP used in designs created in Radiant 1.0, 2.0, or 2.0 SP1 or earlier must be re-generated in Radiant 2.1.
		GDDR7:1 (7:1 LVDS Interface)		
		DDR_MEM (DDR Memory Interfaces)		
		DDR_Generic (DDR Generic Interfaces)		
		MIPI_DPHY (MIPI Interface)		
		ADC (Analog to Digital Converter)		
		SEDC (Soft Error Detection/Correction)		
		OSC (Oscillator)		

The following server IP are not compatible with Radiant 3.0 onwards. Use the latest versions of the IP available on the IP server:

- I2C Master version 1.0.3
- UART 16550 version 1.0.4
- DDR3 SDRAM Controller version 1.1.1
- DDR3 SDRAM Controller version 1.2.1
- LPDDR2 SDRAM Controller Lite version 1.1.1
- LPDDR2 SDRAM Controller Lite version 1.2.1

Supported Devices

Lattice Radiant software can be used with either a free license or a subscription license. The two licenses provide access to different device families.

Device Family	Free License	Subscription License
iCE40 UltraPlus (iCE40UP)	◄	
Lattice Avant (LAV-AT-E) **Note**: A subscription license is required to access full bitstream for the LAV-AT-E device.		◄
CertusPro™-NX (LFCPNX)	Evaluation Mode	◄
Certus™-NX (LFD2NX)	◄	
MachXO5™-NX (LFMXO5)	Evaluation Mode	◄
CrossLink-NX (LIFCL)	◄	
Certus™-NX-RT (UT24C)		RT Subscription
CertusPro™-NX-RT (UT24CP)		RT Subscription

Support for Third-Party Synthesis and Simulator Tools

The Synopsys Synplify Pro® for Lattice synthesis tool and the Siemens ModelSim® Lattice Edition simulator tools are included in the Radiant software.

- **Synopsys Synplify Pro FPGA synthesis software version S-2021.09LR-SP2**
  - Release Notes for Synplify Pro are located in ..\<*install_directory*>\radiant\2022.1\synpbase\doc\. The file name is release_notes.pdf.
  - A full set of documents for Synplify Pro are also located in ..\<*install_directory*>\radiant\2022.1\synpbase\doc\.
- **Siemens ModelSim Lattice Edition 2021.4 revision 2021.10**

- Release Notes for ModelSim Lattice Edition are located in ..\<*install_directory*>\radiant\2022.1\modeltech\. The file names are RELEASE_NOTES.html or RELEASE_NOTES.txt.
- A full set of documents for ModelSim Lattice Edition are located in ..\<*install_directory*>\radiant\2022.1\modeltech\doc\.

- **Siemens Questa® 2020.4, Cadence Xcelium® 20.09-s012, Synopsys VCS® S-2021.09-SP2**

  Note: Cadence Xcelium and Synopsys VCS do not support Lattice Avant (LAV-AT-E).

Help Resources

- Online Help updated with CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP), and Lattice Avant (LAV-AT-E) content.
- To view the Online Help, start the Lattice Radiant software and select the  "Getting Started" icon under Information Center.

System Requirements

The following shows the basic system requirements for Radiant software:

- Intel Pentium or Pentium-compatible PC
- OS Support:

64-bit OS	Radiant	Synplify Pro	ModelSim
Windows 10	✓	✓	✓
Windows 11	✓	✓*	✓*
Red Hat Enterprise Linux 7.7	✓	✓	✓
Red Hat Enterprise Linux 8.4	✓	✓	✓
Ubuntu version 18.04 LTS	✓	✓*	✓*
Ubuntu version 20.04 LTS	✓	✓*	✓*
CentOS 7.7	✓	✓	✓*
CentOS 8.4	✓	✓	✓*

***Note**: The third-party tools have been tested by Lattice on the listed platforms, but the vendors do not officially support them.

- Approximately 50 GB free disk space
- Computer Memory Requirement:
  - Nexus – 16 GB
  - LAV-AT-E – 32 GB Recommended for running a single project. If running multiple projects, the memory requirement will be higher.
- 1024 X 768 graphics display
- Network adapter for license and network connectivity
- A Web browser with JavaScript capability
- Acrobat Reader

Issues Fixed

The following known issues are fixed in this release. Their workarounds are no longer needed.

Forward Referencing Synthesis with Synplify Pro errors out with Reveal Inserter.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-15796

Fixed in Radiant 2022.1.1

The create_clock constraint in *.fdc is ignored in post-synthesis.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-15807

Fixed in Radiant 2022.1.1

Data mismatch in PCS channel 3 when using MCPS IP operating in PCIe mode.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-15486

Fixed in Radiant 2022.1.1

Unable to update the PMI_ROM content using ECO editor.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-16230

Fixed in Radiant 2022.1.1

PAR timing report shows setup errors in the Overall Summary Section but no negative slacks in Endpoint Slacks Section and Detailed Report.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-16046

Fixed in Radiant 2022.1.1

In SGMII soft IP post-PAR netlist simulation, IMONDELAY is always in reset.

Devices affected: Lattice Avant (LAV-AT-E)

Bug number: DNG-15721

Fixed in Radiant 2022.1.1

Synplify Pro High Reliability settings cause FIFO RTL to generate an error.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-14469

Fixed in Radiant 2022.1.1

Large number of clocks in LAV-AT-E are not recognized in Netlist Analyzer with Synplify Pro synthesis.

Devices affected: Lattice Avant (LAV-AT-E)

Bug number: DNG-15027

Fixed in Radiant 2022.1.1

Netlist Analyzer does not show complete path for Avant PLL clock/data delay path using Synplify Pro.

Devices affected: Lattice Avant (LAV-AT-E)

Bug number: DNG-15513

Fixed in Radiant 2022.1

The LFCPNX-100-CBG256 and LFCPNX-100-BFG484 IBIS Package files are missing in the installation folder.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-15455

Fixed in Radiant 2022.1

PCLKDIV primitive cannot be configured automatically in DCS mode.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-15521

Fixed in Radiant 2022.1

The power calculator 'calculation' mode currently underestimates the actual core power by about 1/2.

Devices affected: Lattice Avant (LAV-AT-E)

Bug number: DNG-15498

Fixed in Radiant 2022.1

Radiant Power Calculator TCL command for setting clock frequency based on timing (twr) is not working

Devices affected: LFCPNX

Bug number: DNG-14718

Fixed in Radiant 2022.1

ECO does not show memory instance attribute with SP16K instance.

Devices affected: Lattice Avant (LAV-AT-E)

Bug number: DNG-15329

Fixed in Radiant 2022.1

ECO Editor shows the wrong property value [WIDTH, DEPTH] of “ECO_MEM_SIZE” when Synplify Pro is used.

Devices affected: Lattice Avant (LAV-AT-E)

Bug number: DNG-15129

Fixed in Radiant 2022.1

The RTL simulation flow may fail for Reveal Controller simulation model.

Devices affected: All devices

Bug number: DNG-14964

Fixed in Radiant 2022.1

Synplify Pro synthesis fails in a mixed language design with VHDL top module when reveal is inserted in the design.

Devices affected: All devices

Bug number: DNG-15055

Fixed in Radiant 2022.1

When using Synplify Pro OEM tool, set_multicycle_path with the -hold options defined in the pre-synthesis constraint file may not be forward annotated to Post-Synthesis Timing, MAP, and PAR.

Devices affected: All devices

Bug number: DNG-13681

Fixed in Radiant 2022.1

In certain cases, the Synplify-Pro OEM synthesis tool will error out when reveal is inserted with error message reporting, @E: FO139 "The instance needs internal tristate. Can't be mapped."

Devices affected: All except iCE40UP

Bug number: DNG-13017

Fixed in Radiant 2022.1

In Timing Analyzer, the setup path for set_max_delay displays incorrect endpoints.

Devices affected: All devices

Bug number: DNG-14997

Fixed in Radiant 2022.1

MPCS module IP GUI does not allow to modify the Ref Clock Frequency

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-14480

Fixed in Radiant 2022.1

Inconsistent display of slack and fmax numbers in timing report when MPCS is used.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-14470

Fixed in Radiant 2022.1

EBR out reg's edge is incorrectly interpreted leading to timing violation when set_multicycle_path constraint is used.

Devices affected: All devices

Bug number: DNG-14252

Fixed in Radiant 2022.1

When the set_max_skew constraint is added pre-synthesis to a .sdc file and the Synplify Pro tool is used, Synplify Pro may error out with the message: invalid command name "set_max_skew."

Devices affected: All devices

Bug number: DNG-14769

Fixed in Radiant 2022.1

When set_max_delay constraint with a -datapath_only option is used, Radiant timer incorrectly calculates setup/hold times.

Devices affected: All except iCE40UP

Bug number: DNG-13551, DNG-13555

Fixed in Radiant 2022.1

In Place & Route Reports, the Performance Hardware Data Status displays incorrect version number.

Devices affected: All devices

Bug number: DNG-14928

Fixed in Radiant 2022.1

The "Performance Hardware Data Status" of CertusPro-NX automotive device is “Final.”

Devices affected: CertusPro-NX Auto Device (LFCPNX)

Bug number: DNG-13898

Fixed in Radiant 2022.1

Reveal Controller's Virtual Switch and LEDs are not working properly in JTAG-Chain.

Devices affected: All devices

Bug number: DNG-15124

Fixed in Radiant 2022.1

The Reveal User Status Register feature cannot read out the right value.

Devices affected: All devices

Bug number: DNG-14918

Fixed in Radiant 2022.1

LSE flow fails for MDDR, MIPI, ADC cases.

Devices affected: MachXO5-NX (LFMXO5)

Bug number: DNG-14886

Fixed in Radiant 2022.1

LSE may issue an error: ".. entity 'xxx' is not compiled yet. VHDL-1059 and abort" when the following conditions are met:

1. Verilog module and VHDL entity have the same name.

2. VHDL "entity" and its "architecture" are split into two files.

3. When the "entity" is entered below the "architecture" file in the Radiant Project File list.

Devices affected: All devices

Bug number: DNG-13231

Fixed in Radiant 2022.1

Known Issues for Radiant 2022.1.1

The following are known issues for the Radiant Software 2022.1.1.

Synplify Pro Lattice OEM (*.srr and *.srf files) may incorrectly report the number of LRAMs for the target device.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CertusPro-NX (LFCPNX-50)

Bug number: DNG-16362

Synplify Pro Lattice OEM may take large amounts of Memory for designs involving large shift register chains.

Workaround: Run affected designs on machines with enough available memory.

Devices affected: Lattice Avant (LAV-AT-E)

Bug number: DNG-15024

When simulating Cordic IP using ModelSim, you may encounter an RTL compilation error.

Workaround: In OEM ModelSim, use the "vsim -voptargs=+acc -L work -L pmi_work -L ovi_lifcl tb_top -suppress 8607" command to finish the compilation.

Devices affected: Lattice Avant (LAV-AT-E)

Bug number: DNG-14888

Reveal Power-on Reset (POR) Debug function does not work when using LSE.

Workaround: Use Synplify Pro.

Devices affected: All except iCE40UP

Bug number: DNG-12861, DNG-13901

Reveal Controller will overwrite the registers of the Hard IP.

If LMMI bus IP is used as part of your design for dynamic update and it's connected to a specific instance of hard-IP, then it is recommended to not use the Reveal Controller for that hard IP because the user design controlling the hard IP will be overwritten by Reveal Controller Logic.

Hard IPs: DPHY, I2CFIFO, PLL, PCS, PCIELL, SGMIICDR

Devices affected: All except iCE40UP

Bug number: DNG-12253

When Reveal Controller is used for updating the PCS register (reg80) through the controller, it will cause the PCS Register value to be stuck at a value during successive writes.

Workaround: Re-download the bitstream.

Devices affected: CertusPro-NX (LFCPNX), CertusPro-NX-RT (UT24CP)

Bug number: DNG-12235, DNG-13920

The CSI-2/DSI D-PHY Transmitter and Receiver Soft IP simulations fail when using Synopsys VCS as simulation tool.

Workaround: Use Modelsim or QuestaSim simulation tools.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-13225

When simulating Generic DDR, there may be a mismatch in the RTL and post-route simulation. Silicon is not affected.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: All except iCE40UP

Bug number: DNG-9639

MAP incorrectly reports number of DPHY and PCIE/ADC resources for CrossLink-NX (LIFCL) QFN72 package.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-8297