# DDR Memory Controller IP Core

IP Version: v2.9.0

# User Guide

FPGA-IPUG-02208-2.1

September 2026

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# Abbreviations in This Document

A list of abbreviations used in this document.

| Abbreviations | Definition |
|---|---|
| APB | Advanced Peripheral Bus |
| AXI4 | Advanced eXtensible Interface 4 |
| BL | Burst Length |
| CA | Command and Address |
| CS | Chip Select |
| CBT | Command Bus Training |
| DBI | Data Bus Inversion |
| DDR | Double Data Rate |
| DDRPHY | Double Data Rate Physical Layer |
| DM | Data Mask |
| DQ | Data |
| DQS | Data Strobe |
| ECC | Error Correction Code |
| ECLK | Edge Clock |
| FPGA | Field Programmable Gate Array |
| JEDEC | Joint Electron Device Engineering Council |
| LPDDR | Low Power Double Data Rate |
| LVSTL | Low Voltage Swing Terminated Logic |
| MC | Memory Controller |
| MCE | Memory Controller Engine |
| MR | Mode Register |
| MRS | Mode Register Set |
| ODT | On-Die Termination |
| PRBS | Pseudorandom Binary Sequence |
| PVT | Process, Voltage, and Temperature |
| RISC-V | Reduced Instruction Set Computer – Five |
| RTL | Register Transfer Level |
| SCLK | System Clock |
| SDRAM | Synchronous Dynamic Random Access Memory |
| TCL | Tool Command Language |
| VREF | Voltage Reference |

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# 1. Introduction

The Lattice Semiconductor DDR Memory Controller IP provides a turnkey solution consisting of a controller, DDRPHY, and associated clocking and training logic to interface with DDR4 and LPDDR4 SDRAM. The IP core is implemented in SystemVerilog HDL using the Lattice Radiant™ software integrated with Synopsys® Synplify Pro® synthesis tool. The Memory Controller manages interfacing with external DDR4 and LPDDR4 memory for user applications.

## 1.1. Overview of the IP

The DDR Memory Controller IP is designed for small-footprint, low-power applications and enables high-bandwidth external memory access for edge AI, vision buffering, industrial control, embedded computing, and networking workloads.

## 1.2. Quick Facts

Table 1.1 summarizes the DDR Memory Controller IP.

**Table 1.1. Quick Facts**

| | | |
|---|---|---|
| **IP Requirements** | Supported Devices | Lattice Avant™, Certus™-N2 |
| | IP Changes[1] | For a list of changes to the IP, refer to the DDR Memory Controller IP Release Notes (FPGA-RN-02033) |
| **Resource Utilization** | Supported User Interfaces | AXI4 for data access<br>APB for configuration access |
| | Resources | Refer to Table A.1 and Table A.2 |
| **Design Tool Support** | Lattice Implementation[2] | IP core v2.9.0 – Lattice Radiant software 2026.1<br>Refer to the Lattice Radiant Software User Guide for details. |
| | Synthesis | Synopsys Synplify Pro for Lattice |
| | Simulation | Questasim |
| **Driver Support** | API Reference | Refer to the DDR Memory Controller Driver (FPGA-TN-02379) |

**Notes:**

1. In some instances, the IP may be updated without changes to the user guide. This user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.
2. Lattice Implementation indicates the software version release coinciding with the current IP version. Check the software for IP version compatibility with earlier or later software versions.

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## 1.3. IP Support Summary

**Table 1.2. LPDDR4 and DDR4 Memory Controller IP Support Readiness**

| Device Family | IP | Rank | DDR Width | Data Rate (Mbps) [1] | Timing Model |
|---|---|---|---|---|---|
| Avant | LPDDR4 | Single | x16 | 700 to 1,600 | Preliminary |
| | | | x32 | 700 to 1,600 | |
| | | | x64 | 700 to 1,600 | |
| | | Single | x16 | 1,866 to 2,400 | |
| | | | x32 | 1,866 to 2,400 | |
| | | | x64 | 1,866 to 2,400 | |
| | | Dual | x16 | 700 to 2,400 | |
| | | | x32 | 700 to 2,400 | |
| | | | x64 | 700 to 2,400 | |
| | DDR4 | Single | x16 | 1,333 to 2,400 | |
| | | | x32 | 1,333 to 2,400 | |
| | | | x64 | 1,333 to 2,400 | |
| | | Dual | x16 | 1,333 to 2,400 | |
| | | | x32 | 1,333 to 2,400 | |
| | | | x64 | 1,333 to 2,400 | |
| Certus-N2 | LPDDR4 | Single | x16 | 700 to 2,400 | Preliminary |
| | | | x32 | 700 to 2,400 | |
| | | Dual | x16 | 700 to 2,400 | |
| | | | x32 | 700 to 2,400 | |
| | DDR4 | Single | x16 | 1,333 to 2,400 | |
| | | | x32 | 1,333 to 2,400 | |
| | | Dual | x16 | 1,333 to 2,400 | |
| | | | x32 | 1,333 to 2,400 | |

**Notes:**

1. For the following Lattice Avant devices, the maximum data rate is limited to 1,600 Mbps for DDR Width x16 and x32, and no support for DDR Width x64.
   LAV-AT-E30B
   LAV-AT-E30ES
   LAV-AT-E70B
   LAV-AT-E70ES1
   LAV-AT-G70ES
   LAV-AT-X70ES

The example design for the DDR Memory Controller IP core supports both simulation and deployment to development boards. For instructions on running the example design in hardware or simulation, refer to the Designing and Simulating the IP section.

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## 1.4. Features

The DDR Memory Controller IP supports the following key features for DDR4 and LPDDR4 SDRAM.

### 1.4.1. DDR4

The Memory Controller supports the following key features when configured in DDR4 mode:

- DDR4 SDRAM protocol, compliant to DDR4 JEDEC Standard
- DDR4 SDRAM speeds of:
  - 666 MHz (1,333 Mbps)
  - 800 MHz (1,600 Mbps)
  - 933 MHz (1,866 Mbps)
  - 1,066 MHz (2,133 Mbps)
  - 1,200 MHz (2,400 Mbps)
- DDR4-Specific Memory Controller features
- Component support for interface data widths of x16, x32, x64, and x72
- Up to 16 Gb density support
- x8 and x16 DDR4 device support (8:1 DQ:DQS ratio)
- Fixed burst length of BL8
- 8:1 gearing mode (DDR4:FPGA logic interface clock ratio)
- Dual-rank support (requires dual rank DRAM chip)
- Configurable CAS latencies for Reads and Writes based on target interface speed
- Configurable Address widths to support various memory densities
- Side-band ECC support for single rank, up to 1,600 Mbps, x8 DDR4 device
- Supports component (DRAM soldered on the board) and UDIMM.
- AXI4 data interface support:
  - INCR read/write operations
  - Unaligned transfer using byte strobes
  - Narrow transfers

AXI widths of 32, 64, 128, 256, and 512

  - Aligned addressing to AxSIZE only
- APB configuration interface support:
  - Automatic DDR4 SDRAM initialization
  - Dynamic valid window optimization for Read/Write paths
  - DQ-DQS skew optimization for Write training
- Periodic training support feature:
  - ZQ calibration
- Polling and Out-of-band interrupt support for training error

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**Table 1.3. DDR4 Features Overview**

| Key Features | DDR4 Support Details[1] |
|---|---|
| Device Format | Component, UDIMM |
| Data Widths | x16, x32, x64, x72[2] |
| Data User Interface | AXI4 |
| Configuration Interface | APB |
| Maximum Data Rate | Refer to Table 1.5 |
| **HW Managed Periodic Events** | |
| Refresh | All bank auto refresh |
| ZQ Calibration | Yes |
| Low Power Features | Not yet supported |
| **Other Features** | |
| Error Correction Code (ECC) | Yes[3] |
| Dual rank | Yes |
| Data Bus Inversion (DBI) | No |
| On-Die Termination (ODT) | Yes for DQ, No for CA |
| Bit Swizzle | Not yet supported |
| **Training** | |
| Initialization | Yes |
| CS Training | Not yet supported |
| Write Leveling | Yes |
| Read Training | Yes |
| Write Training | Yes |
| VREF Training | Not yet supported |
| Self-Calibrating Logic | Yes |
| Bit-Level Trim Sweep | Not yet supported |
| 2-D Vref Training | Not yet supported |

**Notes:**

1. *Yes* implies that a configurable option exists to enable or disable the feature. *No* implies that the feature is currently not supported and will not be supported in the future.
2. The x72 data width is supported only when ECC is enabled. It consists of 64 data bits and 8 ECC bits.
3. Supports single-rank configuration, up to 1,600 Mbps data rate, with x8 DDR4 devices.

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### 1.4.2. LPDDR4

The Memory Controller supports the following key features when configured in LPDDR4 mode:

- LPDDR4 SDRAM protocol, compliant to LPDDR4 JEDEC Standard
- LPDDR4 SDRAM speeds of:
  - 350 MHz (700 Mbps)
  - 400 MHz (800 Mbps)
  - 533 MHz (1,066 Mbps)
  - 666 MHz (1,333 Mbps)
  - 800 MHz (1,600 Mbps)
  - 933 MHz (1,866 Mbps)
  - 1,066 MHz (2,133 Mbps)
  - 1,200 MHz (2,400 Mbps)
- LPDDR4-Specific Memory Controller features
- Component support for interface data widths of x16, x32, and x64
- Up to 16 Gb density support per channel
- x16 LPDDR4 device support (8:1 DQ:DQS ratio)
- Burst length of BL16 and BL32, including On-The-Fly (OTF)
- 8:1 gearing mode (LPDDR4:FPGA logic interface clock ratio)
- Dual-rank support (requires dual rank DRAM chip)
- Read DBI support only
- Configurable CAS latencies for Reads and Writes based on target interface speed
- Configurable Address widths to support various memory densities
- AXI4 data interface support:
  - INCR read/write operations
  - Unaligned transfer using byte strobes
  - Narrow transfers

AXI widths of 32, 64, 128, 256, and 512

  - Aligned addressing to AxSIZE only
- APB configuration interface support:
  - Automatic LPDDR4 SDRAM initialization
  - Dynamic valid window optimization for Read/Write paths
  - DQ-DQS skew optimization for Write training
- Periodic training support feature:
  - Temperature tracking
  - Adaptive/Derate refresh rate for extended temperature support
  - ZQ calibration (ZQCAL START and LATCH only)
- Automatic detection of idle triggering Self-Refresh with Power-down entry
- Polling and Out-of-band interrupt support for training error and extended temperature support
- Bit Swizzle (DQ bit swizzle within the DQS group)

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**Table 1.4. LPDDR4 Features Overview**

| Key Features | LPDDR4 Support Details[1] |
|---|---|
| Device Format | Component |
| Data Widths | x16, x32, x64 |
| Data User Interface | AXI4 |
| Configuration Interface | APB |
| Maximum Data Rate | Refer to Table 1.5 |
| **HW Managed Periodic Events** | |
| Refresh | All bank auto refresh |
| ZQ Calibration | *Yes* for ZQ start and latch; *No* for ZQ reset |
| Low Power Features | Self-refresh with power-down |
| **Other Features** | |
| Error Correction Code (ECC) | Not yet supported |
| Dual rank | Yes |
| Data Bus Inversion (DBI) | Yes for reads, No for writes |
| Temperature Tracking | Yes |
| Refresh Adaptation (derate) to Temperature Variation | Yes |
| On-Die Termination (ODT) | Yes for DQ and CA |
| Bit Swizzle | *Yes* for DQ; *Not supported* for CA and DQS Group |
| **Training** | |
| Initialization | Yes |
| Command Training | Yes |
| Write Leveling | Yes |
| Read Training | Yes |
| Write Training | Yes |
| Automatic VREF Training | Yes |
| Self-Calibrating Logic | Yes |
| Bit-Level Trim Sweep | Yes |
| 2-D Vref Training | Yes |

**Note:**

1. *Yes* implies that a configurable option exists to enable or disable the feature. *No* implies that the feature is currently not supported and will not be supported in the future.

## 1.5. Licensing and Ordering Information

The DDR Memory Controller IP is available with the Lattice Radiant software subscription. To purchase the Lattice Radiant subscription license, contact Lattice Sales or go to the Lattice Online Store.

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## 1.6. Minimum Device Requirements

The DDR Memory Controller IP supports the following devices. Table 1.5 summarizes the minimum device requirements for the Memory Controller IP core.

**Table 1.5. Minimum Device Requirements**

| Device/Mode | DDR Data Width | DDR Ranks | Speed Grade | Max Supported Interface Speed |
|---|---|---|---|---|
| **DDR4** | | | | |
| Avant-E/G/X | x16, x32, x64, x72[1] | 1, 2 | 3 | 2,400 Mbps |
| | | | 2 | 2,133 Mbps |
| | | 1 | 1 | 1,866 Mbps |
| Certus-N2 | x16, x32 | 1, 2 | 3 | 2,400 Mbps |
| | | | 2 | 2,133 Mbps |
| | | 1 | 1 | 1,866 Mbps |
| **LPDDR4** | | | | |
| Avant-E/G/X | x16, x32, x64 | 1, 2 | 3 | 2,400 Mbps |
| | | | 2 | 2,133 Mbps |
| | | 1 | 1 | 1,866 Mbps |
| Certus-N2 | x16, x32 | 1, 2 | 3 | 2,400 Mbps |
| | | | 2 | 2,133 Mbps |
| | | 1 | 1 | 1,866 Mbps |

**Note:**

1. Supports single-rank configuration at 1,600 Mbps, using x8 DDR4 devices, with x72 interface when ECC is supported.

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# 2. Functional Description

This section describes the DDR Memory Controller IP architecture and behavior, including clock and reset handling, available user data and configuration interfaces, the calibration sequence, and operation descriptions.

## 2.1. IP Architecture

The DDR Memory Controller IP includes three main blocks: the Memory Controller, DDRPHY, and Training Engine. The following figure shows the memory controller submodules and their connectivity.

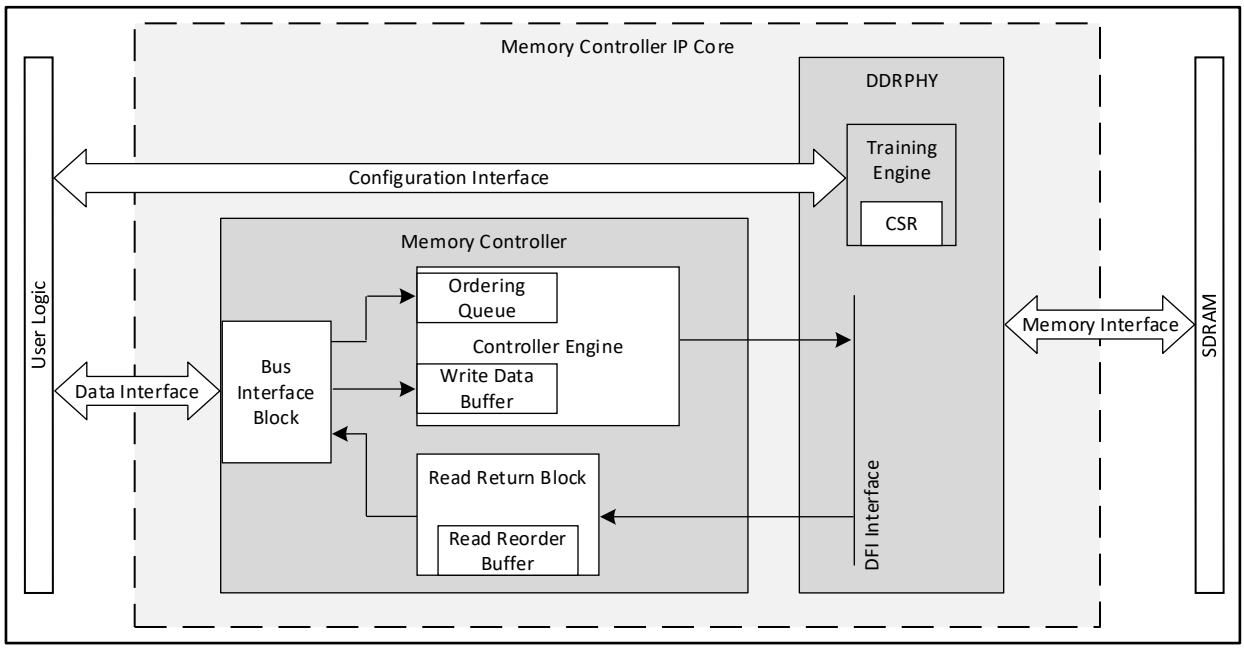



**Figure 2.1. Memory Controller IP Core Functional Diagram**

The data interface allows you to initiate command/address/control and read/write operations to external DDR4/LPDDR4 SDRAM. The configuration interface provides access to the Training Engine and the Configuration Set Registers (CSRs), which configure the Memory Controller and perform the DDR4/LPDDR4 training sequences. The memory interface allows the selected Lattice FPGA to communicate with the external DDR4/LPDDR4 memory. For more information on the data and configuration interfaces, refer to the User Interfaces section of this user guide.

### 2.1.1. Memory Controller

The Memory Controller consists of the following submodules:

- Bus Interface Block
- Controller Engine
- Read Return Block

#### 2.1.1.1. Bus Interface Block

The Bus Interface Block accepts user-initiated operations on the selected data interface and translates them for processing within the Memory Controller. The data provided for the Controller Engine consists of:

- Address interface size: determined based on the selected SDRAM device density and DDR4/LPDDR4 data width
- Read and Write interface sizes: determined based on the selected DDR4/LPDDR4 data width

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#### 2.1.1.2. Controller Engine

The Controller Engine accepts the requests from the Bus Interface Block and translates the address to row, column, rank, and bank format. The ordering queue holds the address, command, and control information coming from the Bus Interface Block. It prioritizes executing commands targeting an already opened bank and maintains the correct order of execution when multiple requests target the same bank in DDR4/LPDDR4 SDRAM. The write data buffer buffers incoming data for write commands.

The Controller Engine supports outstanding writes and reads, which are write/read requests entered into a queue and arbitrated for processing. The following table describes the three types of requests and how they are processed.

**Table 2.1. MCE Request Handling**

| Request type | Prioritization and Definition | Comments |
|---|---|---|
| Read | Varies depending on selected data interface protocol. Refer to the AXI4 Data Interface section of this user guide for details. | The read request size is equal to the supported DDR4/LPDDR4 burst length. |
| Write | Write requests are defined as a write, where the entire data needs to be written for the supported DDR4/LPDDR4 burst length. | Example: For a 32-bit DDR4/LPDDR4 data bus width, with burst length 8 (BL8), a full write would be 8×4B = 32B. |
| Partial write | Partial write requests are defined as a write, where the entire data *is not* written. | Example: For a 32-bit DDR4/LPDDR4 data bus width, a partial write would be a write request that is less than 32B. This is equivalent to a masked write. |

All write requests may be processed out of order if data dependency is not present. For example, an incoming request tied to an already opened page in DDR4/LPDDR4 SDRAM can be prioritized if it is not dependent on the requests already in the queue. Read requests may also be processed out of order if a data dependency is not present, depending on the selected data interface protocol. Refer to the AXI4 Data Interface section of this user guide for information regarding outstanding write/read support.

The Controller Engine contains bank management logic to track all the open and closed pages within each bank, along with timers for each bank and rank. This allows issued memory commands to meet the operational sequence and timing requirements of the DDR4/LPDDR4 SDRAM. The last layer of logic within the Controller Engine handles handshaking between the PHY and external memory. The Controller Engine is also responsible for supporting periodic events compliant with the DDR4/LPDDR4 SDRAM requirements. For more information on supported periodic features, refer to the Operation Descriptions section of this user guide.

#### 2.1.1.3. Read Return Block

The Read Return Block is responsible for responding to the Controller Engine issued read requests. Execution of commands can be out of order, so the Read Return Block handles the reordering to ensure that the read data is sent to the Bus Interface in order. The Read Return Block also handles Data Bus Inversion (DBI), which is an I/O signaling technique that reduces power consumption and improves signal integrity.

### 2.1.2. DDRPHY Module

The DDRPHY Module implements the DFI 4.0 Specification (© Cadence Design Systems, Inc.). It instantiates the hardened DDRPHY Primitive and includes a dedicated PLL and quarter-rate clock generator. The DDRPHY Module implements 8:1 gearing and trains the DDR4/LPDDR4 interface. Figure 2.2 shows a high-level block diagram of the DDRPHY module.

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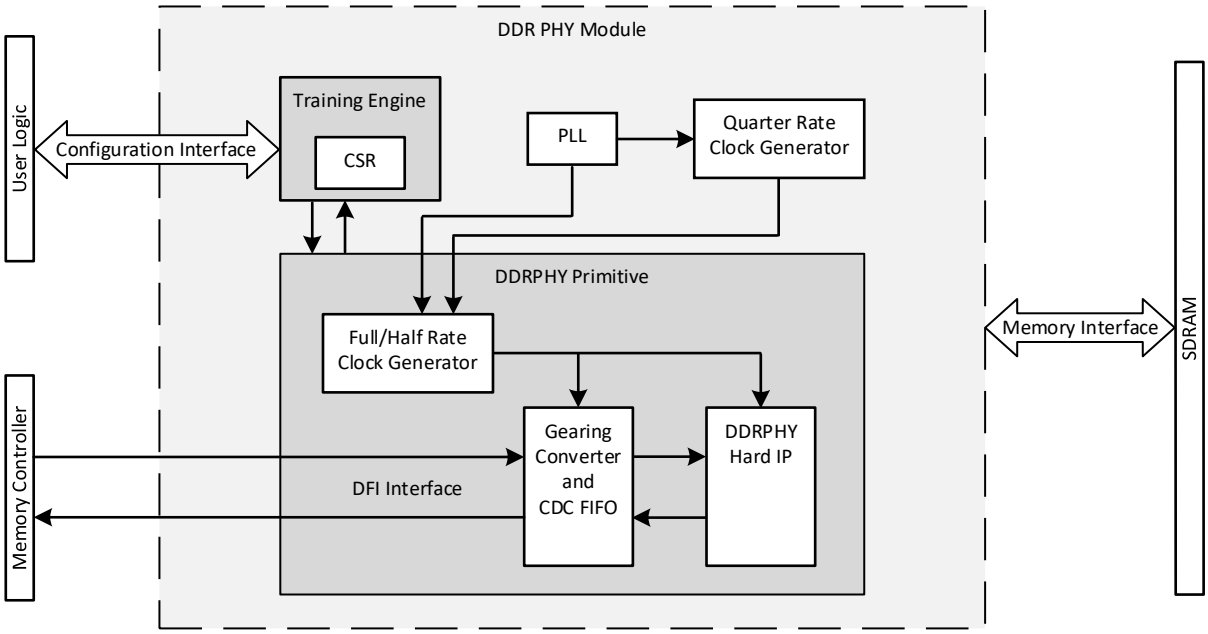



**Figure 2.2. DDR PHY**

#### 2.1.2.1. Hardened DDR PHY Primitive

The PHY uses hardened logic, called I/O modules or hardware primitives, to implement clock synchronization logic and the command/address and data input/output paths. The clock synchronization logic handles Clock Domain Crossing (CDC) between the Edge Clock (ECLK) and System Clock (SCLK). ECLK is an internal clock that clocks the DDR primitives, and SCLK clocks the Memory Controller IP core. Without proper synchronization, the bit order on individual elements might become desynchronized, causing the data bus to scramble.

The Memory Controller operates in 8:1 gearing mode, which means that ECLK operates at the same frequency as the DDR4/LPDDR4 interface and that SCLK operates at a quarter of the DDR4/LPDDR4 memory clock. In other words, for a 400 MHz DDR4/LPDDR4 interface, ECLK operates at 800 MHz and SCLK operates at 200 MHz. This clocking ratio and DDR transfer relationship mean the user data bus is eight times the width of the DDR4/LPDDR4 memory data bus. For example, a 32-bit DDR4/LPDDR4 memory interface requires a 256-bit write and read data bus on the DDR PHY (DFI) side, which is an interface protocol between the Memory Controller and PHY. For more information regarding the DDRPHY, hardware primitives, and clock synchronization logic, refer to the DDR Memory PHY Module User Guide (FPGA-IPUG-02195).

#### 2.1.2.2. Training Engine

The Training Engine initializes and trains the external DDR4/LPDDR4 memory. It provides a configuration interface from user logic to the Configuration Set Registers (CSR). You can issue commands to the Training Engine to perform reads and writes to these registers, allowing you to handle interrupts and obtain details during the memory training sequence. It consists of user-accessible registers, a RISC-V CPU subsystem, and a hardened PHY. For more information regarding the training engine, refer to the DDR Memory PHY Module User Guide (FPGA-IPUG-02195).

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## 2.2. Clocking and Reset

### 2.2.1. General Clocking and Reset

This section describes the required input clocks and resets for the Memory Controller IP, and the reset-assertion combinations to avoid AXI4 bus hang-up.

#### 2.2.1.1. Input Clocks

The Memory Controller IP requires three main input clocks.

1. **Differential reference clock (pll_refclk_i)** generates the clock for the controller core and DDR4/LPDDR4 interfaces. You can provide this clock from an external source through a dedicated FPGA routing path. For a list of valid reference clock frequencies, refer to the IP Parameter Description section. The input clock is then routed through a dedicated PLL within the Memory Controller IP to generate the Edge Clock (ECLK) and System Clock (SCLK). The ECLK signal is used internally by the IP core to clock the I/O modules, and SCLK is used to clock the IP core. Both these clocks scale directly with the DDR data rate.
2. **APB clock (pclk_i)** is used for the configuration interfaces within the controller and its training subsystem. This clock also drives the synchronization logic for SCLK and ECLK. For additional details regarding clock synchronization, refer to DDR Memory PHY Module User Guide (FPGA-IPUG-02195).
3. **AXI clock (aclk_i)** is used for the AXI bus interface. Refer to the AXI4 Data Interface section for information regarding clock selection for the AXI interface.

#### 2.2.1.2. Input Resets

The Memory Controller IP has four main input resets:

1. **Main controller reset (rst_n_i)**. When asserted, the Memory Controller, its training registers, and SDRAM are reset to their default values. The IP core internally synchronizes the reset de-assertion to its internal target clock.
2. **APB reset (preset_n_i)** is used to reset the APB interface and the training subsystem. (PHY training registers are preserved.) The IP core does not synchronize this reset de-assertion to pclk_i.
3. **AXI reset (areset_n_i)** is used to reset the AXI bus interface. The IP core internally synchronizes the reset de-assertion of this reset to its internal target clock.
4. **PLL reset (pll_rst_n_i)** is used to reset the internal PLL in the Memory Controller.

#### 2.2.1.3. Reset-Assertion Expectations (to Prevent Bus Hang-Up)

- When you assert rst_n_i the following conditions apply:
  - If rst_n_i is asserted when the AXI4 bus is not idle: areset_n_i is expected.
  - If rst_n_i is asserted during AXI4 Bus Idle: areset_n_i is not required.
- When you assert areset_n_i the following conditions apply:
  - If areset_n_i is asserted when the AXI4 bus is not idle:  rst_n_i is expected.
  - If areset_n_i is asserted during AXI4 Bus Idle: rst_n_i is not required.
- When you assert pll_rst_n_i the following conditions apply:
  - If pll_rst_n_i is asserted when the AXI4 bus is not idle: both rst_n_i and areset_n_i are expected.
  - If pll_rst_n_i is asserted during AXI4 Bus Idle: rst_n_i is expected.

Note: The AXI Bus state is idle meaning there are no outstanding transactions on the controller AXI interface:

- All read data is returned on the Read Data channel.
- All write completions have returned on Write response channel.
- There is no ongoing activity on the Write Address, Write Data, or Read Address channel.

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## 2.3. User Interfaces

This section describes the protocols used for the data and configuration interfaces of the Memory Controller.

### 2.3.1. AXI4 Data Interface

The data interface allows you to initiate read and write operations to external SDRAM. The AXI4 interface supports high-bandwidth, low-latency operation. The AXI4 interface is a multi-channel bus consisting of five independent channels: write address, read address, write data, read data, and write response channels (read response is sent along with the read data). The AXI4 interface operates off the aclk_i signal when the *Enable Local Bus Clock* attribute is checked. When the *Enable Local Bus Clock* attribute is checked, the Bus Interface Block implements clock domain crossing logic to transfer the request from AXI4 Clock (aclk_i) to the Memory Controller IP core System Clock (SCLK).

The areset_n_i signal resets the AXI4 interface, which is an asynchronous active-low reset; ensure that areset_n_i is synchronously de-asserted relative to aclk_i.

The Memory Controller IP supports the following AXI4 types of burst transfers:

- Burst Type (AxBURST):
  - INCR: incrementing burst that does not wrap at address boundaries
- Burst Size (AxSIZE):
  - [1, 2, 3, 4, 8, 16, 32, 64] Bytes
- Burst Length (AxLEN):
  - 1-64 beat burst: when IP parameter MAX_BURST_LEN = 64
  - 1-128 beat burst: when IP parameter MAX_BURST_LEN = 128
  - 1-256 beat burst: when IP parameter MAX_BURST_LEN = 256
- Burst Address (AxADDR):
  - Unaligned addressing is not supported so all transfers must be aligned to AxSIZE
  - Unaligned transfer is supported by using byte strobes
- For addresses not aligned to BUS_WIDTH × 16 / 8, the maximum allowable AxLEN is as defined below:
  - Burst Length Offset = (BUS_WIDTH × 16) / AXI_DATA_WIDTH

Maximum Allowable AxLEN = MAX_BURST_LEN – Burst Length Offset –1

- Example Use Case: Maximum Burst Length is 64, DDR Bus Width is 32 bits and AXI Data Width is 32 bits
  - Burst Length Offset: 32 × 16/32 = 16
  - Maximum Allowable AxLEN: 64 – 16 – 1 = 47
- Write Strobes (WSTRB):
  - Only the first and last beats of a burst can have incomplete byte strobes (WSTRB cannot go low in the middle of a burst)

The AXI4 protocol supports out-of-order transaction completion and supports multiple outstanding transactions per bus manager. As a result, when AXI4 is configured as the user data interface, the Memory Controller supports up to eight outstanding writes and eight outstanding reads, with both reads and writes having the same priority. For more information regarding the AXI4 protocol, refer to the AMBA AXI Protocol Specification.

**Table 2.2. Supported AXI4 Transactions**

| Transaction Type | AxBURST | AxLEN[7:0] | AxSIZE[2:0] 1 | Comment |
|---|---|---|---|---|
| Write | INCR | [0 – *MAX_BURST_LEN*-1] | [0, 1, 2, 3, 4, 5, 6] | [1-4,096] Byte write |
| Read | INCR | [0 – *MAX_BURST_LEN*-1] | [0, 1, 2, 3, 4, 5, 6] | [1-4,096] Byte read |

**Notes:**

1. For IP parameter AXI_DATA_WIDTH = 32, AxSIZE = [0, 1, 2] are supported.
   For IP parameter AXI_DATA_WIDTH = 64, AxSIZE = [0, 1, 2, 3] are supported.
   For IP parameter AXI_DATA_WIDTH = 128, AxSIZE = [0, 1, 2, 3, 4] are supported.
   For IP parameter AXI_DATA_WIDTH = 256, AxSIZE = [0, 1, 2, 3, 4, 5] are supported.
   For IP parameter AXI_DATA_WIDTH = 512, AxSIZE = [0, 1, 2, 3, 4, 5, 6] are supported.

Start AXI4 transactions only after the initialization and training is complete. Refer to Calibration section for more information.

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### 2.3.2. APB Configuration Interface

The configuration interface allows you to initialize and train the memory interface. The Memory Controller IP core uses the APB protocol for its configuration interface. The APB interface is a low-power protocol intended for accessing programmable control registers. It is not pipelined and operates synchronously with a single address bus and two data buses: write and read. For more information regarding the APB protocol, refer to the AMBA APB Protocol Specification.

The Memory Controller uses this protocol to initialize and train the interface between FPGA logic and SDRAM. The APB interface operates off the pclk_i signal and resets through the preset_n_i signal. Refer to the Clocking and Reset section of this user guide for more details.

The APB interface is unavailable when the *Enable APB interface* attribute is unchecked. For details on how to initialize and train SDRAM without the APB interface, refer to the Initialization and Training without APB Interface section of this user guide.

Start APB transactions only when the PLL is locked (pll_lock_o==1).

## 2.4. Calibration

To ensure proper device functionality, initialize and train the external SDRAM before the Memory Controller performs data accesses. Upon device power-up, the soft RISC-V CPU inside the Training Engine remains in reset. To start the initialization and training sequence of the SDRAM device, complete the following steps using the configuration interface:

- Ensure the DDRPHY Module PLL is in the lock state by polling the PHY Clock Register (PHY_CLOCK_REG) until the pll_lock signal is asserted (PHY_CLOCK_REG[1]=1).
- Enable initialization and training by writing to the Training Operation Register (TRN_OP_REG) as follows:
  - For 1,333 Mbps and below, set TRN_OP_REG=0x0DF. This enables initialization, command-bus training, write leveling, read training, write training, and 1D Vref training sequences to run.
  - For 1,600 Mbps and 1,866 Mbps, set TRN_OP_REG=0x1DF to perform bit-level trim sweep in addition to the above.
  - For 2,133 Mbps and 2,400 Mbps, set TRN_OP_REG=0x3DF to perform bit-level trim sweep and 2D Vref training in addition to the above. This is necessary for the two highest data rates.

For simulation purposes, shorten the initialization and training sequences (including command-bus training) by writing 0x01C to TRN_OP_REG. For more information, refer to the DDR Memory PHY Module User Guide (FPGA-IPUG-02195).

- Pull the training CPU out of reset by writing 1'b1 to the Reset Register (RESET_REG). This begins the initialization and training sequence.
- Wait until initialization and training completes using one of the following methods:

Poll the Status Register (STATUS_REG) until the write_trn_done signal asserts (STATUS_REG[4]=1). This indicates that write training completes, which is the final stage in the initialization and training process.

- Wait for the trn_done_int signal (INT_STATUS_REG[0]=1) or the trn_error_int signal (INT_STATUS_REG[1]=1) to assert in the Interrupt Status Register (INT_STATUS_REG). This method requires the trn_done_en signal (INT_ENABLE_REG[0]=1) and the trn_err_en signal (INT_ENABLE_REG[1]=1) to be asserted in the Interrupt Enable Register (INT_ENABLE_REG).

After completing the above steps, the PHY control transfers to the Memory Controller and you can start accessing the SDRAM memory through the data interface. Once init_done_o asserts, the RISC-V CPU and Training Engine are reset to save power.

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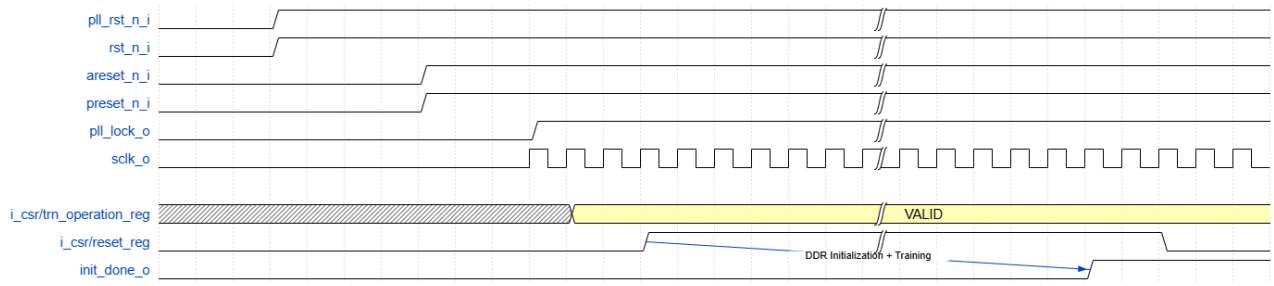



**Figure 2.3. Initialization Sequence (with APB interface)**

### 2.4.1. Initialization and Training Sequence

The Memory Controller IP performs initialization according to the DDR4/LPDDR4 JEDEC standards. For more information on the stages that occur during the initialization and training sequence, refer to the DDR Memory PHY Module User Guide (FPGA-IPUG-02195).

### 2.4.2. Initialization and Training without APB Interface

The APB interface is unavailable when the *Enable APB interface* attribute is unchecked. In this case, the init_start_i and trn_opr_i signals start and configure the DDR4/LPDDR4 initialization and training. The trn_opr_i sets the value of the Training Operation Register (TRN_OP_REG), controlling which specific training steps to perform based on the asserted bits. For hardware implementation:

- For 1,333 Mbps and below, set trn_opr_i=0x0DF to perform command bus training, write leveling, read training, write training, and 1D Vref training procedures.
- For 1,600 Mbps and 1,866 Mbps, set trn_opr_i=0x1DF to perform bit-level trim sweep in addition to the above.
- For 2,133 Mbps and 2,400 Mbps, set trn_opr_i=0x3DF to perform bit-level trim sweep and 2D Vref training. This is necessary for the highest two data rates.

For simulation purposes, shorten the initialization and training sequences (including command bus training) by setting trn_opr_i=0x01C. For more information regarding the initialization and training sequences and relevant registers, refer to the DDR Memory PHY Module User Guide (FPGA-IPUG-02195).

Execute the following steps to start the initialization and training sequence of the DDR4/LPDDR4 SDRAM:

1. Set init_start_i=0 while the Memory Controller IP is in reset or while pll_lock_o=0.
2. Wait until pll_lock_o=1 before setting init_start_i=1. Maintain this value until init_done_o asserts.
3. Once init_done_o=1, set init_start_i=0 to hold the training CPU in reset to save power.

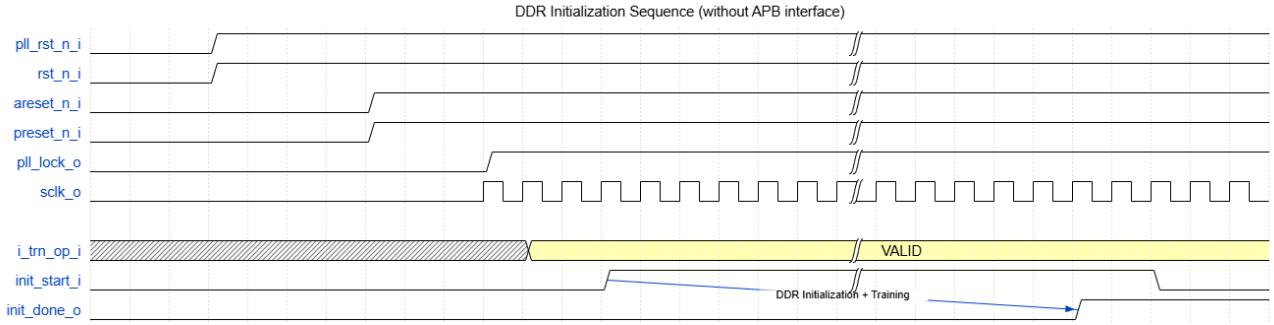



**Figure 2.4. Initialization Sequence (without APB interface)**

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## 2.5. Operation Descriptions

This section provides details on various operations and features supported by the Memory Controller IP.

### 2.5.1. DDR4

The following section describes the operations supported in DDR4 mode.

#### 2.5.1.1. Write and Read Data Access

Once the init_done_o signal asserts, you can initiate write and read accesses. The types of data accesses supported by the Memory Controller IP depend on the selected data interface protocol. Refer to Table 2.2 for a list of all supported AXI4 data accesses.

The Memory Controller decodes the memory-mapped address to check if the row and bank addresses are already opened in the memory device. When a WRITE/READ command issues to DDR4 memory, the following commands issue:

- If the target row, bank, and bank group are not open, the Memory Controller issues an ACTIVE command to the DDR4 SDRAM to open the row. This is followed by the WRITE/READ command.
- If there is an open row in the current bank or bank group and the target row address is different from the open row, the Memory Controller issues a PRECHARGE command to close the open row. This is followed by an ACTIVATE command to open the target row, and then the WRITE/READ command.
- If the target row is already open, the Memory Controller issues only a WRITE/READ command.

The Memory Controller does not immediately close a row after issuing a WRITE/READ command. It issues a separate PRECHARGE command as needed.

The following figures show an example AXI4 write/read to DDR4 transaction.

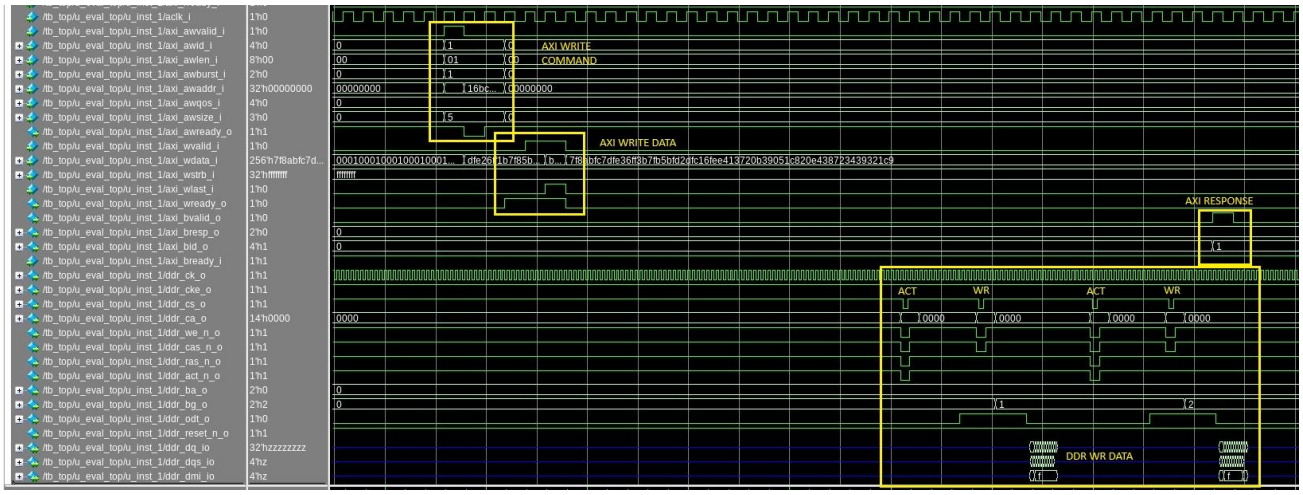



**Figure 2.5. Basic AXI4 Write to DDR4 Write transaction**

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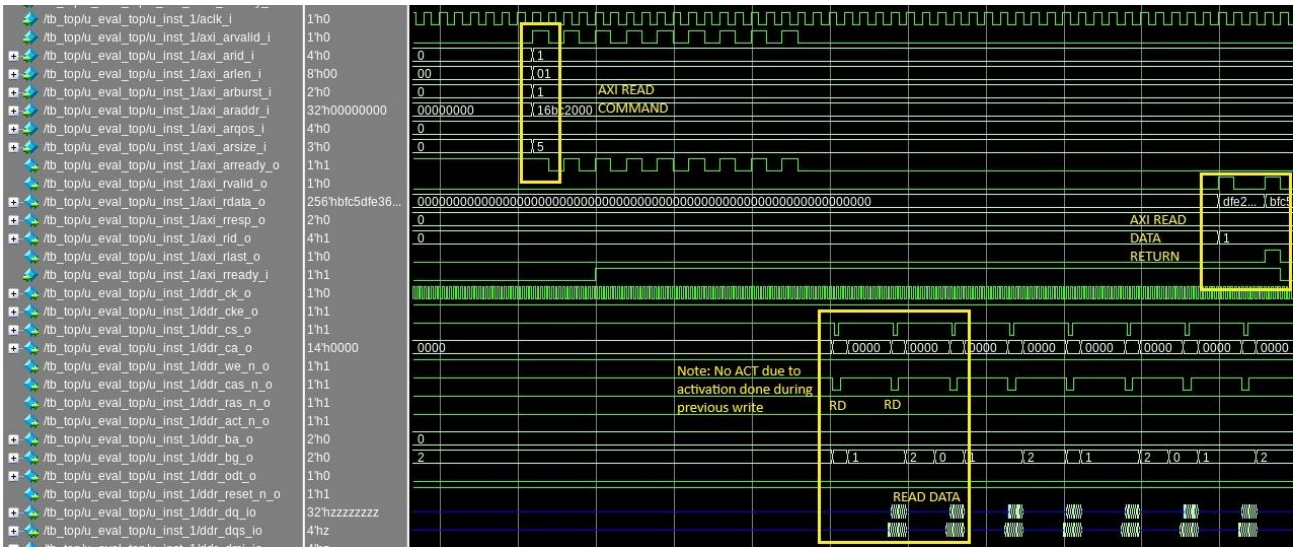



**Figure 2.6. Basic AXI4 Read to DDR4 Read transaction**

The transaction on the wire follows the JEDEC specification and may differ slightly based on training results. A BL8 transaction is similar to the following waveform.

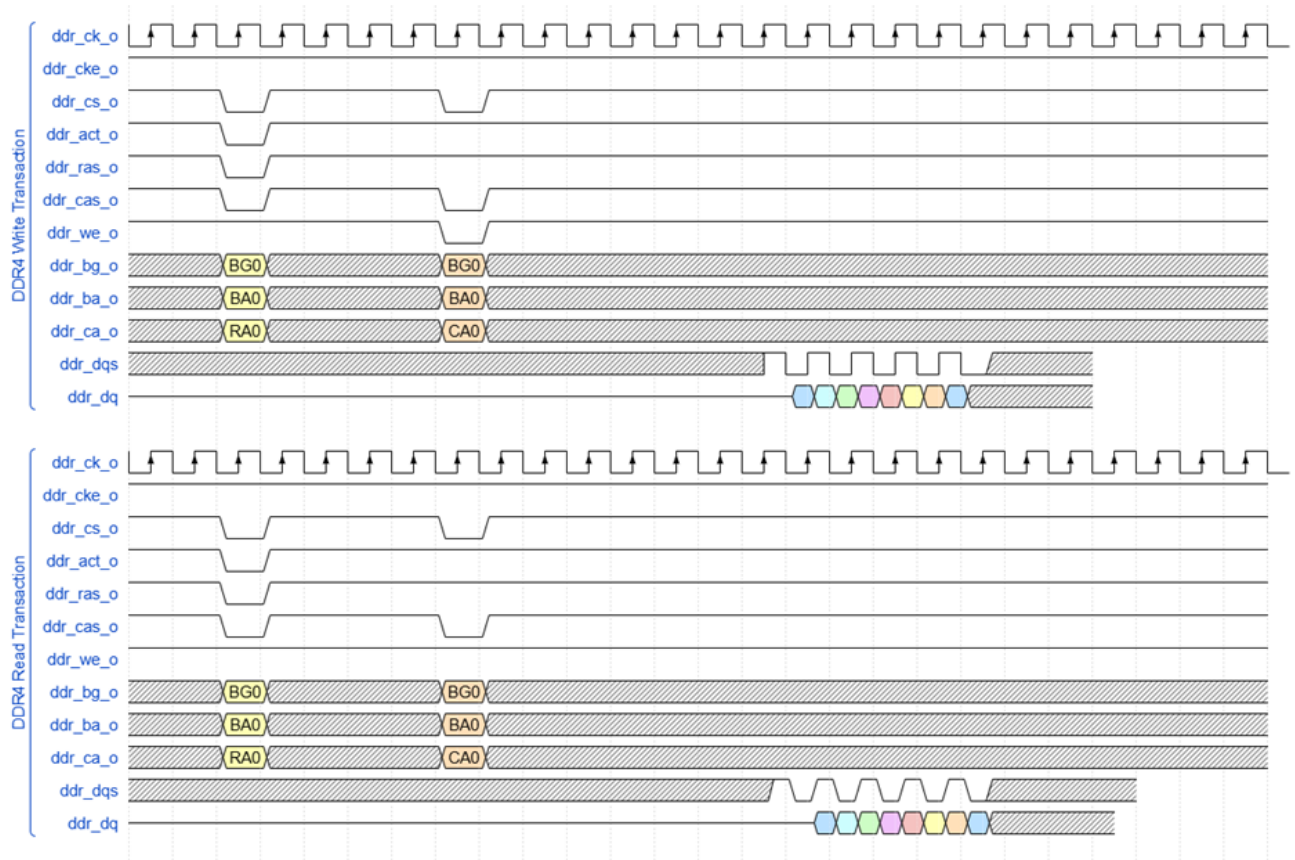



**Figure 2.7. DDR4 Write and Read Transaction**

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#### 2.5.1.2. Auto Refresh Support

Ideally, issue REFRESH commands every refresh interval, as specified by the *Refresh Period* attribute. To improve efficiency in scheduling and switching between tasks, the DDR4 memory allows a maximum of eight REFRESH commands to be postponed throughout the DDR4 operation. The Memory Controller has an internal auto refresh generator that sends out a set of consecutive AUTO REFRESH commands to the memory once it reaches the time specified in the following calculation: *Refresh Period* × *Number of Outstanding Refresh*.

For high-performance applications, set the *Number of Outstanding Refresh* to the maximum value. This increases the DDR4 bus throughput by minimizing Memory Controller intervention.

#### 2.5.1.3. Periodic ZQ Calibration

ZQ Calibration calibrates the output driver impedance and On-Die Termination (ODT) values across PVT. The Memory Controller IP periodically performs ZQ Calibration as the voltage and temperature fluctuate during operation. You can configure the frequency at which ZQ Calibration is performed and its duration through the *ZQ Calibration Period* attribute. Periodic ZQ calibration uses the DDR4 ZQ Calibration Short (ZQCS) command.

#### 2.5.1.4. Side-band ECC

The ECC side-band feature enables data reliability through a Single Error Correction, Double Error Detection (SECDED) implementation. It generates an additional 8-bit ECC during write operations, which is written to DDR4 memory on its dedicated channel along with the user data. This 8-bit ECC is read back with the data and checked for single or double-bit errors during read operations, with error flags set in the ECC status registers. Error correction is performed on single-bit errors without writing back to the DDR4 memory. A read-modify-write (RMW) transaction is executed for ECC generation when a partial write is performed on the DDR4 memory. Therefore, the memory must be initialized with valid data in the region targeted by the partial write. Use full write access to maximize data-access throughput.

#### 2.5.1.5. Auto-Precharge

The Auto-Precharge (AP) feature allows the memory controller to automatically issue read and write commands with the Auto-Precharge flag for single burst Read and Write commands. When *Enable Auto-Precharge* is enabled, the controller issues each read/write request with the AP bit set, ensuring that the DRAM automatically closes the row at the end of the burst without requiring an explicit PRECHARGE command. This feature should be enabled for traffic patterns that use single burst random accesses, reducing command overhead.

### 2.5.2. LPDDR4

This section describes the operations supported in LPDDR4 mode.

#### 2.5.2.1. Write and Read Data Access

Once the init_done_o signal asserts, you can initiate write and read accesses. The types of data accesses supported by the Memory Controller IP depend on the selected data interface protocol. Refer to Table 2.2 for a list of all supported AXI4 data accesses.

The Memory Controller decodes the memory-mapped address to check if the row and bank addresses are already open in the memory device. When a WRITE/READ command issues to LPDDR4 memory, the following commands issue:

- If the target row and bank are not open, the Memory Controller issues an ACTIVATE command to the LPDDR4 SDRAM to open the row. This is followed by the WRITE/READ command.
- If there is an open row in the current bank and the target row address is different from the open row, the Memory Controller issues a PRECHARGE command to close the open row. This is followed by an ACTIVATE command to open the target row, and then the WRITE/READ command.
- If the target row is already open, the Memory Controller issues only a WRITE/READ command.

The Memory Controller does not immediately close a row after issuing a WRITE/READ command. It issues a separate PRECHARGE command as needed.

Figure 2.8 shows an example AXI write to LPDDR4 transaction and Figure 2.9 shows an example AXI read to LPDDR4 transaction.

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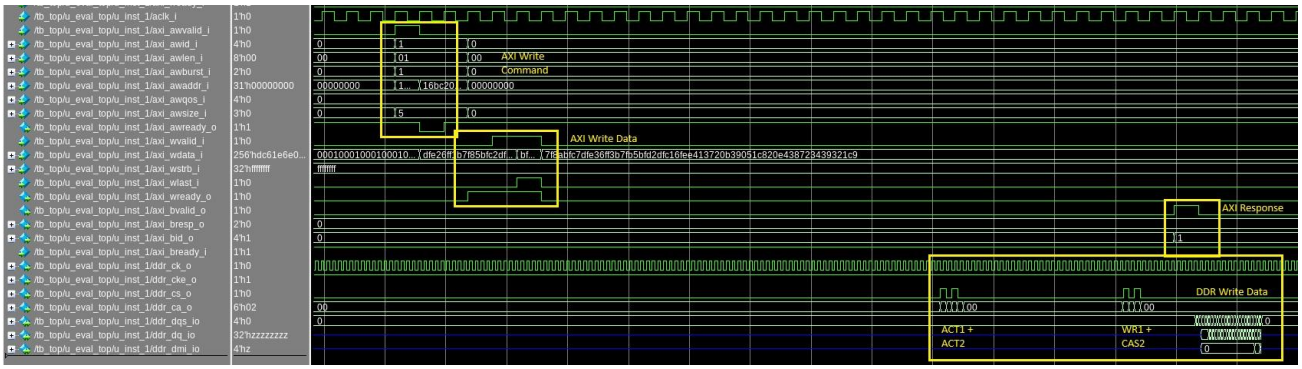



**Figure 2.8. Basic AXI4 Write to LPDDR4 Write transaction**

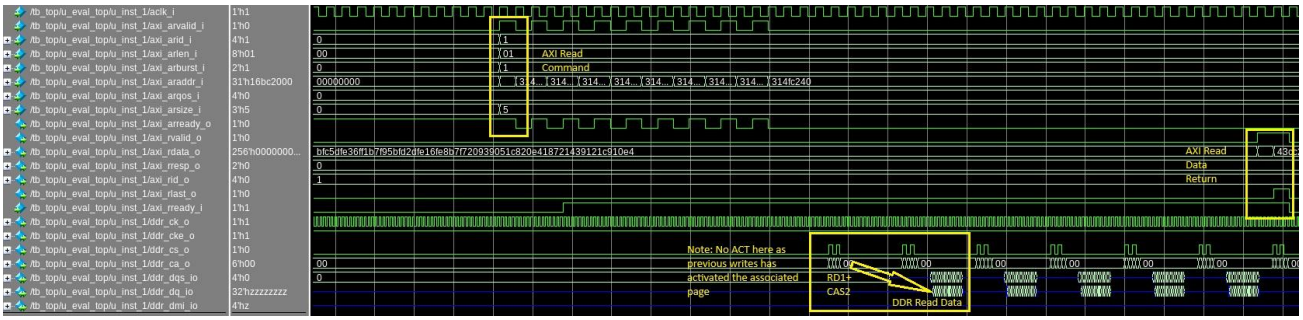



**Figure 2.9. Basic AXI4 Read to LPDDR4 Read transaction**

The transaction on the wire follows the JEDEC specification and may differ slightly based on training results. A BL16 transaction will be similar to the following waveform.

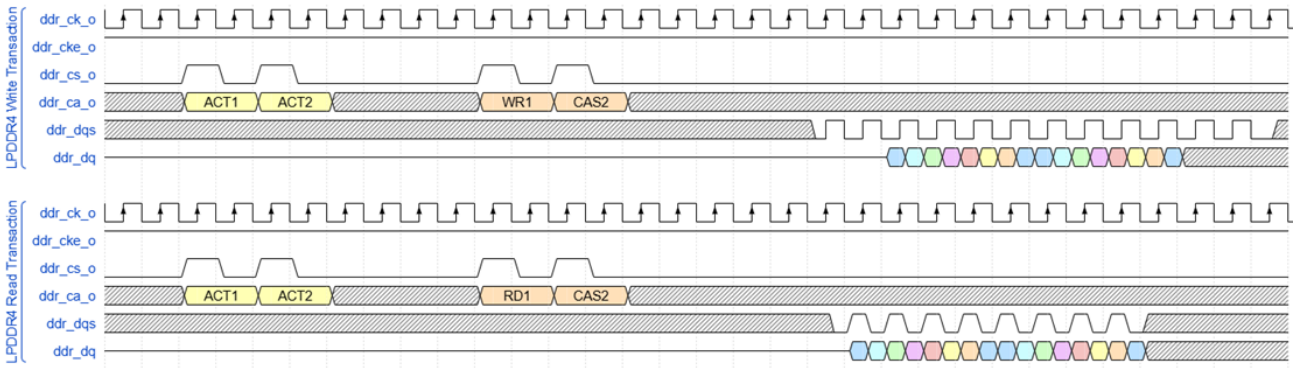



**Figure 2.10. LPDDR4 Write and Read Transaction**

### 2.5.2.2. Auto Refresh Support

Ideally, issue REFRESH commands every refresh interval, as specified by the *Refresh Period* attribute. To improve efficiency in scheduling and switching between tasks, the LPDDR4 memory allows a maximum of eight *REFRESH* commands to be postponed throughout the LPDDR4 operation. The Memory Controller has an internal auto refresh generator that sends out a set of consecutive AUTO REFRESH commands to the memory once it reaches the time specified in the following calculation: *Refresh Period* × *Number of Outstanding Refresh*.

For high-performance applications, set the *Number of Outstanding Refresh* to the maximum value. This increases the LPDDR4 bus throughput by minimizing Memory Controller intervention.

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#### 2.5.2.3. Power Saving Feature

The Memory Controller supports power saving when the *Enable Power Down* attribute is set. The Memory Controller IP tracks the period of inactivity on the local data bus by monitoring the System Clock (SCLK), the main clock used by the Memory Controller IP. When the period of inactivity on the bus reaches the value set in the *Number of SCLK to enter Self-Refresh from no traffic* attribute, the Memory Controller issues SELF REFRESH and Power-Down Entry commands. This puts the memory into Power-Down mode to save power until a new request is received on the local data bus, at which point the Memory Controller issues SELF REFRESH and Power-Down Exit commands, followed by an additional REFRESH command.

The CLK can also be turned off upon entry into SELF REFRESH. This capability applies on a per-DDR-PHY-instance basis. For a single rank implementation, the CLK turns off immediately, while a two-rank implementation will require both ranks to enter SELF REFRESH before the CLK is turned off.

#### 2.5.2.4. Periodic ZQ Calibration

ZQ Calibration calibrates the output driver impedance across PVT. There are two ZQ Calibration modes initiated with the Multi-Purpose Command (MPC): ZQCAL START and ZQCAL LATCH. The ZQCAL START command initiates the SDRAM calibration procedure, and the ZQCAL LATCH command captures the result and loads it into the SDRAM drivers.

The Memory Controller IP periodically performs ZQ Calibration as the voltage and temperature may fluctuate during operation. You can configure the frequency at which ZQ Calibration is performed and its duration through the *ZQ Calibration Period* and *ZQ Calibration Start to Latch* attributes. Periodic ZQ calibration uses the LPDDR4 ZQ Calibration commands.

#### 2.5.2.5. Temperature Tracking and Extended Temperature Support

LPDDR4 SDRAM devices support temperature tracking, where the device refresh rate can change based on the operational temperature. When the memory device temperature is within normal operating conditions, the rate is set to 1x refresh, which is the default case. As the temperature fluctuates below or above the default case, the Memory Controller decreases or increases the frequency of refreshes, respectively. The required refresh rate according to temperature is specified in MR4 within LPDDR4 SDRAM. When the Temperature Update Flag (TUF) is set in MR4, it indicates that the refresh rate has changed from the last read issued to MR4. In this case, the Memory Controller waits for the completion of the current refresh cycle and updates the refresh period based on MR4 for the subsequent timing of the refresh.

LPDDR4 SDRAM devices also support operation at extended temperatures. When the operational temperature increases beyond normal operation conditions, the refresh frequency increases. When the refresh rate in MR4 is set to 3’b110, timing derating is required for certain commands, slowing performance. For more information regarding temperature-derating timing requirements, refer to the LPDDR4 JEDEC Standard.

The Memory Controller IP periodically reads MR4 to track the temperature of the LPDDR4 memory device. Based on the refresh rate set in MR4, the Memory Controller IP issues REFRESH commands at the required frequency. Note that when the refresh rate in MR4 is set to either 3’b000 or 3’b111, the LPDDR4 memory may not work as expected due to exceeding the low/high temperature operating limits.
When the refresh rate is set to 3’b110 in MR4, the Memory Controller accommodates the temperature-derating timing requirements when issuing commands to the memory. You can change the frequency at which the MR4 register is read through the *Temperature Check Period* attribute. For more information regarding supported LPDDR4 operations and relevant registers, refer to the DDR Memory PHY Module User Guide (FPGA-IPUG-02195).

#### 2.5.2.6. Auto-Precharge

The Auto-Precharge (AP) feature allows the memory controller to automatically issue read and write commands with the **Auto-Precharge** flag for single-burst Read and Write commands. When enabled, the controller issues each read/write request with the AP bit set, ensuring that the DRAM automatically closes the row at the end of the burst without requiring an explicit PRECHARGE command. This feature should be enabled for traffic patterns that use single-burst random accesses, reducing command overhead.

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# 3. IP Parameter Description

The following tables show and describe the configurable attributes of the DDR Memory Controller IP. You can configure these attributes through the IP Catalog Module/IP Block Wizard of the Lattice Radiant software. Refer to the Designing and Simulating the IP section of this user guide for information on how to configure and generate the Memory Controller IP.

## 3.1. DDR4

This section describes the parameters available in DDR4 mode.

### 3.1.1. General

This section describes the parameters available in the general tab of the IP parameter editor.

**Table 3.1. DDR4 General Attributes**

| Attribute | Selectable Values | Default | Dependency on Other Attributes |
|---|---|---|---|
| Interface Type | DDR4 | DDR4 | — |
| I/O Buffer Type | POD12 | POD12 | Display only |
| Simulation Mode Enable | Checked, Unchecked | Unchecked | Selectable for Radiant 2026.1 and later |
| DDR Command Frequency (MHz)[1] | 666, 800, 933, 1066, 1200 | 800 | — |
| Gearing Ratio | 8:1 | 8:1 | Display only |
| Enable Auto-Precharge | Checked, Unchecked | Unchecked | — |
| Enable DDR4 Side-band ECC | Checked, Unchecked | Unchecked | Display only |
| Enable Power Down[2] | Checked, Unchecked | Unchecked | Display only |
| Read Latency | 10 | 10 | DDR Command Frequency = 666 MHz |
| | 10, 11, 12 | 12 | DDR Command Frequency = 800 MHz |
| | 12, 13, 14 | 12 | DDR Command Frequency = 933 MHz |
| | 14, 15, 16 | 14 | DDR Command Frequency = 1,066 MHz |
| | 15, 16, 17, 18 | 16 | DDR Command Frequency = 1,200 MHz |
| Write Latency | 9 | 9 | DDR Command Frequency = 666 MHz |
| | 9, 11 | 9 | DDR Command Frequency = 800 MHz |
| | 10, 12 | 10 | DDR Command Frequency = 933 MHz |
| | 11, 14 | 11 | DDR Command Frequency = 1,066 MHz |
| | 12, 16 | 12 | DDR Command Frequency = 1,200 MHz |
| Enable Internal RISC-V CPU | Checked, Unchecked | Checked | Display only<br>(Disabling of Internal RISC-V CPU is not yet supported) |
| Disable Per-bank Timer | Checked, Unchecked | Unchecked | Fixed to Checked when DDR Command Frequency is 1,066 or more, or when Side-band ECC is enabled.<br>Selectable when DDR Command Frequency is below 1,066 |

**Notes:**

1. The supported DDR command frequency depends on the device speed grade. Refer to the Minimum Device Requirements section for the list of maximum supported frequency for each speed grade.
2. The Enable Power Down attribute is hidden due to the known issues mentioned in Appendix B.

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**Table 3.2. DDR4 Clock Settings Attributes**

| Attribute | Selectable Values | Default | Dependency on Other Attributes |
|---|---|---|---|
| Enable PLL | Checked | Checked | Display only |
| Reference Clock Frequency (MHz) | Integer | 100.0 | — |
| DDR Memory Actual Frequency (MHz) | Calculated | N/A | Display only<br>Based on the selection for DDR Command Frequency |

**Table 3.3. DDR4 Memory Configuration Attributes**

| Attribute | Selectable Values | Default | Dependency on Other Attributes |
|---|---|---|---|
| DDR Density (per Channel) | 2 Gb, 4 Gb, 8 Gb, 16 Gb | 4 Gb | — |
| DDR Bus Width (DDR_WIDTH) | 16, 32, 64 | 32 | — |
| Configuration | x8, x16 | x16 | — |
| Number of Ranks (CS_WIDTH) [1] | 1, 2 | 1 | — |
| Number of DDR Clocks (CK_WIDTH) | 1, 2 | 1 | — |

**Note:**

1. Devices with speed grades of 2 and 3 support dual rank.

**Table 3.4. DDR4 Local Data Bus Attributes**

| Attribute | Selectable Values | Default | Dependency on Other Attributes |
|---|---|---|---|
| Local Data Bus Type | AXI4 | AXI4 | Display only |
| Address Width | Calculated | N/A | Display only<br>Calculated based on selection for DDR Density |
| Data Width | 32, 64, 128, 256, 512 | 256 | Calculated based on the selection for DDR Bus Width |
| ID Width | 1, 2, 3, 4, 5, 6, 7, 8 | 4 | — |
| Maximum Burst Length | 64, 128, 256 | 64 | — |
| Write Ordering Queues | 1, 2, 3, 4 | 2 | — |
| Read Ordering Queues | 1, 2, 3, 4 | 2 | — |
| Enable Local Bus Clock | Checked, Unchecked | Checked | — |
| Enable APB interface | Checked, Unchecked | Checked | — |

**Table 3.5. DDR4 General Definitions**

| Attribute | Description |
|---|---|
| **General Group** | |
| Interface Type | Specifies the SDRAM Memory interface: DDR4 |
| I/O Buffer Type | I/O Standard for the memory interface signals.<br>This is fixed to POD12 for DDR4, but the command/address/control signals should be terminated to VTT on the board. See note 2 of Table 4.9. |
| Simulation Mode Enable | Enables the DDRPHY SW primitive for simulation and skips Read Training and Write Training. The purpose of this feature is to reduce the training simulation time.<br>This option should not be enabled when implementing the design on the FPGA. |
| DDR Command Frequency (MHz) | Speed at which the memory controller issues commands to the memory device. |
| Gearing Ratio | Specifies the ratio between the DDR data speed and the memory controller speed. |
| Enable Auto-Precharge | Enables memory controller to automatically send Read with Auto-Precharge for single read accesses (AXI reads with burst length = 0). This is to enhance performance for a design that issues large random single-read accesses. |
| Enable DDR4 Side-band ECC | Enables the DDR4 side-band ECC feature. |

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| Attribute | Description |
|---|---|
| Enable Power Down | Enables memory controller automatically placing the memory device into power-down mode after a specified number of idle controller clock cycles (not yet supported). |
| Read Latency | Specifies the delay from issuing a read command to receiving of read data from SDRAM. Set this based on the target DRAM datasheet. |
| Write Latency | Specifies the delay from issuing a write command to providing of write data to SDRAM. Set this based on the target DRAM datasheet. |
| Enable Internal RISC-V CPU | Enables RISC-V subsystem to support initialization and training of the memory device (disabling is not yet supported) |
| Disable Per-bank Timer | Disables the Per-bank Timer in the design. Per-bank timers increase design LUT size and timing closure complexity. For traffic using mainly large AXI burst length, this can be disabled without much impact on overall performance. Disabled automatically for higher frequency configurations in the IP editor. |
| **Clock Settings Group** | |
| Enable PLL | Enables PLL |
| Reference Clock: Frequency (MHz) | Indicates the PLL reference clock speed |
| DDR Memory Actual Frequency (MHz) | Specifies the actual operating frequency of the memory interface (calculated by the PLL – includes tolerance) |
| **Memory Configuration Group** | |
| DDR Density (per Channel) | Density of SDRAM (number of chips on memory module). Only DDR Density with powers of two are supported. |
| DDR Bus Width | Total number of data pins in memory interface |
| Configuration | Specifies the DRAM's Configuration as x8 or x16. The x4 is not supported. Set this based on the target DRAM datasheet. |
| Number of Ranks | Specifies number of ranks in memory interface |
| Number of DDR Clocks | Specifies the number of CK/CK# clock pairs to be driven to SDRAM |
| **Local Data Bus Group** | |
| Local Data Bus Type | Indicates bus for local data interface: AXI4. |
| Address Width | Specifies the number of address pins in memory interface, dependent on the SDRAM density |
| Data Width (AXI_DATA_WIDTH) | Indicates data width for local data bus |
| ID Width | Indicates bit width of AXI4 ID |
| Maximum Burst Length | Specifies the maximum AXI4 burst length. Recommended to set based on system requirements to save EBR resources. |
| **Local Data Bus Group** | |
| Write Ordering Queues | The number of write/read ordering queues process write and read data requests. The higher the value, the greater the bandwidth on the interface, as gaps between accesses are reduced at the cost of consuming more LUTs. |
| Read Ordering Queues | |
| Enable Local Bus Clock | Enables clock domain crossing logic for the local data bus. |
| Enable APB interface | Enables APB interface. Should be enabled if the target application includes a CPU. When disabled, initialization and training of SDRAM should be handled through init_start_i and trn_opr_i signals. Refer to the Initialization and Training without APB Interface section of this user guide for more information. |

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### 3.1.2. Memory Device Timing

This section describes the parameters available in the Memory Device Timing tab of the IP parameter editor. The default value of the attributes listed under the Memory Device Timing Setting Group is different for each DDR Command Frequency value and is based on the JESD79-4D SDRAM standard. These values may need to be manually adjusted based on the selected DDR4 device.

**Table 3.6. DDR4 Memory Device Timing Setting Attributes**

| Attribute | Selectable Values | Default | Dependency on Other Attributes |
|---|---|---|---|
| Manual Timing Adjust Enable | Checked/Unchecked | Unchecked | — |
| TRCD (tCLK) | 4–65,536 | Calculated | Enabled when Manually Adjust is Checked |
| TRAS (tCLK) | 4–65,536 | Calculated | Enabled when Manually Adjust is Checked |
| TRPPB (tCLK) | 4–65,536 | Calculated | Enabled when Manually Adjust is Checked |
| TWR (tCLK) | 4–65,536 | Calculated | Enabled when Manually Adjust is Checked |
| TRTP (tCLK) | 8–65,536 | Calculated | Enabled when Manually Adjust is Checked |
| TCCD (tCLK) | 8–65,536 | Calculated | Enabled when Manually Adjust is Checked |
| TRRD (tCLK) | 6–65,536 | Calculated | Enabled when Manually Adjust is Checked |
| TRFC (tCLK) | 24–28,080 | Calculated | Enabled when Manually Adjust is Checked |
| TFAW (tCLK) | 40–65,536 | Calculated | Enabled when Manually Adjust is Checked |
| TZQLAT (tCLK) | 4–65,536 | Calculated | Enabled when Manually Adjust is Checked |
| TMRD (tCLK) | 10–65,536 | Calculated | Enabled when Manually Adjust is Checked |
| TRPAB (tCLK) | 4–65,536 | Calculated | Enabled when Manually Adjust is Checked |
| TDQSS (tCLK) | Integer | 0 | Enabled when Manually Adjust is Checked |
| TRD2PRE (tCLK) | 4–65,536 | Calculated | Enabled when Manually Adjust is Checked |
| TWR2PRE (tCLK) | 4–65,536 | Calculated | Enabled when Manually Adjust is Checked |
| TXP (tCLK) | 4–65,536 | Calculated | Enabled when Manually Adjust is Checked |
| TXPSR (tCLK) | 4–65,536 | Calculated | Enabled when Manually Adjust is Checked |

**Table 3.7. DDR4 Periodic Event Setting Attributes**

| Attribute | Selectable Values | Default | Dependency on Other Attributes |
|---|---|---|---|
| Number of SCLK to enter Self Refresh from no traffic | Integer | 5,000 | Enabled when Enable Power Down is Checked |
| Refresh Period (tSCLK) | Calculated | Calculated | Default value is calculated based on selection for DDR Command Frequency |
| Number of Outstanding Refresh | 1, 2, 3, 4, 5, 6, 7 | 7 | — |
| ZQ Calibration Period (sec) | Integer | 32 | — |
| Temperature Check Period (sec) | Integer | 32 | — |

**Table 3.8. DDR4 Memory Device Timing Definitions**

| Attribute | Description |
|---|---|
| **Memory Device Timing Setting Group[1]** | |
| Manual Timing Adjust Enable | Enables you to manually set any of the memory timing parameters |
| TRCD | Indicates the delay between the ACTIVATE command (RAS) and the internal access to data (CAS) |
| TRAS | Indicates how long memory must wait after an ACTIVATE command before a PRECHARGE command can be issued to close the row |
| TRPPB | Row PRECHARGE time for a single bank |
| TWR | Specifies the amount of clock cycles needed to complete a WRITE before a PRECHARGE command can be issued |
| TRTP | Internal READ to PRECHARGE delay |
| TCCD | Minimum time between two READ/WRITE (CAS) commands (burst length / 2) |

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| Attribute | Description |
|---|---|
| TRRD | Minimum time interval between two ACTIVATE commands to different banks |
| TRFC | Indicates how long memory must wait after a REFRESH command before an ACTIVATE command can be accepted by memory |
| TFAW | Specifies the period duration during which only four banks can be active |
| TZQLAT | ZQ calibration time from LATCH command to next allowed command |
| TMRD | Minimum time between two MRS commands |
| TRPAB | Row PRECHARGE time for all banks |
| TDQSS | Describes skew between the output data strobe with respect to the memory clock for writes (DQS to CK) |
| TRD2PRE | READ to PRECHARGE time |
| TWR2PRE | WRITE to PRECHARGE time |
| TXP | Power-down exit latency to next valid command |
| TXPSR | Power-down exit latency to next self-refresh |
| **Periodic Event Setting Group** | |
| Number of SCLK to enter Self-Refresh from no traffic | The memory controller puts the memory in self-refresh when there is no traffic for the specified number of SCLK cycles |
| Refresh Period | Specifies the number of SCLK cycles between refresh commands |
| Number of Outstanding Refresh | Specifies the maximum number of outstanding refresh commands. Refer to the Auto Refresh Support section of this user guide for more information |
| ZQ Calibration Period | Indicates period for performing ZQ Calibration in seconds |
| Temperature Check Period | Indicates period for reading the temperature register (MR4) in DDR4 memory in seconds |

**Note:**

1. The memory device timing parameters listed under the Memory Device Timing tab are defined according to the JESD79-4D SDRAM standard. Refer to the memory device data sheet for detailed descriptions and allowed values for these parameters.

### 3.1.3. Training Settings

This section describes the parameters available in the Training Settings tab of the IP parameter editor.

**Table 3.9. DDR4 Training Settings Attributes**

| Attribute | Selectable Values | Default | Dependency on Other Attributes |
|---|---|---|---|
| DDR Clock Delay Value | 0–20 | 15 | — |
| DDR Clock Delay Value Incr/Decr | Checked, Unchecked | Checked | — |
| CS Delay Value | 0–20 | 15 | — |
| CS Delay Value Incr/Decr | Checked/Unchecked | Checked | — |
| Address Control Delay Value | 0–20 | 4 | — |
| Address Control Delay Value Incr/Decr | Checked, Unchecked | Unchecked | — |
| Memory DQ_Vref Value for Rank0 | 0–114 | 90 | — |
| Memory DQ_Vref Value for Rank1 | 0–114 | 90 | Enabled when *Number of Ranks*==2 |
| MC DQS Grp<0,1> Vref Value | 0–127 | 80 | — |
| MC DQS Grp<2,3> Vref Value | 0–127 | 80 | Enabled when *DDR Bus Width*≥ 32 |
| MC DQS Grp<4,7> Vref Value | 0–127 | 80 | Enabled when *DDR Bus Width*≥64 |
| MC DQS Grp8 Vref Value | 0–127 | 80 | Enabled when *DDR Bus Width*=64 with Enable DDR4 Side-band ECC=1 |

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**Table 3.10. DDR4 MC I/O Settings Attributes**

| Attribute | Selectable Values | Default | Dependency on Other Attributes |
|---|---|---|---|
| CK/CS Slew Rate | Slow, Fast | Fast | — |
| Command Address Slew Rate | Slow, Fast | Fast | — |
| DQS Slew Rate | Slow, Fast | Fast | — |
| DQ/DMI Slew Rate | Slow, Fast | Fast | — |
| MC CA Output Impedance | 240 Ω, 120 Ω, 68 Ω, 60 Ω, 48 Ω, 40 Ω, 34 Ω | 34 Ω | — |
| MC DQ Output Impedance | 240 Ω, 120 Ω, 68 Ω, 60 Ω, 48 Ω, 40 Ω, 34 Ω | 34 Ω | — |
| MC ODT Value | 240 Ω, 120 Ω, 68 Ω, 60 Ω, 48 Ω, 40 Ω, 34 Ω | 60 Ω | — |

**Table 3.11. DDR4 Memory ODT Settings Attributes**

| Attribute | Selectable Values | Default | Dependency on Other Attributes |
|---|---|---|---|
| RTT_WR Value | Dynamic ODT OFF, RZQ/1, RZQ/2, RZQ/3, Hi-Z | Dynamic ODT OFF | — |
| RTT_NOM Value | Disable, RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, RZQ/6, RZQ/7 | RZQ/5 | — |
| RTT_PARK Value | Disable, RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, RZQ/6, RZQ/7 | Disable | — |

**Table 3.12. DDR4 Training Settings Definitions**

| Attribute[1] | Description |
|---|---|
| **Training Settings** | |
| DDR Clock Delay Value | Specifies the DDR clock delay so that the first DQS toggle is at CK = 0 during write leveling. It is recommended to increase this value if write leveling fails |
| DDR Clock Delay Value Incr/Decr | Specifies the adjustment direction<br>Checked: DDR Clock Delay Value is added to the ddr_ck_o signal<br>Unchecked: DDR Clock Delay Value is subtracted from the ddr_ck_o signal |
| CS Delay Value | Specifies the DDR CS delay value |
| CS Delay Value Incr/Decr | Specifies the adjustment direction<br>Checked: CS Delay Value is added to the ddr_cs_o signal<br>Unchecked: CS Delay Value is subtracted from the ddr_cs_o signal |
| Address Control Delay Value | Specifies the DDR address/control signals delay. It is recommended to increase this value if command bus training fails |
| Address Control Delay Value Incr/Decr | Specifies the adjustment direction<br>Checked: Address Control Delay Value is added to the DDR address/control signals<br>Unchecked: Address Control Delay Value is subtracted from the DDR address/control signals |
| Memory DQ_Vref Value for Rank<0,1> | Specifies the DRAM DQ_Vref Value to be written to DDR4 DRAM's MR6 Vref DQ Training Value and Vref DQ Training Range for Rank0/Rank1. When the register field TRN_OP_REG.mem_vref_training_en=0, this will be used as the final DRAM DQ Vref.<br>Refer to the DDR4 JEDEC Standard for the allowed values in MR6 |
| MC DQS Grp<0,1,2,3,4,5,6,7,8> Vref Value | Specifies the MC DQ_Vref Value for each DQS group when DQ_Vref training is disabled by setting TRN_OP_REG.mc_vref_training_en=0.<br>The theoretical mV value is: Vref decimal value × 5mV |
| **DDR4 MC I/O Settings** | |
| CK/CS Slew Rate | Specifies the CK/CS driver strength |
| Command Address Slew Rate | Specifies the CA driver strength |
| DQS Slew Rate | Specifies the DQS driver strength |

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| Attribute[1] | Description |
|---|---|
| DQ/DMI Slew Rate | Specifies the DQ/DMI driver strength |
| MC CA Output Impedance | Memory controller CA I/O impedance to reach VDDQ threshold |
| MC DQ Output Impedance | Memory controller DQ I/O impedance to reach VDDQ threshold |
| MC ODT Value | Memory controller termination resistance value at FPGA |
| **DDR4 Memory ODT Settings** | |
| RTT_WR Value | Specifies the RTT_WR value that is written to MR2 in DDR4 memory |
| RTT_NOM Value | Specifies the RTT_NOM value that is written to MR1 in DDR4 memory |
| RTT_PARK Value | Specifies the RTT_PARK value that is written to MR5 in DDR4 memory |

**Note:**

1. These attributes should only be modified when an error is encountered during DDR4 memory training.

## 3.2. LPDDR4

This section describes the parameters available in LPDDR4 mode.

### 3.2.1. General

This section describes the parameters available in the General tab of the IP parameter editor.

**Table 3.13. LPDDR4 General Attributes**

| Attribute | Selectable Values | Default | Dependency on Other Attributes |
|---|---|---|---|
| Interface Type | LPDDR4 | LPDDR4 | Display only |
| I/O Buffer Type | LVSTL11_I, LVSTL11_II | LVSTL11_I | — |
| Simulation Mode Enable | Checked, Unchecked | Unchecked | Selectable for Radiant 2026.1 and later |
| DDR Command Frequency (MHz)[1] | 350, 400, 533, 666, 800, 933, 1066, 1200 | 800 | — |
| Gearing Ratio | 8:1 | 8:1 | Display only |
| Enable Auto-Precharge | Checked, Unchecked | Unchecked | — |
| Enable Power Down[2] | Checked, Unchecked | Unchecked | Display only |
| Enable Read DBI | Checked, Unchecked | Unchecked | Fixed to Enabled when *DDR Command Frequency* is 400 or less |
| Read Latency | Calculated | N/A | Display only<br>Calculated based on selection for *DDR Command Frequency* |
| Write Latency | Calculated | N/A | Display only<br>Calculated based on selection for *DDR Command Frequency* |
| Enable Internal RISC-V CPU | Checked, Unchecked | Checked | Display only<br>(Disabling of Internal RISC-V CPU is not yet supported) |
| Enable Reveal Debug | Checked, Unchecked | Unchecked | — |
| Enable Bit Swizzle | Checked, Unchecked | Unchecked | — |
| Disable Per-bank Timer | Checked, Unchecked | Unchecked | Fixed to Checked when *DDR Command Frequency* is 1066 or more<br>Selectable when *DDR Command Frequency* is below 1066 |

**Notes:**

1. Devices with speed grades of 2 and 3 support DDR command frequencies up to 1,066 MHz, while devices with speed grades of 3 support frequencies up to 1,200 MHz.
2. The Enable Power Down option is hidden due to the known issue mentioned in Appendix B.

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**Table 3.14. LPDDR4 Clock Settings Attributes**

| Attribute | Selectable Values | Default | Dependency on Other Attributes |
|---|---|---|---|
| Enable PLL | Checked | Checked | Display only |
| Reference Clock: Frequency (MHz) | 25.0, 50.0, 100.0 | 100.0 | — |
| DDR Memory Actual Frequency (MHz) | Calculated | N/A | Display only<br>Based on the selection for *DDR Command Frequency* |

**Table 3.15. LPDDR4 Memory Configuration Attributes**

| Attribute | Selectable Values | Default | Dependency on Other Attributes |
|---|---|---|---|
| DDR Density (per Channel) | 2 Gb, 4 Gb, 8 Gb, 16 Gb | 4 Gb | — |
| DDR Bus Width (DDR_WIDTH) | 16, 32, 64 | 32 | — |
| Number of Ranks (CS_WIDTH) [1] | 1, 2 | 1 | — |
| Number of DDR Clocks (CK_WIDTH) | 1, 2 | 1 | — |

**Note:**

1. Devices with speed grades of 2 and 3 support Dual Rank.

**Table 3.16. LPDDR4 Local Data Bus Attributes**

| Attribute | Selectable Values | Default | Dependency on Other Attributes |
|---|---|---|---|
| Local Data Bus Type | AXI4 | AXI4 | — |
| Address Width | Calculated | N/A | Display only<br>Calculated based on the selection for DDR Density |
| Data Width (AXI_DATA_WIDTH) | 32, 64, 128, 256 | 256 | — |
| ID Width | 1, 2, 3, 4, 5, 6, 7, 8 | 4 | — |
| Maximum Burst Length | 64, 128, 256 | 64 | — |
| Write Ordering Queues | 1, 2, 3, 4 | 2 | — |
| Read Ordering Queues | 1, 2, 3, 4 | 2 | — |
| Enable Local Bus Clock | Checked, Unchecked | Checked | — |
| Enable APB interface | Checked, Unchecked | Checked | — |

**Table 3.17. LPDDR4 General Definitions**

| Attribute | Description |
|---|---|
| **General Group** | |
| Interface Type | Specifies the SDRAM Memory interface: LPDDR4 |
| I/O Buffer Type | I/O Standard for the memory interface signals |
| Simulation Mode Enable | Enables the DDRPHY SW primitive for simulation and skips clock frequency change (starts with operating frequency), Command Bus Training, Read Training and Write Training. The purpose of this feature is to reduce the training simulation time.<br>This option should not be enabled when implementing the design on the FPGA. |
| DDR Command Frequency (MHz) | Speed at which the memory controller issues commands to the memory device |
| Gearing Ratio | Specifies the ratio between the DDR data speed and the memory controller speed |
| Enable Auto-Precharge | Enables memory controller to automatically send Read with Auto-Precharge for single read accesses (AXI reads with burst length = 0). This is to enhance performance for a design that issues large random single-read accesses. |
| Enable Power Down | Enables memory controller automatically placing the memory device into power-down mode after a specified number of idle controller clock cycles. |
| Enable Read DBI | Enables data bus inversion (DBI) for better signal integrity and read/write margins. |
| Read Latency | Specifies the delay from issuing a read command to receiving of read data from SDRAM |
| Write Latency | Specifies the delay from issuing a write command to providing of write data to SDRAM |

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| Attribute | Description |
|---|---|
| Enable Internal RISC-V CPU | Enables RISC-V subsystem to support initialization and training of the memory device (disabling is not yet supported) |
| Enable Reveal Debug | Enables the Reveal debug tool to connect to the MC for improved training debug<br>Refer to the Reveal User Guide for Radiant Software for more information. |
| Enable Bit Swizzle | Enables Bit Swizzle feature. Once checked, the Bit Swizzle Tab will be shown in the IP GUI. You can enable this if swizzling the DQ bit connection on the board will improve the LPDDR4 signal routing on the board. Refer to *Bit Swizzle* section of DDR Memory PHY Module User Guide (FPGA-IPUG-02195) for more information about this feature. |
| Disable Per-bank Timer | Disables the Per-bank Timer in the design. Per-bank timers increase design LUT size and timing closure complexity. For traffic using mainly large AXI burst length, this can be disabled without much impact on overall performance. This is disabled for higher frequency configurations in the GUI. |
| **Clock Settings Group** | |
| Enable PLL | Enables PLL |
| Reference Clock: Frequency (MHz) | Indicates the PLL reference clock speed |
| DDR Memory Actual Frequency (MHz) | Specifies the actual operating frequency of the memory interface (calculated by the PLL – includes tolerance) |
| **Memory Configuration Group** | |
| DDR Density (per Channel) | Density of SDRAM (number of chips on memory module). Only DDR Density with powers of two are supported. |
| DDR Bus Width | Total number of data pins in memory interface |
| Number of Ranks | Specifies number of ranks in memory interface |
| Number of DDR Clocks | Specifies the number of CK/CK# clock pairs to be driven to SDRAM<br>(multiple clocks is not yet supported) |
| **Local Data Bus Group** | |
| Local Data Bus Type | Indicates bus for local data interface: AXI4. |
| Address Width | Specifies number of address pins in memory interface, dependent on the SDRAM density |
| Data Width | Indicates data width for local data bus |
| ID Width | Indicates bit width of AXI4 ID |
| Maximum Burst Length | Specifies the maximum AXI4 burst length. Recommended to set based on system requirements to save EBR resources |
| Write Ordering Queues | The number of write/read ordering queues process write and read data requests. The higher the value, the greater the bandwidth on the interface, as gaps between accesses are reduced at the cost of consuming more LUTs |
| Read Ordering Queues | |
| Enable Local Bus Clock | Enables clock domain crossing logic for the local data bus |
| Enable APB interface | Enables APB interface. Should be enabled if the target application includes a CPU. When disabled, initialization and training of SDRAM should be handled via init_start_i and trn_opr_i signals. Refer to the Initialization and Training without APB Interface section of this user guide for more information. |

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### 3.2.2. Memory Device Timing

This section describes the parameters available in the Memory Device Timing tab of the IP parameter editor. The default value for the attributes listed under Memory Device Timing Setting Group is different for each DDR Command Frequency value and is based on the JESD209-4C SDRAM standard. These values may need to be manually adjusted based on the selected LPDDR4 device.

**Table 3.18. LPDDR4 Memory Device Timing Setting Attributes**

| Attribute | Selectable Values | Default | Dependency on Other Attributes |
|---|---|---|---|
| Manual Timing Adjust Enable | Checked/Unchecked | Unchecked | — |
| TRCD (tCLK) | 4–65,536 | Calculated | Enabled when *Manually Adjust* is Checked |
| TRAS (tCLK) | 4–65,536 | Calculated | Enabled when *Manually Adjust* is Checked |
| TRPPB (tCLK) | 4–65,536 | Calculated | Enabled when *Manually Adjust* is Checked |
| TWR (tCLK) | 4–65,536 | Calculated | Enabled when *Manually Adjust* is Checked |
| TRTP (tCLK) | 8–65,536 | Calculated | Enabled when *Manually Adjust* is Checked |
| TCCD (tCLK) | 8–65,536 | Calculated | Enabled when *Manually Adjust* is Checked |
| MWR2MWR (tCLK) | 32–65,536 | Calculated | Enabled when *Manually Adjust* is Checked |
| TRRD (tCLK) | 6–65,536 | Calculated | Enabled when *Manually Adjust* is Checked |
| TRFC (tCLK) | 24–28,080 | Calculated | Enabled when *Manually Adjust* is Checked |
| TFAW (tCLK) | 40–65,536 | Calculated | Enabled when *Manually Adjust* is Checked |
| TZQLAT (tCLK) | 4–65,536 | Calculated | Enabled when *Manually Adjust* is Checked |
| TMRR2WR (tCLK) | 8–65,536 | Calculated | Enabled when *Manually Adjust* is Checked |
| TMRD (tCLK) | 10–65,536 | Calculated | Enabled when *Manually Adjust* is Checked |
| TRPAB (tCLK) | 4–65,536 | Calculated | Enabled when *Manually Adjust* is Checked |
| TRTW (tCLK) | 21–65,536 | Calculated | Enabled when *Manually Adjust* is Checked |
| TDQSS (tCLK) | Integer | 1 | Enabled when *Manually Adjust* is Checked |
| TRD2PRE (tCLK) | 4–65,536 | Calculated | Enabled when *Manually Adjust* is Checked |
| TWR2PRE (tCLK) | 4–65,536 | Calculated | Enabled when *Manually Adjust* is Checked |
| TXP (tCLK) | 4–65,536 | Calculated | Enabled when *Manually Adjust* is Checked |
| TXPSR (tCLK) | 4–65,536 | Calculated | Enabled when *Manually Adjust* is Checked |

**Table 3.19. LPDDR4 Power Down Setting Attributes**

| Attribute | Selectable Values | Default | Dependency on Other Attributes |
|---|---|---|---|
| Number of SCLK to enter Self-Refresh from no traffic | Integer | 3,000 | Enabled when Enable Power Down is Checked. Determines the number of cycles of inactivity before a Self-Refresh with Power Down is triggered for power savings. |
| Enable CLKOFF in Power Down | Checked, Unchecked | Checked | When enabled, CLK will be turned off during Power Down. |

**Table 3.20. LPDDR4 Periodic Event Setting Attributes**

| Attribute | Selectable Values | Default | Dependency on Other Attributes |
|---|---|---|---|
| Refresh Period (tSCLK) | Calculated | Calculated | Default value is calculated based on selection for DDR Command Frequency |
| No. of Outstanding Refresh | 1, 2, 3, 4, 5, 6, 7 | 7 | — |
| ZQ Calibration Period (sec) | Integer | 32 | — |
| ZQ Calibration Start to Latch (usec) (TZQCAL) | Integer | 1 | — |
| Temperature Check Period (sec) | Integer | 32 | — |

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**Table 3.21. LPDDR4 Memory Device Timing Definitions**

| Attribute | Description |
|---|---|
| **Memory Device Timing Setting Group[1]** | |
| Manual Timing Adjust Enable | Enables you to manually set any of the memory timing parameters |
| TRCD | Indicates the delay between the ACTIVATE command (RAS) and the internal access to data (CAS) |
| TRAS | Indicates how long memory must wait after an ACTIVATE command before a PRECHARGE command can be issued to close the row |
| TRPPB | Row PRECHARGE time for a single bank |
| TWR | Specifies the amount of clock cycles needed to complete a WRITE before a PRECHARGE command can be issued |
| TRTP | Internal READ to PRECHARGE delay |
| TCCD | Minimum time between two READ/WRITE (CAS) commands (burst length / 2) |
| MWR2MWR | Masked WRITE to masked WRITE time |
| TRRD | Minimum time interval between two ACTIVATE commands to different banks |
| TRFC | Indicates how long memory must wait after a REFRESH command before an ACTIVATE command can be accepted by memory |
| TFAW | Specifies the period duration during which only four banks can be active |
| TZQLAT | ZQ calibration time from LATCH command to next allowed command |
| TMRR2WR | Mode register READ command to Write command time |
| TMRD | Minimum time between two MRS commands |
| TRPAB | Row PRECHARGE time for all banks |
| TRTW | READ to WRITE command delay |
| TDQSS | Describes skew between the output data strobe with respect to the memory clock for writes (DQS to CK) |
| TRD2PRE | READ to PRECHARGE time |
| TWR2PRE | WRITE to PRECHARGE time |
| TXP | Power-down exit latency to next valid command |
| TXPSR | Power-down exit latency to next self-refresh |
| **Power Down Settings[2]** | |
| Number of SCLK to enter Self-Refresh from no traffic | The memory controller puts the memory in self-refresh when there is no traffic for the specified number of SCLK cycles |
| Enable CLKOFF in Power Down | Specifies if the CK will be turned off after putting the memory in self-refresh. For 2-rank system, this occurs only when both ranks are in self-refresh. |
| **Periodic Event Setting Group** | |
| Refresh Period | Specifies the number of SCLK cycles between refresh commands |
| Number of Outstanding Refresh | Specifies the maximum number of outstanding refresh commands. Refer to the Auto Refresh Support section of this User Guide for more information. |
| ZQ Calibration Period | Indicates period for performing ZQ Calibration in seconds |
| ZQ Calibration Start to Latch | Indicates time from start to latch during ZQ Calibration in microseconds |
| Temperature Check Period | Indicates period for reading the temperature register (MR4) in LPDDR4 memory in seconds |

**Notes:**

1. The memory device timing parameters listed under the Memory Device Timing tab are defined according to the JESD209-4C SDRAM standard. Refer to the memory device data sheet for detailed descriptions and allowed values for these parameters.
2. This is visible only when the *Enable Power Down* is selected.

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### 3.2.3. Training Settings

This section describes the parameters available in the Training Settings tab of the IP parameter editor.

**Table 3.22. LPDDR4 Training Settings Attributes**

| Attribute | Selectable Values | Default | Dependency on Other Attributes |
|---|---|---|---|
| DDR Clock Delay Value | 0–20 | 0 | DDR Command Frequency!=800 MHz |
| | | 4 | DDR Command Frequency==800 MHz |
| DDR Clock Delay Value Incr/Decr | Checked, Unchecked | Checked | — |
| CS Delay Value | 0–20 | 0 | — |
| CS Delay Value Incr/Decr | Checked/Unchecked | Checked | — |
| Address Control Delay Value | 0–20 | 0 | — |
| Address Control Delay Value Incr/Decr | Checked, Unchecked | Unchecked | — |
| Memory CA_Vref Value for Rank0 | 0–114 | 25 | — |
| Memory CA_Vref Value for Rank1 | 0–114 | 25 | Enabled when Number of Ranks==2 |
| Memory DQ_Vref Value for Rank0 | 0–114 | 25 | — |
| Memory DQ_Vref Value for Rank1 | 0–114 | 25 | Enabled when Number of Ranks==2 |
| MC DQS Grp<0,1> Vref Value | 0–127 | 40 | — |
| MC DQS Grp<2,3> Vref Value | 0–127 | 40 | Enabled when DDR Bus Width=32 |
| MC DQS Grp<4,5,6,7> Vref Value | 0–127 | 40 | Enabled when DDR Bus Width=64 |

**Table 3.23. LPDDR4 MC I/O Settings Attributes**

| Attribute | Selectable Values | Default | Dependency on Other Attributes |
|---|---|---|---|
| CK/CS Slew Rate | Slow, Fast | Fast | — |
| Command Address Slew Rate | Slow, Fast | Fast | — |
| DQS Slew Rate | Slow, Fast | Fast | — |
| DQ/DMI Slew Rate | Slow, Fast | Fast | — |
| MC CA Output Impedance | 240 Ω, 120 Ω, 68 Ω, 60 Ω, 48 Ω, 40 Ω, 34 Ω | 34 Ω | — |
| MC DQ Output Impedance | 240 Ω, 120 Ω, 68 Ω, 60 Ω, 48 Ω, 40 Ω, 34 Ω | 34 Ω | — |
| MC ODT Value | 240 Ω, 120 Ω, 68 Ω, 60 Ω, 48 Ω, 40 Ω, 34 Ω | 48 Ω | — |

**Table 3.24. LPDDR4 Memory ODT Settings Attributes**

| Attribute | Selectable Values | Default | Dependency on Other Attributes |
|---|---|---|---|
| CA_ODT Value | Disable, RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, RZQ/6 | RZQ/2 | — |
| DQ_ODT Value | Disable, RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, RZQ/6 | RZQ/4 | — |
| SoC_ODT Value | Disable, RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, RZQ/6 | RZQ/6 | — |
| CK_ODT Override Enable | Checked, Unchecked | Unchecked | — |
| CS_ODT Override Enable | Checked, Unchecked | Unchecked | — |
| CA_ODT Override Disable | Checked, Unchecked | Unchecked | — |
| ODT-CS/CA/CLK Disable | Checked, Unchecked | Unchecked | — |
| Pull-Down Drive Strength | RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, RZQ/6 | RZQ/6 | — |

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**Table 3.25. LPDDR4 Training Settings Definitions**

| Attribute[1] | Description |
|---|---|
| **LPDDR4 Training Settings** | |
| DDR Clock Delay Value | Specifies the DDR clock delay so that the first DQS toggle is at CK = 0 during write leveling. It is recommended to increase this value if write leveling fails |
| DDR Clock Delay Value Incr/Decr | Specifies the adjustment direction<br>Checked: DDR Clock Delay Value is added to the ddr_ck_o signal<br>Unchecked: DDR Clock Delay Value is subtracted from the ddr_ck_o signal |
| CS Delay Value | Specifies the DDR CS delay value |
| CS Delay Value Incr/Decr | Specifies the adjustment direction<br>Checked: CS Delay Value is added to the ddr_cs_o signal<br>Unchecked: CS Delay Value is subtracted from the ddr_cs_o signal |
| Address Control Delay Value | Specifies the DDR address/control signals delay. It is recommended to increase this value if command bus training fails |
| Address Control Delay Value Incr/Decr | Specifies the adjustment direction.<br>Checked: Address Control Delay Value is added to the DDR address/control signals<br>Unchecked: Address Control Delay Value is subtracted from the DDR address/control signals |
| Memory CA_Vref Value for Rank<0,1> | Specifies the DRAM CA_Vref Value to be written to LPDDR4 DRAM's MR12 VR-CA and VREF(CA) for Rank0/Rank1. This should be set based on SI/PI simulation for the target board design.<br>Refer to the LPDDR4 JEDEC Standard for allowed values in MR12. |
| Memory DQ_Vref Value for Rank<0,1> | Specifies the DRAM DQ_Vref Value to be written to LPDDR4 DRAM's MR14 VR(DQ) and VREF(DQ) for Rank0/Rank1. When the register field TRN_OP_REG.mem_vref_training_en=0, this will be used as the final DRAM DQ Vref.<br>Refer to the LPDDR4 JEDEC Standard for allowed values in MR14. |
| MC DQS Grp<0,1,2,3,4,5,6,7> Vref Value | Specifies the MC DQ*Vref Value for each DQS group (depending on* DDR Bus Width) when DQ_Vref training is disabled by setting the register field TRN_OP_REG.mc_vref_training_en=0.<br>The theoretical mV value is: Vref decimal value × 5mV. |
| **LPDDR4 MC I/O Settings** | |
| CK/CS Slew Rate | Specifies the CK/CS driver strength |
| Command Address Slew Rate | Specifies the CA driver strength |
| DQS Slew Rate | Specifies the DQS driver strength |
| DQ/DMI Slew Rate | Specifies the DQ/DMI driver strength |
| MC CA Output Impedance | Memory controller CA I/O impedance to reach VDDQ threshold |
| MC DQ Output Impedance | Memory controller DQ I/O impedance to reach VDDQ threshold |
| MC ODT Value | Memory controller termination resistance value at FPGA |
| **LPDDR4 Memory ODT Settings** | |
| CA_ODT Value | Memory side CA ODT resistance value |
| DQ_ODT Value | Memory side DQ ODT resistance value |
| SoC_ODT Value | Memory controller ODT resistance value correlating to ZQ calibration |
| CK_ODT Override Enable | Overrides the default CK ODT value for the non-terminating rank when option is checked. Refer to MR22 in LPDDR4 device datasheet for more details |
| CS_ODT Override Enable | Overrides the default CS ODT value for the non-terminating rank when option is checked. Refer to MR22 in LPDDR4 device datasheet for more details |
| CA_ODT Override Disable | Disable termination for CA when option is checked. Refer to MR22 in LPDDR4 device datasheet for more details |
| ODT-CS/CA/CLK Disable | Disable ODT for CS/CA/CLK when option is checked |
| Pull-Down Drive Strength | Memory side pull-down drive strength value |

**Note:**

1. These attributes should only be modified when an error is encountered during LPDDR4 memory training.

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### 3.2.4. Example Design

This section describes the parameters available in the Example Design tab of the IP parameter editor. Use these options when implementing the LPDDR4 Example Design on a Lattice board for Avant-E/G/X70.

**Table 3.26. LPDDR4 Example Design Attributes**

| Attribute | Selectable Values | Default | Dependency on Other Attributes |
|---|---|---|---|
| Select Development Board | None, Avant-E_Evaluation_Board, Avant-E_Development_Board, Avant-G/X_Versa_Board | None | If Avant E/G/X70 device |
| | None | | If not Avant E/G/X70 device |
| Use internal OSC for Eval PLL Refclk | Checked, Unchecked | Checked | If Select Development Board == None |
| | | Unchecked | If Select Development Board != None |
| Eval PLL Refclk I/O Buffer Type | LVDS, SUBLVDS, SLVS, HSTL15_I, HSTL15D_I, LVSTL11D_I, LVTTL33, LVCMOS33, LVCMOS25, 'LVCMOS18', 'LVCMOS18H', 'HSTL15D_I', 'LVCMOS15', 'LVCMOS15H', 'LVCMOS12', 'LVCMOS12H', 'LVCMOS10H', 'LVCMOS10', 'LVCMOS10R' | Calculated | Available when Use internal OSC for Eval PLL Refclk is Unchecked<br>The default value is calculated based on the Select Development Board attribute |
| Eval PLL Refclk Frequency (MHz) | 50, 125 | 50 | If Select Development Board == None |
| | 125 | 125 | If Select Development Board != None |
| Eval Local Bus Clock Frequency (MHz) | 80, 250 | 250 | Available when Enable Local Bus Clock is Checked |

**Table 3.27. LPDDR4 Example Design Attribute Definitions**

| Attribute | Description |
|---|---|
| Select Development Board | Specifies the Lattice board where the LPDDR4 Example Design will be implemented. The pin assignments for the target board will be automatically added to the eval/constraint.pdc (see Table 7.2). When implementing the LPDDR4 Example Design to your board, select none. |
| Use internal OSC for Eval PLL Refclk | Specifies the source of the PLL reference clock in the LPDDR4 Example Design. Only 50 MHz and 125 MHz are currently available. If your board uses either of these frequencies, uncheck this option; otherwise, check this option |
| Eval PLL Refclk I/O Buffer Type | Specifies the I/O buffer type of the PLL reference clock for the LPDDR4 Example Design |
| Eval PLL Refclk Frequency (MHz) | Specifies the frequency of the PLL reference clock for the LPDDR4 Example Design |
| Eval Local Bus Clock Frequency (MHz) | Specifies the frequency of the local AXI4 bus clock for the LPDDR4 Example Design |

### 3.2.5. Bit Swizzle Settings

This section describes the attributes for swapping the DQ bits within the DQS group. This is only shown when you check the *Enable Bit Swizzle* attribute. Use this when swapping the DQ bits will help you improve the routing on the board.

Refer to Bit Swizzle section of DDR Memory PHY Module User Guide (FPGA-IPUG-02195) for more information about this feature.

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**Table 3.28. LPDDR4 Bit Swizzle Attributes**

| Attribute | Selectable Values | Default | Dependency on Other Attributes |
|---|---|---|---|
| **DQS0 Bit Swizzle** | | | |
| MC's DQ<00,01,02,03,04,05,06,07> connects to DRAM DQ | 0, 1, 2, 3, 4, 5, 6, 7 | 0/1/2/3/ 4/5/6/7 | If Enable Bit Swizzle is Checked |
| DQS0 DQ Bit Swizzle | Calculated | 0x76543210 | If Enable Bit Swizzle is Checked |
| **DQS1 Bit Swizzle** | | | |
| MC's DQ<08,09,10,11,12,13,14,15> connects to DRAM DQ | 8, 9, 10, 11, 12, 13, 14, 15 | 8/9/10/11/ 12/13/14/15 | If Enable Bit Swizzle is Checked |
| DQS1 DQ Bit Swizzle | Calculated | 0x76543210 | If Enable Bit Swizzle is Checked |
| **DQS2 Bit Swizzle** | | | |
| MC's DQ<16,17,18,19,20,21,22,23> connects to DRAM DQ | 0, 1, 2, 3, 4, 5, 6, 7 | 0/1/2/3/ 4/5/6/7 | If Enable Bit Swizzle is Checked and DDR Bus Width >= 32 |
| DQS2 DQ Bit Swizzle | Calculated | 0x76543210 | If Enable Bit Swizzle is Checked and DDR Bus Width >= 32 |
| **DQS3 Bit Swizzle** | | | |
| MC's DQ<24,25,26,27,28,29,30,31> connects to DRAM DQ | 8, 9, 10, 11, 12, 13, 14, 15 | 8/9/10/11/ 12/13/14/15 | If Enable Bit Swizzle is Checked and DDR Bus Width >= 32 |
| DQS3 DQ Bit Swizzle | Calculated | 0x76543210 | If Enable Bit Swizzle is Checked and DDR Bus Width >= 32 |
| **DQS4 Bit Swizzle** | | | |
| MC's DQ<32,33,34,35,36,37,38,39> connects to DRAM DQ | 0, 1, 2, 3, 4, 5, 6, 7 | 0/1/2/3/ 4/5/6/7 | If Enable Bit Swizzle is Checked and DDR Bus Width == 64 |
| DQS4 DQ Bit Swizzle | Calculated | 0x76543210 | If Enable Bit Swizzle is Checked and DDR Bus Width == 64 |
| **DQS5 Bit Swizzle** | | | |
| MC's DQ<40,41,42,43,44,45,46,47> connects to DRAM DQ | 8, 9, 10, 11, 12, 13, 14, 15 | 8/9/10/11/ 12/13/14/15 | If Enable Bit Swizzle is Checked and DDR Bus Width == 64 |
| DQS5 DQ Bit Swizzle | Calculated | 0x76543210 | If Enable Bit Swizzle is Checked and DDR Bus Width == 64 |
| **DQS6 Bit Swizzle** | | | |
| MC's DQ<48,49,50,51,52,53,54,55> connects to DRAM DQ | 0, 1, 2, 3, 4, 5, 6, 7 | 0/1/2/3/ 4/5/6/7 | If Enable Bit Swizzle is Checked and DDR Bus Width == 64 |
| DQS6 DQ Bit Swizzle | Calculated | 0x76543210 | If Enable Bit Swizzle is Checked and DDR Bus Width == 64 |
| **DQS7 Bit Swizzle** | | | |
| MC's DQ<56,57,58,59,60,61,62,63> connects to DRAM DQ | 8, 9, 10, 11, 12, 13, 14, 15 | 8/9/10/11/ 12/13/14/15 | If Enable Bit Swizzle is Checked and DDR Bus Width == 64 |
| DQS7 DQ Bit Swizzle | Calculated | 0x76543210 | If Enable Bit Swizzle is Checked and DDR Bus Width == 64 |

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**Table 3.29. LPDDR4 Bit Swizzle Attribute Definitions**

| Attribute | Description |
|---|---|
| **DQS<0,2,4,6> Bit Swizzle[1,2]** | |
| MC's DQ connects to DRAM DQ | Specifies how the DQ bits of the DQS groups 0, 2, 4, and 6 will be connected to the lower byte of the LPDDR4 DRAM channel on the board. You can swap around the bits within the DQS group (DQ byte). |
| DQS<0,2,4,6> DQ Bit Swizzle | This is the actual parameter used in MC's RTL. This is calculated based on the DQ connection settings. |
| **DQS<1,3,5,7> Bit Swizzle[1,2]** | |
| MC's DQ connects to DRAM DQ | Specifies how the DQ bits of the DQS groups 1 , 3, 5 and 7 will be connected to the upper byte of the LPDDR4 DRAM channel on the board. You can swap around the bits within the DQS group (DQ byte). |
| DQS<1,3,5,7> DQ Bit Swizzle | This is the actual parameter used in MC's RTL. This is calculated based on the DQ connection settings. |

**Notes:**

1. These DQS group pairs should be connected to the same DRAM channel: (DQS0, DQS1), (DQS2, DQS3), (DQS4, DQS5), and (DQS6, DQS7).
2. Swapping the DQS group with another DQS group is not yet supported.

The DDRPHY Hard IP connection to the I/O is a dedicated path. The Bit Swizzle feature will not affect the pin mapping in the Lattice Radiant software. This means the following:

- The Radiant **Report Browser** > **Place & Route Reports** -> **Signal/Pad** report will still show the dedicated pin locations.
- If you need to add the pin assignment constraint (ldc_set_location) in the Radiant project **Post-Synthesis Constraint Files**, you should still use the dedicated pin locations.

For consistency, ensure that your schematic shows the swizzled connection for cross-checking with the *Bit Swizzle* settings in the IP GUI.

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# 4. Signal Description

The input and output signals of the DDR Memory Controller IP are covered in this section. The signals available are based on the selected configuration of the Memory Controller IP.

## 4.1. Clock and Reset

**Table 4.1. Clock and Reset Port Definitions**

| Port Name | I/O | Width | Description |
|---|---|---|---|
| pll_refclk_i | In | 1 | PLL reference clock input. It is recommended to use 100 MHz for better clock performance. Refer to the *Design Rules and Guidelines* section of Avant High Speed IO and External Memory Interface User-Guide (FPGA-TN-02300) for more information. |
| pll_rst_n_i | In | 1 | PLL reset active low. The minimum reset pulse width is 5 µs.<br>This causes pll_lock_o to de-assert and sclk_o to stop. If you assert this signal, you should assert the main reset, rst_n_i as well. You can assert the rst_n_i at the same time as pll_rst_n_i or after pll_rst_n_i de-asserts. |
| pclk_i | In | 1 | Clock for APB interface, training CPU and control logic of the internal PLL. This clock is independent of sclk_o, since sclk_o stops during clock frequency changes.<br>Supports 50 MHz to 150 MHz in simulation, but the upper limit for implementation may be less than 150 MHz, depending on the Lattice Radiant timing analysis report. |
| preset_n_i | In | 1 | Asynchronous active low reset for APB interface. This reset must be de-asserted synchronous to pclk_i. |
| aclk_i | In | 1 | Clock for AXI4 interface.<br>The fmax is limited by the Lattice Radiant timing analysis report. |
| sclk_o | Out | 1 | System clock. This is ¼ of the DDR clock frequency and is the main clock of the Memory Controller IP. |
| rst_n_i | In | 1 | Asynchronous active low reset. When asserted, output ports, including the AXI4 Data Interface and the APB Configuration Interface and registers are forced to their reset values. The Memory Controller IP implements logic to de-assert the internal reset synchronous to the internal clocks (sclk_o, pclk_i and aclk_i) after rst_n_i de-asserts. After rst_n_i de-assertion, wait for a minimum of 5 pclk_i before accessing the registers.<br>If you assert this reset signal, you need to perform the full initialization and training as described in the Calibration section. |
| areset_n_i | In | 1 | Asynchronous active low reset for AXI4 interface.<br>This reset must be de-asserted synchronous to aclk_i.<br>This is only available when *Enable Local Bus Clock* attribute is checked. |

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## 4.2. Interrupts and Initialization/Training

This section describes the interface ports for interrupts and initialization/training control in the Memory Controller IP.

**Table 4.2. Interrupts and Initialization/Training Port Definitions**

| Port Name | I/O | Width | Description |
|---|---|---|---|
| irq_o | Out | 1 | Interrupt signal<br>Reset value is 1'b0 |
| init_start_i | In | 1 | Starts the memory initialization and training according to trn_opr_i.<br>This signal is available when *Enable APB interface* attribute is unchecked. |
| init_done_o | Out | 1 | Indicates completion of initialization and training and the memory is available for access through the data interface. |
| pll_lock_o | Out | 1 | PLL lock output indicating when PLL is locked.<br>Do not access the Memory Controller IP in any bus interface or init_start_i when the PLL is not locked. |
| trn_opr_i | In | 10 | Sets the Training Operation Register (TRN_OP_REG), which specifies the training steps to perform. Refer to the DDR Memory PHY Module User Guide (FPGA-IPUG-02195) for more details. |
| trn_err_o | Out | 1 | Indicates memory training has failed when asserted (1'b1) |

## 4.3. APB Configuration Interface

This section describes the configuration interface port when the *Enable APB interface* attribute is checked in the Memory Controller IP. Refer to the AMBA APB Protocol Specification for a description of these signals.

**Table 4.3. APB Interface Port Definitions**

| Port Name | I/O | Width | Description |
|---|---|---|---|
| apb_psel_i | In | 1 | APB Select signal<br>Indicates that the completer device is selected, and a data transfer is required |
| apb_paddr_i | In | 12 | APB Address signal |
| apb_pwdata_i | In | 32 | APB Write data signal<br>Bits [31:8] are not used |
| apb_pwrite_i | In | 1 | APB Direction signal<br>1 = Write, 0 = Read |
| apb_penable_i | In | 1 | APB Enable signal<br>Indicates the second and subsequent cycles of an APB transfer |
| apb_pready_o | Out | 1 | APB Ready signal<br>Indicates transfer completion. Completers use this signal to extend an APB transfer. Reset value is 1'b0. |
| apb_pslverr_o | Out | 1 | APB Error signal<br>Indicates a transfer failure. This signal is tied to 1'b0. |
| apb_prdata_o | Out | 32 | APB Read data signal |

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## 4.4. AXI4 Data Interface

This section describes the AXI4 data interface ports in the Memory Controller IP. Refer to the AMBA AXI Protocol Specification for a description of these signals. The transactions allowed on the AXI4 interface to the Memory Controller are described in Table 2.2.

**Table 4.4. AXI4 Interface Port Definitions**

| Port Name | I/O | Width | Description |
|---|---|---|---|
| axi_arid_i | In | AXI_ID_WIDTH | AXI4 read address channel: Read address ID signal |
| axi_araddr_i[1,2] | In | AXI_ADDR_WIDTH | AXI4 read address channel: Read address signal |
| axi_arlen_i | In | 8 | AXI4 read address channel: Burst length signal<br>Supports up to burst length 64 only, it is prohibited to issue more than this |
| axi_arsize_i | In | 3 | AXI4 read address channel: Burst size signal |
| axi_arburst_i | In | 2 | AXI4 read address channel: Burst type signal<br>Only INCR is supported |
| axi_arqos_i | In | 4 | AXI4 read address channel: Quality of service signal<br>This signal is currently unused |
| axi_arvalid_i | In | 1 | AXI4 read address channel: Read address valid signal |
| axi_arready_o | Out | 1 | AXI4 read address channel: Read address ready signal |
| axi_rid_o | Out | AXI_ID_WIDTH | AXI4 read data channel: Read ID tag signal |
| axi_rdata_o[1] | Out | AXI_DATA_WIDTH | AXI4 read data channel: Read data signal |
| axi_rresp_o | Out | 2 | AXI4 read data channel: Read response signal |
| axi_rlast_o | Out | 1 | AXI4 read data channel: Read last signal |
| axi_rvalid_o | Out | 1 | AXI4 read data channel: Read valid signal |
| axi_rready_i | In | 1 | AXI4 read data channel: Read ready signal |
| axi_awid_i | In | AXI_ID_WIDTH | AXI4 write address channel: Write address ID signal |
| axi_awaddr_i[1,2] | In | AXI_ADDR_WIDTH | AXI4 write address channel: Write address signal |
| axi_awlen_i | In | 8 | AXI4 write address channel: Burst length signal |
| axi_awsize_i | In | 3 | AXI4 write address channel: Burst size signal |
| axi_awburst_i | In | 2 | AXI4 write address channel: Burst type signal |
| axi_awqos_i | In | 4 | AXI4 write address channel: Quality of service signal |
| axi_awvalid_i | In | 1 | AXI4 write address channel: Write address valid signal |
| axi_awready_o | Out | 1 | AXI4 write address channel: Write address ready signal |
| axi_wdata_i[1] | In | AXI_DATA_WIDTH | AXI4 write data channel: Write data signal |
| axi_wstrb_i[1] | In | AXI_DATA_WIDTH/8 | AXI4 write data channel: Write strobe signal |
| axi_wlast_i | In | 1 | AXI4 write data channel: Write last signal |
| axi_wvalid_i | In | 1 | AXI4 write data channel: Write valid signal |
| axi_wready_o | Out | 1 | AXI4 write data channel: Write ready signal |
| axi_bid_o | Out | AXI_ID_WIDTH | AXI4 write response channel: Response ID tag signal |
| axi_bresp_o | Out | 2 | AXI4 write response channel: Write response signal |
| axi_bvalid_o | Out | 1 | AXI4 write response channel: Write response valid signal |
| axi_bready_i | In | 1 | AXI4 write response channel: Response ready signal |

**Notes:**

1. The bit width of axi_araddr_i/axi_rdata_o/axi_awaddr_i/axi_wdata_i/axi_wstrb_i are calculated based on the DDR density and DDR Bus Width attributes in Table 3.3.
2. Refer to the DDR Memory PHY Module User Guide (FPGA-IPUG-02195) for the address mapping.

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### 4.4.1. AXI4 Address Mapping for DDR4 mode

In DDR4 mode, the Bank Group is mapped within the burst address mapping so that sequential writes and sequential reads can be executed in the DDR side without gap. This causes the column address bits to split into two, namely, Column High and Column Low.

**Table 4.5. AXI4 Address Mapping for DDR4 mode**

| Memory Address | Size | Local Address Map | |
|---|---|---|---|
| Rank | If Number of Ranks == 2: RANKW = 1<br>If Number of Ranks == 1: Not available | Local address mapping within each rank remains the same | |
| Row | ROWW = refer to memory device data sheet | ROW_H = ROW_L + ROWW – 1<br>ROW_L = BANK_H + 1 | Addr[ROW_H: ROW_L] |
| Bank | BANKW = 2 | BANK_H = BANK_L + BANKW – 1<br>BANK_L = COL_H_H + 1 | Addr[BANK_H: BANK_L] |
| Column High | COLHW = 7 | COLH_H = COLH_L + COLHW – 1<br>COLH_L = BG_H + 1 | Addr[COLH_H: COLH_L] |
| Bank Group | BGW = 2 | BG_H = BG_L + BGW – 1<br>BG_L = COLL_H + 1 | Addr[BG_H: BG_L] |
| Column Low | COLLW = 3 | COLL_H = COLL_L + COLLW – 1<br>COLL_L = OFFSET_W | Addr[COLL_H: COLL_L] |
| Offset | If DDR Bus Width == 64: OFFSETW = 3<br>If DDR Bus Width == 32: OFFSETW = 2<br>If DDR Bus Width == 16: OFFSETW = 1 | N/A | |

**Table 4.6. AXI4 Address Mapping Example for DDR4 mode**

| Memory Address | Example User Value | Actual Line Size | Local Address Map |
|---|---|---|---|
| Offset | DDR Bus Width = 32 | 2 | *addr_i[1:0] |
| Column Low Width (COLLW) | 3 (Fixed for DDR4) | 3 | *addr_i[4:2] |
| Bank Group Width (BGW) | 2 (Fixed for DDR4) | 2 | *addr_i[6:5] |
| Column High Width (COLHW) | 7 (Fixed for DDR4) | 7 | *addr_i[13:7] |
| Bank Width (BANKW) | 2 (Fixed for DDR4) | 2 | *addr_i[15:14] |
| Row Width (ROWW) | *DDR Density* = 4 | 15 | *addr_i[30:16] |
| Rank Width (RANKW) | Number of Ranks = 1 | 0 | -- |
| Total Local Address Line Size | | 31 | *addr_i[30:0] |

### 4.4.2. AXI4 Address Mapping for LPDDR4 mode

**Table 4.7. AXI4 Address Mapping for LPDDR4 mode**

| Memory Address | Size | Local Address Map | |
|---|---|---|---|
| Rank | If Number of Ranks == 2: RANKW = 1<br>If Number of Ranks == 1: RANKW = 0 | Local address mapping within each rank remains the same | |
| Row | ROWW = refer to memory device data sheet | ROW_H = ROW_L + ROWW – 1<br>ROW_L = BANK_H + 1 | Addr[ROW_H: ROW_L] |
| Bank | BANKW = 3 | BANK_H = BANK_L + BANKW – 1<br>BANK_L = COL_H + 1 | Addr[BANK_H: BANK_L] |
| Column | COLW = 10 | COL_H = COL_L + COLW – 1<br>COL_L = OFFSET_W | Addr[COL_H: COL_L] |
| Offset | If DDR Bus Width == 64: OFFSETW = 3<br>If DDR Bus Width == 32: OFFSETW = 2<br>If DDR Bus Width == 16: OFFSETW = 1 | N/A | |

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**Table 4.8. AXI4 Address Mapping Example for LPDDR4 mode**

| Memory Address | Example User Value | Actual Line Size | Local Address Map |
|---|---|---|---|
| Offset | *DDR Bus Width* = 32 | 2 | *addr_i[1:0] |
| Column Width (COLW) | 10 (Fixed for LPDDR4) | 10 | *addr_i[11:2] |
| Bank Width (BANKW) | 3 (Fixed for LPDDR4) | 3 | *addr_i[14:12] |
| Row Width (ROWW) | *DDR Density* = 4 | 15 | *addr_i[29:15] |
| Rank Width (RANKW) | Number of Ranks = 1 | 0 | -- |
| Total Local Address Line Size | | 30 | *addr_i[29:0] |

# 4.5. Memory Interface Signals

## 4.5.1. DDR4 Memory Interface

This section describes the interface ports for DDR4 SDRAM.

**Table 4.9. DDR4 Interface Port Definitions**

| Port Name | I/O | Width | Description |
|---|---|---|---|
| ddr_ck_o[1,2] | Out | CK_WIDTH | DDR4 CK signal |
| ddr_cke_o[1,2] | Out | CK_WIDTH | DDR4 CKE signal |
| ddr_cs_o[1,2] | Out | CS_WIDTH | DDR4 CS signal |
| ddr_ca_o[2] | Out | CA_WIDTH | DDR4 CA signal |
| ddr_we_n_o[2] | Out | 1 | DDR4 WE signal |
| ddr_cas_n_o[2] | Out | 1 | DDR4 CAS signal |
| ddr_ras_n_o[2] | Out | 1 | DDR4 RAS signal |
| ddr_act_n_o[2] | Out | 1 | DDR4 ACT_n signal |
| ddr_ba_o[2] | Out | BANK_WIDTH | DDR4 BA signal |
| ddr_bg_o[2] | Out | BG_WIDTH | DDR4 BG signal |
| ddr_odt_o[2] | Out | ODT_WIDTH | DDR4 ODT signal |
| ddr_reset_n_o[2] | Out | 1 | Memory reset signal |
| ddr_dq_io[1] | In/Out | BUS_WIDTH | DDR4 DQ signal |
| ddr_dqs_io[1] | In/Out | DQS_WIDTH | DDR4 DQS signal |
| ddr_dmi_io[1] | In/Out | DQS_WIDTH | DDR4 DMI signal |

**Notes:**

1. The bit width of SDRAM Memory Interface signals is defined based on the attributes listed in Table 3.3.
2. For component, the command, address and control signals should be terminated to VTT on the board. This is not needed for UDIMM because it already has the termination within UDIMM.

## 4.5.2. LPDDR4 Memory Interface

This section describes the interface ports for LPDDR4 SDRAM.

**Table 4.10. LPDDR4 Interface Port Definitions**

| Port Name | I/O | Width | Description |
|---|---|---|---|
| ddr_ck_o[1] | Out | CK_WIDTH | LPDDR4 CK signal |
| ddr_cke_o[1] | Out | CK_WIDTH | LPDDR4 CKE signal |
| ddr_cs_o[1] | Out | CS_WIDTH | LPDDR4 CS signal |
| ddr_ca_o | Out | 6 | LPDDR4 CA signal |
| ddr_reset_n_o | Out | 1 | Memory reset signal |
| ddr_dq_io[1] | In/Out | BUS_WIDTH | LPDDR4 DQ signal |
| ddr_dqs_io[1] | In/Out | DQS_WIDTH | LPDDR4 DQS signal |
| ddr_dmi_io[1] | In/Out | DQS_WIDTH | LPDDR4 DMI signal |

**Note:**

1. The bit width of the SDRAM Memory Interface signal is defined based on the attributes listed in Table 3.15.

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# 5. Register Description

The Memory Controller IP contains user-accessible registers. For a description of these registers, refer to section 5 of the DDR Memory PHY Module User Guide (FPGA-IPUG-02195).

## 5.1. ECC Specific Registers

When ECC feature is enabled, the following additional registers are accessible.

**Table 5.1 ECC Related Registers**

| Register Offset | Bits | Register Field Name | Access Type | Description |
|---|---|---|---|---|
| 0x210 | | **INT_STATUS_REG** | | **Interrupt Status Register** |
| | 3 | Uncorrectable error detected | WR1C | Indicator that uncorrectable error(s) has occurred and exceeds Error Count Interrupt Threshold.<br>When set, all the UE ECC status registers are cleared |
| | 2 | Correctable error detected | WR1C | Indicator that correctable error(s) has occurred and exceeds Error Count Interrupt Threshold.<br>When set, all the CE ECC status registers are cleared. |
| 0x214 | | **INT_ENABLE_REG** | **RW** | **Interrupt Enable Register** |
| | 3 | Uncorrectable error interrupt enable[1] | | Enables Uncorrectable ECC Error (UE) Interrupt. |
| | 2 | Correctable error interrupt enable[1] | | Enables 1-bit Correctable ECC Error (CE) Interrupt. |
| 0x2A0 | | **ECC_CONTROL_REG** | | |
| | 0 | Enable Correctable error logging[2] | RW | Enables the correctable error logging in ECC_STATUS registers. |
| | 1 | Correctable error log selection | RW | Controls if the ECC_STATUS will log the First Error (0) or Last Error (1) location. |
| | 2 | Correctable error log “Partial Write” disable | RW | Disables checking for reads initiated during partial writes. |
| | 9:3 | Correctable error count Interrupt Threshold | RW | Controls the correctable errors count before an interrupt is raised. |
| | 15:10 | RSVD | RO | Reserved |
| | 16 | Enable Uncorrectable error logging[2] | RW | Enables the Uncorrectable error logging in ECC_STATUS registers. |
| | 17 | Uncorrectable error log Selection | RW | Controls if the ECC_STATUS will log the First Error (0) or Last Error (1) location. |
| | 18 | Uncorrectable error log “Partial Write” disable | RW | Disables checking for reads initiated during partial writes. |
| | 25:19 | Uncorrectable error count Interrupt Threshold | RW | Controls the uncorrectable errors count before an interrupt is raised. |
| | 31:26 | RSVD | RO | Reserved |
| 0x2A4 | | **ECC_STATUS1_REG** | | |
| | 7:0 | Correctable Error phase location | RO | First/Last Single-Error Location [phase]<br>Note: Phase refers to which phase of the BL8. |
| | 15:8 | Correctable Error Count | RO | Error Count |
| | 23:16 | Uncorrectable Error phase location | RO | First/Last Uncorrectable-Error Location [phase]<br>Note: Phase refers to which phase of the BL8. |
| | 31:24 | Uncorrectable Error Count | RO | Error Count |

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| Register Offset | Bits | Register Field Name | Access Type | Description |
|---|---|---|---|---|
| 0x2A8 | | **ECC_STATUS2_REG** | | |
| | 7:0 | Correctable Error byte location. | RO | Correctable error byte location [OR of all phase]<br>Note: This is the location of the x8 that has the error. |
| | 14:8 | RSVD | RO | Reserved |
| | 15:15 | Correctable Error type | RO | Correctable Error type. This determines whether an error occurs during a Read or Partial Write<br>(0 = Read, 1 = Partial Write) |
| | 30:16 | RSVD | RO | Reserved |
| | 31 | Uncorrectable Error type | RO | Uncorrectable Error type. This determines whether an error occurs during a Read or Partial Write<br>(0 = Read, 1 = Partial Write) |
| 0x2AC | | **ECC_STATUS3_REG** | | |
| | 31:0 | AXI-based address log of Correctable Error | RO | AXI address of location of correctable error logged. |
| 0x2B0 | | **ECC_STATUS4_REG** | | |
| | 31:0 | AXI-based address log of Uncorrectable Error | RO | AXI address of location of uncorrectable error logged. |

**Notes:**
1. Enable this only after training.
2. Enable this only after training to avoid excessive error logging during training.

When ECC is enabled, you must implement the following software flow to handle a correctable error.

1. Enable the correctable error log after training is complete.
   a. INT_STATUS_REG[2] = 1 (valid after ECC_CONTROL_REG[0]=1)
   b. INT_ENABLE_REG[2] = 1 (enables IRQ generation)
   c. ECC_CONTROL_REG[0] = 1 (to enable actual correction)
   d. ECC_CONTROL_REG[9:3] = N (set up threshold for interrupt)
2. An interrupt is triggered when a correctable error exceeds the configured threshold.
   a. Halt ongoing traffic to avoid inaccurate status-register readings.
   b. Read the ECC_STATUS1/ECC_STATUS2 registers.
   c. Perform any required diagnostics.
      i. Read the ECC_STATUS1_REG to determine the number of accumulated errors that have occurred.
   d. To determine the DRAM error location:
      i. Read the ECC_STATUS3_REG to obtain the AXI address.
      ii. Read the ECC_STATUS1_REG error-phase field to obtain the 1-hot column-offset value, which indicates the BL# within the BL8 where the error occurred.
      iii. Read the ECC_STATUS2_REG.ce_bloc field to obtain the 1-hot error-byte location within the x64 (applicable only to correctable errors under the SECDED scheme).
      iv. For a single error, determine the error location as follows (assuming a single-rank x64 configuration):

```
row       = ce_err_addr[AXI_ADDR_WIDTH-1: (bl8_base+11) ];
bank      = ce_err_addr  [ (bl8_base+9) +:1];
col       = {ce_err_addr [ ([bl8_base+2)  +: 7] , log2(ce_err_phase) }
bankgrp   = ce_err_addr  [ (bl8_base)     +: 1]
byte(x8)  = $clog2(ce_err_byte)
bl8_base= log2(DDR_WIDTH)
```

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**Note:** When more than one correctable error occurs within the same BL8, it is counted as single error. In this case, the phase and byte location information becomes ambiguous; for example, error_phase[1:0] = 11 and error_byte[1:0] = 11 could correspond to col0-byte0, col1-byte1, col0-byte1, or col1-byte0 (any of the two combinations).

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# 6. Memory Controller Example Design

This section describes the Memory Controller Example Design, which you can use for synthesis and simulation after generating the IP.

## 6.1. Overview

Table 6.1 summarizes the IP parameter configurations in the Memory Controller Example Design. To generate the Memory Controller IP core, refer to the Designing and Simulating the IP section of this user guide.

**Table 6.1. Supported Example Design Configurations**

| Attribute | Supported Setting |
|---|---|
| I/O Buffer Type | All |
| DDR Command Frequency | All |
| Enable Power Down | Checked, Unchecked |
| Enable DBI | Checked, Unchecked |
| PLL Reference Clock from Pin | Checked, Unchecked |
| DDR Bus Width | 16, 32, 64 |
| Local Data Bus Type | AXI4 |
| ID Width | All |
| Number of Outstanding Writes/Reads | All |
| Write/Read Ordering Queues | All |
| Enable Local Bus Clock | Checked, Unchecked |
| Enable APB interface | Checked, Unchecked |
| Memory Device Timing Tab[1] | All |
| Training Settings Tab[1] | All |

**Note:**

1. The DDR Clock Delay Value and Address Control Delay Value are not supported/reflected in Memory Controller Simulation Example Design. All other configurable attributes are supported in the Memory Controller Example Design.

## 6.2. Synthesis Example Design

After generating the DDR Memory Controller IP, you can access a synthesizable example design. This design includes a test program for evaluating the Memory Controller IP on hardware. Figure 6.1 represents a block diagram of the Memory Controller Example Design.

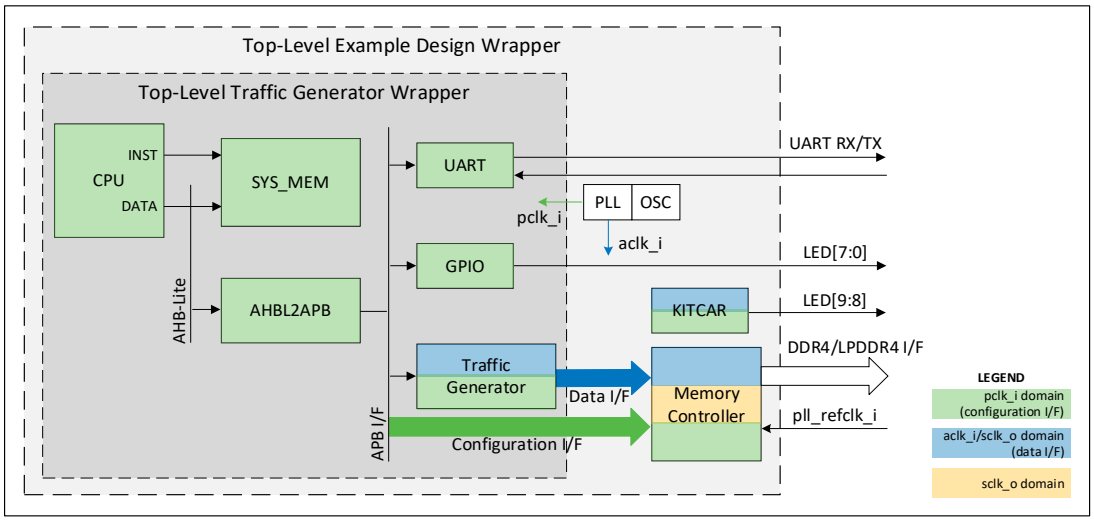



**Figure 6.1. Synthesis Example Design**

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The main blocks that make up the synthesizable example design include the following:

- **RISC-V CPU subsystem** – handles initialization and training of the DDR4/LPDDR4 interface and performs data access checks.
- **System Memory (SYS_MEM)** – stores the instruction code for the example design test program.
- **AHBL2APB bridge** – converts the CPU data interface (AHB-Lite) to the configuration interface (APB).
- **UART block** – allows you to interface with the test program and prints out results through a serial terminal connection.
- **GPIO block** – allows you to verify the result of the DDR4/LPDDR4 training sequences and the functionality of pclk_i and aclk_i clock signals.
- **Traffic generator block** – implements a series of pseudo-random (PRBS) writes and reads, and compares the read data to the expected data, displaying the result over a UART connection.
- **Memory Controller IP** – provides an interface to external DDR4/LPDDR4 memory to issue reads and writes.
- **Oscillator (OSC)** – generates a 50 MHz clock for the PLL.
- **PLL** – takes the oscillator output as an input reference clock to the PLL. The PLL generates both the configuration interface clock (pclk_i = 100 MHz) and the user data interface AXI clock (aclk_i = 250 MHz).

The synthesizable example design includes a test program stored in system memory, fetched by the CPU instruction port. The CPU data port accesses system memory and connects to Configuration Set Registers (CSRs), UART, GPIO, traffic generator, and Memory Controller. The test program associated with the example design performs the following tasks:

- Waits for user input over a serial terminal connection upon asserting the reset signal: rstn_i
- Configures the Memory Controller to perform a complete reset, initialization, and training of the DDR4/LPDDR4 interface.

If data rate ≤ 1,333 Mbps : TRN_OP_REG = 0x0DF during training

If data rate in [1,600 Mbps, 1,866 Mbps]: TRN_OP_REG = 0x1DF during training

If data rate ≥ 2,133 Mbps: TRN_OP_REG = 0x3DF during training

- Performs a series of loop-back data access checks
- Calculates the performance of the DDR4/LPDDR4 interface

The top-level example design wrapper file, eval_top.sv, provides ports for a PLL reference clock, DDR4/LPDDR4 interface, UART interface, and a 10-bit LED output. LED[7:0] corresponds to bits STATUS_REG[8:1], whereas toggling on LED[8] indicates aclk_i is functioning and toggling on LED[9] indicates pclk_i is functioning. For information on the example design test program and instructions on generating and performing hardware evaluation of the Memory Controller Example Design, refer to the Designing and Simulating the IP section of this user guide.

## 6.3. Simulation Example Design

The simulation example design is similar to the synthesizable example design, apart from the following changes:

- Disables UART connection
- External DDR4/LPDDR4 memory is replaced with DDR4/LPDDR4 memory model

The UART connection is disabled in simulation since it takes a long time to simulate. The DDR4/LPDDR4 memory model allows simulation of user-initiated operations to DDR4/LPDDR4 SDRAM. For instructions on simulating the Memory Controller, including the example design, refer to the Designing and Simulating the IP section of this user guide.

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### 6.3.1. DDR4

Table 6.2 summarizes the simulation runtime of the DDR4 Memory Controller for various configurations.

**Table 6.2. DDR4 Simulation Runtime Summary**

| DDR4 Configuration | Typical Initialization Time | Typical Training Time |
|---|---|---|
| x32, 1,066 MHz (single rank) | 46.014 µs | 30.753 µs |
| x16, 933 MHz (single rank) | 48.289 µs | 30.853 µs |
| x32, 933 MHz (single rank) | 48.169 µs | 30.853 µs |
| x64, 933 MHz (single rank) | 47.899 µs | 30.853 µs |
| x16, 800 MHz (single rank) | 50.807 µs | 35.475 µs |
| x32, 666 MHz (single rank) | 55.387 µs | 37.278 µs |
| x64, 666 MHz (single rank) | 55.087 µs | 37.278 µs |
| x16, 1,066 MHz (dual rank) | 46.134 µs | 60.735 µs |

Initialization time is measured from the moment the CPU and Controller Engine are pulled out of reset (RESET_REG) to the assertion of the DDR4 Clock Enable signal (ddr_cke_o). Training time is measured from the ddr_cke_o assertion to the assertion of init_done_o, indicating the completion of the initialization and training sequence. For more details on the initialization and training sequences, refer to the Calibration section of this user guide.

### 6.3.2. LPDDR4

Table 6.3 summarizes the simulation runtime of the LPDDR4 Memory Controller for various configurations.

**Table 6.3. LPDDR4 Simulation Runtime Summary**

| LPDDR4 Configuration | Typical Initialization Time | Typical Training Time |
|---|---|---|
| x32, 1,066 MHz (single rank) | 53.019 µs | 102.459 µs |
| x16, 933 MHz (single rank) | 54.281 µs | 106.248 µs |
| x32, 933 MHz (single rank) | 54.311 µs | 106.998 µs |
| x64, 933 MHz (single rank) | 54.191 µs | 108.468 µs |
| x16, 800 MHz (single rank) | 54.981 µs | 109.709 µs |
| x32, 666 MHz (single rank) | 58.288 µs | 114.854 µs |
| x64, 533 MHz (single rank) | 63.128 µs | 128.906 µs |
| x16, 1,066 MHz (dual rank) | 52.989 µs | 162.369 µs |

Initialization time is measured from the moment the CPU and Controller Engine are pulled out of reset (RESET_REG) to the assertion of the LPDDR4 Clock Enable signal (ddr_cke_o). Training time is measured from the ddr_cke_o assertion to the assertion of init_done_o, indicating the completion of the initialization and training sequence. For more details on the initialization and training sequences, refer to the Calibration section of this user guide.

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# 7. Designing and Simulating the IP

This section describes the steps required within Lattice Radiant software to configure and generate the DDR Memory Controller IP. It also provides information on the design implementation and hardware evaluation of the synthesizable example design. The screenshots shown are for reference only and may vary depending on the IP or software version being used.

## 7.1. Generating the IP

This section describes the steps required to create, configure, and generate an instance of the DDR Memory Controller IP.

### 7.1.1. Creating a Lattice Radiant Project

To generate an instance of the Memory Controller IP, you must first create a Lattice Radiant project.

1. Launch the Lattice Radiant software and select **File > New > Project**. This action opens the **New Project** dialog box. Click **Next**.

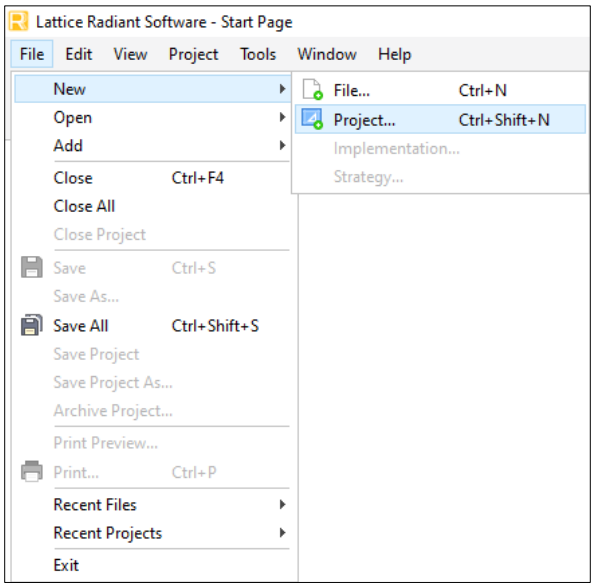



**Figure 7.1. Creating a New Lattice Radiant Project**

2. Specify a name (<project_name>) for the Lattice Radiant project, a directory (<project_directory>) to store the project files, and a top-level design implementation name (<top_level_instance_name>). Click **Next** twice.

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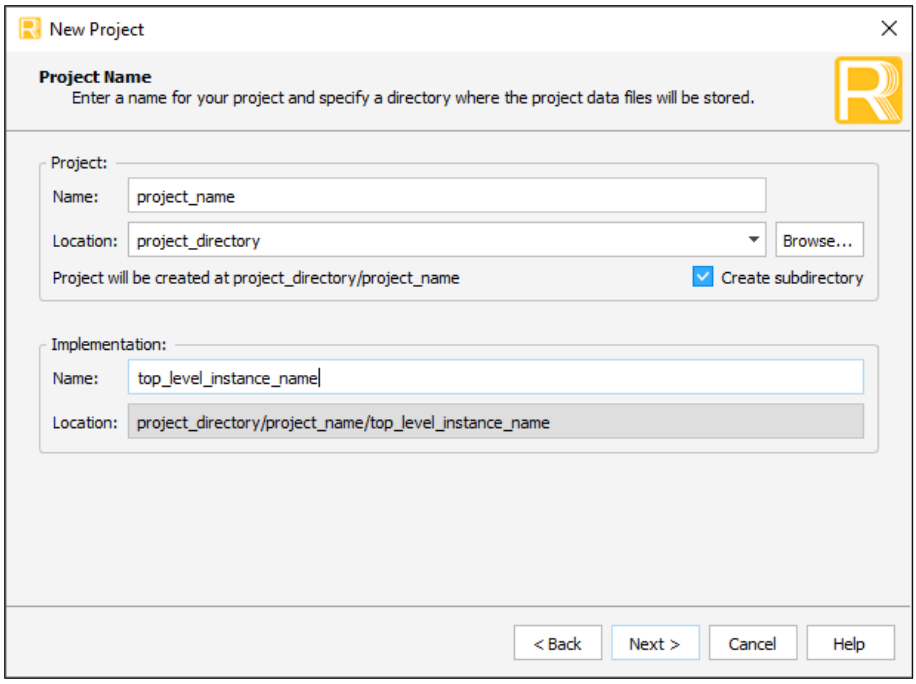



**Figure 7.2. New Project Settings**

3. Under **Family**, select **Avant**. Under **Device, Package, Operating Condition, and Performance Grade**, make the appropriate selections representative of the selected device part number. Click **Next**.

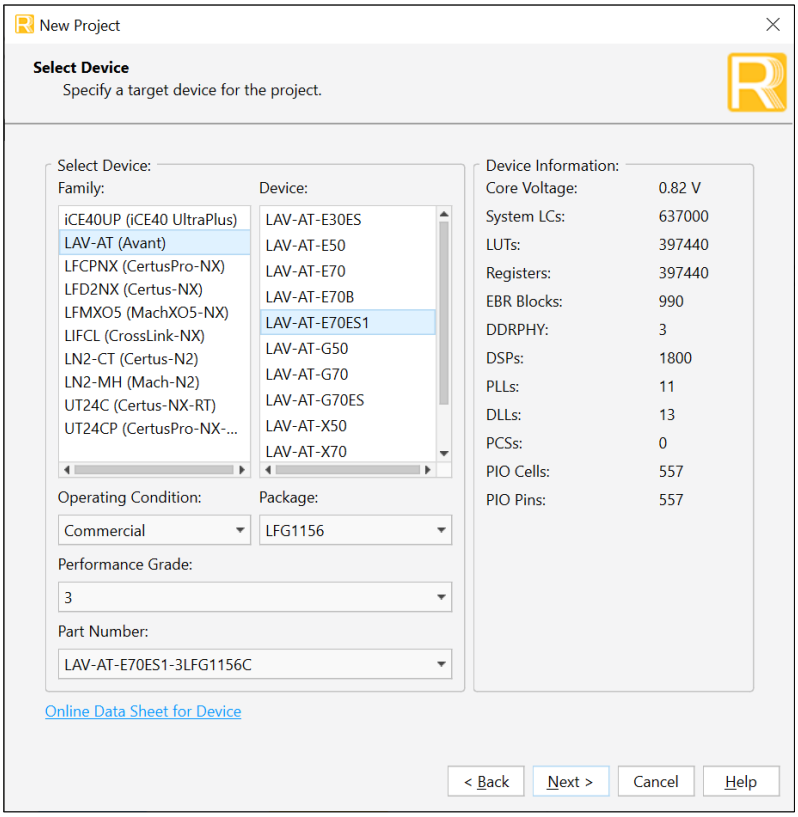



**Figure 7.3. Project Device Settings**

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4. Specify the desired synthesis tool for the implementation of the Lattice Radiant project. Click **Next** and **Finish**.

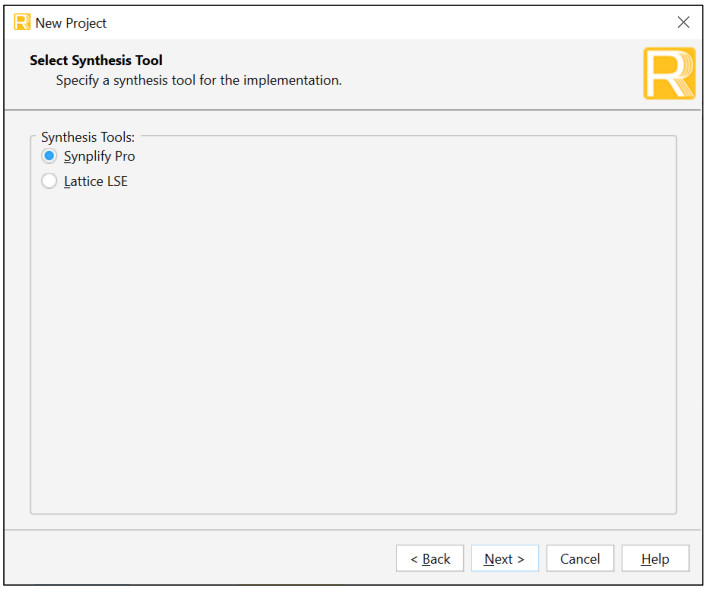



**Figure 7.4. Project Synthesis Tool Selection**

### 7.1.2. Configuring and Generating the IP

The following steps illustrate how to generate the Memory Controller IP core in Lattice Radiant software.

1. Under the **IP Catalog** (Tools > IP Catalog), locate and double-click on the desired Memory Controller IP listed under **IP > Processors_Controllers_and_Peripherals**.
   a. If no Memory Controller IPs are installed on the system, select the **IP on Server** tab within the IP Catalog.
   b. Click the **Download from Lattice IP Server** icon next to the desired Memory Controller IP for installation. This will open an **IP License Agreement** dialog box.
   c. Click **Accept**, then click on the **Refresh IP Catalog** icon.
   d. Locate the installed Memory Controller IP under the **IP on Local** tab within the IP Catalog and double-click.
      - IP core v2.x.x = Memory Controller (DDR4/LPDDR4 mode)
2. The **Module/IP Block Wizard** dialog box opens. Provide a name (<instance_name>) and directory (<instance_directory>) for the Memory Controller IP, where the default directory is set to <project_directory>/<project_name>. Click **Next**.

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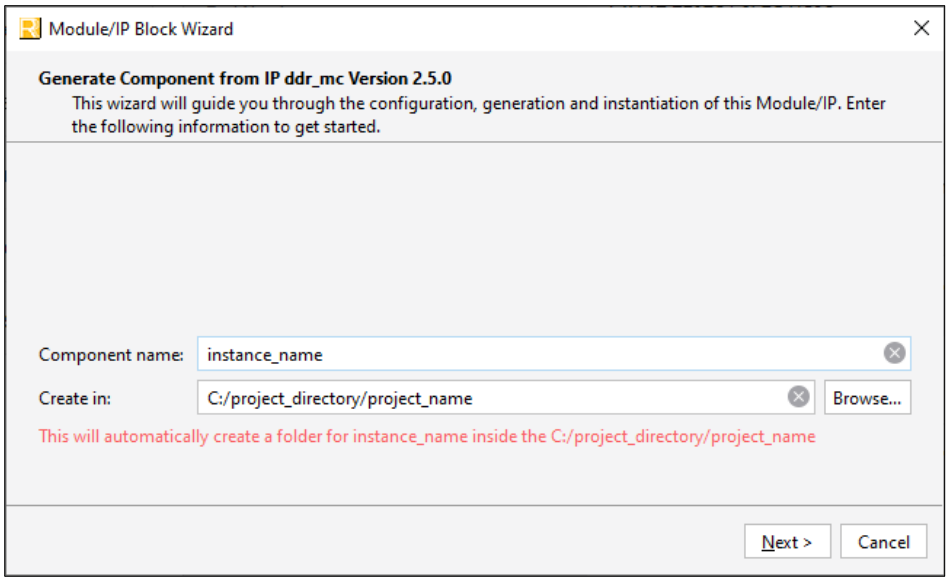



**Figure 7.5. IP Instance Settings**

3. The Memory Controller IP editor contains multiple tabs that need to be configured according to the desired DDR4/LPDDR4 memory interface implementation. The following table provides high-level guidance for configuring the tabs in the Memory Controller IP editor. For detailed information on the individual attributes, refer to the IP Parameter Description section of this user guide.

**Table 7.1. Memory Controller Attribute Guidelines**

| Memory Controller IP Attribute Tab | Guidelines |
|---|---|
| **DDR4** | |
| General | • Ensure that the Memory clock frequency (*DDR Command Frequency*) is entered correctly.<br>• Refer to the datasheet for the selected DDR4 memory device to ensure the channel density (*DDR Density per Channel*) is set correctly. |
| Memory Device Timing | Refer to the datasheet for the selected DDR4 memory device to modify the default timing parameters as needed. |
| Training Settings | • You should perform signal integrity analysis with the system IBIS model, using a tool such as HyperLynx, to determine the optimal I/O and ODT settings for custom boards.<br>• Modify the DDR Clock Delay value only if an error occurs during write leveling.<br>• Modify the Address Control Delay value only if an error occurs during command bus training. |
| **LPDDR4** | |
| General | • Ensure that the Memory clock frequency *(DDR Command Frequency)* is entered correctly.<br>• Refer to the datasheet for the selected LPDDR4 memory device to ensure the channel density (*DDR Density per Channel*) is set correctly. |
| Memory Device Timing | Refer to the datasheet for the selected LPDDR4 memory device to modify the default timing parameters as needed. |
| Training Settings | • You should perform signal integrity analysis with system IBIS model, using a tool such as HyperLynx, to determine the optimal I/O and ODT settings for custom boards.<br>• Modify the DDR Clock Delay value only if an error occurs during write leveling.<br>• Modify the Address Control Delay value only if an error has occurred during command bus training. |

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4. Click **Generate**. The Check Generating Result dialog box opens, showing design block messages and results as shown in Figure 7.6. Click **Finish**.

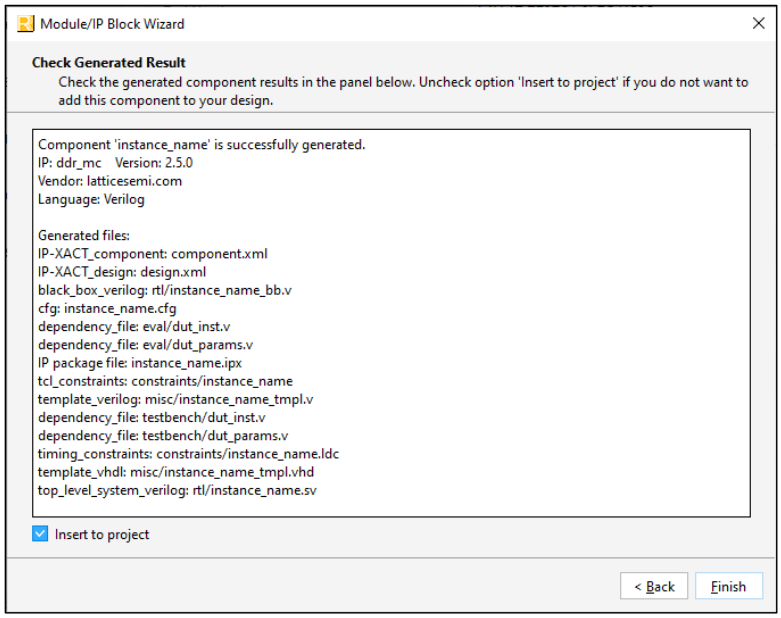



**Figure 7.6. IP Generation Result**

5. All the generated files are placed under the <instance_directory>/<instance_name> directory path. The generated files in the <instance_directory>/<instance_name> directory are listed in the following table.

**Table 7.2. Generated File List**

| File Name | Description |
|---|---|
| component.xml | Contains the ipxact:component information of the IP. |
| design.xml | Lists the set parameters of the IP in IP-XACT 2014 format. |
| <instance_name>.cfg | Lists only the configured/changed parameter values set during IP configuration. |
| <instance_name>.ipx | Lists the files associated with IP generation. |
| constraints/<instance_name>.ldc | Defines the I/O standard for DDR4/LPDDR4 memory interface signals. |
| constraints/constraint.sdc | Pre-Synthesis and Pre-Map constraints for the IP. |
| eval/apb2init.sv | Implements handshaking between APB accesses and internal RISC-V CPU for initialization of DDR4/LPDDR4 memory in the Memory Controller Example Design. |
| eval/assign_pins.py | Add the pin assignment to eval constraint.pdc based on the *Select Development Board* settings. |
| eval/async_reset_sync_deassert.v | Synchronize the reset de-assertion to the rising edge of the clock. |
| eval/blink_led.v | Drives LEDs on and off to indicate that internal clocks (pclk and aclk_i) are active in the Memory Controller Example Design. |
| eval/clock_constraint.sdc | Pre-synthesis constraint for setting the PLL reference clock frequency of the Memory Controller Example Design. |
| eval/constraint.pdc | Post-synthesis constraints for the Memory Controller Example Design. When the attribute Select Development Board is set (not None) in the IP GUI, this file will contain the pin assignments for the target Lattice board. |
| eval/dut_inst.v | Instantiation of generated IP core in eval_top.sv for the Memory Controller Example Design. |
| eval/dut_params.v | Defines local parameters for eval_top based on parameter values set during IP configuration for the Memory Controller Example Design. |
| eval/eval_top.sv | Top-level RTL file for the Memory Controller Example Design. |

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| File Name | Description |
|---|---|
| eval/measure_trn.sv | May be used to measure the training time on silicon/board and observe the result through Reveal tool. |
| eval/pll0.v | PLL is responsible for generating APB clock (pclk) and AXI4 (aclk_i) in the Memory Controller Example Design. |
| eval/pll0_refclk125.v | |
| eval/select_protocol.py | Script that defines DDR4/LPDDR4 protocol for eval_top and tb_top files in the Memory Controller Example Design. |
| eval/axi_bridge/ | Contains RTL for AXI bus interface to native interface. |
| eval/traffic_gen/ | Contains RTL files for the Memory Controller Example Design. |
| misc/<instance_name>_tmpl.v<br>misc/<instance_name>_tmpl.vhd | These files provide instance templates for the IP core. |
| rtl/<instance_name>.sv | Example RTL top-level file that instantiates the IP core. |
| rtl/<instance_name>_bb.v | Example synthesizable RTL black box file that instantiates the IP core. |
| testbench/debug_c_code.sv | For internal debugging use only. |
| testbench/delay_1dir.sv | |
| testbench/dqs_grp_delay.sv | |
| testbench/dq_bit_swizzle.vh | Specifies the MC to DRAM connection based on the Bit Swizzle settings. |
| testbench/dut_inst.v | Template instance files. |
| testbench/dut_params.v | List of parameters based on user IP configurations. |
| testbench/tb_top.sv | Top level testbench file. |
| testbench/ddr4/ | Contains DDR4/LPDDR4 memory model and instances for simulation. |
| testbench/lpddr4/ | |

## 7.2. Design Implementation

This section outlines the steps to properly run a Memory Controller for Avant IP design on hardware.

### 7.2.1. Pin Placement

Typically, all external memory interfaces require the following FPGA resources:

- Data, data mask, and data strobe signals
- Command, address, and control signals
- PLL and clock network signals
- RZQ signals
- Other FPGA resources

In Lattice Avant FPGA devices, the DDRPHY supports external memory interfaces. Each DDRPHY consists of three High Performance I/O (HPIO) banks, labeled as HIGHSPEED in the device pinout tables. Since Lattice Avant devices leverage a hardened PHY, the external memory interface pinouts are in fixed locations. Each pin location is specified under DDRPHY in the device pinout tables. Dedicated clock routing within HPIO banks is represented as PLL or PCLK, and dedicated reference voltage pins are represented as VREF in the device pinout tables. Refer to the Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300) and Pinout files located on the Avant-E, Avant-G, and Avant-X web pages.

Observe the following guidelines when placing pins for external memory interfaces:

- Ensure that pins for external memory interfaces reside within a DDRPHY.
- You must assign the input reference clock to the PLL to use dedicated clock routing (PLL or PCLK). Place the input reference clock on the pin closest to the dedicated PLL within each DDRPHY (labeled as PLL under DDRPHY in device pinout tables). This ensures better performance by minimizing jitter/routing.

Always test proposed pinouts in Lattice Radiant software with the correct I/O standards before finalizing. Note that unused pins within a DDRPHY can be used as general-purpose I/O under certain conditions. Refer to the Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300) for more details.

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### 7.2.2. Constraints

To ensure proper design coverage and hardware functionality, you must include the following necessary constraints in the Memory Controller for the Avant IP project.

**Table 7.3. Project Constraints**

| File Name | Description | Action Required |
|---|---|---|
| Memory Controller IP LDC file: constraints/<instance_name>.ldc | Sets the I/O type for each of the ports necessary to interface with the DDR4/LPDDR4 SDRAM | No. These constraints are automatically propagated |
| Memory Controller IP SDC file: constraints/constraint.sdc | Pre-synthesis and pre-map IP timing constraints | No. These constraints are automatically propagated |
| Clock Constraint SDC file: eval/clock_constraint.sdc | Contains an example constraint for the input PLL reference clock | Yes – you need to include a create_clock constraint based on the frequency of the input PLL reference clock. This should be placed in a user-created SDC file |
| Example Design PDC file: eval/constraint.pdc | Contains generated clock uncertainty constraints and example design constraints based on IP configuration | Yes – you need to copy the clock uncertainty constraints listed in this file directly into your top-level PDC file. You need to copy the example design constraints to run the LPDDR4/DDR4 memory Controller Example Design |

The Memory Controller IP constraints do not define the input and output delay on the DDR I/O since the routing from the DDRPHY primitive to/from the I/O is a dedicated path. Additionally, the Memory Controller calibration sequence compensates for the controller to DRAM end-to-end skew, making it unnecessary to specify I/O timing constraints by design.

#### 7.2.2.1. Reference Clock SDC

The provided clock_constraint.sdc file contains a single create_clock constraint for the PLL reference clock (pll_refclk_i). This constraint is necessary for the PLL to generate the constraint for its output clock. Copy this constraint into the Lattice Radiant Project SDC file (not in PDC file) to allow the synthesis tool to optimize the logic for the target clock.

#### 7.2.2.2. Example Design PDC

The provided constraint.pdc file contains two or three sets of constraints:

- Clock Uncertainty – defines the clock name for sclk_o and specifies its clock uncertainty based on the measured clock jitter during HW validation.
- Eval constraints – specific to the Memory Controller Example Design.
- Pinouts – specifies the pin assignment for the selected board in the *Select Development Board* attribute. This is only available for LPDDR4, Avant-E/G/X70 devices, and the *Select Development Board* attribute is not set to *None.*

If you implement your own Memory Controller design, you need to copy the clock uncertainty constraints into the top-level user PDC file.

The eval constraints composed of set_false_path, set_max_delay, and ldc_create_group constraints, should only be copied if running the provided Memory Controller Example Design. Eval constraints are located below the following comment in the provided constraint.pdc file:

```
 ##############################################################################
# Below are the constraints for eval design, you don’t need these if you are not using the eval
```

Refer to the Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059) for details regarding the implementation of constraints.

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## 7.3. Example Design Hardware Evaluation

After successfully configuring and generating the Memory Controller IP core, you can use the included synthesis example design for hardware evaluation of the Memory Controller. For a detailed description of the Memory Controller Example Design, refer to the Synthesis Example Design section of this user guide. The traffic generator file set is located under the eval/traffic_gen directory and is described in the Table 7.4.

**Table 7.4. Contents of eval/traffic_gen**

| File List | Description |
|---|---|
| ahbl0.v | AHBL_1x2. It routes CPU data access to SYS_MEM or AHBL2APB |
| ahbl2apb0.v | AHBL to APB bridge |
| apb0.v | APB_1x4. It routes CPU data access through AHBL2APB going to each module's CSR |
| cpu0.v | RISC-V CPU |
| gpio0.v | GPIO module |
| ctrl_fifo.v | RTL files for AXI4 traffic generator |
| lscc_axi4_traffic_gen.sv | |
| lscc_axi4_m_csr.sv | |
| lscc_axi4_m_rd.sv | |
| lscc_axi4_m_wr.sv | |
| lscc_axi4_perf_calc.sv | |
| lscc_lfsr.v | |
| mc_axi4_traffic_gen.v | |
| lscc_osc.v | RTL files for OSC module |
| osc0.v | |
| lscc_ram_dp_true.v | Copy of Lattice Radiant RAM_DP_True Foundational IP (needed by SYS_MEM) |
| memc_apb.v | RTL file for APB configuration interface |
| sysmem0.v | The SYS_MEM for hardware validation, enabled when eval_top.SIM=0 (Implementation) |
| uart0.v | The UART module |

### 7.3.1. Preparing the Bitstream

After configuring and generating the Memory Controller IP core, all associated example design files are created under the eval directory. Refer to Table 7.2 for more details. The following steps illustrate how to prepare the Memory Controller Example Design project and generate the associated bitstream.

1. After generating the Memory Controller IP core, the Lattice Radiant project contains <instance_name>.ipx under the project's input files. If not, right-click on **Input Files** and select **Add > Existing File** under the **File List** tab in the lower-left corner of the Lattice Radiant window. This action opens the **Add Existing File** dialog box. Navigate to the <instance_directory>/<instance_name> directory and select the <instance_name>.ipx file. Ensure the **Copy file to directory** option is unchecked. Click **Add**.
2. To add the top-level example design file to the project, right-click on **Input Files** and select **Add > Existing File**. This action opens the **Add Existing File** dialog box. Navigate to the eval directory and select the eval_top.sv file. Ensure the **Copy file to directory** option is unchecked. Click **Add**.

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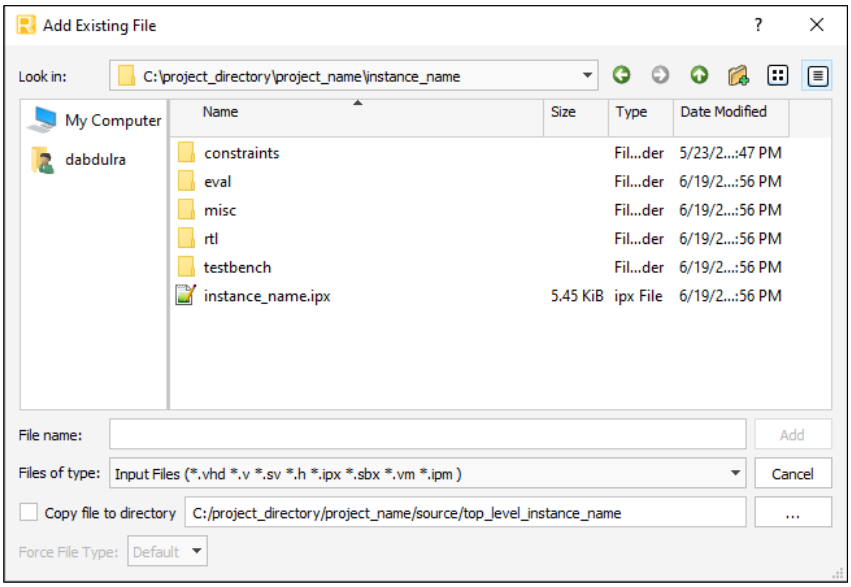



**Figure 7.7. Add Existing File Dialog Box**

3. To add the pre-synthesis constraint file to the project, right-click on **Pre-Synthesis Constraint Files** and select **Add > Existing File**. In the **Add Existing File** dialog box, check the **Copy file to directory** option. This ensures any user modifications are not overwritten when the Memory Controller IP core is regenerated. Navigate to the eval directory and select the clock_constraint.sdc file. Click **Add**.
4. To add the post-synthesis constraint file to the project, right-click on **Post-Synthesis Constraint Files** and select **Add > Existing File**. In the **Add Existing File** dialog box, check the **Copy file to directory** option. Navigate to the eval directory and select the constraint.pdc file. Click **Add**.
5. Modify the constraint.pdc to add the pin assignment for the Avant-E/G/X board. You can do this by either modifying the constraint.pdc file directly or first synthesizing the Lattice Radiant project by clicking on the Synthesize Design button and then adding pinouts through the Device Constraint Editor under **Tools > Device Constraint Editor**. Note that when assigning the UART pins, the UART TX signal connects to the UART RX on the FPGA side, and the UART RX signal connects to the UART TX signal on the FPGA side.
   You can skip this step when implementing the LPDDR4 Example Design to a Lattice board and the board is chosen in the *Select Development Board* attribute in IP GUI.
6. Before running the example design on hardware, you need to generate a bitstream. You can do this by clicking on the ▶ button. This generates a <project_name>_<top_level_instance_name>.bit file under the <project_directory>/<project_name>/<top_level_instance_name> directory specified in Step 2 of the Configuring and Generating the IP section of this user guide.

Timing failures may occur during Place and Route due to unconstrained paths specific to the design. For details on implementing constraints, refer to the Constraints section of this user guide.

### 7.3.2. Running on Hardware

The DDR Memory Controller IP core has been hardware-validated on both Avant-E Evaluation board and Avant-G/X Versa Board. To perform a hardware evaluation of the Memory Controller Example Design, the following are needed:

- Avant-E/G/X FPGA board with UART connection
- Associated power supply and programming cable
- Personal computer running Lattice Radiant software 2024.1 or later
- Lattice Propel™ software 1.0 or later, or any terminal that supports serial communication

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To run the example design on hardware, you need a bitstream file. To generate the .bit file, refer to the Preparing the Bitstream section of this user guide. The following steps illustrate how to program the FPGA board with the example design.

1. Connect the FPGA board to the computer and power on the board.
2. Run the Lattice Radiant Programmer by clicking the button. This launches the Lattice Radiant Programmer, which scans for devices and configures the programmer automatically.

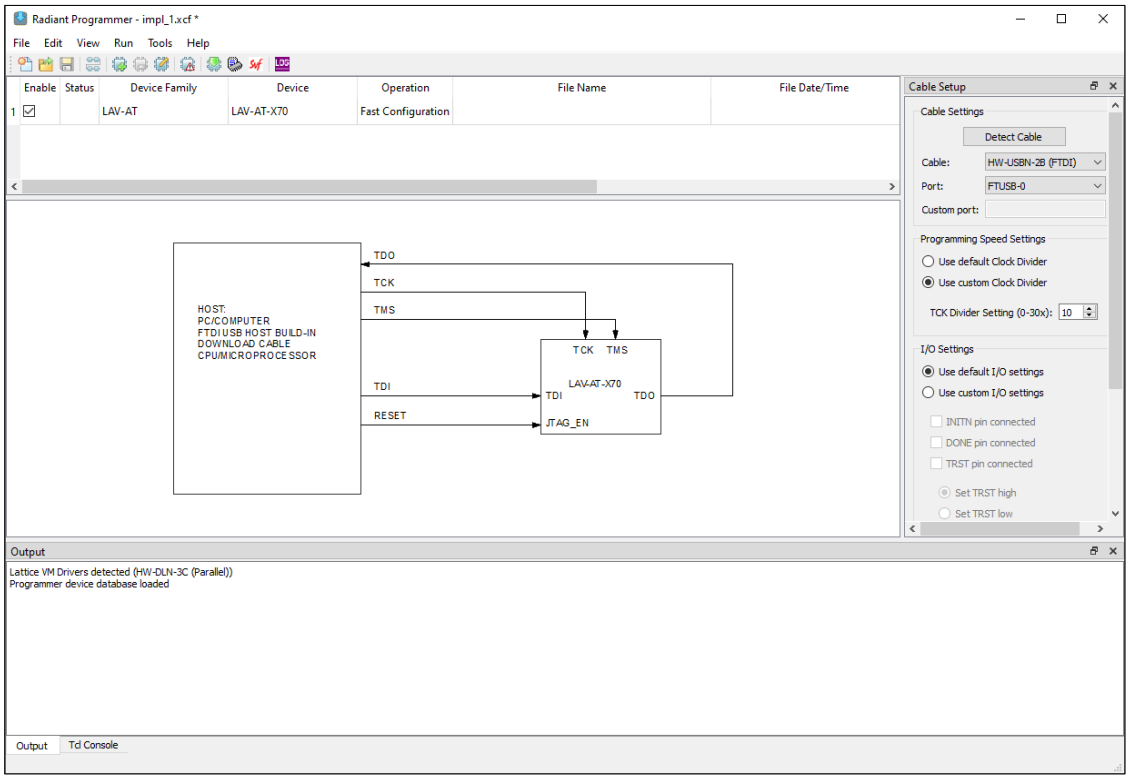



**Figure 7.8. Lattice Radiant Programmer**

3. Click under the **File Name** field, and then click on **…** to the right of the field to launch the **Open File** dialog box. Navigate to the bitstream file generated in Step 6 of the Preparing the Bitstream section of this user guide and click **Open**.

To run the example design, you need to launch a serial terminal. If you wish to use your own serial communication terminal, proceed to Step 6. If you wish to use the Lattice Propel software terminal, continue with Step 4.

4. Launch the Lattice Propel software and select **Launch**. This action opens the default workspace.
5. To open the terminal, click on the button.
6. Configure the terminal settings to be a **Serial Terminal** with the appropriate **Baud rate, Data size, Parity, Stop bits, and Encoding**. Click **OK** to launch the **Terminal** pane at the bottom of the Propel window. Note that the **Serial port** will vary depending on the computer setup.

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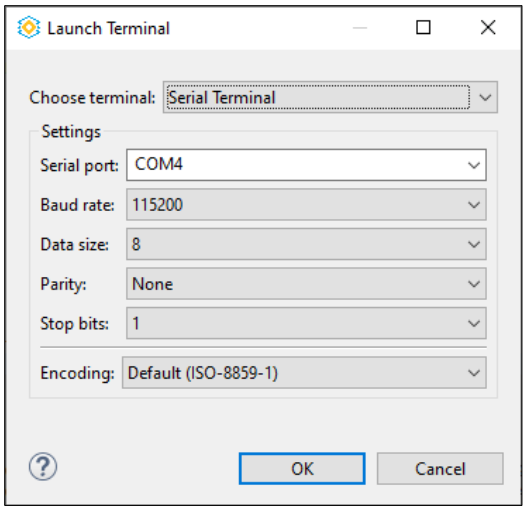



**Figure 7.9. Serial Terminal Settings**

7. Program the Lattice FPGA device by clicking the button. Upon successful programming, assert the rstn_i signal to run the example design, resulting in the following prompt appearing in the terminal.
   - If no message is received, close the current serial terminal, click **Detect Cable** in the programmer window, and repeat steps 3–7 in the Running on Hardware section of this user guide with a different **Serial port**.

```
================================================================
DDR Memory Controller Example Design
================================================================
Select Test to Run (press corresponding key)
0 = Print Memory Training Stages and Data Access Pattern Definition
1 = Run Memory Training and Data Access Check
2 = Run Memory Training and Data Access In a loop With Reset
```

Pressing **0** prints a series of definitions correlating to the memory training and data access test pattern:

```
------------------------------------------------
Memory Training Stage Definitions
------------------------------------------------
A sequence of letters will print out to indicate which stages were successfully
completed.
I = Initialization
C = Command Bus Training
L = Write Leveling
R = Read Training
W = Write Training
S = SCL Training
B = Bit-Level Trim Sweep Training
------------------------------------------------
Memory Data Access Pattern Definitions
------------------------------------------------
A sequence of numbers will print out to indicate which data access patterns were
successful.
0 = INCR2: 2-beat incrementing single burst write followed by 10 burst reads with no
delay between transactions
1 = INCR2: 2-beat incrementing 10 burst writes followed by 10 burst reads with no delay
between transactions
```

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```
2 = INCR4: 4-beat incrementing single burst write followed by 10 burst reads with no
delay between transactions
3 = INCR4: 4-beat incrementing 10 burst writes followed by 10 burst reads with no delay
between transactions
4 = INCR8: 8-beat incrementing burst write followed by burst read with no delay between
transactions
5 = INCR8: 8-beat incrementing burst write followed by a delay before issuing burst read
6 = INCR64: 64-beat incrementing burst write followed by burst read with no delay
between transactions
7 = INCR128: 128-beat incrementing burst write followed by burst read with no delay
between transactions
8 = INCR256: 256-beat incrementing burst write followed by burst read with no delay
between transactions
a = RAND1: 1-beat random address single write followed by single read with no delay
between transactions
```

p = INCR64 Performance Test: 64-beat incrementing parallel burst write and burst read with no delay between transactions. Pressing **1** starts the training sequence, followed by 7-9 (based on *Maximum Burst Length*) different data access checks:

```
Note: Optimal Values found during testing should be set in the IP GUI
-----------------------------------------------
Starting Memory Training
-----------------------------------------------
I
 C
  L
   R
    W
     S
      B
RESULT: Training passed with STATUS_REG_ADDR value: 0x3007F
VREF has been trained to the following values:
MC DQS Grp Vref [DQS0 -> DQS3] : 45,45,47,41
-----------------------------------------------
Starting Data Access Check
-----------------------------------------------
0
 1
  2
   3
    4
     5
      6
       a
        p
-----------------------------------------------
Starting Performance Test
-----------------------------------------------
The Performance Test measures the throughput of the MC and calculates efficiency via the
calculation:
        Total number of wr_rd transactions  /  Duration of the MC clock (sclk)
```

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```
BUS EFFICIENCY in %: 80
Performance in Mbps : 55482
Ran : 20000 transactions across sequential address
RESULT : All transaction types have PASSED.
```

The bus efficiency value represents the efficiency percentage of the DDR4/LPDDR4 bus utilization, while the performance value represents the bandwidth of the DDR4/LPDDR4 interface. The following formulas are used to calculate efficiency and bandwidth:

Efficiency = (Total number of bytes transferred) / (number of DDR clock cycles × (DDR_WIDTH / 8) × gearing ratio)

Bandwidth = (Total number of bytes transferred) / (number of DDR clock cycles × DDR clock period)

The bandwidth can also be calculated using the following equation:

DDR4/LPDDR4 Data Width × DDR4/LPDDR4 Data Rate × (DDR4/LPDDR4 Bus Efficiency / 100), where the DDR4/LPDDR4 Data Rate is in Mbps.

Pressing **2** performs the Test 1 mentioned above, followed by a reset input to the DDR MC, the test repeats as many times as specified in the input prompt. In the following example,  Test 1 will be repeated 100 times.

```
Enter Number of Iterations: 100
```

If a failure occurs during training, a message is sent over the serial connection notifying you of the particular stage that has failed. This also aborts the loop-back data access checks.

```
-----------------------------------------------
Starting Memory Training
-----------------------------------------------
I
Command Bus Training Failed
```

## 7.4. Example Design Simulation

After successfully configuring and generating the Memory Controller IP core, you can use the included example design to simulate the Memory Controller. All associated simulation files are located in the testbench directory. Refer to Table 7.2 for more details.

The following steps illustrate how to prepare the Memory Controller Example Design project for simulation.

1. Before simulating the example design, complete steps 1-2 under the Preparing the Bitstream section of this user guide. To add the top-level testbench file to the project, select **File > Add > Existing Simulation File**. This action opens the **Add Existing Simulation File** dialog box. Navigate to the testbench directory and select the tb_top.sv file. In the **Add Existing File** dialog box, ensure that the **Copy file to directory** option is unchecked. Click **Add**.
2. Before creating the simulation environment, set the SIM parameter in eval_top.sv to 1 and uncomment the RTL_SIM macro definition in tb_top.sv. These parameters and macro shortens the initialization sequence of the DDR4/LPDDR4 interface and disables the UART interface for simulation. Do not modify the SIM parameter for hardware implementation.

When you enable the macro, it programs 0x01C to the Training Operation Register (TRN_OP_REG) to speed up the simulation runtime by reducing the reset and CKE initialization times.

Note that the memory model in the example design simulation requires a minimum simulation timescale of 1 ps, as defined by the memory manufacturer. To ensure proper functionality, generate the PLL reference clock with a minimum timescale of 1 ps. Lattice recommends skipping the training sequences (including command-bus training) by writing 8'h1C to TRN_OP_REG/trn_opr_i. This will reduce simulation time by programming the verified trained values into the PHY. Refer to the Simulation Example Design section of this user guide for more details.

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To simulate the Memory Controller Example Design perform the following steps to create the simulation environment.

1. Launch the simulation wizard in Lattice Radiant software by selecting **Tools > Simulation Wizard**. This action opens the **Simulation Wizard** dialog box. Click **Next** and provide a name (<sim_name>) and directory (<sim_directory>) for the simulation project, where the default directory is set to <project_directory>/<project_name>. Click **Next**.

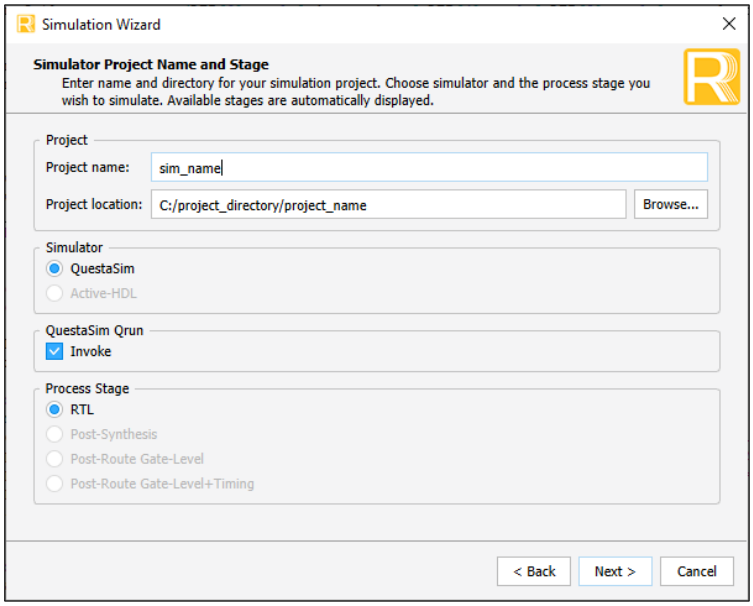



**Figure 7.10. Simulation Wizard**

2. In the **Add and Reorder Source** window, notice that the **Source Files** only contain the top-level evaluation (eval_top.sv) and top-level testbench (tb_top.sv) files. Click **Next**.

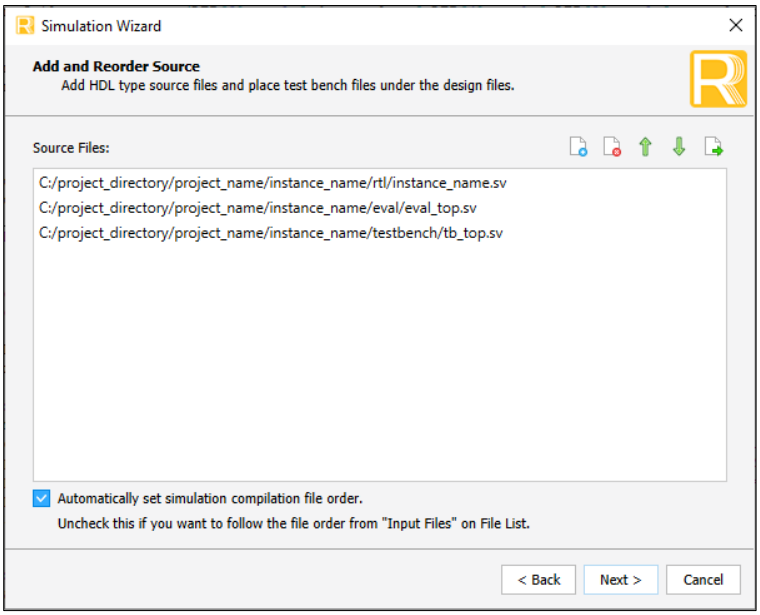



**Figure 7.11. Adding and Reordering Simulation Source Files**

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3. In the **Parse HDL files for simulation** window, notice that the **Simulation Top Module** is set to eval_top. Click **Next**.

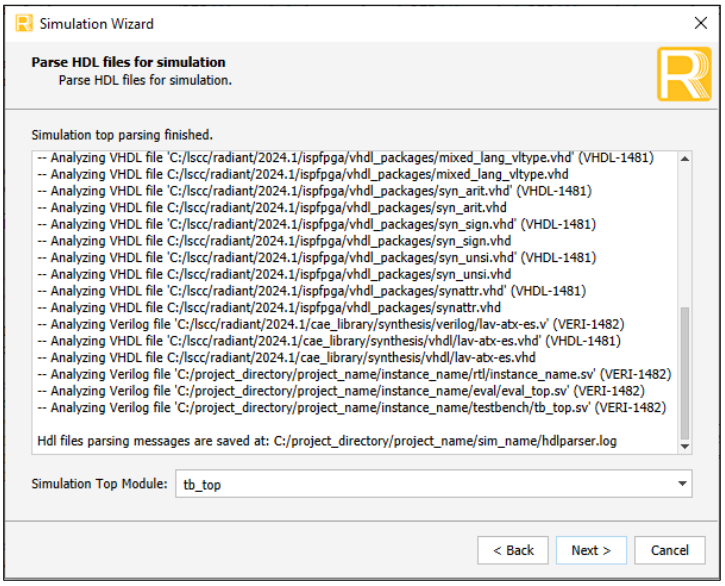



**Figure 7.12. Parsing Simulation HDL Files**

The following error message is expected during the parsing of the HDL files using the Simulation Wizard. These messages are due to the DDR4 simulation models being encrypted and will not affect the simulation behavior since Questasim is able to decrypt the DDR4 memory model.

```
ERROR <1009990> - key_keyowners are not support. Must have "Lattice Semiconductor".
```

4. This action opens the **Summary** window. By default, the simulation runs for 100 µs, allowing you to configure the waveform to log signals of interest in the QuestaSim simulator before continuing. You can then enter the following TCL command in QuestaSim to run the simulation until completion: **run -all**. Alternatively, if you want to run the simulation with the default top-level signals, change the 100 µs value to 0 µs to execute the simulation completely.

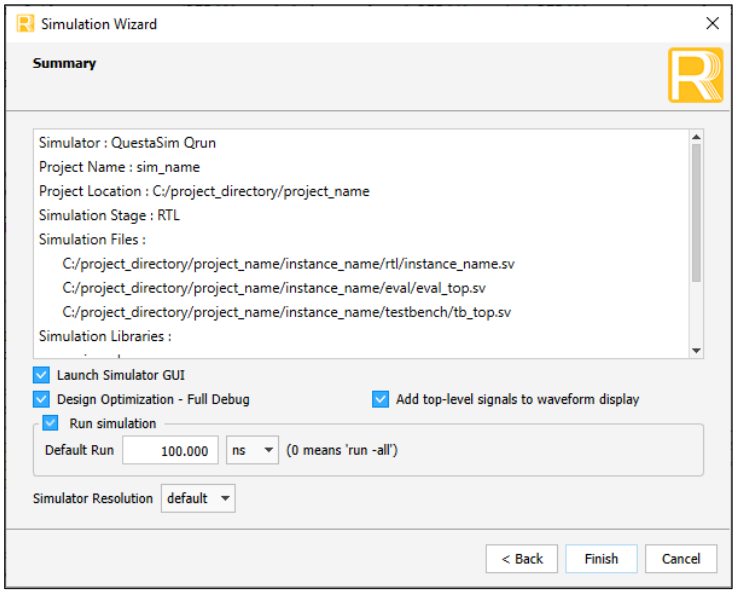



**Figure 7.13. Simulation Summary**

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The Memory Controller IP simulation waveform example is shown in Figure 7.14.

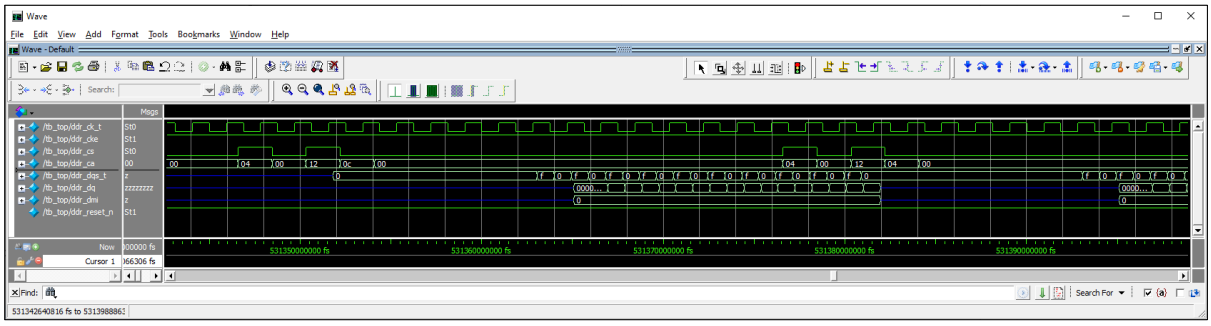


**Figure 7.14. Simulation Waveform Example**

The following error messages are expected in the QuestaSim simulation log and should be disregarded. These messages are due to the violation of timing requirements regarding the DDR4/LPDDR4 simulation model as a consequence of shortening the reset and CKE initialization:

```
# tb_top.LP4MEM_00.mem_x16_00.ins_1ch.<protected> 26083125000 : ###  lpddr4_debug
RESET_n high input
# tb_top.LP4MEM_01.mem_x16_01.ins_1ch.<protected> 26083125000 : ###  lpddr4_debug
RESET_n high input
# Error: tb_top.LP4MEM_01.mem_x16_01.ins_1ch.<protected>.<protected> 26083125000  tINIT1
Error.
# Error: tb_top.LP4MEM_00.mem_x16_00.ins_1ch.<protected>.<protected> 26083125000  tINIT1
Error.
# tb_top.LP4MEM_00.mem_x16_00.ins_1ch.<protected> 32804075000 : ###  lpddr4_debug CKE
high input
# tb_top.LP4MEM_01.mem_x16_01.ins_1ch.<protected> 32804075000 : ###  lpddr4_debug CKE
high input
# Error: tb_top.LP4MEM_01.mem_x16_01.ins_1ch.<protected>.<protected> 32804075000  tINIT3
Error.
# Error: tb_top.LP4MEM_00.mem_x16_00.ins_1ch.<protected>.<protected> 32804075000  tINIT3
Error.
```

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# 8. Debugging

This section discusses tools and strategies available to help you debug your DDR memory interface. Additional debugging information is planned for future releases.

## 8.1. Debug with Example Design

The provided example design helps debug functional issues regarding the training of external DDR memory or data accesses issued by the Memory Controller. For a description of the example design and instructions on how to run the test program for hardware evaluation, refer to the Synthesis Example Design and Running on Hardware sections of this user guide.

The example design prints the optimal settings after the training and before the data access check when current user settings are non-optimal. The Running on Hardware section shows the print when the settings are optimal and below is an example when it is not:

```
...
RESULT: Training PASSED with STATUS_REG_ADDR value: 1007F
DDR Clock Delay Value is not Optimal.
Please update the IP GUI with this value : 0
VREF has been trained to the following values:
MC DQS Grp Vref [DQS0 -> DQS3] : 43,43,42,42
--------------------------------------------------
Starting Data Access Check
--------------------------------------------------
...
```

Set these values in the IP Wizard Training Settings tab for faster training time and better training results. Using the optimal DDR Clock Delay Value improves write leveling performance. Note that when write leveling fails, the training engine finds the optimal DDR clock delay and retries the write leveling. Tuning Address Control Delay Value improves CBT results.

## 8.2. Debug with Reveal Analyzer

The DDR Memory Controller introduces a Memory Controller Debug interface that is available on the Reveal Analyzer to assist users with training-related information and debugging for LPDDR4. Refer to Using the Memory Controller Debug section in the Reveal User Guide for Radiant Software document for guidance on setting up the debugger.

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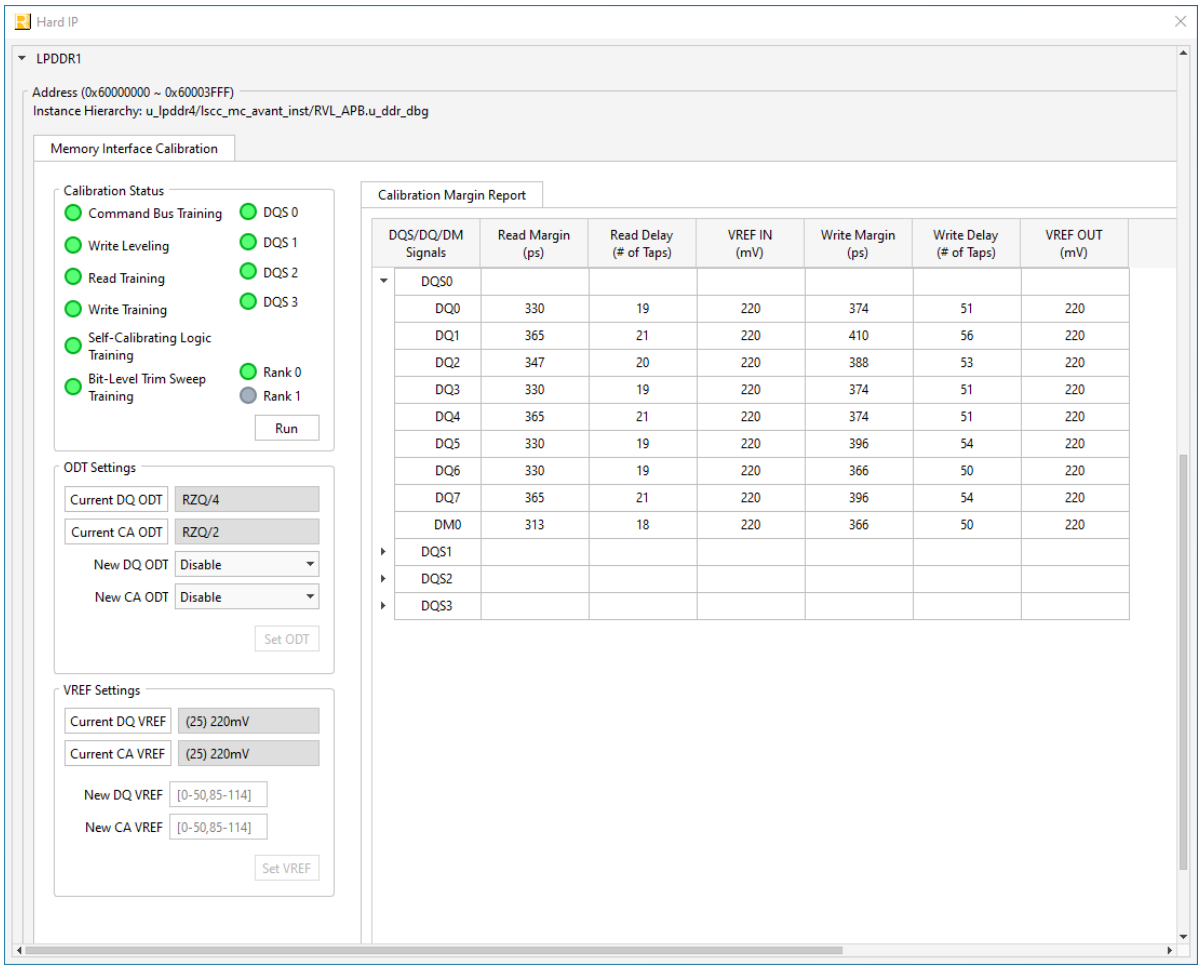



**Figure 8.1. Memory Controller Debug Interface in Reveal Analyzer**

The Calibration Status section reports the result of each training step, where a green indicator denotes a pass and a red indicator denotes a failure. Per-DQS (DQS0–DQS3) and per-rank status indicators are also displayed for each enabled rank. The ODT Settings and VREF Settings sections display the current memory ODT and VREF values and allow these values to be updated by selecting a New DQ/CA ODT option or by entering a New DQ/CA VREF decimal value that corresponds to the binary representation defined in the LPDDR4 JEDEC Standard. Clicking Set ODT or Set VREF applies the new settings, after which clicking Run re-executes the training and updates the calibration status accordingly. For modifications to memory controller-related settings, refer to the IP parameters described in the IP Parameter Description section and follow the configuration flow outlined in the Designing and Simulating the IP section. The Calibration Margin Report section lists the per-signal read and write margins, delay tap counts, and VREF values for each DQS group.

### 8.2.1. Command Bus Training (CBT)

The Command Bus Training (CBT) centers the entire CA bus relative to CK by aligning the rising edge of CK to the middle of the CA valid window. For more information on CBT, refer to the Command Bus Training (CBT) section of the DDR Memory PHY Module User Guide (FPGA-IPUG-02195).

If CBT fails, the cause is most likely an issue with the MC-to-DRAM connection. Check the following:

- The pin assignments are correct.
- The Number of DDR Clocks (CK_WIDTH) and Number of Ranks (CS_WIDTH) match the schematic.
- The DRAM ODT(ca)_A/B pins are enabled on the board.
- CK/CS Slew Rate and Command Address Slew Rate – use the default, Fast

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Combination of the following Training Settings IP parameters improves the CBT result; it is recommended to set these based on the SI/PI simulation of your board design:

- Memory CA_Vref Value for Rank<0/1>
- MC CA Output Impedance
- CA_ODT Value

### 8.2.2. Write Leveling

Write leveling aligns the DQS signals to CK by sampling the CK with the rising edge of DQS and asynchronously providing feedback to the Memory Controller through the DQ pins. For more information on write leveling, refer to the Write Leveling section of the DDR Memory PHY Module User Guide (FPGA-IPUG-02195).

The Training Settings IP parameter – *DDR Clock Delay Value* can be increased to improve the Write Leveling result depending on your board design.

### 8.2.3. Read Training

Read training center-aligns the DQS to the read DQ window by adjusting the read DQ to determine the window where the expected DQ burst pattern is sampled correctly by DQS. For more information on read training, refer to the Read Training (Read Bit-Leveling) section of the DDR Memory PHY Module User Guide (FPGA-IPUG-02195).

The read training or the MC-side Vref training may fail if the read DQ/DQS/DM signal quality is bad. Combination of the following Training Settings IP parameters improves the read DQ signal quality (hence the read training as well); it is recommended to set these based on the SI/PI simulation of your board design:

- MC ODT Value
- SoC_ODT Value
- Pull-Down Drive Strength

### 8.2.4. Write Training

Write training center-aligns the DQS to the write DQ window by adjusting the write DQ to determine the window where the expected DQ burst pattern is sampled correctly by DQS. For more information on write training, refer to the Write Training (Write Bit-Leveling) section of the DDR Memory PHY Module User Guide (FPGA-IPUG-02195).

The initial write training may fail if the write DQ/DQS/DM signal quality is bad. Combination of the following Training Settings IP parameters improves the write DQ signal quality (hence the write training as well); it is recommended to set these based on the SI/PI simulation of your board design:

- Memory DQ_Vref Value for Rank<0/1> – the initial value during bring-up may be the default value or from the SI/PI simulation. However, if the example design recommends a different Memory DQ_Vref value, use it.
- MC DQ Output Impedance
- DQ_ODT Value

### 8.2.5. Self-Calibrating Logic (SCL)

SCL optimizes the setup and hold time margins for internal sampling of the read data by adjusting the data_capture_clk and the sampling latency. For more information on SCL, refer to the Self-Calibrating Logic (SCL) section of the DDR Memory PHY Module User Guide (FPGA-IPUG-02195).

The Training Settings IP parameter – *DDR Clock Delay Value* can be increased to improve the SCL result depending on your board design.

### 8.2.6. Bit-Level Trim Sweep (BLTS)

Bit-level trim sweep uses the worst-case DQ pattern to further train the read and write transactions for better stability over system SI/PI variations or jitter in high-speed applications. The trained values may be sufficient for read and write training in the prior steps, but it may be suboptimal for the worst-case pattern. For more information on BLTS, refer to the Bit-Level Trim Sweep (BLTS) section of the DDR Memory PHY Module User Guide (FPGA-IPUG-02195).

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The BLTS may fail if the read or write DQ/DQS/DM signal quality is bad. The combination of the following Training Settings IP parameters may improve the DQ signal quality further with this worst-case pattern:

- MC ODT Value
- SoC_ODT Value
- Pull-Down Drive Strength
- Memory DQ_Vref Value for Rank<0/1> – the initial value during bring-up may be the default value or from the SI/PI simulation. However, if the example design recommends a different Memory DQ_Vref value, use it.
- MC DQ Output Impedance
- DQ_ODT Value

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# 9. Design Considerations

## 9.1. IP Configuration

- Ensure that the selected DRAM device configuration matches the intended setup.
- Ensure that all timing parameters are configured and aligned with the DRAM vendor's datasheet and usage, even though the IP applies JEDEC-compliant default values.
- Ensure that IP frequency and PLL configuration match board-level clocking requirements.
- Ensure that the required power-up sequencing is followed to prevent inconsistent IP behavior. Refer to the Calibration section of this user guide.

## 9.2. Board-level Signal Integrity and Routing

- Ensure that recommended board design routing rules for DQ/DQS/CK skew, impedance, and trace-length matching are followed. Refer to the PCB Layout Recommendations for BGA Packages (FPGA-TN-02024).
- Ensure that proper termination schemes are consistent with the IP configuration and PCB implementation.
- Ensure clean power-rail delivery for VDD/VDDQ/VREF to prevent training-reliability issues.
- Ensure that any bit-swapping is consistent with IP configuration (if applicable).

## 9.3. Performance

- For good performance, ensure that the user-side AXI issues burst transactions aligned with the IP burst length.
- For users that issue short burst with random addresses, enable the Auto-Precharge option in the IP Wizard to improve performance.
- Use bank interleaving when mapping addresses for parallel workloads to achieve sustained throughput.

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# Appendix A. Resource Utilization

**Note:** Resource utilization values in this section are provided for reference only and may change based on the compilation strategy and selected tool options.

The following table shows the configuration and resource utilization for LAV-AT-E70ES1-3LFG1156C using Synplify Pro of Lattice Radiant software 2026.1.

**Table A.1. DDR4 Resource Utilization for IP Core v2.9.0**

| Configuration | aclk_i Fmax (MHz) | sclk_o Fmax[1] (MHz) | Registers | LUTs[2] | EBR | DSP |
|---|---|---|---|---|---|---|
| DDR Command Frequency = 1066, Others = Default | 311.139 | 311.139 | 7,539 | 8,577 | 25 | 0 |
| DDR Command Frequency = 1066, DDR Bus Width = 16, Others = Default | 328.731 | 300.120 | 5,904 | 7,732 | 21 | 0 |
| DDR Command Frequency = 1066, DDR Bus Width = 64, Others = Default | 306.466 | 304.466 | 10,378 | 10,378 | 33 | 0 |

**Notes:**

1. The sclk_o Fmax is generated using the top-level example design wrapper file, eval_top.sv, that is described in the Synthesis Example Design section of this user guide. These values may increase when the IP Core is used with the user logic.
2. The resource usage number in the LUTs column represents the total LUT4 usage, including logic, distributed RAM and ripple logic.

**Table A.2. LPDDR4 Resource Utilization for IP Core v2.9.0**

| Configuration | aclk_i Fmax (MHz) | sclk_o Fmax[1] (MHz) | Registers | LUTs[2] | EBR | DSP |
|---|---|---|---|---|---|---|
| DDR Command Frequency = 1066, Others = Default | 327.225 | 300.120 | 8,126 | 9,068 | 25 | 0 |
| DDR Command Frequency = 1066, DDR Bus Width = 16, Others = Default | 335.345 | 300.120 | 6,560 | 8,105 | 21 | 0 |
| DDR Command Frequency = 1066, DDR Bus Width = 64, Others = Default | 325.521 | 300.120 | 11,240 | 10,835 | 33 | 0 |

**Notes:**

1. The sclk_o Fmax is generated using the top-level example design wrapper file, eval_top.sv, that is described in the Synthesis Example Design section of this user guide. These values may increase when the IP Core is used with the user logic.
2. The resource usage number in the LUTs column represents the total LUT4 usage, including logic, distributed RAM and ripple logic.

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# Appendix B. Known Issue

Some DQ swizzle settings on DQS group 1 may encounter a CBT error due to the initialization values of the DDRPHY Hard IP input DQ. This causes the CBT pattern to appear as already matching at the start of CBT. This issue occurs only in simulation, not in hardware. In hardware, the actual default input DQ value in silicon is zero because the DQ signal is in a high-impedance state and the termination pulls it down to zero. This issue occurs when using the Lattice Radiant software version 2025.2.1 or earlier.

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# References

For more information refer to:

- DDR Memory Controller IP Release Notes (FPGA-RN-02033)
- DDR Memory Controller Driver (FPGA-TN-02379)
- DDR Memory PHY Module User Guide (FPGA-IPUG-02195)
- Avant High Speed IO and External Memory Interface User-Guide (FPGA-TN-02300)
- Avant-E web page
- Avant-G web page
- Avant-X web page
- Certus-N2 web page
- Lattice Propel Design Environment web page
- AMBA AXI Protocol Specification
- AMBA APB Protocol Specification
- DDR4 JEDEC Standard
- LPDDR4 JEDEC Standard
- Lattice Radiant Software User Guide
- Reveal User Guide for Radiant Software
- Lattice Propel Builder User Guide (FPGA-UG-02243)
- Lattice Radiant Timing Constraints Methodology User Guide (FPGA-AN-02059)
- Lattice Radiant FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

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# Revision History

**Note:** In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

**Revision 2.1, IP v2.9.0, September 2026**

| Section | Change Summary |
|---|---|
| All | Minor editorial fixes. |
| Debugging | • Updated the Debug with Reveal Analyzer section.<br>  • Clarified that the Memory Controller Debug interface in Reveal Analyzer applies specifically to LPDDR4 training only.<br>  • Documented how to read and use the Calibration Status, ODT Settings, VREF Settings, and Calibration Margin Report areas of the Reveal Analyzer debug interface shown in Figure 8.1, including how to update ODT and VREF values and re-run training.<br>  • Added a new Command Bus Training (CBT) subsection explaining the CBT mechanism and giving a troubleshooting checklist and relevant IP parameters for resolving CBT failures.<br>  • Added a new Write Leveling subsection explaining the write-leveling mechanism and identifying DDR Clock Delay Value as the parameter to adjust to improve results.<br>  • Added a new Read Training subsection explaining the read-training mechanism and the IP parameters that improve read DQ signal quality when read training or MC-side VREF training fails.<br>  • Added a new Write Training subsection explaining the write-training mechanism and the IP parameters that improve write DQ signal quality when initial write training fails.<br>  • Added a new Self-Calibrating Logic (SCL) subsection explaining the SCL mechanism and identifying DDR Clock Delay Value as the parameter to adjust to improve results.<br>  • Added a new Bit-Level Trim Sweep (BLTS) subsection explaining its purpose and the IP parameters that can further improve DQ signal quality for the worst-case pattern. |
| References | • Added the Reveal User Guide for Radiant Software in the list. |

**Revision 2.0, IP v2.9.0, June 2026**

| Section | Change Summary |
|---|---|
| All | • Updated IP version to *2.9.0*.<br>• Updated Lattice Radiant software to *2026.1*.<br>• Replaced *I/F* with *interface* in this version.<br>• Minor editorial fixes. |
| Abbreviations in This Document | Added the RISC-V abbreviation and its definition to the abbreviations table. |
| Introduction | • Added *note 1* to Table 1.2. LPDDR4 and DDR4 Memory Controller IP Support Readiness identifying six specific Avant devices that are limited to 1,600 Mbps and do not support x64 DDR Width.<br>• Added *AXI width of 512* to the supported DDR4 AXI data interface widths in the DDR4 features section.<br>• Added *note 3* to Table 1.3. DDR4 Features Overview to specify the conditions under which DDR4 side-band ECC is supported.<br>• Added *AXI width of 512* to the supported LPDDR4 AXI data interface widths in the LPDDR4 features section.<br>• Updated Table 1.5. Minimum Device Requirements to include x72 DDR data width for Avant-E/G/X DDR4 and added a note clarifying the x72 ECC constraint. |
| Functional Description | • Revised the Functional Description section introduction to more precisely describe the |

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| Section | Change Summary |
|---|---|
| | section scope.<br>• Reworked the Clocking and Reset section into structured subsections, clarifying the three input clocks and four input resets separately, and adding pll_rst_n_i reset-assertion scenarios and an AXI Bus Idle definition.<br>• Updated the Calibration section.<br>  • Corrected the register name from *PHY_CLOCK* to *PHY_CLOCK_REG* in the Calibration sequence steps.<br>  • Added Figure 2.3. Initialization Sequence (with APB interface), a timing waveform showing the DDR initialization sequence when the APB interface is used.<br>  • Added Figure 2.4. Initialization Sequence (without APB interface), a timing waveform showing the DDR initialization sequence when the APB interface is not used.<br>• Added Figure 2.5. Basic AXI4 Write to DDR4 Write transaction, Figure 2.6. Basic AXI4 Read to DDR4 Read transaction, and Figure 2.7. DDR4 Write and Read Transaction, illustrating DDR4 AXI4 write/read transaction flow and the BL8 on-wire waveform.<br>• Added new Auto-Precharge subsection under DDR4 Operation Descriptions section, describing the AP feature behavior and recommended use case.<br>• Updated the LPDDR4 Operations Description section.<br>  • Added Figure 2.8. Basic AXI4 Write to LPDDR4 Write transaction, Figure 2.9. Basic AXI4 Read to LPDDR4 Read transaction, and Figure 2.10. LPDDR4 Write and Read Transaction, illustrating LPDDR4 AXI4 write/read transaction flow and the BL16 on-wire waveform.<br>  • Added description of CLK turn-off capability during SELF REFRESH Power Down, specifying per-PHY-instance behavior and dual-rank.<br>  • Added new Auto-Precharge subsection describing the AP feature behavior and recommended use case. |
| IP Parameter Description | • Updated Table 3.1. DDR4 General Attributes.<br>  • Added *Simulation Mode Enable* attribute.<br>  • Renamed *Enable Sideband ECC* to *Enable DDR4 Side-band ECC.*<br>  • Updated *Disable Per-bank Timer* dependency to include ECC condition.<br>  • Added Enable Auto-Precharge attribute.<br>• Updated Table 3.5. DDR4 General Definitions.<br>  • Added *Simulation Mode Enable* attribute.<br>  • Added *Enable DDR4 Side-band ECC* attribute.<br>  • Added *Enable Auto-Precharge* attribute.<br>  • Removed *Enable DBI* entry.<br>• Renamed the DDR4 timing parameter *TZQCAL* to *TZQLAT*, updated its definition, and removed the ZQ Calibration Start to Latch attribute in Table 3.7. DDR4 Periodic Event Setting Attributes.<br>• Added *MC DQS Grp8 Vref Value* attribute to Table 3.9. DDR4 Training Settings Attributes.<br>• Updated the MC DQS Vref Value definition entry to Table 3.12. DDR4 Training Settings Definitions.<br>• Added *Simulation Mode Enable* attribute to Table 3.13. LPDDR4 General Attributes and Table 3.17. LPDDR4 General Definitions.<br>• Removed the *not yet supported* note from the Enable Power Down description in Table 3.17. LPDDR4 General Definitions, indicating the feature is now available for LPDDR4.<br>• Renamed *TZQCAL* to *TZQLAT* in Table 3.18. LPDDR4 Memory Device Timing Setting Attributes.<br>• Added Table 3.19. LPDDR4 Power Down Setting Attributes in this section.<br>• Updated *DDR Clock Delay Value* in Table 3.22. LPDDR4 Training Settings Attributes.<br>  • Default is *4* when DDR Command frequency is 800 MHz<br>  • Default is *0* for all other frequencies.<br>  • Renamed the *MC DQS Grp<4,7>* Vref Value attribute to *Grp<4,5,6,7>*. |

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| Section | Change Summary |
|---|---|
| Signal Description | • Updated APB interface port descriptions to replace *subordinate* with *completer*, aligning with AMBA APB protocol terminology.<br>• Corrected the table reference in Table 4.10. LPDDR4 Interface Port Definitions *note 1* from Table 3.12. DDR4 Training Settings Definitions to Table 3.15. LPDDR4 Memory Configuration Attributes. |
| Register Description | • Added *ECC_STATUS3_REG* and *ECC_STATUS4_REG* to Table 5.1 ECC Related Registers.<br>• Updated the software diagnostic flow to reference ECC_STATUS3_REG for AXI address retrieval.<br>• Simplified ECC_CONTROL_REG description. |
| Memory Controller Example Design | • Updated the Synthesis Example Design section.<br>  • Changed the threshold symbol for the highest data rate TRN_OP_REG setting from > to ≥, ensuring the 2,133 Mbps case is explicitly included.<br>• Updated the Running on Hardware section.<br>  • Added *a = RAND1* in the Memory Data Access Pattern Definitions.<br>  • Updated the example output to include patterns *0* and *a* reflecting the newly added data access patterns in the Starting Data Access Check. |
| Designing and Simulating the IP | Updated the SDC constraints filename in Table 7.2. Generated File List and Table 7.3. Project Constraints from *constraints.sdc* to *constraint.sdc* to match the generated file name. |
| Debugging | Added this section. |
| Design Considerations | • Added reference to the Calibration section in the IP Configuration section.<br>• Added reference to the PCB Layout Recommendations for BGA Packages (FPGA-TN-02024) in the Board-level Signal Integrity and Routing section. |
| Appendix A. Resource Utilization | • Added a note to Appendix A clarifying that resource utilization values are reference values subject to change based on compilation strategy and tool options.<br>• Updated Table A.1 and Table A.2 to IP Core v2.9.0 values generated with Lattice Radiant software 2026.1.<br>• Added note 2 in Table A.1 and Table A.2. |
| Appendix B. Known Issue | • Retained the DQ swizzle / CBT simulation issue.<br>• Removed the resolved issues; dual rank simulation failures, power down hardware failures, and DDR4 timing closure. |
| References | Added the PCB Layout Recommendations for BGA Packages (FPGA-TN-02024) as a new reference. |

**Revision 1.9, IP v2.8.0, March 2026**

| Section | Change Summary |
|---|---|
| All | Updated IP version to *2.8.0*. |
| Abbreviations in This Document | Added *MCE* in the list. |
| Introduction | • Added Overview of the IP section.<br>• Removed the *hardware validation* column and *note 1* in Table 1.2. LPDDR4 and DDR4 Memory Controller IP Support Readiness.<br>• Added a write-up that the *DDR Memory Controller IP Core example design supports simulation and deployment on development boards* before the Features section.<br>• Added support for DDR4 Memory Controller interface for *data width of x72* in the DDR4 Features section.<br>• Added *Side-band ECC* support for single rank in the DDR4 Features section.<br>• Added *ECC x72 support* under *note 2* in Table 1.3. DDR4 Features Overview.<br>• Updated the ECC feature from *not supported* to *supported*.<br>• Removed the *Hardware Support* section.<br>• Removed the *Naming Conventions* section. |
| Functional Description | Added the Side-band ECC section. |
| IP Parameter Description | • Added the *Disable per-Bank Timer (PBT)* attribute in Table 3.1. DDR4 General Attributes and Table 3.13. LPDDR4 General Attributes. |

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| Section | Change Summary |
|---|---|
| | • Added the *Enable Auto-Precharge* attribute in Table 3.13. LPDDR4 General Attributes. |
| Register Description | Added this section. |
| Designing and Simulating the IP | Added a write-up that the DDR Memory Controller IP Core has been hardware-validated on both Avant-E Evaluation Board and Avant-G/X Versa Board in the Running on Hardware section. |
| Design Considerations | Added this section. |
| Appendix A. Resource Utilization | • Updated Table A.1. DDR4 Resource Utilization for IP Core v2.9.08.0 and Table A.2. LPDDR4 Resource Utilization for IP Core v2.9.0.<br>  • Updated the resource values for DDR Command Frequency = 1066, DDR Bus Width = 64, and Others = Default.<br>  • Renamed *LUT4 Logic* to *LUTs*<br>  • Added *note 2* |
| Appendix B. Known Issues | Added item no. 4 issue – *DQ swizzle settings on DQS group 1.* |

**Revision 1.8, IP v2.7.0, December 2025**

| Section | Change Summary |
|---|---|
| All | Updated IP version from *2.6.1* to *2.7.0*. |
| Introduction | • Updated Table 1.1. Quick Facts.<br>  • Added notes *1* and *2*.<br>  • Added *Driver Support*.<br>• Added *Bit Swizzle* in the LPDDR4 features section.<br>• Added *Bit Swizzle* and *2-D Vref Training* in Table 1.3. DDR4 Features Overview and Table 1.4. LPDDR4 Features Overview.<br>• Reworked the Licensing and Ordering Information section. |
| Functional Description | • Updated the Clocking and Reset section.<br>• Minor updates at the end of AXI4 Data Interface and APB Configuration Interface sections.<br>• Updated the steps to start the initialization and training sequence of the SDRAM device in the Calibration section.<br>• Updated the Initialization and Training without APB Interface section.<br>• Minor updates added in Temperature Tracking and Extended Temperature Support section. |
| IP Parameter Description | • Added *Enable Bit Swizzle* attribute in Table 3.13. LPDDR4 General Attributes and Table 3.17. LPDDR4 General Definitions.<br>• Table 3.22. LPDDR4 Training Settings Attributes.<br>  • Updated the *DDR Clock Delay Value*.<br>  • Updated the Address Control Delay Value Incr/Decr to *Unchecked*.<br>• Updated the *Eval Local Bus Clock Frequency (MHz)* attribute in Table 3.26. LPDDR4 Example Design Attributes and Table 3.27. LPDDR4 Example Design Attribute Definitions.<br>• Added Bit Swizzle Settings section. |
| Signal Description | • Updated description of pll_refclk_i, pll_rst_n_i, and rst_n_i signals in Table 4.1. Clock and Reset Port Definitions.<br>• Updated description of pll_lock_o signal in Table 4.2. Interrupts and Initialization/Training Port Definitions. |
| Memory Controller Example Design | • Updated the Synthesis Example Design section.<br>  • Updated data rate from *≤ 1,866 Mbps* to *≤ 1,333 Mbps.*<br>  • Added a bullet stating, *If data rate in [1,600 Mbps, 1866Mbps]: TRN_OP_REG = 0x1DF during training.* |
| Designing and Simulating the IP | • Updated Table 7.2. Generated File List to add the new generated files.<br>• Updated the Example Design Simulation section.<br>  • Reworked Step no. 2 on how to prepare the Memory Controller Example Design |

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| Section | Change Summary |
|---|---|
| | project for simulation.<br>• Updated the 3rd paragraph.<br>  • Replaced set *SIM to 1* to *enable the macro*.<br>  • Removed, *You can configure the simulation of reset and the initialization and training sequences by forcing the value of TRN_OP_REG by locating the following line in tb_top.sv: force `DUT_INST_NAME.lscc_mc_avant_inst.u_ddrphy.i_csr.trn_operation_reg = 10'h01C;* |
| Appendix A. Resource Utilization | Updated the values in Table A.1. DDR4 Resource Utilization for IP Core v2.9.0 and Table A.2. LPDDR4 Resource Utilization for IP Core v2.9.0. |
| Appendix B. Known Issues | Added a known issue simulation issue with DQ Swizzle settings on DQS Group 1. |
| References | Added the Avant High Speed IO and External Memory Interface User-Guide (FPGA-TN-02300) in this section. |
| Revision history | Added a note, *In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates* to this section. |

**Revision 1.7, IP v2.6.1, October 2025**

| Section | Change Summary |
|---|---|
| All | Updated IP version from *2.6.0* to *2.6.1*. |
| Introduction | Added note for limitation on support in Table 1.2. |
| Functional Description | • Updated TRN_OP_REG value in Calibration section.<br>• Updated trn_opr_i value in Initialization and Training without APB Interface section. |
| IP Parameter Description | Updated DDR Clock Delay Value in LPDDR4 Training Settings section. |
| Memory Controller Example Design | • Updated TRN_OP_REG value in Synthesis Example Design section. |

**Revision 1.6, IP v2.6.0, June 2025**

| Section | Change Summary |
|---|---|
| All | • Minor editorial fixes.<br>• Updated IP version from *2.5.2* to *2.6.0*. |
| Introduction | • Updated Supported Devices and removed Target Devices in Table 1.1.<br>• Updated DDR4 Features:<br>  • Removed read DBI<br>  • Added component (DRAM soldered on the board) and UDIMM support.<br>  • Added note on dual rank support<br>• Updated LPDDR4 Feature: Added note on dual rank support<br>• Updated Table 1.3.<br>  • Updated Key Feature Device Format to *Component, UDIMM*.<br>  • Updated VREF Training to *Not yet supported*. |
| IP Parameter Description | • Updated *Read Latency* options and default values in Table 3.1.<br>• Updated *I/O Buffer Type*, *Read Latency* and *Write Latency* description in Table 3.5.<br>• Updated Slew Rate settings default value in Table 3.10 and Table 3.22.<br>• Added training settings attributes in Table 3.9, Table 3.12 , Table 3.21 , and Table 3.24.<br>• Updated *RTT_WR Value* default value in Table 3.11.<br>• Updated the DDR Clock Delay default value from *4* to *2* in Table 3.21. |
| Signal Description | • Updated descriptions of pll_refclk_i, pclk_i, aclk_i, rst_n_i in Table 4.1.<br>• Removed DDR4 in table label for Table 4.1, Table 4.2 , Table 4.3, and Table 4.4.<br>• Added note 2 in Table 4.9. |
| Appendix B | • Added a known issue for dual rank. |

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**Revision 1.5, IP v2.5.2, March 2025**

| Section | Change Summary |
|---|---|
| All | • Minor editorial fixes.<br>• Updated IP version from *2.4.0* to *2.5.2*. |
| Introduction | Updated the *Targeted Devices* in Table 1.1. Quick Facts. |
| Functional Description | • Updated the AXI Data Interface section.<br>  • Modified the *AxADDR* description.<br>  • Added *WSTRB* description.<br>• Updated the recommended value for *TRN_OP_REG/trn_opr_i* in the Calibration section. |
| IP Parameter Description | • Added *Pull-Down Drive Strength* in the LPDDR4 Training Settings section, Table 3.23 and Table 3.24.<br>• Added the Example Design section under LPDDR4. |
| Signal Description | • Unified the following sections for both DDR4 and LPDDR4.<br>  • Clock and Reset<br>  • Interrupts and Initialization/Training<br>  • APB Register Interface<br>  • AXI4 Data Interface<br>• Updated the *width* of *trn_opr_i* in Table 4.2. DDR4 Interrupts and Initialization/Training Port Definitions.<br>• Added the following subsections under AXI Data Interface section:<br>  • AXI4 Address Mapping for DDR4 mode<br>  • AXI4 Address Mapping for LPDDR4 mode |
| Memory Controller Example Design | • Updated the *TRN_OP_REG* value in the Synthesis Example Design section.<br>• Updated Table 6.2 and Table 6.3 in the Simulation Example Design section. |
| Designing and Simulating the IP | • Updated the Pin Placement section to remove *VREF* pin.<br>• Added *Pinouts* in the Example Design PDC section.<br>• Updated *Step 5* in the Preparing the Bitstream section.<br>• Updated *Step 3* in the Example Design Simulation section to show the expected error message for DDR4.<br>• Updated the *serial port print outs* in the Running on Hardware section. |
| Appendix B | Removed the pll lock issue. |
| References | Added DDR Memory Controller Driver (FPGA-TN-02379) in this section. |

**Revision 1.4, IP v2.4.0, December 2024**

| Section | Change Summary |
|---|---|
| All | • Changed the document title from *Memory Controller IP Core for Avant Devices* to *DDR Memory Controller IP Core*.<br>• Minor editorial fixes. |
| Abbreviations in This Document | Changed *Acronyms* to *Abbreviations*. |
| Introduction | • Updated Table 1.1. Quick Facts.<br>  • Added Lattice Nexus 2 to the supported FPGA family.<br>  • Added LAV-AT-E30 and LN2-CT-20 to the targeted device.<br>• Added the IP Support Summary section.<br>• Added Certus-N2 in Table 1.5. Ordering Part Number.<br>• Added the Hardware Support section.<br>• Removed the IP Validation Summary section.<br>• Added Certus-N2 in Table 1.5. Minimum Device Requirements. |
| IP Parameter Description | • Updated Table 3.1. DDR4 General Attributes.<br>  • Updated the Read Latency attribute and Write Latency attribute.<br>• Added table note 1 – Only devices with speed grades of 2 and 3 can support dual rank |

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| Section | Change Summary |
|---|---|
| | to Table 3.3, and Table 3.15.<br>• Updated Table 3.4. DDR4 Local Data Bus Attributes.<br>  • *ID Width* – added *1* as the selectable value.<br>• Updated Table 3.5 and Table 3.17.<br>  • Removed, only single rank is supported under Number of Ranks attribute.<br>• Removed Avant E/G/X in table note 1 of Table 3.13. LPDDR4 General Attributes.<br>• Updated Table 3.16. LPDDR4 Local Data Bus Attributes.<br>  • *ID Width* – added *1* as the selectable value. |
| Designing and Simulating the IP | • Reworked Constraints section.<br>• Updated Table 7.3. Project Constraints. |
| Appendix B | Added this section. |
| References | Added the DDR Memory Controller IP Release Notes (FPGA-RN-02033) in this section. |

**Revision 1.3, August 2024**

| Section | Change Summary |
|---|---|
| All | • Minor editorial fixes<br>• Replaced ModelSim with *QuestaSim*<br>• Replaced Avant-AT-E/Avant-AT-G/Avant-AT-E with *Avant-E/Avant-G/Avant-X* |
| Introduction | • Updated Features subsection<br>  • Updated Avant-E DDR4/LPDDR4 SDRAM speeds<br>  • Added Dual-rank support<br>  • Added DDR4 VREF Training<br>• Updated IP Validation Summary subsection<br>  • Added Dual rank to Table 1.5.<br>• Updated Minimum Device Requirements subsection<br>  • Updated Table 1.6. |
| Functional Description | • Renamed section 2.1.1 Hardened Memory Controller to *Memory Controller*<br>• Renamed section 2.1.2 Hardened DDRPHY to *DDRPHY Module*<br>• Renamed section 2.1.2.1 DDRPHY Primitive to 2.1.2.1 *Hardened DDRPHY Primitive*<br>• Updated AXI4 Data Interface subsection<br>  • Removed write strobe limitation<br>  • Updated supported AXI4 transactions<br>• Updated Calibration subsection<br>  • Added polling for PLL lock signal<br>• Updated Periodic ZQ Calibration subsection<br>• Updated Operation Descriptions subsection |
| IP Parameter Description | • Updated subsections based off Memory Controller IP Core for Avant Devices version 2.1.0 |
| Signal Description | • Updated signal name reset_n_i to *areset_n_i*<br>• Updated Table 4.2 and Table 4.7. |
| Designing and Simulating the IP | • Updated Figure 7.5.<br>• Updated Table 7.1<br>• Updated Pin Placement subsection<br>  • Recommend dedicated PLL reference clock<br>• Updated Constraints subsection |
| Appendix A. Resource Utilization | Reworked section contents. |

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**Revision 1.2, December 2023**

| Section | Change Summary |
|---|---|
| All | • Changed the document title from *Lattice Avant Memory Controller IP Core - Lattice Radiant Software* to *Memory Controller IP for Avant Devices*.<br>• Reworked document content and structure for clarity. |
| Acronyms in this document | • Reworked section contents. |
| Introduction | • Reworked section contents.<br>• Reworked *section 4 Ordering Part Number* and renamed to *subsection 1.3 Licensing and Ordering Information*. Added IP Validation Summary and Minimum Device Requirements subsection.<br>• Reworked *subsection 1.3 Naming Conventions* and renamed to *subsection 1.6 Naming Conventions* |
| Functional Description | • Reworked *subsection 2.1. Overview* and renamed to *subsection 2.1 IP Architecture.*<br>• Added subsection 2.2 Clocking and Reset.<br>• Reworked *subsection 2.2.1 AXI4 Interface* and moved under added *subsection* 2.3 User Interfaces.<br>• Reworked *subsection 2.5. Initialization and Training* and renamed to *subsection* 2.4 Calibration.Reworked *subsection 2.6. Operations Details* and renamed to *subsection* 2.5 Operation Descriptions. |
| IP Parameter Description | Reworked *subsection 2.3 Attributes Summary* and moved this under IP Parameter Description section. |
| Signal Description | Reworked *subsection 2.2 Signal Description* and converted it to Signal Description section. |
| Register Description | Reworked *subsection 2.4 Register Description* and converted it to Register Description section. |
| Memory Controller Example Design | Added this section. |
| Designing and Simulating the IP | Reworked *section 3 IP Generation, Simulation, and Verification* and renamed to this main section. |
| Appendix A. Resource Utilization | Reworked section contents. |
| References | Reworked section contents. |

**Revision 1.1, September 2023**

| Section | Change Summary |
|---|---|
| All | • Changed the document title from 'Avant Memory Controller IP Core - Lattice Radiant Software' to 'Lattice Avant Memory Controller IP Core - Lattice Radiant Software'.<br>• Updated the document to JESD209-4C |
| Introduction | • Updated Lattice Radiant Version to 2023.1 in Table 1.1. Quick Facts.<br>• Removed 933 MHz and BL32 from the Features section. |
| Functional Description | • Added AXI4 Interface section under Signal Description.<br>• Updated Table 2.2. Supported AXI4 Transactions, Table 2.3. Attributes Table, and Table 2.4. Attributes Descriptions. |
| IP Generation, Simulation, and Validation | • Added Creating a Radiant Project section.<br>• Updated Configuring and Generating the IP section for the new IP GUI.<br>• Added Figure 3.7 in the IP Evaluation section.<br>• Updated the Hardware Validation section. |
| Ordering Part Number | Updated this section. |
| Appendix A. Resource Utilization | Updated this section. |
| References | Updated this section. |
| Technical Support Assistance | Added reference link to the Lattice Answer Database. |

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**Revision 1.0, November 2022**

| Section | Change Summary |
|---|---|
| All | Changed document title to Avant Memory Controller IP Core - Lattice Radiant Software. |
| Introduction | • Updated Table 1.1. Quick Facts.<br>• Added 266 and 933 MHz in the Features section. |
| Functional Description | • Updated rst_n_i description and added Note 6 in Table 2.1. Memory Controller IP Core Signal Description.<br>• Updated Table 2.3 Attributes Table.<br>  • Updated DDR Command Frequency and Write/Read Ordering Queue.<br>  • Added note on supporter frequency per speed grade.<br>• Improved Enable DBI description in Table 2.4. Attributes Descriptions.<br>• Updated Initialization and Training section. |
| IP Generation, Simulation, and Validation | • Updated subsections in the IP Generation, Simulation, and Validation section.<br>• Updated the IP Evaluation section.<br>• Updated the Hardware Validation section. |
| Ordering Part Number | Updated this section. |
| Appendix A. Resource Utilization | Updated this section. |
| References | Updated this section. |

**Revision 0.80, September 2022**

| Section | Change Summary |
|---|---|
| All | Preliminary release |

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