



Lattice Avant/Nexus 2 PLL Module

IP Version: 2.7.1

User Guide

FPGA-IPUG-02220-1.6

October 2026

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Inclusive Language

This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language [FAQ 6878](#) for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
APB	Advanced Peripheral Bus
DDRPHY	Double Data Rate Physical Interface
FPGA	Field Programmable Gate Array
GPLL	Global Phase-Locked Loop
GUI	Graphical User Interface
HDL	Hardware Description Language
IP	Intellectual Property
LMMI	Lattice Memory Mapped Interface
PLL	Phase-Locked Loop
RTL	Register Transfer Level
SSC	Spread Spectrum Clocking
VCO	Voltage Controlled Oscillator

1. Introduction

The Phase-Locked Loop (PLL) Module is capable of frequency synthesis and clock phase management, including clock injection delay cancellation. It has the flexibility of input and feedback source selections, multiple output selections, voltage-controlled oscillator (VCO) phase rotation, and independent phase-shifting features. You can synchronize the multiple output clocks, or enable and control each output dynamically.

1.1. Quick Facts

Table 1.1 presents a summary of the PLL Module.

Table 1.1. Quick Facts

IP Requirements	Supported Devices	Lattice Avant™ (LAV-AT-E30, LAV-AT-E/G/X70, LAV-AT-E/G/X70ES), Certus™-N2, Mach™-N2
	IP Changes ¹	Refer to the Lattice Avant PLL Module Release Notes (FPGA-RN-02066) .
Design Tool Support	Lattice Implementation	IP Core v2.7.1 – Lattice Radiant™ software 2026.1.1
	Synthesis	Synopsys® Synplify Pro® for Lattice
	Simulation	Refer to the Lattice Radiant Software User Guide for the list of supported simulators.

Note:

1. In some instances, the IP may be updated without changes to the user guide. This user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

1.2. Features

The key features of the PLL Module include:

- Multiple feedback inputs
- Multiple output clocks
- Lock detector – Phase and Frequency
- Reference clock divider values (NR) – 1 to 64
- Integer Feedback divider values (NF) – 2 to 4095
- Output divider values (NO) – 1 to 256
- Supports Fractional-N divider – up to 14-bit resolution
- Supports Spread Spectrum Clock Generation
 - Spreading rate adjustment range 15 kHz–4 MHz
 - Spreading depth 0%–10%
- VCO phase shift – 8 VCO phases
- Post Divider phase shift
- Dynamic VCO and divider phase shift
- Output clock bypass
- Programmable bandwidth

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal names that end with:

- `_n` are active low signals
- `_i` are input signals
- `_o` are output signals

1.3.3. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

2. Functional Description

2.1. Overview

The PLL Module is capable of clock synthesis and clock phase management, including clock tree delay cancellation. The PLL Module performs frequency synthesis, multiplication, division, and clock injection delay removal. For clock synthesis applications where the removal of clock injection delay is not a requirement, the Global Phase-Locked Loop (GPLL) block has an internal feedback path that is used to complete the feedback loop. Applications that require the removal of the clock injection delay take the feedback clock from the output of the relevant clock tree.

A top-level block diagram of the Global Phase-Locked Loop Module is shown in [Figure 2.1](#).

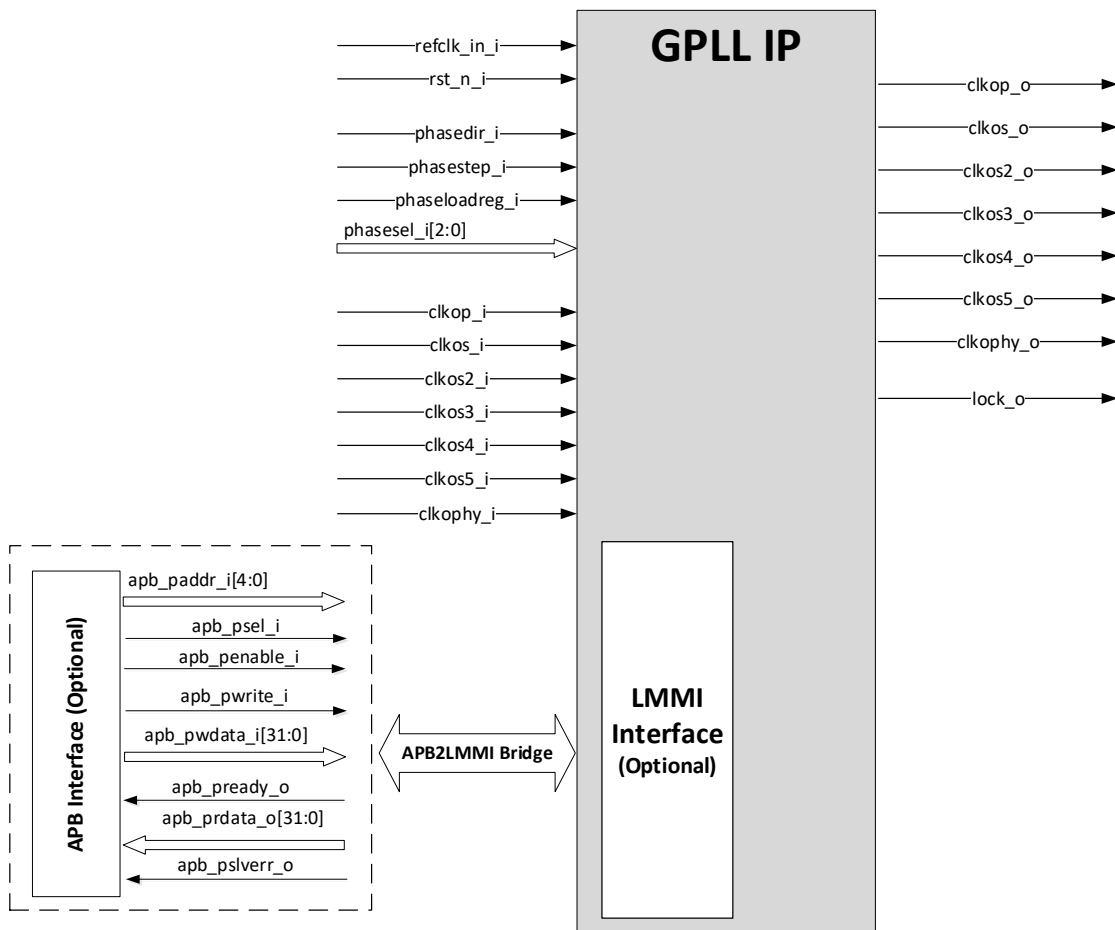


Figure 2.1. GPLL Top Level Block Diagram

This PLL Module has the flexibility of multiple feedback clock source selections. The PLL Module main logic features include seven independent output clocks, output phase shifting through VCO phases, synchronous outputs, and divider phase shifts.

2.2. Signal Description

Table 2.1. PLL Module Signal Description

Port Name	I/O	Width	Description
Clock and Reset			
refclk_in_i	In	1	Reference clock.
rst_n_i	In	1	PLL reset signal that you enable in the IP GUI through <i>PLL Reset Options: Provide PLL Reset</i> . Minimum reset pulse width is 5 μ s.
clkop_o	Out	1	PLL output clock that you enable in the IP GUI through <i>CLKOUT [n]: Port Name</i> set as <i>CLKOP</i> .
clkos_o	Out	1	PLL output clock that you enable in the IP GUI through <i>CLKOUT [n]: Port Name</i> set as <i>CLKOS</i> .
clkos2_o	Out	1	PLL output clock that you enable in the IP GUI through <i>CLKOUT [n]: Port Name</i> set as <i>CLKOS2</i> .
clkos3_o	Out	1	PLL output clock that you enable in the IP GUI through <i>CLKOUT [n]: Port Name</i> set as <i>CLKOS3</i> .
clkos4_o	Out	1	PLL output clock that you enable in the IP GUI through <i>CLKOUT [n]: Port Name</i> set as <i>CLKOS4</i> .
clkos5_o	Out	1	PLL output clock that you enable in the IP GUI through <i>CLKOUT [n]: Port Name</i> set as <i>CLKOS5</i> .
clkophy_o	Out	1	PLL output clock that you enable in the IP GUI through <i>CLKOUT [n]: Port Name</i> set as <i>CLKOPHY</i> . This clock is reserved for DDRPHY.
Miscellaneous / Optional Ports			
phasedir_i	In	1	Dynamic Phase direction signal that you enable in the IP GUI through <i>Optional Ports: Dynamic Phase Control Ports</i> . 0 – Phase Delayed 1 – Phase Advance
phasestep_i	In	1	Dynamic Phase step signal that you enable in the IP GUI through <i>Optional Ports: Dynamic Phase Control Ports</i> .
phaseloadreg_i	In	1	Dynamic Phase load signal that you enable in the IP GUI through <i>Optional Ports: Dynamic Phase Control Ports</i> .
phasesel_i [2:0]	In	3	Dynamic Phase clock select signal that you enable in the IP GUI through <i>Optional Ports: Dynamic Phase Control Ports</i> . 0 – clkop_o 1 – clkos_o 2 – clkos2_o 3 – clkos3_o 4 – clkos4_o 5 – clkos5_o 6 – clkophy_o
clkop_i	In	1	Output Clock Enable signals that you enable in the IP GUI through <i>Optional Port Selections: Clock Enable Ports</i> .
clkos_i	In	1	
clkos2_i	In	1	
clkos3_i	In	1	
clkos4_i	In	1	
clkos5_i	In	1	
clkophy_i	In	1	
lock_o	Out	1	PLL lock signal that you enable in the IP GUI through <i>PLL Lock: Provide PLL Lock Signal</i> .
refclk_out_o	Out	1	Optional signal that you enable in the IP GUI through <i>Miscellaneous Ports</i> . Reference clock output.
div_change_fbclk_o	Out	1	Optional signal that you enable in the IP GUI through <i>Miscellaneous Ports</i> .

Port Name	I/O	Width	Description
			Feedback divider (NF) count change enables output.
div_change_refclk_o	Out	1	Optional signal that you enable in the IP GUI through <i>Miscellaneous Ports</i> . Reference divider (NR) count change enables output.
slip_fbclk_o	Out	1	Optional signal that you enable in the IP GUI through <i>Miscellaneous Ports</i> . PLL IP provides two lower-level signals (slip_fbclk_o and slip_refclk_o) which detect cycle slips between the VCO (that is, feedback) and reference clocks. A brown-out condition may cause the PLL to lose lock. A brown-out condition occurs when the analog or digital supply voltage that drives the PLL becomes smaller than the specified minimum levels. When a brown-out condition occurs, pulses may be observed on the slip_* signals, indicating an out of lock condition. The LOCK output of the detector circuit simultaneously outputs a low signal. The slip_* and LOCK signals, along with a brown-out detector circuit, can be used to force the PLL to go through the reset sequence to re-lock.
slip_refclk_o	Out	1	Note that you cannot assume that the PLL recovers to its locked condition after the brown-out condition subsides. It is possible that during the brown-out condition, the PLL loop can become stuck in a state from which the PLL cannot recover without a reset sequence. Therefore, following a brown-out condition, the PLL must always go through a reset sequence to ensure relock.
ouresetack_clkop_o	Out	1	Optional signal that you enable in the IP GUI through <i>Miscellaneous Ports</i> . Internal OUTRESET change occurred output.
ouresetack_clkos_o	Out	1	
ouresetack_clkos2_o	Out	1	
ouresetack_clkos3_o	Out	1	
ouresetack_clkos4_o	Out	1	
ouresetack_clkos5_o	Out	1	
ouresetack_clkophy_o	Out	1	
stepack_clkop_o	Out	1	Optional signal that you enable in the IP GUI through <i>Miscellaneous Ports</i> . Internal STEP change occurred output.
stepack_clkos_o	Out	1	
stepack_clkos2_o	Out	1	
stepack_clkos3_o	Out	1	
stepack_clkos4_o	Out	1	
stepack_clkos5_o	Out	1	
stepack_clkophy_o	Out	1	
LMMI Interface ¹ – This is currently not available			
lmmi_clk_i	In	1	LMMI Clock
lmmi_resetrn_i	In	1	Reset (active low) Resets the LMM interface. Does not reset the internals of the Hard IP block.
lmmi_request_i	In	1	Start transaction
lmmi_wr_rdn_i	In	1	Write = HIGH, Read = LOW
lmmi_offset_i [4:0]	In	5	Offset (5 bits) – register offset within the secondary register space, starting at offset 0.
lmmi_wdata_i [15:0]	In	16	Write data (16 bits)
lmmi_rdata_o [15:0]	Out	16	Read data (16 bits)
lmmi_rdata_valid_o	Out	1	Read transaction is complete and lmmi_rdata_o contains valid data.
lmmi_ready_o	Out	1	Secondary is ready to start a new transaction. Secondary can insert wait states by holding this signal low.
APB Interface ¹ – This is currently not available			
apb_pclk_i	In	1	APB clock

Port Name	I/O	Width	Description
apb_preset_n_i	In	1	APB reset (active low)
apb_paddr_i [4:0]	In	5	APB Address signal
apb_psel_i	In	1	APB Select signal
apb_penable_i	In	1	APB Enable signal
apb_pwrite_i	In	1	APB Direction signal
apb_pwdata_i [31:0]	In	32	APB Write Data signal
apb_pready_o	Out	1	APB Ready signal
apb_prdata_o [31:0]	Out	32	APB Read Data signal
apb_pslverr_o	Out	1	APB Completer Error signal

Note:

- Only one of the two interfaces is available, depending on the *Interface* attribute selection. For more details, refer to the [Lattice Avant sysCLOCK PLL Design User Guide \(FPGA-TN-02298\)](#) and the [Lattice Nexus 2 sysCLOCK PLL Design User Guide \(FPGA-TN-02364\)](#).

2.3. Attribute Summary

The configurable attributes of the PLL Module are shown in [Table 2.2](#). The attributes can be configured through the IP Catalog Module/IP wizard of the Lattice Radiant Software.

Table 2.2. Attributes Table

Attribute	Selectable Values	Default	Description
General			
Set Minimum VCO Frequency (MHz)	—	1600	Display only. Minimum VCO frequency.
Set Maximum VCO Frequency (MHz)	—	4000	Display only. Maximum VCO frequency.
Set Maximum Error Option	Use large multiplication factor to reduce error, Use reasonable tolerance (NF <= 128), Find solution with lowest error, Use specified tolerance value	Find solution with lowest error	Select the tolerance mode that the script considers when calculating the PLL parameters.
Set Number of Clock Outputs	1–7	1	Specify the number of PLL clock outputs.
Enable Fractional Accumulation (Dithering)	Checked, Unchecked	Checked	Enables the fractional feedback divider; otherwise, the feedback divider uses integer values only.
Enable Spread Spectrum Clock Generation	Checked, Unchecked	Unchecked	Enables Spread Spectrum Clock Generation.
Synchronize CLKOUT Enable to CLKOP	Checked, Unchecked	Unchecked	
Select Output Divider Path	—	External Output Divider (1–256)	Display only.
Actual VCO Frequency	Calculated	—	Display only.
Reference Clock			
Reference Clock: Frequency (MHz)	10–800	100	Set the Reference Clock frequency.
Reference Clock: Divider Actual Value	Calculated	—	Display only.
Phase Detector Frequency (MHz)	Calculated	—	Display only.
Feedback			
Select Feedback Clock	Internal VCO, CLKOP, CLKOS, CLKOS2, CLKOS3, CLKOS4,	Internal VCO	Select the feedback clock from the enabled PLL clock outputs or internal VCO. The feedback clock is the internal VCO if

Attribute	Selectable Values	Default	Description
	CLKOS5, CLKOPHY		Fractional-N or Spread Spectrum Clock is enabled.
Feedback Clock: Actual Divider Value (Float)	Calculated	—	Display only (Integer + Fractional).
Feedback Clock: Actual Divider Value (Integer)	Calculated	—	Display only.
Feedback Clock: Actual Divider Value (Fractional)	Calculated	—	Display only (value/256).
Feedback Clock: Actual Divider Value (Fractional-SSC)	Calculated	—	Display only (value/16384).
Spread Spectrum – Applicable only if Spread Spectrum Clock Generation is enabled			
Spread Spectrum Profile	—	Down Spread	Display Only.
Bandwidth Adjustment Factor	0.5–2.0	1	Set the bandwidth adjustment factor.
Desired Modulation Frequency kHz	15–4000	30	Set the spreading frequency.
Actual Modulation Frequency kHz	Calculated	—	Display only.
Triangle Modulation Depth %	0.0244–10.0	2.5	Set the modulation depth.
Actual Triangle Modulation Depth %	Calculated	—	Display only.
SSC Minimum Feedback Divider	Calculated	—	Display only.
Spreading Slope Control Value	Calculated	—	Display only.
Spreading Rate Divider Value	Calculated	—	Display only.
Clock Output [n], n = 0 – 6			
CLKOUT [n]: Port Name	CLKOP, CLKOS, CLKOS2, CLKOS3, CLKOS4, CLKOS5, CLKOPHY	CLKOP	Select which PLL clock to configure.
CLKOUT [n]: Bypass	Checked, Unchecked	Unchecked	Bypass the actual divider output and output the reference clock instead.
CLKOUT [n]: Desired Frequency Value (MHz)	15.625–1250 MHz For CLKOPHY: 400–2400 MHz	100	Set the desired Output Clock frequency.
CLKOUT [n]: Actual Frequency Value (MHz)	Calculated	—	Display Only.
CLKOUT [n]: Actual Divider Value	Calculated	—	Display Only.
CLKOUT [n]: Tolerance (%)	0–10	0.0	Set the acceptable tolerance for actual vs desired output frequency. Available only if the selected <i>Maximum Error Option</i> is “Use specified tolerance value”.
CLKOUT [n]: ERROR (PPM)	Calculated	0	Display Only. Difference between desired and actual frequencies.
CLKOUT [n]: Static Phase Shift (Degrees)	0, 45, 90, 135, 180, 225, 270, 315	0	Set the desired clock output phase.
Optional Ports			
Dynamic Phase Control Ports			
Enable Dynamic Phase Ports	Checked, Unchecked	Unchecked	Enable/Disable dynamic phase control ports.
Clock Enable Ports			
CLKOUT [n] Enable Port	Checked, Unchecked	Unchecked	Set to provide clock enable port.
PLL Reset			
Provide PLL Reset	Checked, Unchecked	Unchecked	Set to provide PLL reset port.

Attribute	Selectable Values	Default	Description
PLL Lock			
Provide PLL Lock Signal	Checked, Unchecked	Unchecked	Set to provide PLL lock port.
Enable Fast Lock	Checked, Unchecked	Unchecked	Set the behavior of PLL lock signal.
Register Interface			
Select Register Interface	None, APB, LMMI	None	Select the type of register interface.
Miscellaneous Ports			
Enable Misc Port	Checked, Unchecked	Unchecked	Set to provide optional status ports.

3. IP Generation and Evaluation

This section provides information on how to generate the PLL Module using the Lattice Radiant software and how to run simulation and synthesis. For more information about the Lattice Radiant software, refer to the Lattice Radiant Software User Guide.

3.1. Licensing the IP

No license is required for this IP module.

3.2. Generating and Synthesizing the IP

The Lattice Radiant software allows you to generate and customize modules and IP and integrate them into the device architecture.

To generate the PLL Module:

1. Create a new Lattice Radiant Software project or open an existing project.
2. In the **IP Catalog** tab, double-click on **PLL** under **Module, Architecture_Modules** category. The **Module/IP Block Wizard** opens as shown in [Figure 3.1](#). Enter values in the **Instance name** and the **Create in** fields and click **Next**.

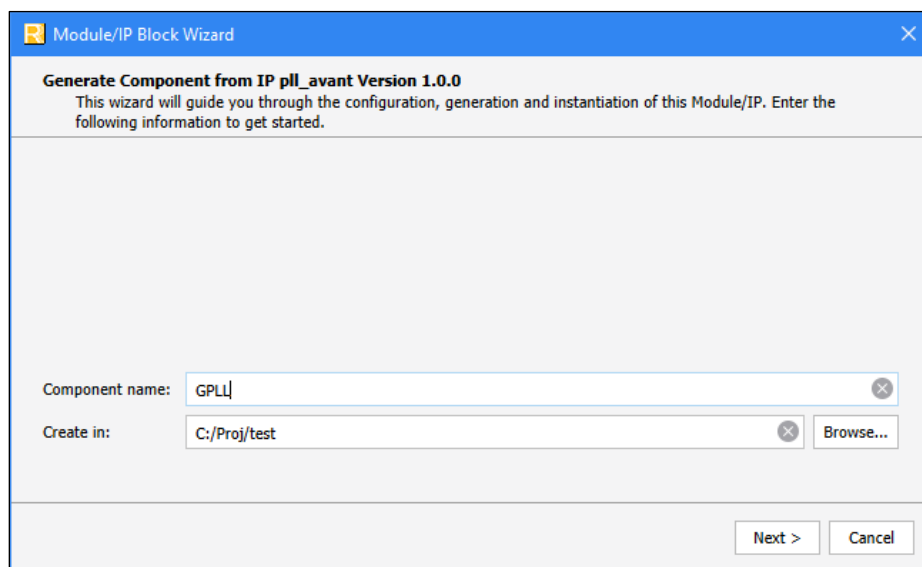


Figure 3.1. Configure Module/IP Block Wizard

3. In the module dialog box of the **Module/IP Block Wizard** window, customize the selected PLL Module using drop-down menus and checkboxes. As a sample configuration, see [Figure 3.2](#). For configuration options, see the [Attribute Summary](#) section.

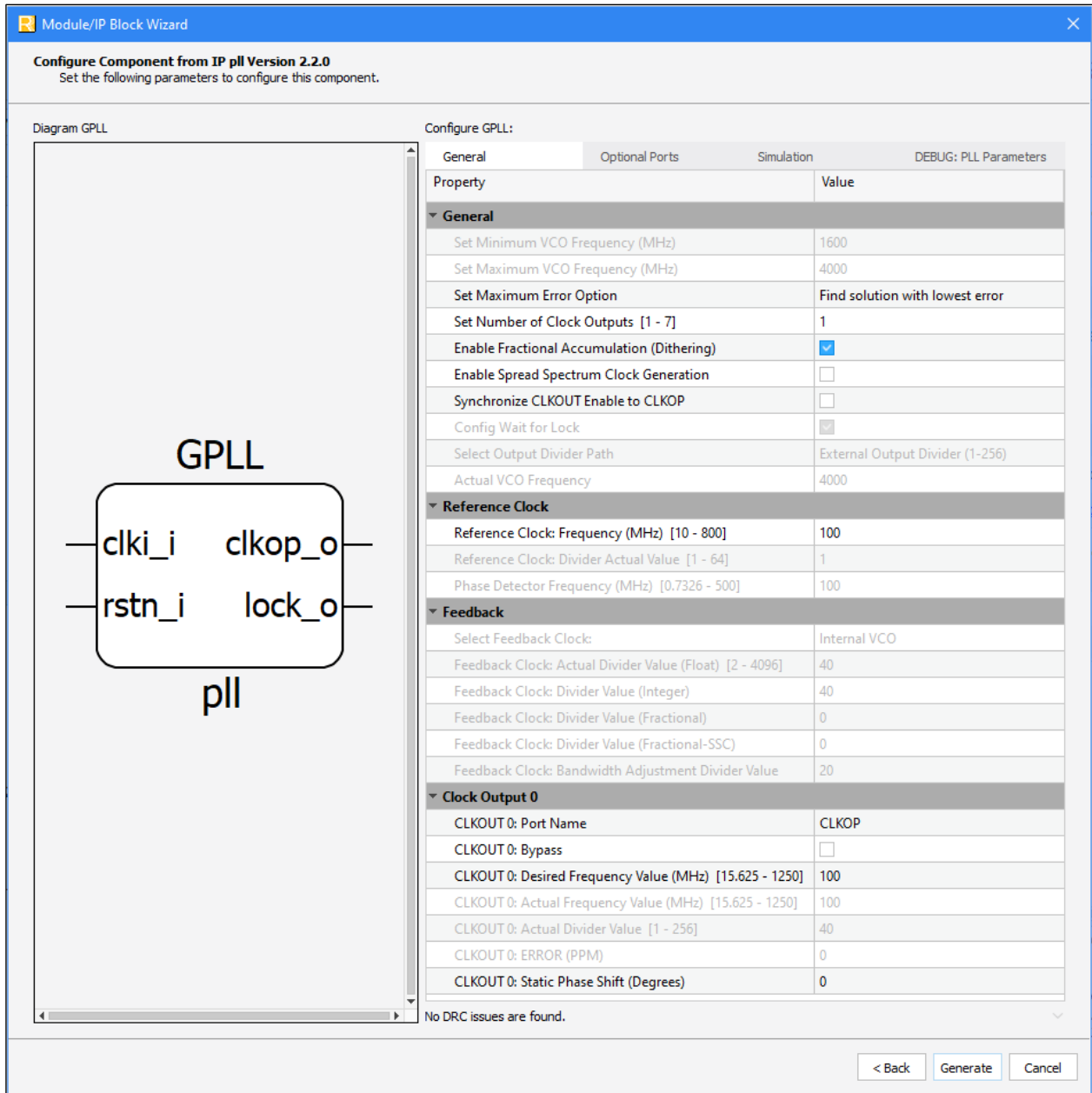


Figure 3.2. Configure User Interface of PLL Module

- Click **Generate**. The **Check Generating Result** dialog box opens, showing design block messages and results as shown in [Figure 3.3](#).

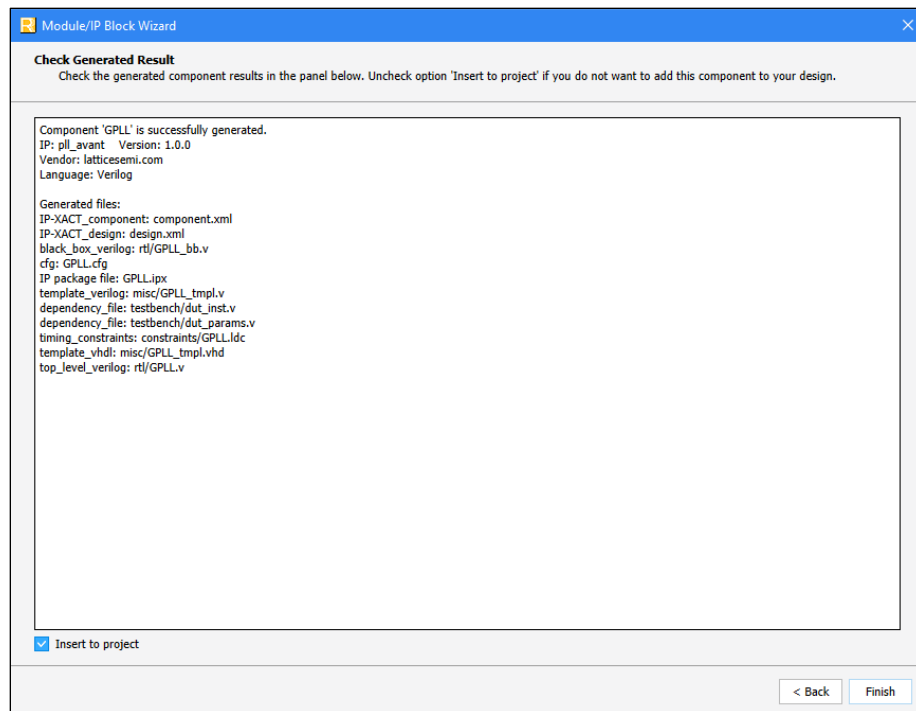


Figure 3.3. Check Generating Result

- Click **Finish**. All generated files are placed under the directory paths specified in the **Create in** and **Instance name** fields are shown in [Figure 3.1](#).

The generated PLL Module package includes the closed-box (<Instance Name>_bb.v) and instance templates (<Instance Name>_tmpl.v/vhd) that can be used to instantiate the module in a top-level design. An example RTL top-level reference source file (<Instance Name>.v) that can be used as an instantiation template for the module is also provided. You may also use this top-level reference as the starting template for the top-level for your complete design. The generated files are listed in [Table 3.1](#).

Table 3.1. Generated File List

File Name	Description
<Instance Name>.ipx	This file contains the information on the files associated with the generated IP.
<Instance Name>.cfg	This file contains the attribute values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration attributes of the IP in IP-XACT 2014 format.
rtl/<Instance Name>.v	This file provides an example RTL top file that instantiates the module.
rtl/<Instance Name>_bb.v	This file provides the synthesis closed-box.
misc/<Instance Name>_tmpl.v misc/<Instance Name>_tmpl.vhd	These files provide instance templates for the module.

3.3. Running the Functional Simulation

Functional simulation can be performed after the IP is generated and the testbench is added. For this module, an example testbench is provided.

To add the generated testbench:

- Go to **File List** tab, right-click **Input Files**.
- Click **Add > Existing Simulation File**.
- A window appears. Open the instance folder **testbench**, then double-click **tb_top.v**.

To run the simulation:

1. Click the  button located on the **Toolbar** to initiate **Simulation Wizard**, as shown in [Figure 3.4](#).

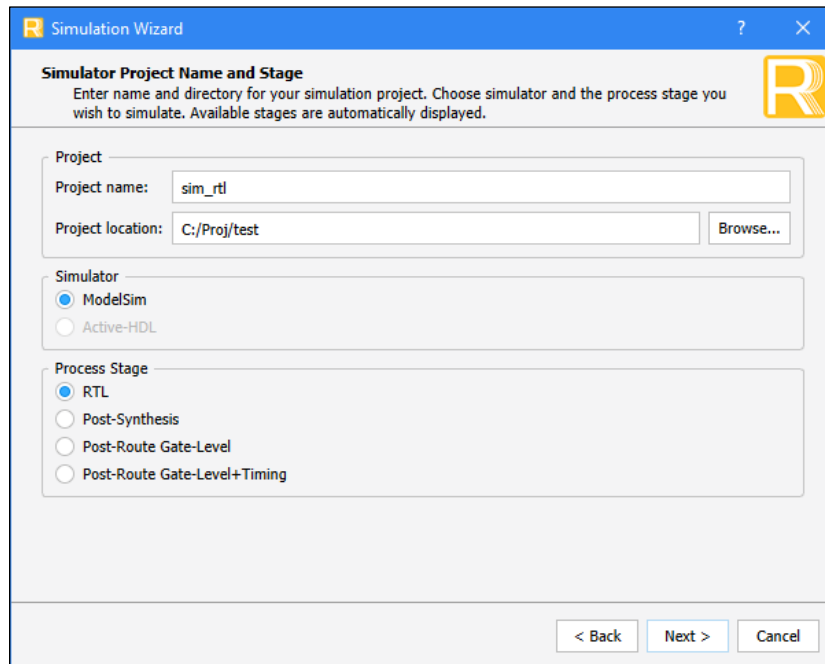


Figure 3.4. Simulation Wizard

2. Click **Next** to open the **Add and Reorder Source** window as shown in [Figure 3.5](#).

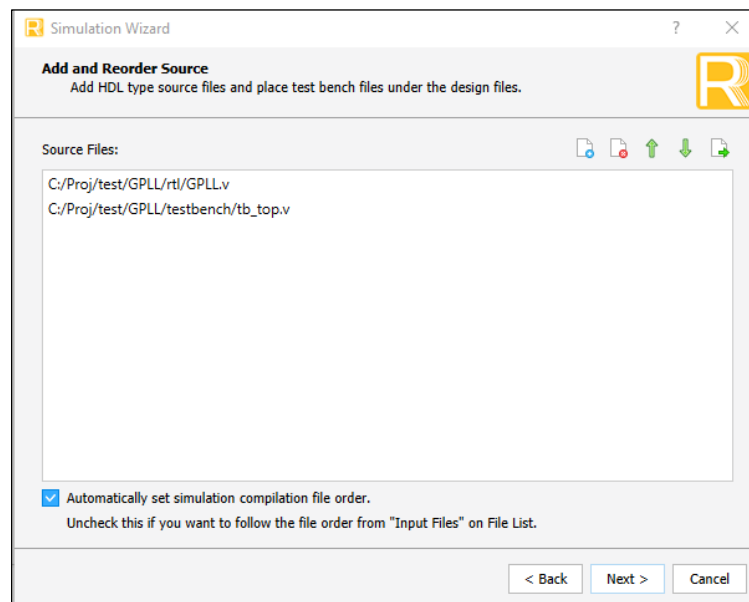


Figure 3.5. Adding and Reordering Source

Note: Follow the procedure above until the simulation is fully automated in the Lattice Radiant software. The simulation results for this example are shown in [Figure 3.6](#).

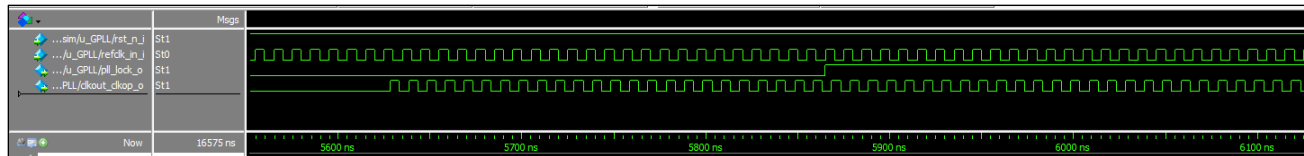


Figure 3.6. Simulation Waveform

Note: If you create your own testbench, follow these guidelines:

- If the PLL Reset is disabled in the IP Generation GUI, you must add the following line to your custom testbench:

```
defparam <tb_module_name>.<pll_inst_name_in_tb_file>.<pll_inst_name_in_top_file>.lsccl_pll_inst.SIMULATION = 1;
```

The PLL has a soft logic that requires initialization or reset; otherwise, the simulation may fail because of uninitialized registers and propagation of x. This is only true for simulation as the FPGA fabric is reset after power on in actual implementation.
- If the PLL Reset is enabled in the IP Generation GUI, you must toggle the reset at the beginning.

3.4. PLL Constraint Guidelines

Follow these guidelines to constrain the PLL clocks correctly:

- The clock must be defined on the top-level port that feeds the reference clock pin of the PLL using the create_clock constraints. If this is not followed:
 - Insertion delay is inaccurate.
 - The relationship between PLL output clocks is lost if clocks are defined at the output of the PLL using create_clock constraint.
- Define create_generated_clocks yourself, or preferably let the timing engine generate the signals at the PLL output pins.
- When using the PLL lock (lock_o) signal, add a set_false_path constraint from the lock_o signal. An example of the constraint is as follows:

```
set_false_path -through [get_nets <pll lock signal>]
```

Define clock at port

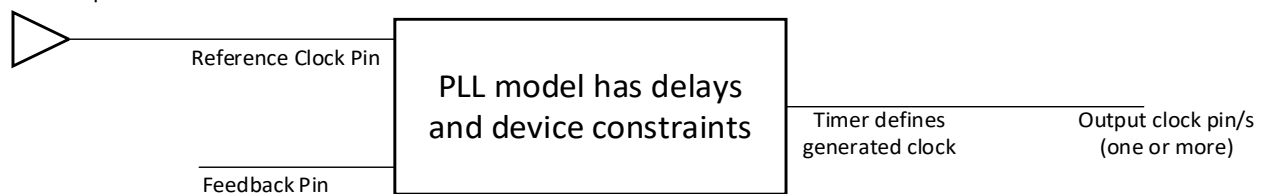


Figure 3.7. PLL Using the create_clock Constraints

3.5. Hardware Evaluation

There is no restriction on the hardware evaluation of this module.

References

- [Lattice Avant PLL Module Release Notes \(FPGA-RN-02066\)](#)
- [Lattice Avant sysCLOCK PLL Design User Guide \(FPGA-TN-02298\)](#)
- [Lattice Nexus 2 sysCLOCK PLL Design User Guide \(FPGA-TN-02364\)](#)
- [Lattice Radiant Timing Constraints Methodology \(FPGA-AN-02059\)](#)
- [Avant-E web page](#)
- [Avant-G web page](#)
- [Avant-X web page](#)
- [Certus-N2 web page](#)
- [Mach-N2 web page](#)
- [Lattice Radiant Software web page](#)
- [Lattice Insights web page for Lattice Semiconductor training courses and learning plans](#)

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/en/Support/AnswerDatabase.

Revision History

Note: In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

Revision 1.6, IP v2.7.1, October 2026

Section	Change Summary
All	- Renamed document from <i>Lattice Avant PLL Module</i> to <i>Lattice Avant/Nexus 2 PLL Module</i>. - Added a note on IP version in Quick Facts and <i>Revision History</i> sections. - Performed minor formatting and editorial edits.
Acronyms in This Document	Updated list of acronyms.
Introduction	Added Table 1.1. Quick Facts as follows: - Renamed <i>Supported FPGA Families</i> to <i>Supported Devices</i>, and added Certus-N2 and Mach-N2 devices. - Removed the <i>Targeted Devices</i> row. - Updated IP version.
Functional Description	- Updated Figure 2.1. GPLL Top Level Block Diagram. - Updated Table 2.1. PLL Module Signal Description as follows: - Updated the port name for <code>apb_pwdata_i [31:0]</code> and <code>apb_prdata_o [31:0]</code>, and updated the width. - Updated the note to the LMMI interface and APB interface. - Added the <i>Select Register Interface</i> attribute in Table 2.2. Attributes Table.
References	Updated references.

Revision 1.5, IP v2.6.0, April 2025

Section	Change Summary
Introduction	Added IP changes and updated IP version in Table 1.1. Quick Facts .
IP Generation and Evaluation	Added constraint on the PLL lock (<code>lock_o</code>) signal in the PLL Constraint Guidelines section.
References	Added link to the IP release notes.

Revision 1.4, October 2024

Section	Change Summary
Functional Description	Removed the <i>Config Wait for Lock</i> attribute in Table 2.2. Attributes Table .
IP Generation and Evaluation	Added a note on the guidelines to create testbench in the Running the Functional Simulation section.

Revision 1.3, June 2024

Section	Change Summary
All	Renamed document from <i>PLL Module User Guide</i> to <i>Lattice Avant PLL Module User Guide</i> .
Introduction	Updated targeted devices and software version in Table 1.1. Quick Facts .
Functional Description	- Updated the description for <code>rst_n_i</code> port in Table 2.1. PLL Module Signal Description. - Updated the <i>Config Wait for Lock</i> attribute in Table 2.2. Attributes Table.
References	Updated references.

Revision 1.2, December 2023

Section	Change Summary
All	Changed the document name from <i>PLL Module - Lattice Radiant Software</i> to <i>PLL</i>

Section	Change Summary
	<i>Module.</i> Minor adjustments to ensure that the document is consistent with Lattice Semiconductor's inclusive language policy.
Disclaimers	Updated boilerplate.
Inclusive Language	Added boilerplate.
Introduction	Updated the device name from <i>LAV-AT-E500</i> to <i>LAV-AT-E70</i> in Table 1.1.
IP Generation and Evaluation	Added PLL Constraint Guidelines section and updated header number for Hardware Evaluation section.
References	- Updated the names of all the listed web pages. - Added reference to the <i>Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059)</i> document.

Revision 1.1, August 2023

Section	Change Summary
Functional Description	- Updated Table 2.1. PLL Module Signal Description to correct the description for <i>phasedir_i</i>. - Updated Table 2.2. Attributes Table.
IP Generation and Evaluation	Updated Figure 3.2. Configure User Interface of PLL Module.
References	Updated to add website links for the Avant-E and Lattice Insights.
Technical Support Assistance	Added reference link to the Lattice Answer Database.

Revision 1.0, November 2022

Section	Change Summary
All	Initial release.



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