Lattice Radiant 3.2 Software Release Notes

Welcome to Lattice Radiant® software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs).

What's New in Radiant 3.2 Software

- **Device Support:**
  - MachXO5™-NX (LFMXO5)
    - 25K (-7/-8/-9) HP/LP 1.0V (COM/IND) – BBG256
    - 25K (-7/-8/-9) HP/LP 1.0V (COM/IND) – BBG400
  - CrossLink™-NX (LIFCL)
    - 33K (-7/-8) HP/LP 1.0V (COM) – WLCSP84
    - 33K (-8) HP/LP 1.0V (IND) – WLCSP84

- **Tool and Other Enhancements:**

  - **License Debugger –** The License Debug tool now displays all Network Feature Card (NIC) IDs. A direct link to LmTools has also been added to access the license server.

  - **Power On Reset (POR) Debug** – This new feature has been added to the Reveal Analyzer/Controller tool for the Radiant 3.2 software.
  - **Programmer, Reveal Logic Analyzer/Controller, SEI Editor**
    - These tools have been updated to support the MachXO5-NX (LFMXO5) and CrossLink-NX (LIFCL-33) devices with bitstream generation capability and full encryption/ authentication.
    - Added I3C Bridge support to Programmer.

  - **Radiant File Type Support –** The "Force File Type" option has been added to the "Add Existing File" dialog box. This new feature allows users to change their file types to Verilog or VHDL.

  - **Radiant Project File** – The Radiant Project (.rdf) file has been updated to include the Radiant version number.

  - **Simulation Wizard** – The Simulation Wizard tool has been updated. Users can now specify the simulation run length if the "Run simulation" option is selected.

  - **Timing Analyzer –** The "-datapath_only" option has been added to the set_max_delay constraint.

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Radiant software, it may be necessary to re-create some IP, per the procedures described in the following table.

These procedures adapt the project for the changes in Radiant software.

Versions	IP		IP Regeneration Procedures
	CrossLink-NX (LIFCL), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP)	**iCE40UP**	
3.2	ADC_Sequencer (Analog to Digital Converter with Sequencer)	N/A	These IP used in designs created in Radiant 3.1.1 or earlier must be re-generated in Radiant 3.2.
	MPCS (Multi-Protocol PCS)		
	FIFO		
	FIFO_DC (Dual Clock FIFO)		
	RAM_DP (Dual Port RAM)		
3.1.1	PLL (Phase Locked Loop)	N/A	These IP used in designs created in Radiant 3.1 or earlier must be re-generated in Radiant 3.1.1.
	ADC (Analog to Digital Converter)		
	ROM (Read-only Memory)		
	MPCS (Multi-Protocol PCS)		
	DDR_Generic (DDR Generic Interfaces)		
	GDDR7:1 (LVDS Interface)		
	DDR_MEM (DDR Memory Interfaces)		
	LPDDR4_MEM (LPDDR4 Memory Interface)		
	MIPI_DPHY (MIPI D-PHY Interface)		
	ADC_Sequencer (Analog to Digital Converter with Sequencer)		
3.1	PLL (Phase Locked Loop)	N/A	These IP used in designs created in Radiant 3.0 or earlier must be re-generated in Radiant 3.1.
	DDR_Generic (DDR Generic Interfaces)		
	GDDR7:1 (LVDS Interface)		
	DDR_MEM (DDR Memory Interfaces)		
	LPDDR4_MEM (LPDDR4 Memory Interface)		
	MIPI_DPHY (MIPI D-PHY Interface)		
	ADC_Sequencer (Analog to Digital Converter)		
	Large_RAM_DP (Dual Port Large RAM)		
	Large_RAM_DP_True (True Dual Port Large RAM)		
	Large_RAM_SP (Single Port Large RAM)		
	Large_ROM (Read-only Large Memory)		
	FIFO_DC (Dual Clock FIFO)		
	Complex Mult		
	MPCS (Multi-Protocol PCS)		
3.0	PLL (Phase Locked Loop)	N/A	These IP used in designs created in Radiant 2.2.1 or earlier must be re-generated in Radiant 3.0.
	DDR_Generic (DDR Generic Interfaces)		
	GDDR7:1 (LVDS Interface)		
	DDR_MEM (DDR Memory Interfaces)		
	MIPI_DPHY (MIPI D-PHY Interface)		
	LFSR (Linear Feedback Shift Register)		
	ADC_Sequencer (Analog to Digital Converter)		
	RAM_DP_True (True Dual Port RAM)		
	RAM_DQ (Single Port RAM)		
	ROM (Read-only Memory)		
	FIFO		

Versions	IP		IP Regeneration Procedures
	CrossLink-NX (LIFCL), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP)	**iCE40UP**	
	FIFO_DC		
	Shift Register		
	Sine-Cosine Table		
	Convert		
2.2.1	PLL (Phase Locked Loop)	N/A	These IP used in designs created in Radiant 2.2 or earlier must be re-generated in Radiant 2.2.1.
	DDR_Generic (DDR Generic Interfaces)		
	GDDR7:1 (LVDS Interface)		
	DDR_MEM (DDR Memory Interfaces)		
	MIPI_DPHY (MIPI D-PHY Interface)		
	LFSR (Linear Feedback Shift Register)		
	ADC_Sequencer (Analog to Digital Converter)		
	RAM_DP (Pseudo Dual Port RAM)		
2.2	PLL (Phase Locked Loop)	PLL (Phase Locked Loop)	These IP used in designs created in Radiant 2.1 or earlier must be re-generated in Radiant 2.2.
	DDR_Generic (DDR Generic Interfaces)		
	GDDR7:1 (7:1 LVDS Interface)		
	SDR (Single Data Rate)		
	DDR_MEM (DDR Memory Interfaces)		
	ADC (Analog to Digital Converter)		
	SEDC (Soft Error Detection/Correction)		
	Sin_Cos_Table (Sine Cosine Table)		
	OSC (Oscillator)		
	RAM_DQ (Single Port RAM)		
	RAM_DP_True (True Dual Port RAM)		
	FIFO		
	FIFO_DC (FIFO Dual Clock)		
2.1	PLL (Phase Locked Loop)	N/A	These IP used in designs created in Radiant 1.0, 2.0, or 2.0 SP1 or earlier must be re-generated in Radiant 2.1.
	GDDR7:1 (7:1 LVDS Interface)		
	DDR_MEM (DDR Memory Interfaces)		
	DDR_Generic (DDR Generic Interfaces)		
	MIPI_DPHY (MIPI Interface)		
	ADC (Analog to Digital Converter)		
	SEDC (Soft Error Detection/Correction)		
	OSC (Oscillator)		

All IP:

- Starting with Radiant 2.1, PMIs for any IP created in Radiant software versions 1.0, 2.0, 2.0 SP1, user must add the Family attribute in all PMI instantiations.
- For designs created in previous versions of Radiant software (2.0 or prior), it is necessary to re-generate PLL IP in Radiant software 2.1. Otherwise, Radiant software 2.1 will issue an error when the previous generated PLL IP is detected in the design. Designs created using Radiant Software 2.0 SP1 with PLL will work without any errors.
- The IO_TYPE HDL attribute default value has been changed since Radiant 2.0 SP1 from LVCMOS18 to LVCMOS33.
- If a LARGE_RAM IP generated from a previous Radiant version needs to be re-configured in Radiant 2.1, the IP must be re-created.

The following server IP are not compatible with Radiant 3.0 onwards. Use the latest versions of the IP available on the IP server:

- I2C Master version 1.0.3
- UART 16550 version 1.0.4

- DDR3 SDRAM Controller version 1.1.1
- DDR3 SDRAM Controller version 1.2.1
- LPDDR2 SDRAM Controller Lite version 1.1.1
- LPDDR2 SDRAM Controller Lite version 1.2.1

Supported Devices

Lattice Radiant software can be used with either a free license or a subscription license. The two licenses provide access to different device families.

Device Family	Free License	Subscription License
iCE40UP (iCE40 UltraPlus)	◀	◀
CertusPro™NX (LFCPNX)		◀
Certus™-NX (LFD2NX)	◀	◀
CrossLink™-NX (LIFCL)	◀	◀
Certus™-NX-RT (UT24C)		◀
CertusPro™-NX-RT (UT24CP)		◀
MachXO5-NX (LFMXO5)		◀

Support for Third-Party Synthesis and Simulator Tools

The Synopsys Synplify Pro® for Lattice synthesis tool and the Siemens ModelSim® Lattice Edition simulator tools are included in the Radiant software.

- **Synopsys Synplify Pro FPGA synthesis software version S-2021.09LR-1**
  - Release Notes for Synplify Pro are located in ..\<*install_directory*>\radiant\3.2\synpbase\doc\. The file name is release_notes.pdf.
  - A full set of documents for Synplify Pro are also located in ..\<*install_directory*>\radiant\3.2\synpbase\doc\.
- **Siemens ModelSim Lattice Edition 2021.4 revision 2021.10**

- Release Notes for ModelSim Lattice Edition are located in ..\<*install_directory*>\radiant\3.2\modeltech\. The file names are RELEASE_NOTES.html or RELEASE_NOTES.txt.
- A full set of documents for ModelSim Lattice Edition are located in ..\<*install_directory*>\radiant\3.2\modeltech\doc\.

- **Siemens Questa® 2020.4**
- **Cadence Xcelium® 20.09-s004**
- **Synopsys VCS® Q-2020.03**

Help Resources

Available information resources for the Radiant software include the following:

- Online Help updated with CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), and CertusPro-NX-RT (UT24CP) content.
- To view the Online Help, start the Lattice Radiant software and select the  "Getting Started" icon under Information Center.

System Requirements

The following shows the basic system requirements for Radiant software:

- Intel Pentium or Pentium-compatible PC
- 64-bit OS:
  - Windows 10
  - Red Hat Enterprise Linux 7.8 or 8.4
  - Ubuntu version 18.04 LTS or 20.04 LTS
  - CentOS 7.8 or 8.4
- Approximately 10 GB free disk space
- Computer Memory Requirement:
  - Nexus – 16GB
- 1024 X 768 graphics display
- Network adapter for license and network connectivity
- A Web browser with JavaScript capability
- Acrobat Reader

Issues Fixed

The following known issues are fixed in this release. Their workarounds are no longer needed.

CSI-2/D-PHY Transmitter IP hangs during Post synthesis/PAR simulations.

Devices affected: CrossLink-NX (LIFCL), Certus-NX (LFD2NX)

Bug number: DNG-9697

Fixed in Radiant 3.1.1

Modify default INIT value for HardDPHY RX soft IP when running at DPHY v1.1 data rate (<=1.5 Gbps).

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-10731

Fixed in Radiant 3.1.1

When you program a target device with designs involving EBRs with initial data, the initial data programmed into the EBRs may output incorrectly.

Devices affected: CrossLink-NX (LIFCL), Certus-NX (LFD2NX), CertusPro-NX (LFCPNX)

Bug number: DNG-11514

Fixed in Radiant 3.1.1

When Reveal is used with mixed language design projects, synthesis may fail using both LSE and Synplify Pro.

Devices affected: CrossLink-NX (LIFCL), Certus-NX (LFD2NX), CertusPro-NX (LFCPNX)

Bug number: DNG-11576

Fixed in Radiant 3.1.1

ADC Soft-IP “ADC Clock Divide” value must be a string.

Devices affected: CrossLink-NX (LIFCL), Certus-NX (LFD2NX), CertusPro-NX (LFCPNX)

Bug number: DNG-12220

Fixed in Radiant 3.1.1

Reveal Eye Opening Diagram cannot be generated on Linux OS.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-12259

Fixed in Radiant 3.1.1

Known Issues for Radiant 3.2

The following are known issues for the Radiant Software 3.2.

MAP incorrectly reports number of DPHY and PCIE/ADC resources for CrossLink-NX (LIFCL) QFN72 package.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-8297

When simulating Generic DDR, there may be a mismatch in the RTL and post-route simulation. Silicon is not affected.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: All except iCE40UP

Bug number: DNG-9639

For some SystemVerilog designs, Synplify Pro may fail to identify multi-driven nets and the flow passes with no errors.

Workaround: Check the design for multi-driven nets and run the flow using LSE to verify.

Devices affected: All except iCE40UP

Bug number: DNG-10132

Lattice Synthesis Engine (LSE) incorrectly reduces the number of valid states of the extracted state machine (FSM).

When a state machine in the design has unreachable states, synchronous set/reset, and the states are set to non-full zero value, LSE could incorrectly remove reachable state when cleaning up unreachable states. State machine not synchronously reset to all-0 states is not commonly seen.

Devices affected: All except iCE40UP

Bug number: DNG-11412

When Reveal Controller is used for updating the PCS register (reg80) through the controller, it will cause the PCS Register value to be stuck at a value during successive writes.

Workaround: Re-download the bitstream.

Devices affected: CertusPro-NX (LFCPNX), CertusPro-NX-RT (UT24CP)

Bug number: DNG-12235, DNG-13920

If you have a Hard IP in the design and are controlling it with Reveal Controller, Reveal Controller logic will overwrite the user logic which controls the Hard IP.

If LMMI bus IP is used as part of your design for dynamic update, it is recommended to not use the Reveal Controller for hard IP because the user design controlling the hard IP will be overwritten by Reveal Controller Logic.

Hard IPs: DPHY, I2CFIFO, PLL, PCS, PCIELL, SGMIICDR

Devices affected: All except iCE40UP

Bug number: DNG-12253

When using Synplify-Pro OEM tool, if the input widths are above a certain value (58x58) and the LUT implementation is selected, the complex mult IP will infer too many LUT4 and will not fit on the device, causing an error in MAP.

Workaround: Use LSE synthesis tool to synthesize affected designs.

Devices affected: All except iCE40UP

Bug number: DNG-12337

LSE might produce an incorrect netlist while expanding an if-statement inside a for loop if the expanded multiplexer/decoder gets constant inputs.

Workaround: Set "Resource Sharing" to "F(alse)" in "LSE Strategy Settings."

Devices affected: All devices

Bug number: DNG-12813

If ECLKSYNC input is driven by PLL output, there is no output from ECLKSYNC.

Workaround: Do not use the PLL clock output to ECLKSYNC.

Devices affected: CrossLink-NX (LIFCL 33K)

Bug number: DNG-13841

Reveal Power-on Reset (POR) Debug function does not work when using LSE.

Workaround: Use Synplify Pro.

Devices affected: All except iCE40UP

Bug number: DNG-12861, DNG-13901

In certain cases, the Synplify-Pro OEM synthesis tool will error out when reveal is inserted with error message reporting, @E: FO139 "The instance needs internal tristate. Can't be mapped."

Workaround: Use LSE for synthesis or disable Reveal Inserter.

Devices affected: All except iCE40UP

Bug number: DNG-13017

The CSI-2/DSI D-PHY Transmitter and Receiver Soft IP simulations fail when using Synopsys VCS as simulation tool.

Workaround: Use Modelsim, QuestaSim, or Aldec-HDL simulation tools.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-13225

LSE may issue an error: ".. entity 'xxx' is not compiled yet. VHDL-1059 and abort" when the following conditions are met:

1. Verilog module and VHDL entity have the same name.

2. VHDL "entity" and its "architecture" are split into two files.

3. When the "entity" is entered below the "architecture" file in the Radiant Project File list.

Workaround: In the Radiant Project File list, move the "entity" file above its "architecture" file.

Devices affected: All devices

Bug number: DNG-13231

When using LSE, user may encounter a linking issue between the Verilog and VHDL versions of the design module.

When you declare a module in a VHDL file, the content gets defined in another Verilog file.

Workaround: Declare and define the module in the same HDL library in the same language.

Devices affected: All devices

Bug number: DNG-13531

When set_max_delay constraint with a -datapath_only option is used, Radiant timer incorrectly calculates setup/hold times.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: All except iCE40UP

Bug number: DNG-13551, DNG-13555

When using Synplify-Pro OEM tool, set_multicycle_path with the -hold options defined in the pre-synthesis constraint file may not be forward annotated to Post-Synthesis Timing, MAP, and PAR.

Workaround: Define the constraint in a post synthesis constraint file. If Post-Synthesis timing is necessary. Edit the Synplify-Pro output .ldc file to include the dropped contraint, then rerun Post-Synthesis and Timing using the Tcl console.

Devices affected: All devices

Bug number: DNG-13681

The timing path of the DQSBUF, DQSW, and DQSW270 ports are missing from the timing report.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: All except iCE40UP

Bug number: DNG-13835