AXI4 to AHB-Lite Bridge Module

IP Version: 1.5.0

User Guide

FPGA-IPUG-02199-1.6

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This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AMBA	Advanced Micro-controller Bus Architecture
AXI	Advanced Extensible Interface Bus
AHB	Advanced High-performance Bus
FPGA	Field Programmable Gate Array
RTL	Register Transfer Level

1. Introduction

The Lattice Semiconductor AXI4 to AHB-Lite Bridge Module provides an interface between the high-speed AXI4 and AHB-Lite.

The design is implemented in Verilog HDL. Table 1.1 indicates the software used for IP configuration, generation, and implementation.

Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation

Supported Devices	IP Configuration and Generation	IP Implementation (Synthesis, Map, Place and Route)
LatticeECP3™	Lattice Propel™ Builder software	Lattice Diamond™ software
ECP5™	Lattice Propel Builder software	Lattice Diamond software
CrossLink™-NX	Lattice Propel Builder software	Lattice Radiant™ software
Certus™-NX	Lattice Propel Builder software	Lattice Radiant software
Certus-N2	Lattice Propel Builder software	Lattice Radiant software
MachXO5™-NX	Lattice Propel Builder software	Lattice Radiant software
CertusPro™-NX	Lattice Propel Builder software	Lattice Radiant software
Lattice Avant™	Lattice Propel Builder software	Lattice Radiant software

1.1. Features

The key features of the AXI4 to AHB-Lite Bridge Module include:

- Compliance with AMBA AXI4 and AMBA 3 AHB-Lite Protocol
- Support for configurable data interface: 8, 16, 32, 64, 128, 256, 512, and 1024
- Support for configurable AXI4 ID width: 1 to 11
- Support for configurable AXI4 user width: 1 to 128
- Support for AXI4 INCR and fixed burst transfers
- Number of supported AHB-Lite subordinates is one
- Registered output

1.2. Limitations

- AXI4 wrap burst not supported.
- AxQOS, AxREGION, AxUSER, AxCACHE, and AxLOCK, AxWSTRB are considered as don't care.
- AxPROT is a pass through to the AHB-Lite interface.
- Unaligned transfers are not supported in burst transfers and consistently respond with SLVERR.

2. Functional Descriptions

2.1. Overview

The Lattice Semiconductor AXI4 to AHB-Lite Bridge Module is used for interfacing one AXI4 Manager to one AHB-Lite Subordinate. When interfacing to multiple AHB-Lite Subordinates, this IP should be used together with an AHB-Lite interconnect. The read and write transfers on the AXI4 are converted into equivalent transfers on the AHB-Lite.

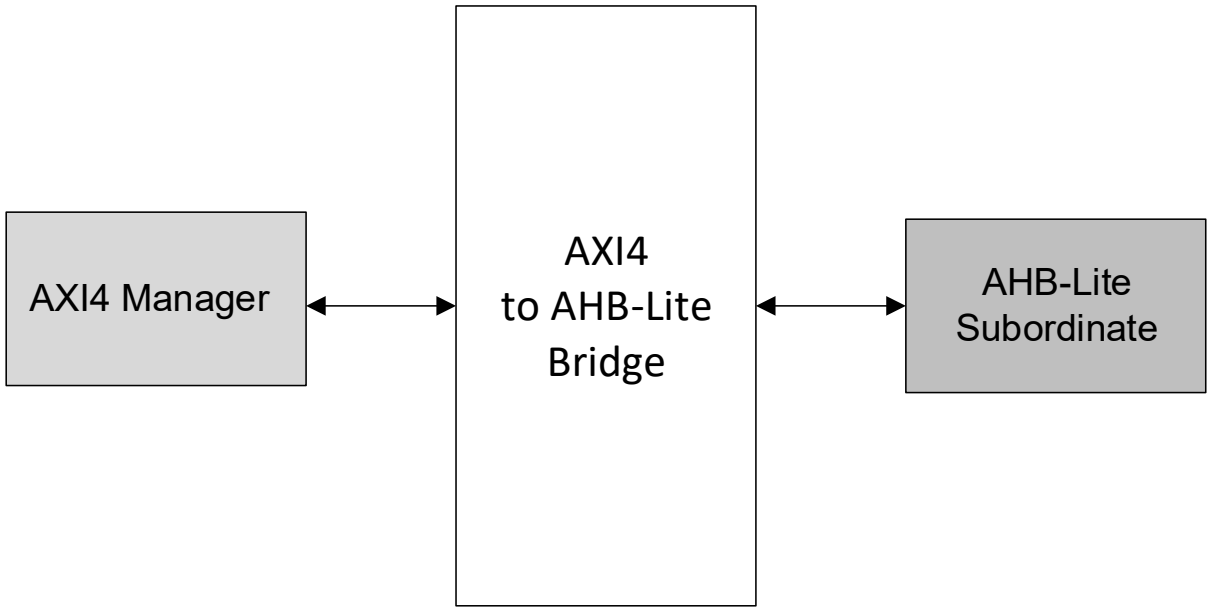

Figure 2.1. AXI4 to AHB-Lite Bridge

2.2. Interface Description

Figure 2.2 shows the interface diagram of the AXI4 to AHB-Lite Bridge Module. The diagram shows all the available ports for the IP core.

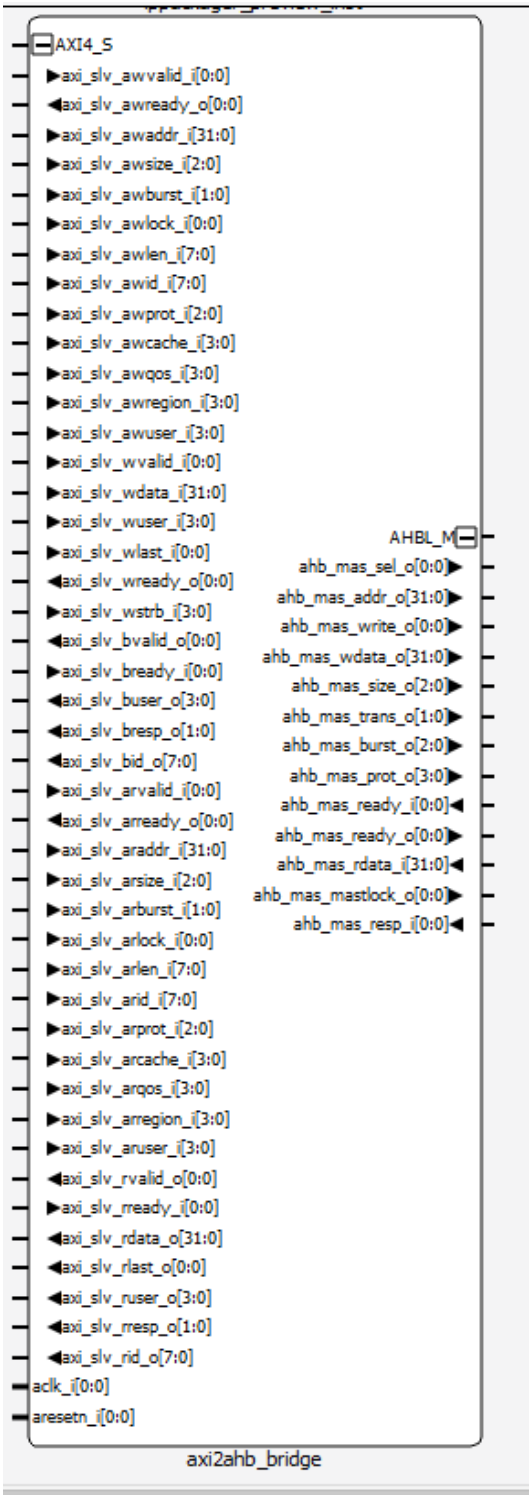

Figure 2.2. AXI4 to AHB-Lite Bridge Module Interface Diagram

Table 2.1. AXI4 to AHB-Lite Bridge Module Signal Description

Pin Name	Direction	Width (Bits)	Description
Clock and Reset			
aclk_i	In	1	AXI4 to AHB-Lite bridge clock.
aresetn_i	In	1	Active low reset.
AXI4 Manager Interface (AXI4_S)			
axi_slv_awvalid_i	In	1	Write address valid. This signal indicates that the channel is signaling valid write address and control information.
axi_slv_awaddr_i	In	32	Write address. The write address gives the address of the first transfer in a write burst transaction
axi_slv_awsize_i	In	3	Burst size. This signal indicates the size of each transfer in the burst
axi_slv_awburst_i	In	2	Burst type. The burst type and the size information, determine how the address for each transfer within the burst is calculated
axi_slv_awlen_i	In	8	Burst length. This indicates the number of beats per AXI4 burst.
axi_slv_awid_i	In	AXI_ID_WIDTH	AXI4 write ID width.
axi_slv_awlock_i	In	1	Lock type. AXI4: Optional
axi_slv_awcache_i	In	4	Memory type. AXI4: Optional
axi_slv_awprot_i	In	3	Protection type AXI4: Optional
axi_slv_awqos_i	In	4	Quality of Service. AXI4: Optional
axi_slv_awregion_i	In	4	Region AXI4: Optional
axi_slv_awuser_i	In	AXI_USER_WIDTH	User signals. AXI4: Optional
axi_slv_awready_o	Out	1	Write address ready. This signal indicates that the Subordinate is ready to accept an address and associated control signals
axi_slv_wvalid_i	In	1	Write valid. This signal indicates that valid write data and strobes are available
axi_slv_wdata_i	In	AXI_AHB_DATA_WIDTH	Write data.
axi_slv_wlast_i	In	1	Write last. This signal indicates the last transfer in a write burst
axi_slv_wuser_i	In	AXI_USER_WIDTH	User signals. AXI4: Optional
axi_slv_wstrb_i	In	AXI_AHB_DATA_WIDTH/8	Write strobes. This signal indicates which byte lanes hold valid data. There is one write strobe bit for each eight bits of the write data bus
axi_slv_wready_o	Out	1	Write data ready. This signal indicates that the Subordinate is ready to accept write data.
axi_slv_bvalid_o	Out	1	Write response valid. This signal indicates that the channel is signaling a valid write response
axi_slv_bid_o	Out	AXI_ID_WIDTH	Write response ID.
axi_slv_bresp_o	Out	2	Write response. This signal indicates the status of the write transaction
axi_slv_buser_o	Out	AXI_USER_WIDTH	User signals. AXI4: Optional

Pin Name	Direction	Width (Bits)	Description
axi_slv_bready_i	In	1	Response ready. This signal indicates that the Manager can accept a write response
axi_slv_arvalid_i	In	1	Read address valid. This signal indicates that the channel is signaling valid read address and control information
axi_slv_araddr_i	In	32	Read address. The read address gives the address of the first transfer in a read burst transaction
axi_slv_arsize_i	In	3	Burst size. This signal indicates the size of each transfer in the burst.
axi_slv_arburst_i	In	2	Burst type. The burst type and the size information determine how the address for each transfer within the burst is calculated.
axi_slv_arlen_i	In	8	AXI4 read burst length. This indicates the number of beats per AXI4 burst
axi_slv_arid_i	In	AXI_ID_WIDTH	AXI4 read address ID width.
axi_slv_arlock_i	In	1	Lock type. AXI4: Optional
axi_slv_arcache_i	In	4	Memory type. AXI4: Optional
axi_slv_arprot_i	In	3	Protection type AXI4: Optional
axi_slv_arqos_i	In	4	Quality of Service. AXI4: Optional
axi_slv_arregion_i	In	4	Region AXI4: Optional
axi_slv_aruser_i	In	AXI_USER_WIDTH	User signals. AXI4: Optional
axi_slv_arready_o	Out	1	Read address ready. This signal indicates that the Subordinate is ready to accept an address and associated control signals
axi_slv_rvalid_o	Out	1	Read valid.
axi_slv_rdata_o	Out	AXI_AHB_DATA_WIDTH	Read data.
axi_slv_ruser_o	Out	AXI_USER_WIDTH	User signals. AXI4: Optional
axi_slv_rlast_o	Out	1	Read last. This signal indicates the last transfer in a read burst.
axi_slv_rresp_o	Out	2	Read response. This signal indicates the status of the read transaction
axi_slv_rready_i	In	1	Read ready. This signal indicates that the Manager can accept the read data and response information
AHB-Lite Interface (AHBL_M)			
ahb_mas_sel_o	Out	1	AHB-Lite Subordinate select.
ahb_mas_addr_o	Out	32	This is the AHB-Lite address bus width.
ahb_mas_write_o	Out	1	Indicates the transfer direction, this signal indicates an AHB-Lite write access when High and an AHB-Lite read access when Low
ahb_mas_wdata_o	Out	AXI_AHB_DATA_WIDTH	Write data. The write data bus transfers data from the Manager to the Subordinates during write operations. Width of the port can be 32/64-bit.
ahb_mas_size_o	Out	3	AHB-Lite Size of Transfer

Pin Name	Direction	Width (Bits)	Description
ahb_mas_trans_o	Out	2	AHB-Lite transfer type, which can be NONSEQUENTIAL, SEQUENTIAL, IDLE, or BUSY.
ahb_mas_prot_o	Out	4	Protection type. Indicates the normal, privileged transaction and whether the transaction is a data access or an instruction access. ahb_mas_prot_o is driven with {1'b0, axi_slv_axprot_i}.
ahb_mas_mastlock_o	Out	1	Indicates that the current Manager is performing a locked sequence of transfers.
ahb_mas_burst_o	Out	3	AHB-Lite burst type. The burst type indicates if the transfer is a single transfer or forms part of a burst. The burst can be incrementing or wrapping.
ahb_mas_ready_o	Out	1	AHB-Lite Manager ready.
ahb_mas_ready_i	In	1	Ready. The AHB-Lite Subordinate uses this signal to extend an AHB-Lite transfer.
ahb_mas_rdata_i	In	AXI_AHB_DATA_WIDTH	AHB-Lite read data driven by Subordinate. Width of the port can be 32/64-bit.
ahb_mas_resp_i	In	1	Transfer Response. When Low, indicates that the transfer status is OKAY. When High, indicates that the transfer status is ERROR.

2.3. Attributes

Table 2.2 provides the list of user-configurable attributes for the AXI4 to AHB-Lite Bridge Module. The attribute values are specified using the IP core Configuration user interface in the Propel Builder software as shown in Figure 2.3.

Table 2.2. Attributes Table

Attribute Name	Description
General Settings Tab	
AXI_AHB data bus width	Specifies the bit width of AXI4 and AHB-Lite data bus signals.
AXI ID width	Specifies the bit width of AXI4 ID signals.
AXI user width	Specifies the bit width of AXI4 user signals.

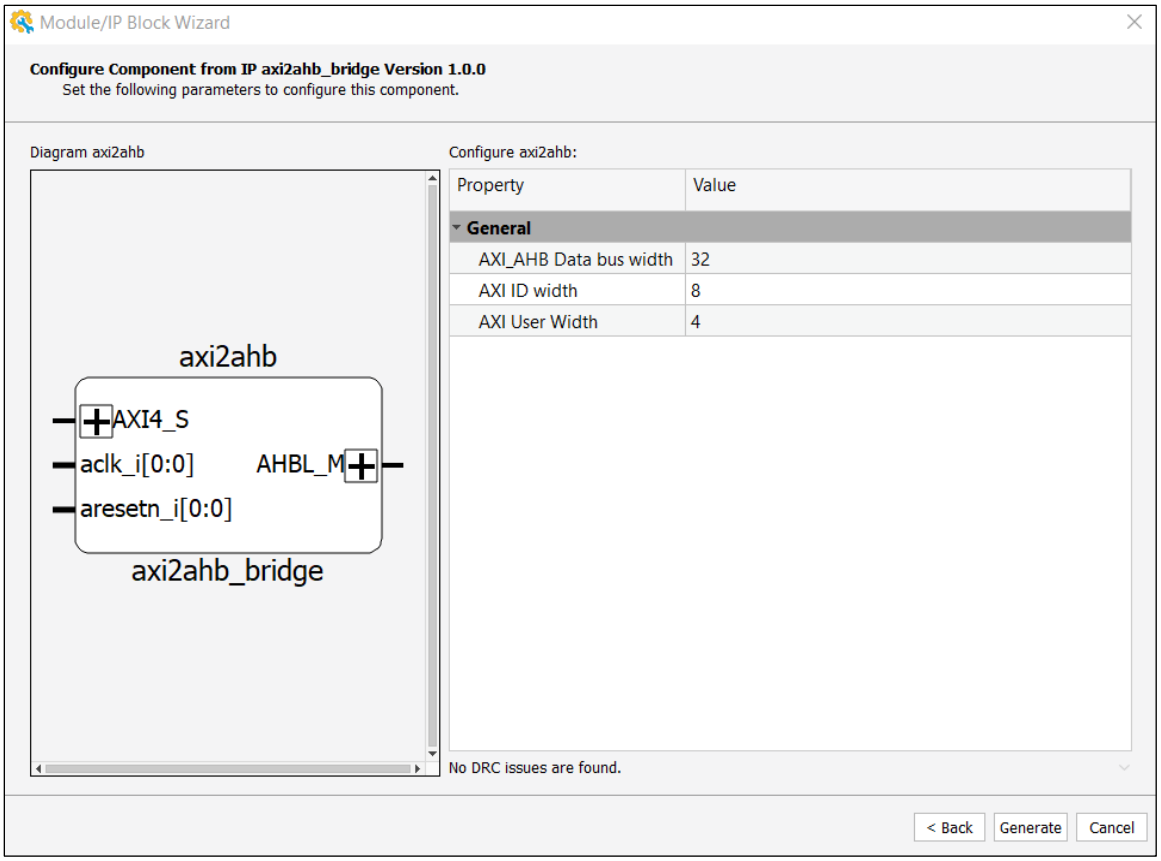

Figure 2.3. AXI4 to AHB-Lite Bridge Module Configuration User Interface

Table 2.3. Attribute Configuration Settings

Attribute Name	Attribute ID	Selectable Values	Default	Dependency on Other Attributes
General Settings Tab				
AXI_AHB data bus width	AXI_AHB_DATA_WIDTH	8, 16, 32, 64, 128, 256, 512, 1024	32	—
AXI ID width	AXI_ID_WIDTH	1 to 11	8	—
AXI user width	AXI_USER_WIDTH	1-128	4	—

Appendix A. Resource Utilization

The following tables show the resource utilization of the AXI4 to AHB-Lite Bridge Module for different Lattice FPGA devices using Lattice Radiant Software 2025.2 with Synplify Pro (W-2025.03LR-SP1-Beta1, Aug 12, 2025) as the Synthesis Tool. The different Data Widths were used while the other attributes are the default configuration.

Table A.1. Resource Utilization Using LAV-AT-E70-3LFG1156I

Configuration	Clock Fmax (MHz)	Registers	LUTs	EBRs
AXI_AHB Data Bus Width = 1024 AXI ID Width = 8, AXI User Width = 4	250.000	4261	5853	0
AXI_AHB Data Bus Width = 256 AXI ID Width = 8, AXI User Width = 4	250.000	1188	1717	0
AXI_AHB Data Bus Width = 32 AXI ID Width = 8, AXI User Width = 4	250.000	283	819	0
AXI_AHB Data Bus Width = 8 AXI ID Width = 8, AXI User Width = 4	250.000	188	742	0

Table A.2. Resource Utilization Using LAV-AT-E70-1LFG1156I

Configuration	Clock Fmax (MHz)	Registers	LUTs	EBRs
AXI_AHB Data Bus Width = 1024 AXI ID Width = 8, AXI User Width = 4	233.863	4261	7467	0
AXI_AHB Data Bus Width = 256 AXI ID Width = 8, AXI User Width = 4	241.721	1188	2179	0
AXI_AHB Data Bus Width = 32 AXI ID Width = 8, AXI User Width = 4	250.000	283	945	0
AXI_AHB Data Bus Width = 8 AXI ID Width = 8, AXI User Width = 4	250.000	188	742	0

Table A.3. Resource Utilization Using LFCPNX-100-9LFG672I

Configuration	Clock Fmax (MHz)	Registers	LUTs	EBRs
AXI_AHB Data Bus Width = 1024 AXI ID Width = 8, AXI User Width = 4	99.088	4258	7465	0
AXI_AHB Data Bus Width = 256 AXI ID Width = 8, AXI User Width = 4	122.835	1181	2185	0
AXI_AHB Data Bus Width = 32 AXI ID Width = 8, AXI User Width = 4	128.634	283	919	0
AXI_AHB Data Bus Width = 8 AXI ID Width = 8, AXI User Width = 4	129.735	179	707	0

Table A.4. Resource Utilization Using LFCPNX-100-7LFG672I

Configuration	Clock Fmax (MHz)	Registers	LUTs	EBRs
AXI_AHB Data Bus Width = 1024 AXI ID Width = 8, AXI User Width = 4	93.941	4258	7443	0
AXI_AHB Data Bus Width = 256 AXI ID Width = 8, AXI User Width = 4	97.647	1179	2166	0
AXI_AHB Data Bus Width = 32 AXI ID Width = 8, AXI User Width = 4	99.206	281	882	0
AXI_AHB Data Bus Width = 8 AXI ID Width = 8, AXI User Width = 4	105.396	185	704	0

References

- AXI4 to AHB-Lite Bridge Module Release Notes (FPGA-RN-02046)
- Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059)
- AMBA AXI Protocol Specification web page for IHI0022H_c_amba_axi_protocol_spec
- AMBA 3 AHB-Lite Protocol Specification web page
- LatticeECP3 web page
- ECP5 web page
- CrossLink-NX web page
- CertusPro-NX web page
- Certus-NX web page
- Certus-N2 web page
- MachXO5-NX web page
- Avant-E web page
- Avant-G web page
- Avant-X web page
- Lattice Radiant Software web page
- Lattice Propel Design Environment web page
- Lattice Diamond Software web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

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Revision History

Note: In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

Revision 1.6, IP v1.5.0, December 2025

Section	Change Summary
Introduction	• Added *AxWSTRB* in second statement of Limitations section: *AxQOS, AxREGION, AxUSER, AxCACHE, and AxLOCK, AxWSTRB are considered as don't care.* • Added statement in Limitations section: *Unaligned transfers are not supported in burst transfers and consistently respond with SLVERR.*
Appendix A. Resource Utilization	Updated value of *Clock Fmax (MHz)*, *Registers*, *LUTs* in Table A.1. Resource Utilization Using LAV-AT-E70-3LFG1156I, Table A.2. Resource Utilization Using LAV-AT-E70-1LFG1156I, Table A.3. Resource Utilization Using LFCPNX-100-9LFG672I, and Table A.4. Resource Utilization Using LFCPNX-100-7LFG672I.
Revision History	Added note.

Revision 1.5, IP v1.4.0, June 2025

Section	Change Summary
Introduction	Renamed *Supported FPGA Family* to *Supported Devices* in Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation.
References	Updated references.

Revision 1.4, IP v1.3.0, December 2024

Section	Change Summary
Introduction	Added Certus-N2, LatticeECP3, and ECP5 devices in Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation.
Functional Descriptions	Updated figure title from *AXI4 to AHB-Lite Bridge Module Interface Diagram* to Figure 2.3. AXI4 to AHB-Lite Bridge Module Configuration User Interface.
References	Updated references.

Revision 1.3, June 2024

Section	Change Summary
All	• This release is for version 1.2.0 of the AXI4 to AHB-Lite Bridge Module. • Renamed document from *AXI4 to AHB-Lite Bridge Module – Lattice Propel Builder* to *AXI4 to AHB-Lite Bridge Module*. • Changed *AXI* to *AXI4*. • Changed *AHB* to *AHB-Lite*.
Inclusive Language	Added the inclusive language boilerplate.
Introduction	Added CrossLink-NX, Certus-NX, and MachXO5-NX devices in Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation.
Appendix A. Resource Utilization	Updated the device name for Avant devices from LAV-AT-500E to LAV-AT-E70.
References	Updated references.
Technical Support Assistance	Updated the link to the Lattice Answer Database.

Revision 1.2, July 2023

Section	Change Summary
Introduction	• Minor editorial changes in the Feature section. • Changed Slaves to Subordinates in the Feature section.

Section	Change Summary
Functional Description	Changed *Master* to *Manager*, and *Slaves* to Subordinates in the Overview section and Table 2.1. AXI4 to AHB-Lite Bridge Module Signal Description.

Revision 1.1, November 2022

Section	Change Summary
Introduction	Updated Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation. • Removed MachXO5-NX to supported FPGA Family • Added Lattice Avant to supported FPGA Family
References	Adjusted CertusPro-NX product page link.
Appendix A. Resource Utilization	Added Resource Utilizations for CertusPro-NX and Lattice Avant.
Technical Support Assistance	Added reference to the Lattice Answer Database on the Lattice website.
All	Minor editorial and style changes.

Revision 1.0, May 2022

Section	Change Summary
All	Initial release

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