Flash Access IP

IP Version: v2.3.0

User Guide

FPGA-IPUG-02171-2.1

October 2026

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviations	Definition
CFG	Configuration
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
IP	Intellectual Property
JTAG	Joint Test Action Group
LMMI	Lattice Memory Mapped Interface
LSE	Lattice Synthesis Engine
RTL	Register Transfer Level
SSPI	Target Serial Peripheral Interface
UFM	User Flash Memory

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1. Introduction

The Flash Access IP core for Lattice MachXO5™-NX devices enables you to perform write and read access to the internal flash memory of MachXO5-NX devices. The write access and read access are performed through the LMMI interface.

1.1. Overview of the IP

The Flash Access IP enables you to access the MachXO5-NX device flash memory through the LMMI interface.

1.2. Quick Facts

Table 1.1. Summary of the Flash Access IP Core

IP Requirements	Supported Devices	MachXO5-NX (LFMXO5-25, LFMXO5-25P, LFMXO5-35, LFMXO5-35T, LFMXO5-55T, LFMXO5-55TP, LFMXO5-65, LFMXO5-65T, LFMXO5-100T, LFMXO5-100TP)
	IP Changes[1]	Refer to the Flash Access IP Release Notes (FPGA-RN-02064).
Resource Utilization	Supported User Interface	Lattice Memory Mapped Interface (LMMI)
Design Tool Support	Lattice Implementation	IP Core v2.3.0 – Lattice Radiant™ software 2026.1.1
	Synthesis	Synopsys® Synplify Pro for Lattice, Lattice Synthesis Engine
	Simulation	Refer to the Lattice Radiant Software User Guide for the list of supported simulators.

Note:

1. In some instances, the IP may be updated without changes to the user guide. This user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

1.3. IP Support Summary

Table 1.2. Flash Access IP Support Readiness

Device Family	IP Configuration Settings	Clock Frequency	Flash Settings	Flash Commands	Radiant Timing Model
MachXO5-NX (LFMXO5-25 and LFMXO5-25P)	*Use UFM0 with size (blocks)* = 4, *Use USERDATA0 to USEDATA8* = *Checked, Instantiate Internal Oscillator* = *Checked, Config LMMI Interface Enable* = Unchecked	50 MHz	Standard SPI	Check Status, Sector Erase (4KB), Block Erase (32KB), Block Erase (64KB), On-Chip Flash Erase, Write Access, Read Access (Normal Read), Fast Read	Final
	Use UFM0 with size (blocks) = 4, *Use USERDATA0 to USEDATA8* = Checked, *Instantiate Internal Oscillator* = Checked, *Config LMMI Interface Enable* = Checked	50 MHz	Standard SPI	Check Status, Sector Erase (4KB), Block Erase (32KB), Block Erase (64KB), On-Chip Flash Erase, Write Access, Read Access (Normal Read), Fast Read	Final

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Device Family	IP Configuration Settings	Clock Frequency	Flash Settings	Flash Commands	Radiant Timing Model
MachXO5-NX (LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T)	*Use UFM0 with size (blocks)* = 4, *Use USERDATA0 to USEDATA8* = Checked, *Instantiate Internal Oscillator* = Checked, *Config LMMI Interface Enable* = Unchecked, Access Mode = STANDARD	50 MHz	Standard SPI	Check Status, Sector Erase (4KB), Block Erase (32KB), Block Erase (64KB), On-Chip Flash Erase, Write Access, Read Access (Normal Read), Fast Read	Final
	Use UFM0 with size (blocks) = 4, *Use USERDATA0 to USEDATA8* = Checked, *Instantiate Internal Oscillator* = Checked, *Config LMMI Interface Enable* = Unchecked, Access Mode = QUAD	50 MHz	Quad SPI	Check Status, Sector Erase (4KB), Block Erase (32KB), Block Erase (64KB), On-Chip Flash Erase, Write Access, Fast Read Quad Output, Fast Read Quad IO	Final
MachXO5-NX (LFMXO5-55T, LFMXO5-55TP, LFMXO5-100T, and LFMXO5-100TP)	*Use UFM0 with size (blocks)* = 4, *Use USERDATA0 to USEDATA8* = Checked, *Instantiate Internal Oscillator* = Checked, *Config LMMI Interface Enable* = Unchecked, Access Mode = STANDARD	50 MHz	Standard SPI	Check Status, Sector Erase (4KB), Block Erase (32KB), Block Erase (64KB), On-Chip Flash Erase, Write Access, Read Access (Normal Read), Fast Read	Final
	Use UFM0 with size (blocks) = 4, *Use USERDATA0 to USEDATA8* = Checked, *Instantiate Internal Oscillator* = Checked, *Config LMMI Interface Enable* = Unchecked, Access Mode = QUAD	50 MHz	Quad SPI	Check Status, Sector Erase (4KB), Block Erase (32KB), Block Erase (64KB), On-Chip Flash Erase, Write Access, Fast Read Quad Output, Fast Read Quad IO	Final

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1.4. Features

The IP Core has the following features:

- Supports LMMI interface.
- Supports initial user data to be programmed into the flash memory.
- Supports up to 50 MHz input clock frequency.
- Optional LMMI interface for configuration access.
- This is only supported in LFMXO5-25, LFMXO5-25P, LFMXO5-35, LFMXO5-35T, LFMXO5-55T, LFMXO5-55TP, LFMXO5-65, LFMXO5-65T, LFMXO5-100T, and LFMXO5-100TP devices.

1.5. Licensing and Ordering Information

The Flash Access IP is provided at no additional cost with the Lattice Radiant software.

1.6. Naming Conventions

1.6.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.6.2. Signal Names

Signal names that end with:

- _n are active low signals (asserted when value is logic 0).
- _i are input signals.
- _o are output signals.

1.6.3. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

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2. Functional Description

2.1. IP Architecture Overview

The Flash Access IP Core for MachXO5-NX device has a LMMI target interface. This is used to perform the write and read access to the internal flash memory.

The IP implements the CONFIG_LMMI primitive in it to provide the Config LMMI interface that allow user logic inside the FPGA fabric to access the device configuration (CFG) functionalities. This option can be enabled by checking the *Config LMMI Interface Enable* option in the Flash Access IP core.

Refer to Appendix D. Configuration Access from User Logic, in sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099) for more details.

Note: With SSPI persistence enabled in user mode, there is a limitation on operation of the SSPI/JTAG bus when using the Flash Access IP for MachXO5-NX devices. Do not access the SSPI/JTAG port when accessing flash memory using the Flash Access IP or vice versa.

Figure 2.1 and Figure 2.2 show the Flash Access Block diagram with the *Use HFCLK for LMMI CLK* attribute unchecked and checked respectively. Figure 2.3 shows the Flash Access Block diagram with the C*onfig LMMI Interface Enable* attribute checked.

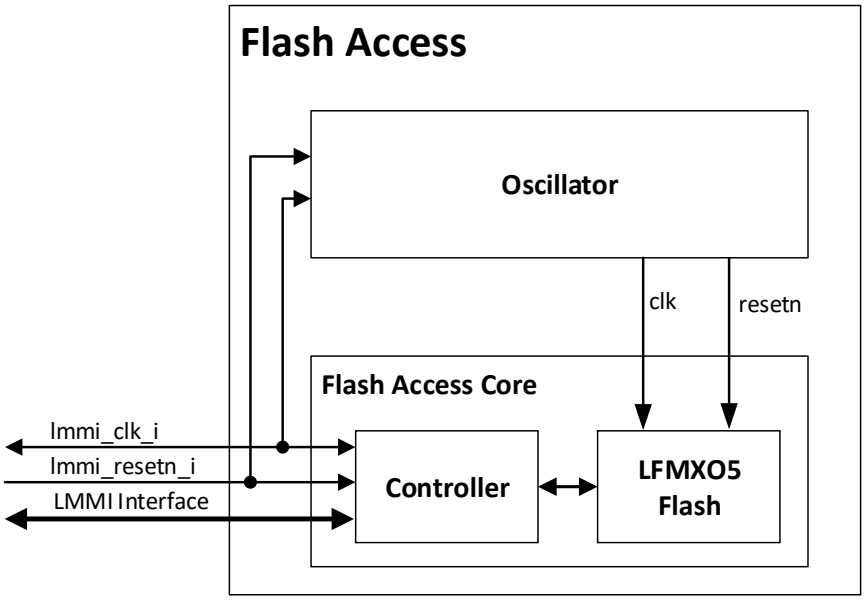


Figure 2.1. Flash Access Block Diagram (Use HFCLK for LMMI CLK = Unchecked)

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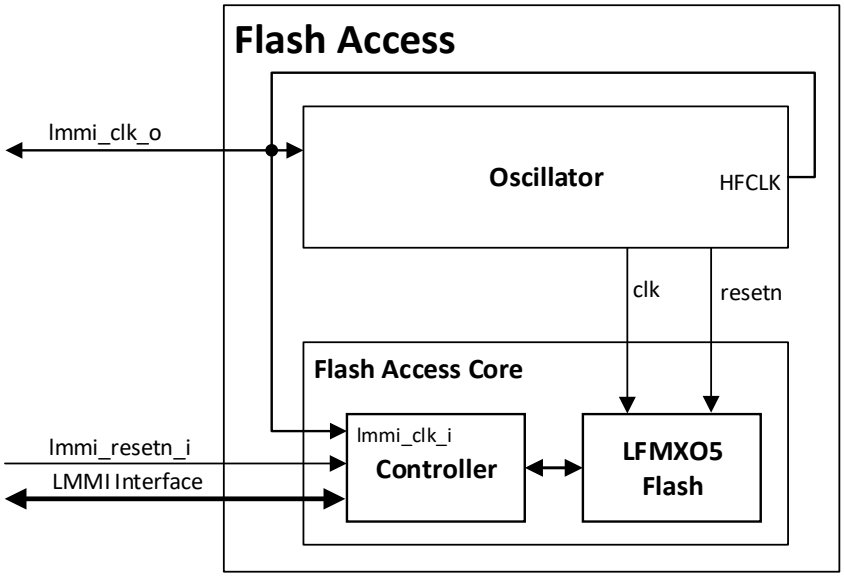


Figure 2.2. Flash Access Block Diagram (Use HFCLK for LMMI CLK = Checked)

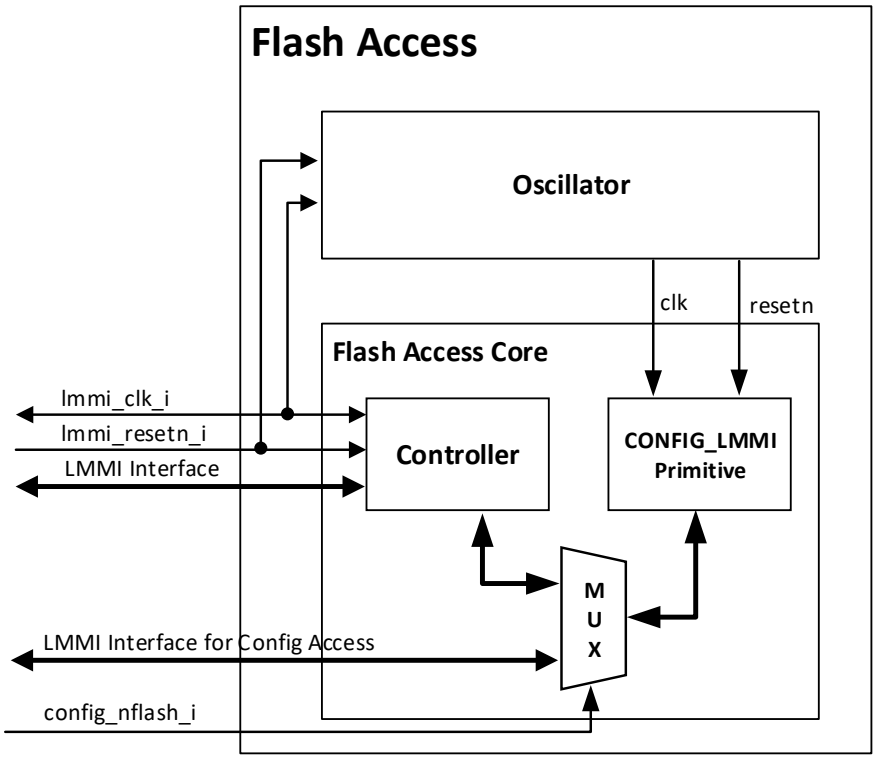


Figure 2.3. Flash Access Block Diagram (Config LMMI Interface Enable = Checked)

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2.2. Clocking

2.2.1. Clocking Overview

The Oscillator block is required by the Flash Access Core. In LFMXO5-25, LFMXO5-25P, LFMXO5-35, LFMXO5-35T, LFMXO5-55T, LFMXO5-55TP, LFMXO5-65, LFMXO5-65T, LFMXO5-100T, and LFMXO5-100TP devices, only one Oscillator block can be instantiated. If you need to use the Oscillator block for other modules in your design, you should uncheck the *Instantiate Internal Oscillator* attribute. You should instantiate an Oscillator Soft IP outside of the Flash Access soft IP. Unchecking this, however, requires manual instantiation and connection of the Oscillator Soft IP to the Flash Access IP to enable the Lattice Radiant flow and simulation.
Figure 2.4 shows a sample connection of an Oscillator Soft IP to the ports of the Flash Access IP.

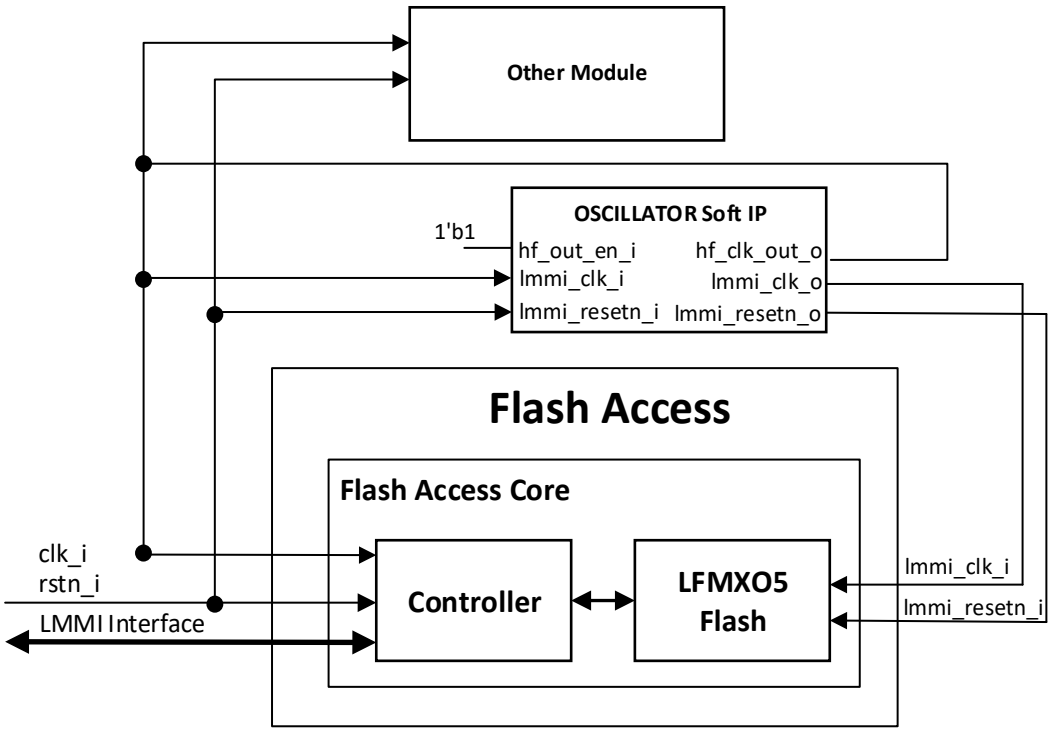


Figure 2.4. Sample Connection between Oscillator Soft IP and Flash Access IP

Note: Figure 2.4 shows the clk_i and lmmi_clk_i input clock is supplied from the HFCLK output clock from Oscillator Soft IP, you have an option to source the clock from LFCLK clock from Oscillator Soft IP or from the external/onboard oscillator.
When the *Instantiate Internal Oscillator* attribute is checked, Flash Access soft IP instantiates the Oscillator block internally. You have two options for the LMMI clock.
If you opt to provide input to the LMMI clock, the *Use HFCLK for LMMI CLK* attribute should be unchecked. The lmmi_clk_i is used directly by the Controller of the Flash Access Core. This input is also passed to the Oscillator block where an output clock (clk) connects to the flash memory, as shown in Figure 2.1.
The Oscillator block generates the LMMI clock. In this case, the *Use HFCLK for LMMI CLK* attribute should be checked. The clock (HFCLK) generated by the Oscillator is connected to the output port lmmi_clk_o. During this setting, lmmi_clk_o is connected to lmmi_clk_i internally. This output clock can be used for synchronization on other designs to be used with the Flash Access IP. You can select the frequency of HFCLK using the *Frequency of the internal LMMI CLK (MHz)* attribute, as shown in Figure 2.2.

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2.3. Reset

2.3.1. Reset Overview

The lmmi_resetn_i input to the Flash Access IP is an asynchronous reset to reset the IP core and is an active low reset signal.

2.4. User Interfaces

The LMMI interface of the Flash Access IP Core is accessible to you to perform the write and read access to the internal flash memory.

Note: Refer to Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039) for more information.

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3. IP Parameter Description

3.1. General

The configurable attributes of the Flash Access for MachXO5-NX IP Core are shown in Table 3.1 and are described in Table 3.2. The attributes can be configured through the Lattice Radiant™ software.

Table 3.1. Attributes Table

Attribute	Selectable Values[1]	Default[1]	Dependency on Other Attributes[1]
CFG0/1/2 and UFM0/1/2 Settings Tab			
CFG0 and UFM0 Settings Group			
Use CFG0 with size (blocks)	A: 0, 11, 15 B: 0, 21, 28 C: 0, 33, 48	A: 0 B: 0 C: 0	—
CFG0 Initial Value Format	ALL 1, ALL 0, NONE, HEXFILE, BINFILE	—	*Use CFG0 with size (blocks)* > 0
CFG0 Initial Value File Path	—	—	*CFG0 Initial Value Format* = HEXFILE or BINFILE
Use UFM0 with size (blocks)	A: 0, 4 B: 0, 7 C: 0, 15	A: 4 B: 7 C: 15	A: *Use CFG0 with size (blocks)* < 15 B: *Use CFG0 with size (blocks)* < 28 C: *Use CFG0 with size (blocks)* < 48
UFM0 Initial Value Format	ALL 1, ALL 0, NONE, HEXFILE, BINFILE	ALL 1	*Use UFM0 with size (blocks)* > 0
UFM0 Initial Value File Path	—	—	*UFM0 Initial Value Format* = HEXFILE or BINFILE
CFG1 and UFM1 Settings Group			
Use CFG1 with size (blocks)	A: 0, 11, 15 B: 0, 21, 28 C: 0, 33, 48	A: 0 B: 0 C: 0	—
CFG1 Initial Value Format	ALL 1, ALL 0, NONE, HEXFILE, BINFILE	—	*Use CFG1 with size (blocks)* > 0
CFG1 Initial Value File Path	—	—	*CFG1 Initial Value Format* = HEXFILE or BINFILE
Use UFM1 with size (blocks)	A: 0, 4 B: 0, 7 C: 0, 15	A: 0 B: 0 C: 0	A: *Use CFG1 with size (blocks)* < 15 B: *Use CFG0 with size (blocks)* < 28 C: *Use CFG1 with size (blocks)* < 48
UFM1 Initial Value Format	ALL 1, ALL 0, NONE, HEXFILE, BINFILE	—	*Use UFM1 with size (blocks)* > 0
UFM1 Initial Value File Path	—	—	*UFM1 Initial Value Format* = HEXFILE or BINFILE
CFG2 and UFM2 Settings Group			
Use CFG2 with size (blocks)	A: 0, 11, 15 B: 0, 21, 28 C: 0, 33, 48	A: 0 B: 0 C: 0	—
CFG2 Initial Value Format	ALL 1, ALL 0, NONE, HEXFILE, BINFILE	—	*Use CFG2 with size (blocks)* > 0
CFG2 Initial Value File Path	—	—	*CFG2 Initial Value Format* = HEXFILE or BINFILE
Use UFM2 with size (blocks)	A: 0, 4 B: 0 C: 0, 15	A: 0 B: 0 C: 0	A: *Use CFG1 with size (blocks)* < 15 B: *Use CFG0 with size (blocks)* < 28 C: *Use CFG1 with size (blocks)* < 48
UFM2 Initial Value Format	ALL 1, ALL 0, NONE, HEXFILE, BINFILE	—	*Use UFM2 with size (blocks)* > 0
UFM2 Initial Value File Path	—	—	*UFM2 Initial Value Format* = HEXFILE or BINFILE

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Attribute	Selectable Values[1]	Default[1]	Dependency on Other Attributes[1]
USERDATA0 to USERDATA8 Settings Tab			
Use USERDATA0 to USERDATA8	Checked, Unchecked	Unchecked	—
USERDATA0 Settings Group			
Use USERDATA0 with size (blocks)	A: 1–17 B: 1–6 C: 1–110	—	*Use USERDATA0 to USERDATA8* = Checked
USERDATA0 Initial Value Format	ALL 1, ALL 0, NONE, HEXFILE, BINFILE	—	*Use USERDATA0 to USERDATA8* = Checked Refer to Table 3.2 for the rules of USERDATA block size.
USERDATA0 Initial Value File Path	—	—	*USERDATA0 Initial Value Format* = HEXFILE or BINFILE
USERDATA1 Settings Group			
Use USERDATA1 with size (blocks)	A: 1–17 B: 1–36 C: 1–110	—	*Use USERDATA0 to USERDATA8* = Checked Refer to Table 3.2 for the rules of USERDATA block size.
USERDATA1 Initial Value Format	ALL 1, ALL 0, NONE, HEXFILE, BINFILE	—	*Use USERDATA1 with size (blocks)* ≥ 1
USERDATA1 Initial Value File Path	—	—	*USERDATA1 Initial Value Format* = HEXFILE or BINFILE
USERDATA2 Settings Group			
Use USERDATA2 with size (blocks)	A: 1–17 B: 1–36 C: 1–110	—	*Use USERDATA0 to USERDATA8* = Checked Refer to Table 3.2 for the rules of USERDATA block size.
USERDATA2 Initial Value Format	ALL 1, ALL 0, NONE, HEXFILE, BINFILE	—	*Use USERDATA2 with size (blocks)* ≥ 1
USERDATA2 Initial Value File Path	—	—	*USERDATA2 Initial Value Format* = HEXFILE or BINFILE
USERDATA3 Settings Group			
Use USERDATA3 with size (blocks)	A: 1–17 B: 1–36 C: 1–110	—	*Use USERDATA0 to USERDATA8* = Checked Refer to Table 3.2 for the rules of USERDATA block size.
USERDATA3 Initial Value Format	ALL 1, ALL 0, NONE, HEXFILE, BINFILE	—	*Use USERDATA3 with size (blocks)* ≥ 1
USERDATA3 Initial Value File Path	—	—	*USERDATA3 Initial Value Format* = HEXFILE or BINFILE
USERDATA4 Settings Group			
Use USERDATA4 with size (blocks)	A: 1–17 B: 1–36 C: 1–110	—	*Use USERDATA0 to USERDATA8* = Checked Refer to Table 3.2 for the rules of USERDATA block size.
USERDATA4 Initial Value Format	ALL 1, ALL 0, NONE, HEXFILE, BINFILE	—	*Use USERDATA4 with size (blocks)* ≥ 1
USERDATA4 Initial Value File Path	—	—	*USERDATA4 Initial Value Format* = HEXFILE or BINFILE
USERDATA5 Settings Group			
Use USERDATA5 with size (blocks)	A: 1–17 B: 1–36 C: 1–110	—	*Use USERDATA0 to USERDATA8* = Checked Refer to Table 3.2 for the rules of USERDATA block size.
USERDATA5 Initial Value Format	ALL 1, ALL 0, NONE, HEXFILE, BINFILE	—	*Use USERDATA5 with size (blocks)* ≥ 1
USERDATA5 Initial Value File Path	—	—	*USERDATA5 Initial Value Format* = HEXFILE or BINFILE

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Attribute	Selectable Values[1]	Default[1]	Dependency on Other Attributes[1]
USERDATA6 Settings Group			
Use USERDATA6 with size (blocks)	A: 1–17 B: 1–36 C: 1–110	—	*Use USERDATA0 to USERDATA8* = Checked Refer to Table 3.2 for the rules of USERDATA block size.
USERDATA6 Initial Value Format	ALL 1, ALL 0, NONE, HEXFILE, BINFILE	—	*Use USERDATA6 with size (blocks)* ≥ 1
USERDATA6 Initial Value File Path	—	—	*USERDATA6 Initial Value Format* = HEXFILE or BINFILE
USERDATA7 Settings Group			
Use USERDATA7 with size (blocks)	A: 1–17 B: 1–36 C: 1–110	—	*Use USERDATA0 to USERDATA8* = Checked Refer to Table 3.2 for the rules of USERDATA block size.
USERDATA7 Initial Value Format	ALL 1, ALL 0, NONE, HEXFILE, BINFILE	—	*Use USERDATA7 with size (bocks)* ≥ 1
USERDATA7 Initial Value File Path	—	—	*USERDATA7 Initial Value Format* = HEXFILE or BINFILE
USERDATA8 Settings Group			
Use USERDATA8 with size (blocks)	A: 1–17 B: 1–36 C: 1–110	—	*Use USERDATA0 to USERDATA8* = Checked Refer to Table 3.2 for the rules of USERDATA block size.
USERDATA8 Initial Value Format	ALL 1, ALL 0, NONE, HEXFILE, BINFILE	—	*Use USERDATA8 with size (blocks)* ≥ 1
USERDATA8 Initial Value File Path	—	—	*USERDATA8 Initial Value Format* = HEXFILE or BINFILE
Oscillator Settings Group			
Instantiate Internal Oscillator	Checked, Unchecked	Checked	—
Use HFCLK for LMMI CLK	Checked, Unchecked	Unchecked	*Instantiate Internal Oscillator* = Checked
Frequency of the Internal LMMI CLK (MHz)	50.0, 45.0, 40.909, 30.0	50.0	*Use HFCLK for LMMI CLK* = Checked
Access Mode			
Config LMMI Interface Enable	Checked, Unchecked	Unchecked	—
Read Access Mode	Standard, Quad	Standard	Editable when the device used is LFMXO5-35, LFMXO5-35T, LFMXO5-55T, LFMXO5-55TP, LFMXO5-65, LFMXO5-65T, LFMXO5-100T, or LFMXO5-100TP. Otherwise, the default value is Standard.

Note:

1. *A* applies to LFMXO5-25 and LFMXO5-25P; *B* applies to LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T; *C* applies to LFMXO5-55T, LFMXO5-55TP, LFMXO5-100T, and LFMXO5-100TP.

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Table 3.2. Attributes Description

Attribute	Description

Use CFG<0/1/2> with size (blocks)	Allows you to select if CFG<0/1/2> partition is used or not.
	• If the CFG<0/1/2> partition is used, you have two options for the partition size.
	  • For LFMXO5-25 and LFMXO5-25P devices, you can select 11 blocks or 15 blocks.
	  • For LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T, you can select 21 blocks or 28 blocks
	  • For LFMXO5-55T, LFMXO5-55TP, LFMXO5-100T, and LFMXO5-100TP devices, you can select 33 blocks or 48 blocks.
	• Do not access the partition if the partition size is set to 0.

Use UFM<0/1/2> with size (blocks)	Allows you to select if UFM<0/1/2> partition is used or not. • If the UFM<0/1/2> partition is used, you can select four blocks for LFMXO5-25 and LFMXO5-25P devices and 15 for LFMXO5-55T, LFMXO5-55TP, LFMXO5-100T, and LFMXO5-100TP devices. • If the partition size of the corresponding CFG is set to 15 (LFMXO5-25 and LFMXO5-25P), 28 (LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T), or 48 (LFMXO5-55T, LFMXO5-55TP, LFMXO5-100T, and LFMXO5-100TP), this parameter is automatically set to 0. • Do not access the partition if the partition size is set to 0.
Use USERDATA0 to USERDATA8	Allows you to select if USERDATA0 to USERDATA8 partition is used or not by checking and unchecking this attribute respectively. • Unchecked partition should not be accessed. • At least the USERDATA0 partition (for LFMXO5-25, LFMXO5-25P, LFMXO5-55T, LFMXO5-55TP, LFMXO5-100T, and LFMXO5-100TP) and both the USERDATA0 and USERDATA1 partitions (for LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T) should be used if this attribute is checked. • USERDATA1 to USERDATA8 require the preceding USERDATAx to have at least one block used.

Use USERDATA<0..8> with size (blocks)	Allows you to select the size of each USERDATA<0..8> partition in block with the following rules:
	• Selecting 0 option means that the partition is not used.
	  0 option is not available for USERDATA0. USERDATA0 should be used if *Use USERDATA0 to USERDATA8* = Checked.
	• If a partition is set to 0, the succeeding partitions cannot be used.
	  For example, if USERDATA3 size is set to 0, USERDATA4 to USERDATA8 are automatically set to 0.
	• The total number of blocks should not exceed 17 blocks (for LFMXO5-25 and LFMXO5-25P) and 110 blocks (for LFMXO5-55T, LFMXO5-55TP, LFMXO5-100T, and LFMXO5-100TP).
	• The total number of blocks should not exceed 6 blocks for USERDATA0 and 36 blocks for USERDATA1 to USERDATA8 (for LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T).
	Available options change depending on the selected value of other USERDATAx partitions.

CFG<0/1/2> / UFM<0/1/2> / USERDATA<0..8> Initial Value Format	Allows you to select how to initialize the flash memory partition. Options: • ALL 1: each bit in the whole partition is set to 1. • ALL 0: each bit in the whole partition is set to 0. • NONE: no initial data is set. Lattice factory value is used. • HEXFILE: You specify a custom memory file with HEX format. • BINFILE: You specify a custom memory file with BIN format.
CFG<0/1/2> / UFM<0/1/2> / USERDATA<0..8> Initial Value File Path	Allows you to browse to the memory file to select the custom memory file.

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Attribute	Description
Instantiate Internal Oscillator	Allows you to select if the internal oscillator is instantiated (checked) or not (unchecked).
Use HFCLK for LMMI CLK	Allows you to use HFCLK output of the internal oscillator as LMMI CLK. lmmi_clk_o is available when this attribute is selected. This clock output should be used to sync the LMMI transactions.
Frequency of the internal LMMI CLK (MHz)	Allows you to select the frequency of the HFCLK when Use HFCLK for LMMI CLK= Checked.
Config LMMI Interface Enable	Allows you to choose either flash interface or Config LMMI interface. Flash interface is limited to flash functions while Config LMMI interface provides more function options. Refer to the sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099) for more information about the supported LMMI target commands and the user guide of the flash device you intend to use.
Read Access Mode	Allows you to choose from Standard or Quad access mode. Not available for the LFMXO5-25 and LFMXO5-25P devices.

3.2. Setting Initial Data in Flash Memory

This section provides information on how to set the initial data for the flash device using attributes. There are five options available to you on how to initialize each flash memory partition. Table 3.3 describes these options.

Table 3.3. Partition Initial Value Format Attributes Description

Partition Initial Value Format	Description
ALL 1	An init data file is generated automatically containing each bit of the whole memory partition set to 1.
ALL 0	An init data file is generated automatically containing each bit of the whole memory partition set to 0.
NONE	No init data file is generated.
BINFILE	You need to provide the init data file of the memory partition. The init data file is in binary memory file format.
HEXFILE	You need to provide the init data file of the memory partition. The init data file is in hex memory file format.

3.2.1. Binary File

The binary file is a text file of 0s and 1s. The number of rows is equal to the block size of the partition multiplied by 128 (block size × 128). Each row has 4096 bits.

3.2.2. Hex File

The hex file is a text file of hexadecimal characters. The number of rows is equal to the block size of the partition multiplied by 128 (block size × 8). Each row has 1024 hex characters.

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3.3. Internal Memory Block Partitioning

Table 3.4 shows the flash memory map of LFMXO5-25 and LFMXO5-25P devices. You can modify the partition sizes by changing the attributes prior to IP generation.

You have five options for configuring each of the three CFGx/UFMx partition sizes, as shown in Table 3.7.

The rules of configuring the partition sizes of USERDATAx are described in Table 3.2.

Table 3.8 and Table 3.9 show some sample settings for different flash partition block sizes.

Table 3.4. Flash Memory Map LFMXO5-25 and LFMXO5-25P

Block Start Address (24-Bit Byte address)	Block End Address (24-Bit Byte Address)	Block Size	Sector Size	Contents
00 (0x00_0000)	00 (0x00_FFFF)	1	16	—
01 (0x01_0000)	11 (0x0B_FFFF)	11	176	CFG0
12 (0x0C_0000)	15 (0x0F_FFFF)	4	64	UFM0
16 (0x10_0000)	26 (0x1A_FFFF)	11	176	CFG1
27 (0x1B_0000)	30 (0x1E_FFFF)	4	64	UFM1
31 (0x1F_0000)	41 (0x29_FFFF)	11	176	CFG2
42 (0x2A_0000)	45 (0x2D_FFFF)	4	64	UFM2
46 (0x2E_0000)	63 (0x3E_FFFF)	Total ≤ 17	Total ≤ 272	USERDATA0
				USERDATA1
				USERDATA2
				USERDATA3
				USERDATA4
				USERDATA5
				USERDATA6
				USERDATA7
				USERDATA8

Notes:

1. One page is composed of 256 bytes of data. One 4 KB sector is equivalent to 16 pages while one 64 KB block is equivalent to 256 pages.
2. For dual-boot implementation using this IP targeting the LFMXO5-25 or LFMXO5-25P device, follow these guidelines:
   - Program or store the primary image at either address 0x00_0000 or 0x01_0000 (CFG0). Leave the flash header (0x00_0000–0x00_FFFF) blank if the primary image is stored at address 0x01_0000 (CFG0).
   - Program or store the golden image at either address 0x10_0000 (CFG1) or 0x1F_0000 (CFG2).
   - Program or store the jump instruction only at address 0x3F_FF00 (USERDATA8).

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For LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T devices, each CFG and UFM has 21 and 7 64 KB blocks respectively. A CFG can be used with 28 64 KB blocks, with a CFG and UFM combined. There are CFG0, CFG1, CFG2, and UFM0, UFM1, UFM2. USERDATA0 has 6 64 KB blocks and USERDATA1 to USERDATA8 have a total of 36 64 KB blocks. Table 3.6 shows the boundary address for each memory partition of LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T devices.

Table 3.5. Flash Memory Map LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T

Sector Start Address (24-bit Byte Address)	Sector End Address (24-bit Byte Address)	Number of 64 KB Block	Number of 4 KB Sector	Contents
00 (0x00_0000)	00 (0x00_FFFF)	1	16	—
01 (0x01_0000)	21 (0x15_FFFF)	21	336	CFG0
22 (0x16_0000)	28 (0x1C_FFFF)	7	112	UFM0
29 (0x1D_0000)	49 (0x31_FFFF)	21	336	CFG1
50 (0x32_0000)	56 (0x38_FFFF)	7	112	UFM1
57 0x39_0000	62 (0x3E_FFFF)	6	96	USERDATA0
64 (0x40_0000)	84 (0x54_FFFF)	21	336	CFG2
85 (0x55_0000)	91 (0x5B_FFFF)	7	112	UFM2
92 (0x5C_0000)	127 (0x7F_FFFF)	Total ≤ 36	Total ≤ 576	USERDATA1
				USERDATA2
				USERDATA3
				USERDATA4
				USERDATA5
				USERDATA6
				USERDATA7
				USERDATA8

Notes:

1. One page is composed of 256 bytes of data. One 4 KB sector is equivalent to 16 pages while one 64 KB block is equivalent to 256 pages.
2. For dual-boot implementation using this IP targeting the LFMXO5-35, LFMXO5-35T, LFMXO5-65, or LFMXO5-65T device, follow these guidelines:
   - Program or store the primary image at either address 0x00_0000 or 0x01_0000 (CFG0). Leave the flash header (0x00_0000–0x00_FFFF) blank if the primary image is stored at address 0x01_0000 (CFG0).
   - Program or store the golden image at either address 0x1D_0000 (CFG1) or 0x40_0000 (CFG2).
   - Program or store the jump instruction only at address 0x3F_FF00.

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For LFMXO5-55T, LFMXO5-55TP, LFMXO5-100T, and LFMXO5-100TP devices, each CFG and UFM has 33 and 15 64 KB blocks respectively. A CFG can be used with 48 64 KB blocks, with a CFG and UFM combined. There are CFG0, CFG1, CFG2, and UFM0, UFM1, UFM2. USERDATA0 to USERDATA8 have a total of 110 64 KB blocks. Table 3.6 shows the boundary address for each memory partition of LFMXO5-55T, LFMXO5-55TP, LFMXO5-100T, and LFMXO5-100TP devices.

Table 3.6. Flash Memory Map LFMXO5-55T, LFMXO5-55TP, LFMXO5-100T, and LFMXO5-100TP

Sector Start Address (24-bit Byte Address)	Sector End Address (24-bit Byte Address)	Number of 64 KB Block	Number of 4 KB Sector	Contents
00 (0x00_0000)	00 (0x00_FFFF)	1	16	—
01 (0x01_0000)	33 (0x21_FFFF)	33	528	CFG0
34 (0x22_0000)	48 (0x30_FFFF)	15	240	UFM0
49 (0x31_0000)	81 (0x51_FFFF)	33	528	CFG1
82 (0x52_0000)	96 (0x60_FFFF)	15	240	UFM1
97 (0x61_0000)	129 (0x81_FFFF)	33	528	CFG2
130 (0x82_0000)	144 (0x90_FFFF)	15	240	UFM2
145 (0x91_0000)	255 (0xFE_FFFF)	Total ≤ 110	Total ≤ 1760	USERDATA0
				USERDATA1
				USERDATA2
				USERDATA3
				USERDATA4
				USERDATA5
				USERDATA6
				USERDATA7
				USERDATA8

Notes:

1. One page is composed of 256 bytes of data. One 4 KB sector is equivalent to 16 pages while one 64 KB block is equivalent to 256 pages.
2. For dual-boot implementation using this IP targeting the LFMXO5-55T, LFMXO5-55TP, LFMXO5-100T, or LFMXO5-100TP device, follow these guidelines:
   - Program or store the primary image at either address 0x00_0000 or 0x01_0000 (CFG0). Leave the flash header (0x00_0000–0x00_FFFF) blank if the primary image is stored at address 0x01_0000 (CFG0).
   - Program or store the golden image at either address 0x31_0000 (CFG1) or 0x61_0000 (CFG2).
   - Program or store the jump instruction only at address 0xFF_FF00 (USERDATA8).

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Table 3.7. Different Combinations of CFGx/UFMx Block Size

LFMXO5-25				
Number	**CFGx Block Size**	**UFMx Block Size**	**Use Partition Setting**	**Description**
1	15	0	Use CFGx with size = 15 Use UFMx with size = 0	There is only one partition. CFGx has 15 block size.
2	11	0	Use CFGx with size = 11 Use UFMx with size = 0	There is only one partition. CFGx has 11 block size. You should not access the partition for UFMx.
3	0	4	Use CFGx with size = 0 Use UFMx with size = 4	There is only one partition. UFMx has four block size. You should not access the partition for CFGx.
4	11	4	Use CFGx with size = 11 Use UFMx with size = 4	There are two partitions. CFGx has 11 block size and UFMx has four block size.
5	0	0	Use CFGx with size = 0 Use UFMx with size = 0	Neither CFGx nor UFMx should be accessed.
LFMXO5-65T				
Number	**CFGx Block Size**	**UFMx Block Size**	**Use Partition Setting**	**Description**
1	28	0	Use CFGx with size = 28 Use UFMx with size = 0	There is only one partition. CFGx has 28 block size.
2	21	0	Use CFGx with size = 21 Use UFMx with size = 0	There is only one partition. CFGx has 21 block size. You should not access the partition for UFMx.
3	0	7	Use CFGx with size = 0 Use UFMx with size = 7	There is only one partition. UFMx has 7 block size. You should not access the partition for CFGx.
4	21	7	Use CFGx with size = 21 Use UFMx with size = 7	There are two partitions. CFGx has 21 block size and UFMx has 7 block size.
5	0	0	Use CFGx with size = 0	Neither CFGx nor UFMx should be accessed.
LFMXO5-100T				
Number	**CFGx Block Size**	**UFMx Block Size**	**Use Partition Setting**	**Description**
1	48	0	Use CFGx with size = 48 Use UFMx with size = 0	There is only one partition. CFGx has 48 block size.
2	33	0	Use CFGx with size = 33 Use UFMx with size = 0	There is only one partition. CFGx has 33 block size. You should not access the partition for UFMx.
3	0	15	Use CFGx with size = 0 Use UFMx with size = 15	There is only one partition. UFMx has 15 block size. You should not access the partition for CFGx.
4	33	15	Use CFGx with size = 33 Use UFMx with size = 15	There are two partitions. CFGx has 33 block size and UFMx has 15 block size.
5	0	0	Use CFGx with size = 0	Neither CFGx nor UFMx should be accessed.

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3.4. IP Parameter Settings for Example Use Cases

Table 3.8. Sample Settings 1

LFMXO5-25			
CFGx Block Size	**UFMx Block Size**	**Use Partition Setting**	**Description**
15	N/A	Use CFG0 with size = 15	CFG0
N/A	0	Use UFM0 with size = 0	You should not access.
11	N/A	Use CFG1 with size = 11	CFG1
N/A	0	Use UFM1 with size = 0	You should not access.
0	N/A	Use CFG2 with size = 0	You should not access.
N/A	4	Use UFM2 with size = 4	UFM2
USERDATAx Block Size		**Use Partition Setting**	**Description**
10		USERDATA0 Size = 10	USERDATA0
7		USERDATA1 Size = 7	USERDATA1
N/A		Automatically set to 0	You should not access.
N/A		Automatically set to 0	You should not access.
N/A		Automatically set to 0	You should not access.
N/A		Automatically set to 0	You should not access.
N/A		Automatically set to 0	You should not access.
N/A		Automatically set to 0	You should not access.
N/A		Automatically set to 0	You should not access.
N/A		Automatically set to 0	You should not access.
LFMXO5-65T			
CFGx Block Size	**UFMx Block Size**	**Use Partition Setting**	**Description**
28	N/A	Use CFG0 with size = 28	CFG0
N/A	0	Use UFM0 with size = 0	You should not access it.
0	N/A	Use CFG1 with size = 0	You should not access it.
N/A	7	Use UFM1 with size = 7	UFM1
28	N/A	Use CFG2 with size = 28	CFG2
N/A	7	Use UFM2 with size = 7	UFM2
USERDATAx Block Size		**Use Partition Setting**	**Description**
6		USERDATA0 Size = 6	USERDATA0
4		USERDATA1 Size = 4	USERDATA1
4		USERDATA2 Size = 4	USERDATA2
4		USERDATA3 Size = 4	USERDATA3
4		USERDATA4 Size = 4	USERDATA4
4		USERDATA5 Size = 4	USERDATA5
4		USERDATA6 Size = 4	USERDATA6
4		USERDATA7 Size = 4	USERDATA7
8		USERDATA8 Size = 8	USERDATA8

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LFMXO5-100T			
CFGx Block Size	**UFMx Block Size**	**Use Partition Setting**	**Description**
48	N/A	Use CFG0 with size = 48	CFG0
N/A	0	Use UFM0 with size = 0	You should not access it.
0	N/A	Use CFG1 with size = 0	You should not access it.
N/A	15	Use UFM1 with size = 15	UFM1
33	N/A	Use CFG2 with size = 33	CFG2
N/A	15	Use UFM2 with size = 15	UFM2
USERDATAx Block Size		**Use Partition Setting**	**Description**
13		USERDATA0 Size = 13	USERDATA0
13		USERDATA1 Size = 13	USERDATA1
13		USERDATA2 Size = 13	USERDATA2
13		USERDATA3 Size = 13	USERDATA3
13		USERDATA4 Size = 13	USERDATA4
13		USERDATA5 Size = 13	USERDATA5
13		USERDATA6 Size = 13	USERDATA6
13		USERDATA7 Size = 13	USERDATA7
6		USERDATA8 Size = 6	USERDATA8

Table 3.9. Sample Settings 2

LFMXO5-25			
CFGx Block Size	**UFMx Block Size**	**Use Partition Setting**	**Description**
11	N/A	Use CFG0 with size = 11	CFG0
N/A	4	Use UFM0 with size = 4	UFM0
0	N/A	Use CFG1 with size = 0	You should not access it.
N/A	0	Use UFM1 with size = 0	You should not access it.
0	N/A	Use CFG2 with size = 0	You should not access it.
N/A	0	Use UFM2 with size = 0	You should not access it.
USERDATAx Block Size		**Use Partition Setting**	**Description**
8		USERDATA0 Size = 8	USERDATA0
4		USERDATA1 Size = 4	USERDATA1
2		USERDATA2 Size = 2	USERDATA2
1		USERDATA3 Size = 1	USERDATA3
2		USERDATA4 Size = 2	USERDATA4
N/A		Automatically set to 0	You should not access it.
N/A		Automatically set to 0	You should not access it.
N/A		Automatically set to 0	You should not access it.
N/A		Automatically set to 0	You should not access it.

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LFMXO5-65T			
CFGx Block Size	**UFMx Block Size**	**Use Partition Setting**	**Description**
0	N/A	Use CFG0 with size = 0	You should not access it.
N/A	0	Use UFM0 with size = 0	You should not access it.
21	N/A	Use CFG1 with size = 21	CFG1
N/A	7	Use UFM1 with size = 7	UFM1
21	N/A	Use CFG2 with size = 21	CFG2
N/A	7	Use UFM2 with size = 7	UFM2
USERDATAx Block Size		**Use Partition Setting**	**Description**
6		USERDATA0 Size = 6	USERDATA0
32		USERDATA1 Size = 32	USERDATA1
4		USERDATA2 Size = 4	USERDATA2
N/A		Automatically set to 0	You should not access it.
N/A		Automatically set to 0	You should not access it.
N/A		Automatically set to 0	You should not access it.
N/A		Automatically set to 0	You should not access it.
N/A		Automatically set to 0	You should not access it.
N/A		Automatically set to 0	You should not access it.
LFMXO5-100T			
CFGx Block Size	**UFMx Block Size**	**Use Partition Setting**	**Description**
0	N/A	Use CFG0 with size = 0	You should not access it.
N/A	0	Use UFM0 with size = 0	You should not access it.
33	N/A	Use CFG1 with size = 33	CFG1
N/A	15	Use UFM1 with size = 15	UFM1
33	N/A	Use CFG2 with size = 33	CFG2
N/A	15	Use UFM2 with size = 15	UFM2
USERDATAx Block Size		**Use Partition Setting**	**Description**
64		USERDATA0 Size = 64	USERDATA0
32		USERDATA1 Size = 32	USERDATA1
14		USERDATA2 Size = 14	USERDATA2
N/A		Automatically set to 0	You should not access it.
N/A		Automatically set to 0	You should not access it.
N/A		Automatically set to 0	You should not access it.
N/A		Automatically set to 0	You should not access it.
N/A		Automatically set to 0	You should not access it.
N/A		Automatically set to 0	You should not access it.

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4. Signal Description

Table 4.1 lists the ports of the Flash Access for MachXO5-NX IP Core.

4.1. Flash Access IP Module Signal

Table 4.1. Flash Access Module Signal Description

Name	Type	Width	Description
clk_i	In	1	Input Clock Available when *Instantiate Internal Oscillator* = Unchecked. The maximum frequency supported is 50 MHz.
lmmi_clk_i[2]	In	1	Clock Signal Input Available when *Instantiate Internal Oscillator* = Checked and *Use HFCLK for LMMI_CLK* = Unchecked. The maximum frequency supported is 50 MHz.
lmmi_clk_o	Out	1	Clock Signal Output Available when Use HFCLK for LMMI CLK= Checked.
lmmi_resetn_i	In	1	Active Low Reset Signal
lmmi_request_i	In	1	Start Transaction This signal is asserted to initiate a function to be performed by the flash access IP. This signal also controls the duration of the write and read access to the flash memory.
lmmi_offset_i	In	8	Address Bus This bus is used to specify the type of function to be performed by the flash access IP. Refer to Table 5.1 for more details.
lmmi_wr_rdn_i	In	1	When high, indicates write transaction. When low, indicates read transaction.
lmmi_wdata_i	In	Standard: 1 Quad: 4	Standard: serial interface for transmitting data Quad: four data input for transmitting data
lmmi_rdata_o	Out	Standard: 1 Quad: 4	Standard: serial interface for receiving data Quad: four data input for receiving data
lmmi_rdata_valid_o	Out	1	This signal indicates that lmmi_rdata_o contains valid data.
lmmi_ready_o	Out	1	Ready to start a new lmmi transaction.
rstn_i	In	1	Active Low Reset Input Available when *Instantiate Internal Oscillator* = Unchecked.
When the Config LMMI Interface Enable option is checked. By default, it is unchecked.			
config_nflash_i	In	1	Input selector to enable Config LMMI Interface 0: Enable Flash Access Interface. Config LMMI Interface is disabled. 1: Enable Config LMMI Interface.
config_lmmi_request_i	In	1	LMMI Start transaction. This signal is multiplexed with the lmmi_request_i signal, with the config_nflash_i signal as a selector.
config_lmmi_offset_i[7:0]	In	8	LMMI register offset. This signal is multiplexed with the lmmi_offset_i signal, with the config_nflash_i signal as a selector.
config_lmmi_wr_rdn_i	In	1	LMMI Write/Read control. 1=Write; 0=Read. This signal is multiplexed with the lmmi_wr_rdn_i signal, with the config_nflash_i signal as a selector.
config_lmmi_wdata_i[7:0]	In	8	LMMI Write data. This signal is multiplexed with the lmmi_wdata_i, with the config_nflash_i signal as a selector.

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Name	Type	Width	Description
config_lmmi_ready	Out	1	LMMI Ready signal. This signal is connected to the LMMIREADY signal of the CONFIG_LMMIB primitive. When config_nflash_i is low, this is zero.
config_lmmi_rdata_valid_o	Out	1	LMMI Read transaction is complete and LMMIRDATA contains valid data. This signal is connected to the LMMIRDATAVALID signal of the CONFIG_LMMIB primitive. When config_nflash_i is low, this is zero.
config_lmmi_rdata_o[7:0]	Out	8	LMMI Read data. This signal is connected to the LMMIRDATA signal of the CONFIG_LMMIB primitive. When config_nflash_i is low, this signal can be ignored since config_lmmi_rdata_valid_o is low.

Notes:

1. Refer to the Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039) for more information.
2. For lmmi_clk_i frequency equal to or greater than 25 MHz, it is mandatory by design that CONFIG_IOSLEW be set to FAST. This guarantees proper operation of the internal flash. Failure to comply might cause configuration related issues resulting in the device not being able to boot from its internal flash or issues in operation specifically during the read sequence.

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5. Flash Access Function

5.1. Flash Functions

This section describes the functions that the Flash Access IP supports.

Table 5.1 lists the functions supported by the Flash Access IP and the succeeding subsections provide more details.

Table 5.1. Functions Supported by Flash Access IP

Function Group	Function	LMMI Offset	Access Type	Description
Check Status	Check Status	0x00	Read/Write	Allows you to check if the flash access is busy or not.
Erase	Sector Erase (4 KB)	0x10	Write-only	Allows you to set the 4 KB sector to erased state.
	Block Erase (32 KB)	0x11		Allows you to set the 32 KB block to erased state.
	Block Erase (64 KB)	0x12		Allows you to set the 64 KB block to erased state.
	On-chip Flash Erase	0x13		Allows you to set the whole flash memory to erased state.
Write	Write Access	0x20	Write-only	Allows you to perform the write access to flash memory. Memory location should be in erased state prior to performing the write access.
Read	Standard Read Access	0x30	Read/Write	Allows you to perform the read access to flash memory.
	Standard Read Access	0x31	Read/Write	Allows you to perform the read access to flash memory. After sending the 24-bit address, valid data comes later using this read access compared to when lmmi_offset_i = 0x30. See Figure 5.7.
	Quad Read Access	0x34	Read/Write	Similar to Standard Read Access (lmmi_offset_i = 0x31), except that the data can be read in four bits lmmi_rdata_o [3:0], allowing the data to be transferred at four times the rate of Standard Read Access (0x31). Valid data comes later after 24-bit address with eight clock dummy cycles.
	Quad Read Access	0x35	Read/Write	Similar to Quad Read Access (lmmi_offset_i = 0x34), except that the address and data bits can be accessed using four bits lmmi_wdata_i and lmmi_rdata_o respectively, allowing the data to be transferred at four times the rate of Standard Read Access (0x31). Valid data comes after six clock cycles for address and six clock dummy cycles.

Note: All bits are set to 1 during erased state.

5.1.1. Check Status Sequence

This function is used to check if the Flash Access IP is busy or not. You should use this function to ensure that the Flash Access IP is not busy before performing other functions.

Use the following steps to Check Status:

1. Wait for lmmi_ready_o = 1.
2. Set lmmi_offset_i = 0x00, lmmi_wdata_i = 1, lmmi_request_i = 1, and lmmi_wr_rdn_i = 1.
3. Set lmmi_wr_rdn_i = 0.
4. Wait for lmmi_rdata_valid_o = 1.
5. Wait for the 8th bit of lmmi_rdata_o. This corresponds to the BUSY flag.
6. Set lmmi_request_i = 0 to complete the function.
7. You can opt to hold the lmmi_request_i = 1, while lmmi_rdata_o continuously outputs data until lmmi_request_i = 0 is set. The BUSY flag can be observed every eight bits.

Step 7 can be performed if you intend to wait until the Flash Access IP is not busy before performing other operations.

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Figure 5.1 shows a sample waveform for performing the Check Status sequence.

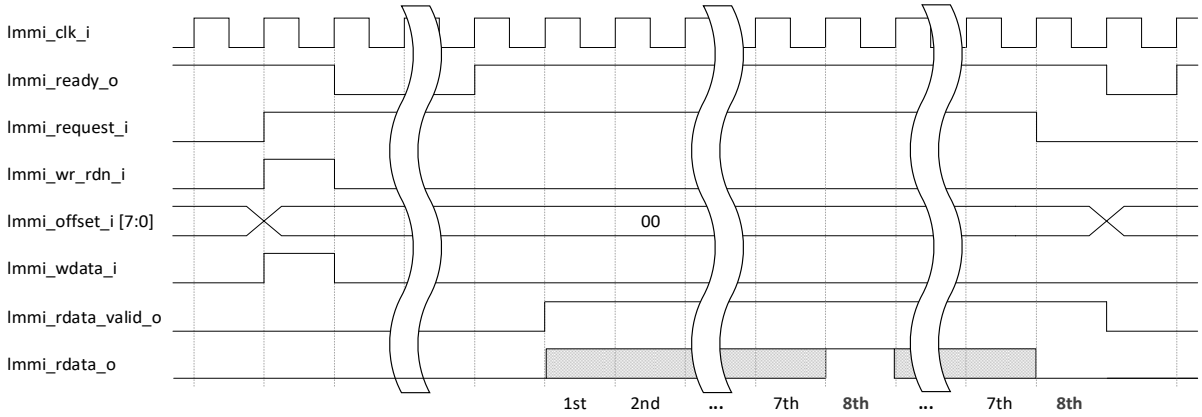


Figure 5.1. Sample Waveform for Check Status Sequence

5.1.2. Erase Sequence

This function is used to set all the memory within the specified sector/block to erased state. You should use this function to ensure that the memory location is in erased state prior to performing write access. All bits are set to 1 during erased state.

You can opt to erase a 4 KB sector, a 32 KB block or a 64 KB block by selecting the lmmi_offset_i that is sent in Step 2 below. Refer to Table 5.1 for the list of lmmi_offset_i.

Use the following steps to perform an Erase function:

1. Wait for lmmi_ready_o = 1.
2. Set lmmi_offset_i based on Table 5.1, lmmi_request_i = 1, and lmmi_wr_rdn_i = 1.
3. Send the 24-bit address of the sector/block that is to be erased through lmmi_wdata_i. The address is sent through the lmmi_wdata_i with the MSB of the address sent first (A23 – A0).
4. Set lmmi_request_i = 0 to complete the function.

The BUSY flag is set to 1 after the last step indicating that the Flash Access IP is performing the erase function on the memory sector/block. The BUSY flag is automatically set to 0 after the erase function is completed. The Flash Access IP cannot perform other functions while it is busy except for the Check Status Sequence.

You must ensure that the flash access IP is not busy before performing other functions.

Figure 5.2 shows a sample waveform for performing a Sector Erase Sequence.

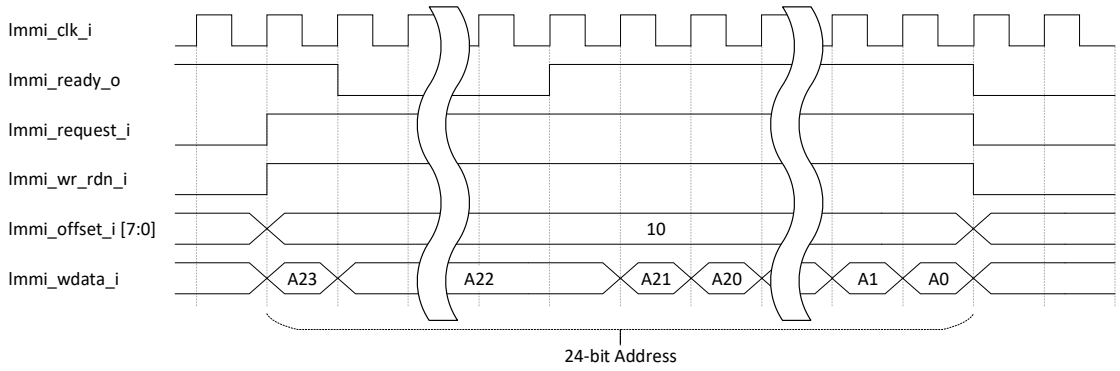


Figure 5.2. Sample Waveform for Sector Erase Sequence

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5.1.3. On-chip Flash Erase Sequence

This function is used to set the whole on-chip flash to erased state.

Use the following steps to perform On-chip Flash Erase function:

1. Wait for lmmi_ready_o = 1.
2. Set lmmi_offset_i = 0x13, lmmi_wdata_i = 1, lmmi_request_i = 1, and lmmi_wr_rdn_i = 1.
3. Set lmmi_request_i = 0 to complete the function.

The BUSY flag is set to 1 after the last step indicating that the Flash Access IP is performing the erase function on the flash memory. The BUSY flag is automatically set to 0 once the erase function is completed. Flash Access IP cannot perform other functions while the BUSY flag = 1, except for the Check Status Sequence.

You must ensure that the flash access IP is not busy before performing other functions.

Figure 5.3 shows a sample waveform for performing On-chip Flash Erase Sequence.

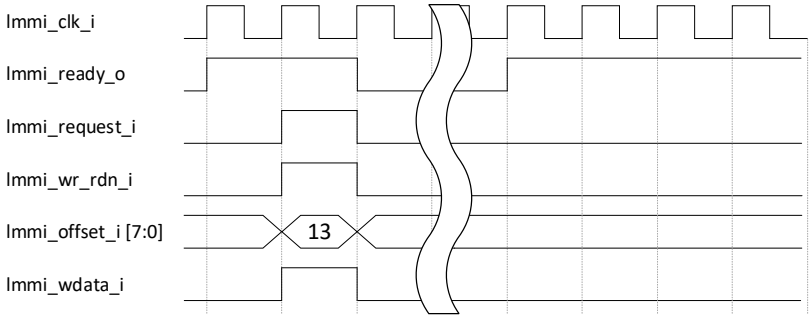


Figure 5.3. Sample Waveform for On-chip Erase Sequence

5.1.4. Write Access Sequence

This function is used to perform write access to the flash memory. Each write access can perform one byte to 256 bytes of a memory page by controlling the lmmi_request_i signal. The memory location to be written should be in erased state prior to performing write access.

Use the following steps to perform the Write Access function:

1. Wait for lmmi_ready_o = 1.
2. Set lmmi_offset_i = 0x20, lmmi_request_i = 1, and lmmi_wr_rdn_i = 1.
3. Send the 24-bit write address using 24 transactions through lmmi_wdata_i. The address is sent through lmmi_wdata_i with the MSB of the address sent first (A23 – A0).
4. Send the bytes of data to be written through lmmi_wdata_i. The data to be written is sent through lmmi_wdata_i with the MSB of each byte sent first.
5. Set lmmi_request_i = 0 once all the bytes of data to be written have been sent. If lmmi_request_i = 0 is set in the middle of sending a byte while only the first part of the byte has been sent, the whole write access function is not performed.

The BUSY flag is set to 1 after the last step indicating that the Flash Access IP is performing the Write Access function on the flash memory. The BUSY flag is automatically set to 0 once the Write Access function is completed. The Flash Access IP cannot perform other functions while BUSY flag = 1, except for Check Status Sequence.

You must ensure that the Flash Access IP is not busy before performing other functions.

The write address sent in Step 3 is used as a starting point of the write access. For every one byte sent in Step 4, the write address increments. If the page border is reached, the write address wraps around the start of the page, as shown in
Figure 5.4. You can send one up to 256 bytes of data to be written. However, you must ensure that the number of bytes sent are aligned to 256 bytes or a page address to avoid wrap-around of data.

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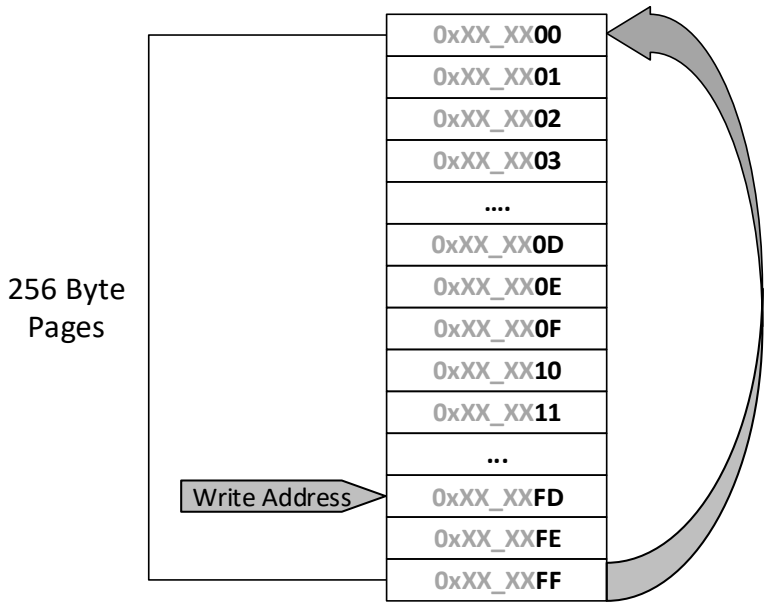


Figure 5.4. Write Data Address Pointer Behavior

Figure 5.5 shows a sample waveform for performing the Write Access function.

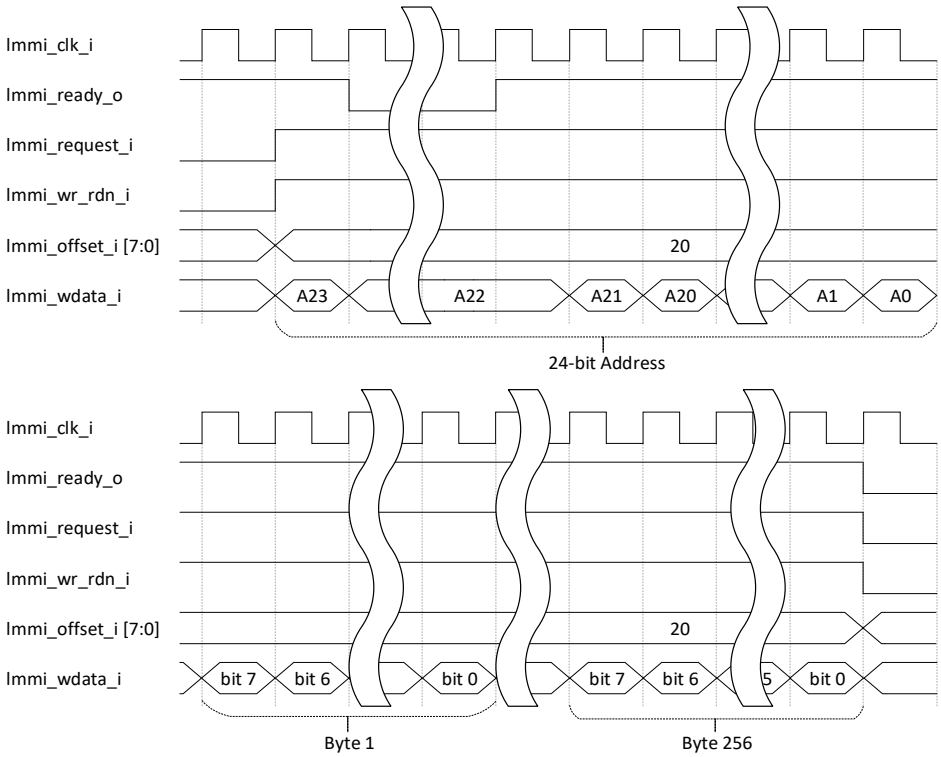


Figure 5.5. Sample Waveform for 256-byte Write Access Sequence

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5.1.5. Read Access Sequence

Standard Read Access

This function is used to perform Standard Read Access to the flash memory. You can read one or more data bytes by controlling the lmmi_request_i signal.

Use the following steps to perform the Standard Read Access function:

1. Wait for lmmi_ready_o = 1.
2. Set lmmi_offset_i based on Table 5.1, lmmi_request_i = 1, and lmmi_wr_rdn_i = 1.
3. Send the 24-bit read address using 24 transactions through lmmi_wdata_i. The address is sent through lmmi_wdata_i with the MSB of the address sent first (A23 – A0).
4. Set lmmi_wr_rdn_i = 0 to enable lmmi_rdata_o.
5. Wait for lmmi_rdata_valid_o = 1.
6. Read data is available in lmmi_rdata_o with the MSB of each byte sent first.
7. Set lmmi_request_i = 0 once all the bytes of data to be read have been received.

The read address sent in Step 3 is used as a starting point of the read access. For every one byte received in Step 6, the read address increments. There is no limit on the number of bytes to be read in one read access function.

Figure 5.6 and Figure 5.7 show sample waveform for performing read access with lmmi_offset_i equal to 0x30 and 0x31. When lmmi_offset_i is equal to 0x31, the first valid data comes nine clocks after the first valid LMMI read. This result to extended read data even when lmmi_request_i is already de-asserted.

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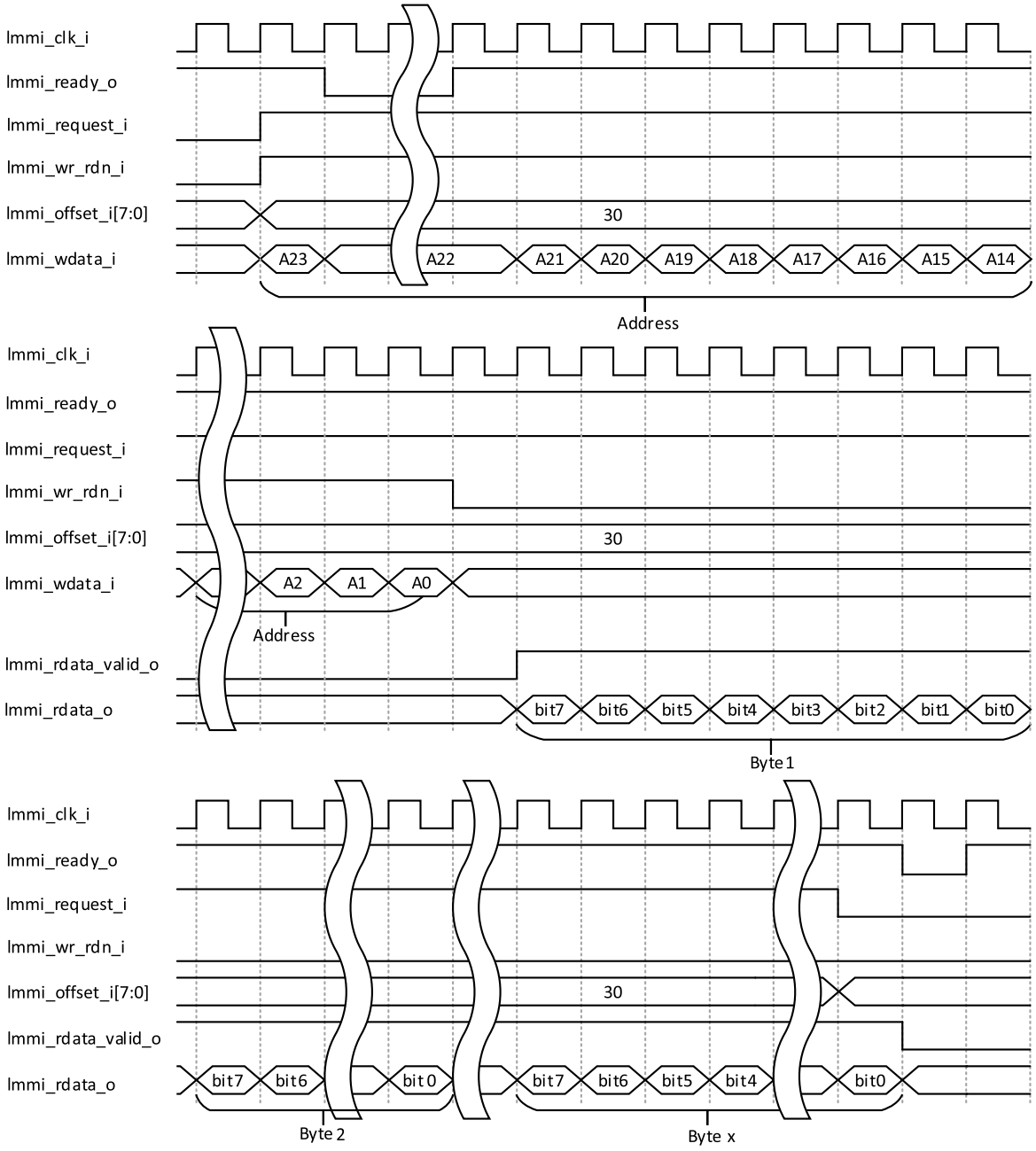


Figure 5.6. Sample Waveform for Read Access – lmmi_offset = 0x30

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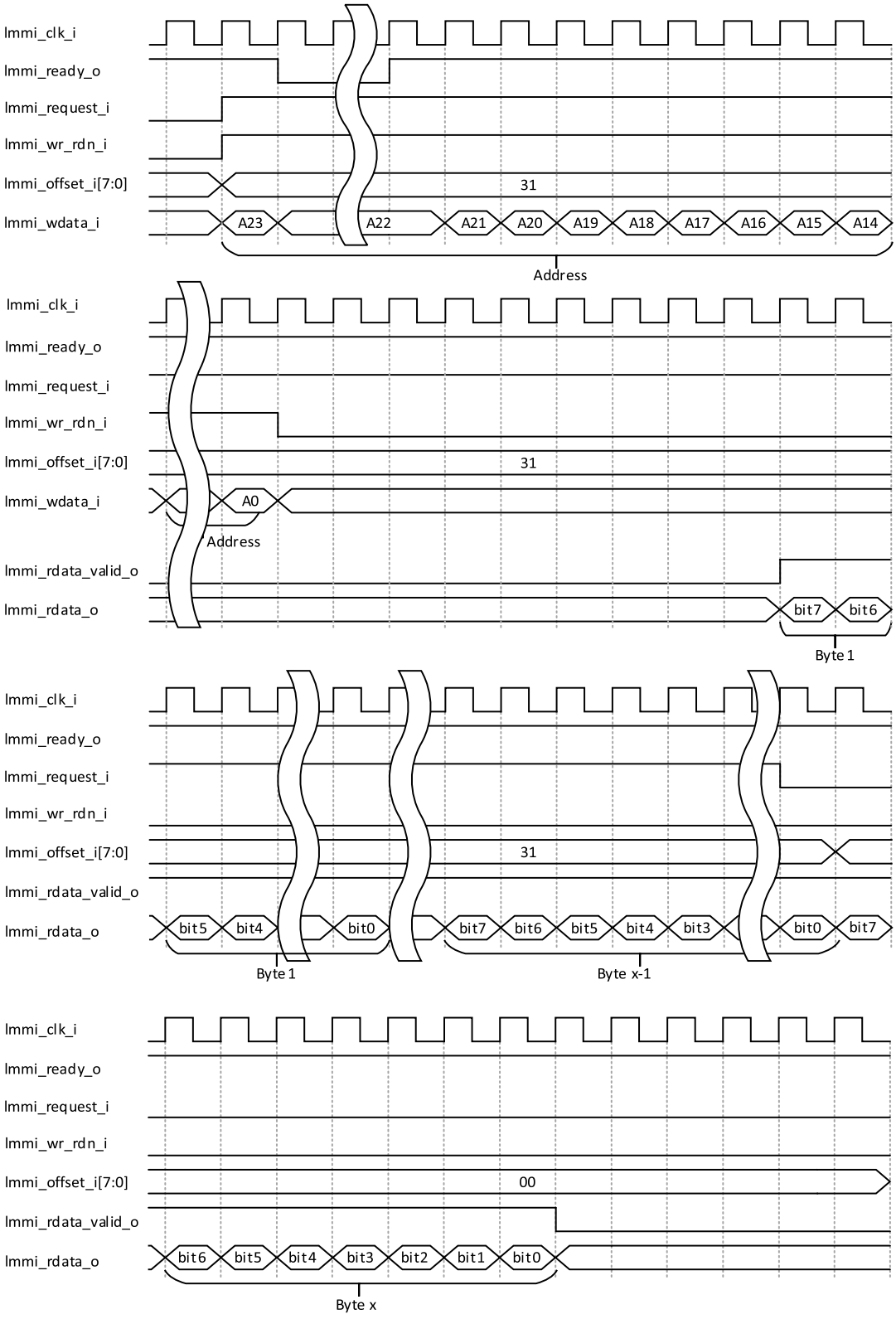


Figure 5.7. Sample Waveform for Read Access – lmmi_offset_i = 0x31

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Quad Read Access (0x34)

This function is used to perform Quad Read Access to the flash memory. You can read one or more data bytes by controlling the lmmi_request_i signal.

Use the following steps to perform Quad Read Access function:

1. Wait for lmmi_ready_o = 1.
2. Set lmmi_offset_i based on Table 5.1, lmmi_request_i = 1, and lmmi_wr_rdn_i = 1.
3. Send the 24-bit read address using 24 transactions through lmmi_wdata_i. The address is sent through lmmi_wdata_i [0] with the MSB of the address sent first (A23 – A0).
4. Set lmmi_wr_rdn_i = 0 to enable lmmi_rdata_o[3:0].
5. Wait for lmmi_rdata_valid_o = 1.
6. Read data is available in lmmi_rdata_o with the MSB of each byte sent first in lmmi_rdata_o[3]. The data sequence is lmmi_rdata_o[3:0] = {bit7,bit6,bit5,bit4}.
7. Set lmmi_request_i = 0 once all the bytes of data to be read has been received.

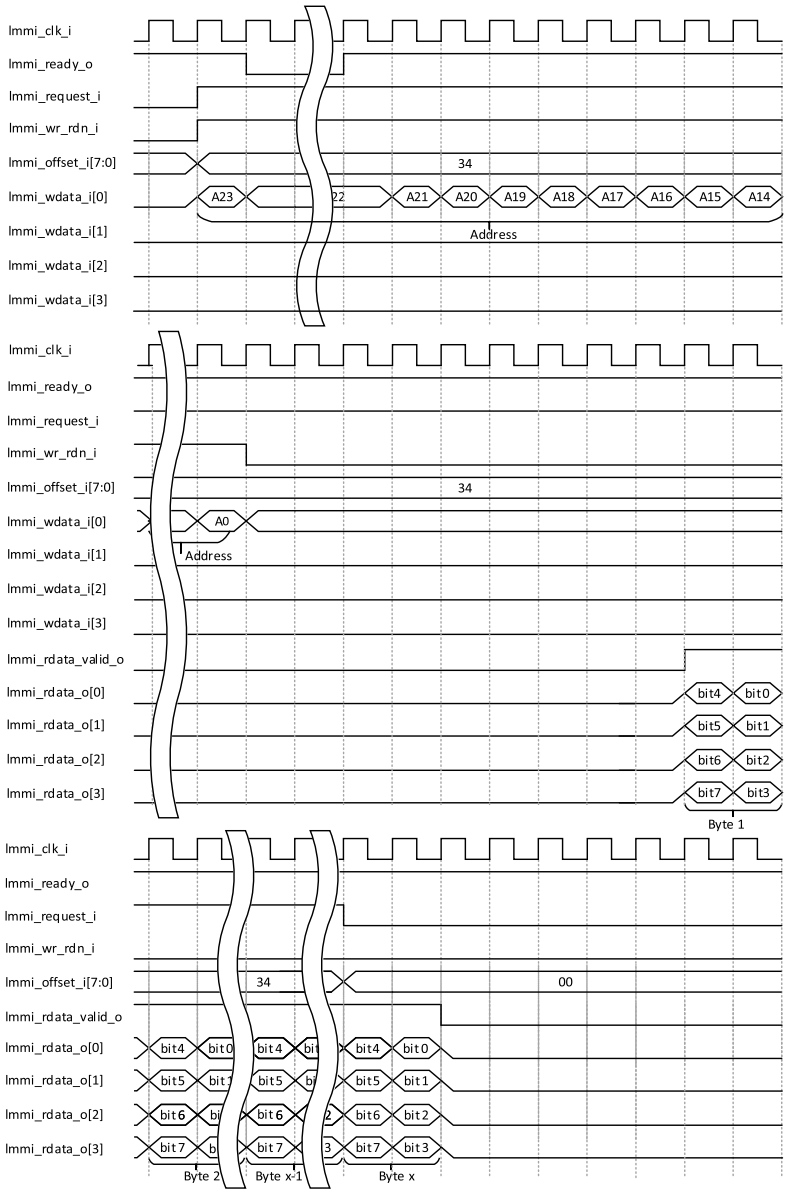


Figure 5.8. Sample Waveform for Read Access – lmmi_offset_i = 0x34

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Quad Read Access (0x35)

This function is used to perform Quad Read Access to the flash memory. You can read one or more data bytes by controlling the lmmi_request_i signal.

Use the following steps to perform the Quad Read Access function:

1. Wait for lmmi_ready_o = 1.
2. Set lmmi_offset_i based on Table 5.1, lmmi_request_i = 1, and lmmi_wr_rdn_i = 1.
3. Send the 24-bit read address using 24 transactions through lmmi_wdata_i. The address is sent through the lmmi_wdata_i[3:0] with the MSB of the address sent first (A23 – A0), the address sequence would be lmmi_wdata_i[3:0] = {A23,A22,A21,A20}.
4. Set lmmi_wr_rdn_i = 0 to enable lmmi_rdata_o[3:0].
5. Wait for lmmi_rdata_valid_o = 1.
6. Read data is available in lmmi_rdata_o with the MSB of each byte sent first in lmmi_rdata_o[3]. The data sequence is lmmi_rdata_o[3:0] = {bit7,bit6,bit5,bit4}.
7. Set lmmi_request_i = 0 once all the bytes of data to be read have been received.

The read address sent in Step 3 is used as a starting point of the read access. For each byte received in Step 6, the read address increments. There is no limit on the number of bytes to be read in one read access function.

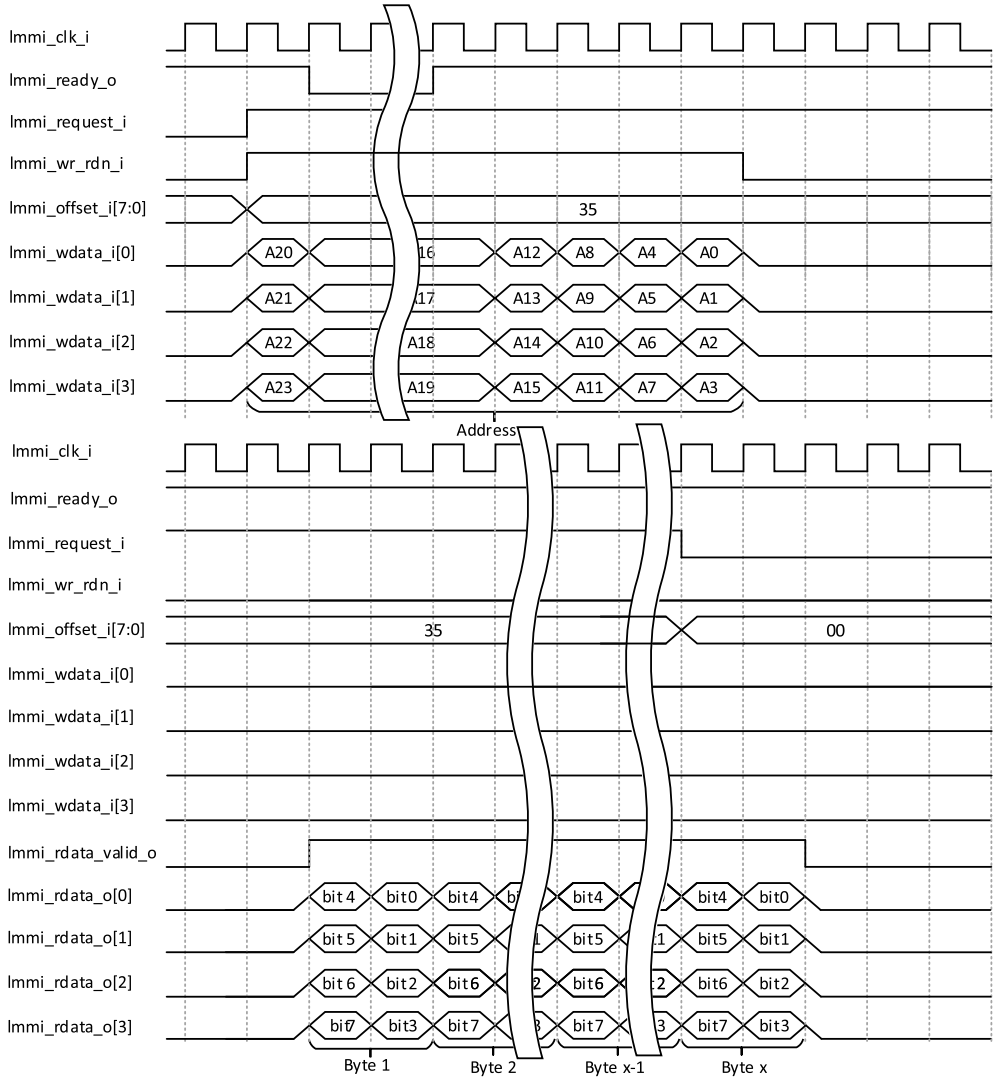


Figure 5.9. Sample Waveform for Read Access – lmmi_offset_i = 0x35

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6. Designing with the IP

This section provides information on how to generate the IP Core using the Lattice Radiant software and how to run simulation and synthesis. For more details on the Lattice Radiant software, refer to the Lattice Radiant Software User Guide.

Note: The screenshots provided are for reference only. Details may vary depending on the version of the IP or software being used. If there have been no significant changes to the GUI, a screenshot may reflect an earlier version of the IP.

6.1. Generating and Instantiating the IP

The Lattice Radiant Software can be customized to generate modules and IPs and integrate them into the device architecture. The procedure for generating the Flash Access for MachXO5-NX IP Core in Lattice Radiant software is described below.

To generate the Flash Access for MachXO5-NX IP Core:

1. Create a new Lattice Radiant software project or open an existing project.
2. In the **IP Catalog** tab, double-click **Flash Access for MachXO5-NX** under **IP, Architecture_Modules** category. The **Module/IP Block Wizard** opens, as shown in Figure 6.1. Enter values in the **Component name** and the **Create in** fields and click **Next**.

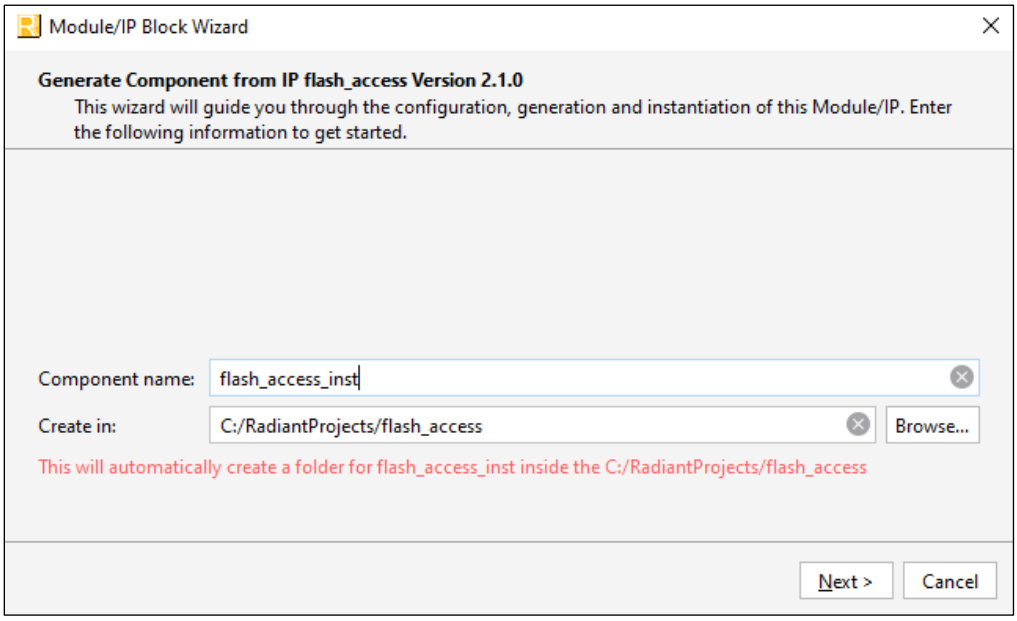


Figure 6.1. Module/IP Block Wizard

3. In the **Module/IP Block Wizard** window, customize the selected Flash Access for MachXO5-NX IP Core using drop-down menus and check boxes. For a sample configuration, see Figure 6.2, Figure 6.3, Figure 6.4, and Figure 6.5. For configuration options, see the General section.

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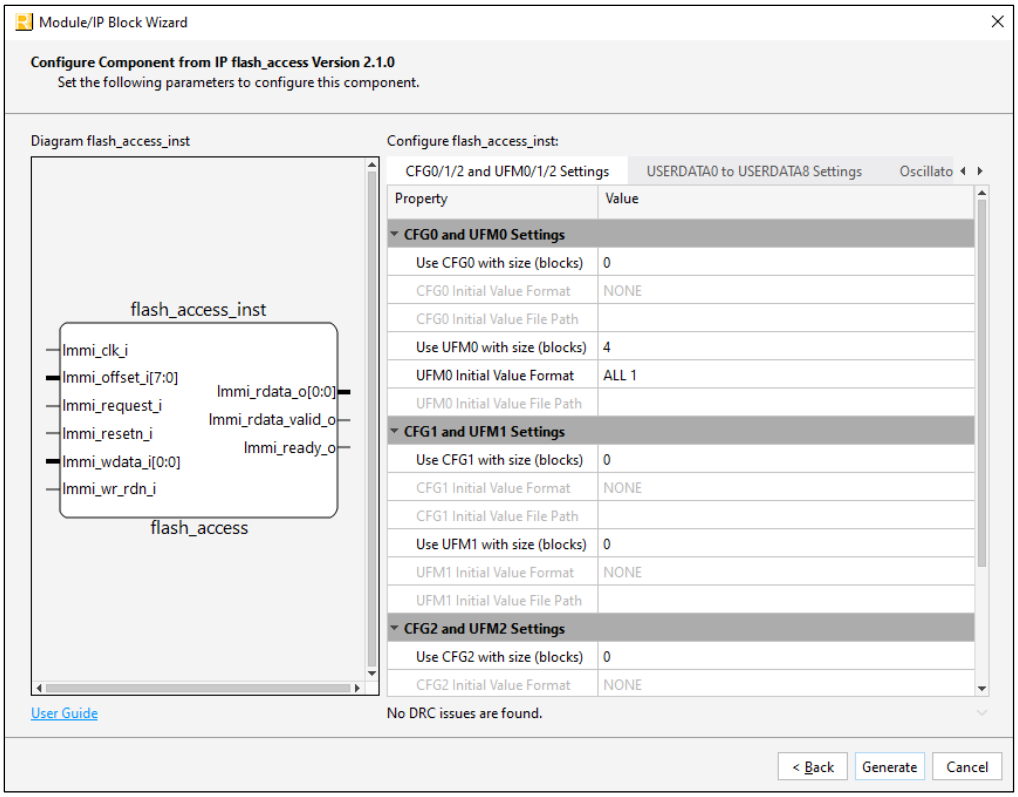


Figure 6.2. Configure User Interface of Flash Access for MachXO5-NX IP Core – CFG0/1/2 and UFM0/1/2/3 Settings

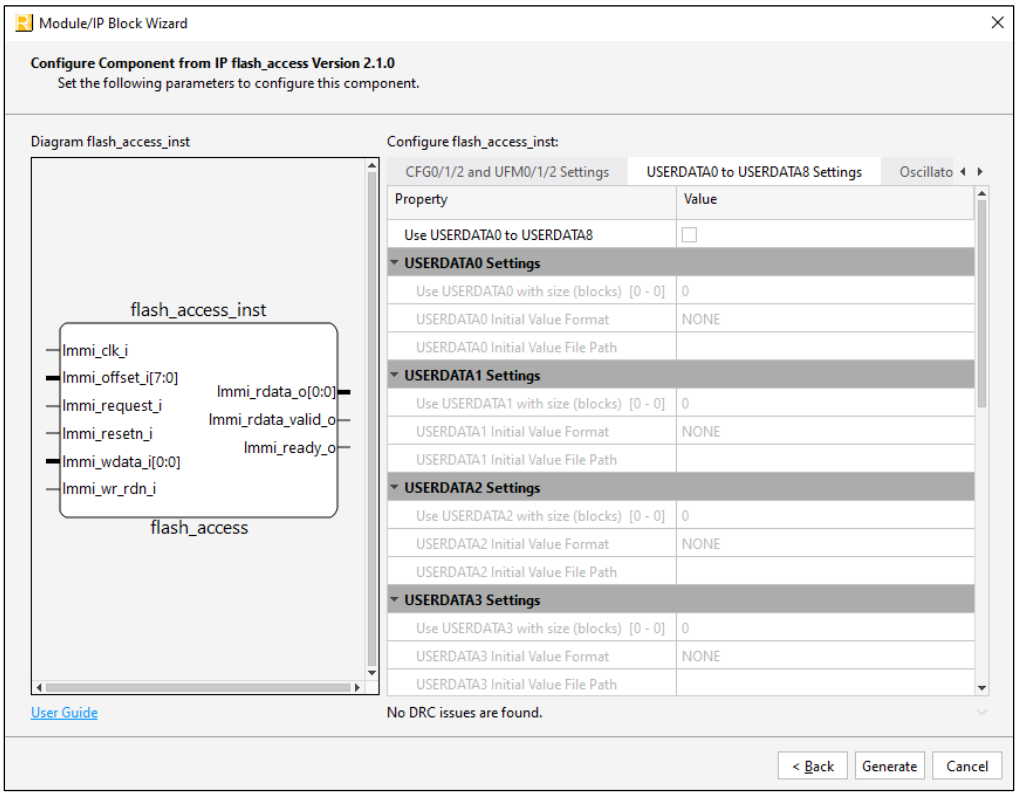


Figure 6.3. Configure User Interface of Flash Access for MachXO5-NX IP Core – USERDATA0 to USERDATA8 Settings

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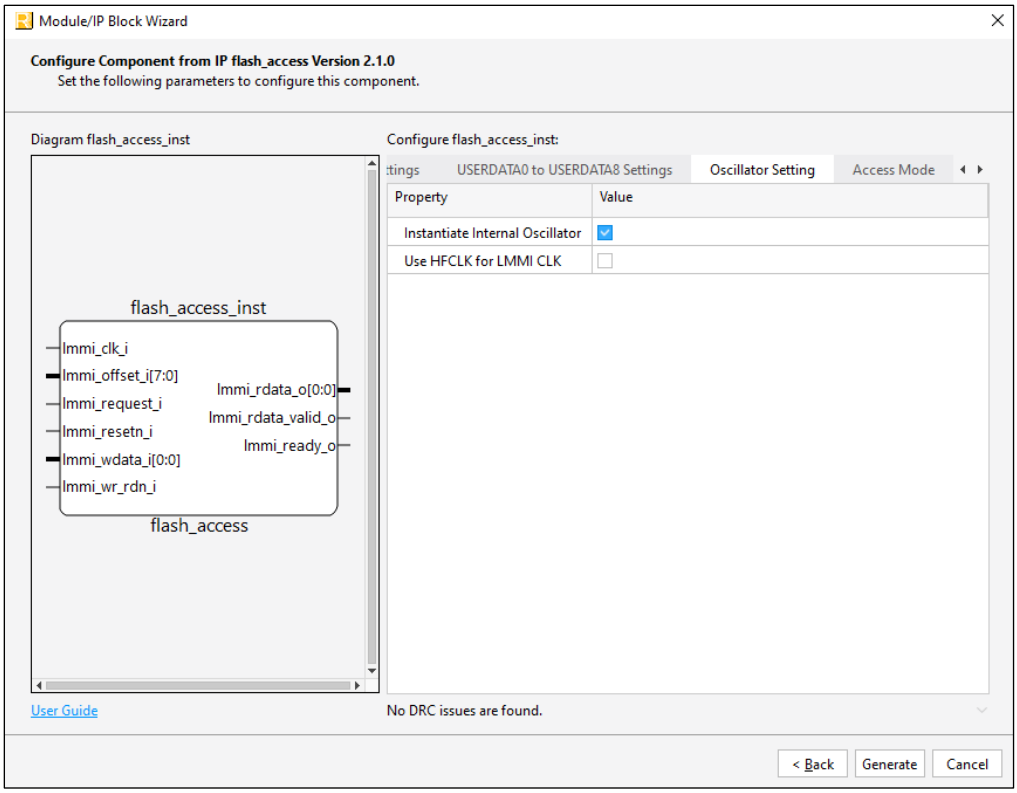


Figure 6.4. Configure User Interface of Flash Access for MachXO5-NX IP Core – Oscillator Settings

4. Enable Config LMMI Interface to access CONFIG_LMMI primitive. This option is unchecked by default (Figure 6.5).

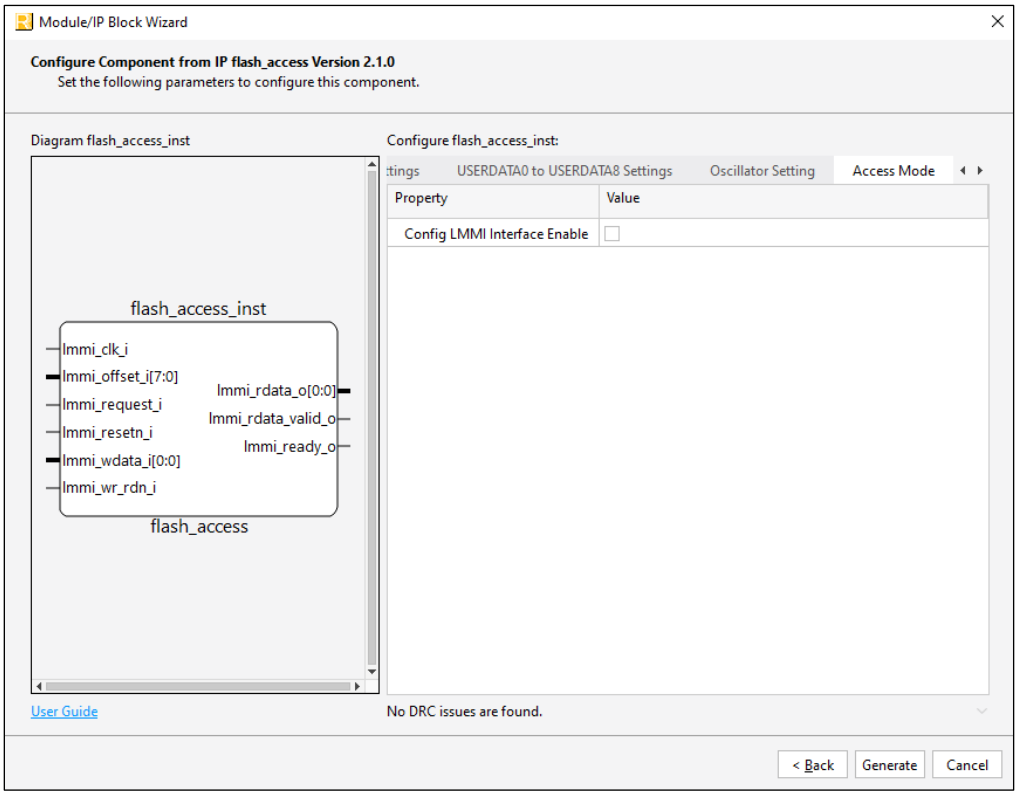


Figure 6.5. Configure User Interface of Flash Access for MachXO5-NX IP Core – Access Mode

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5. Click **Generate**. The **Check Generated Result** dialog box opens, displaying design block messages and results (Figure 6.6).

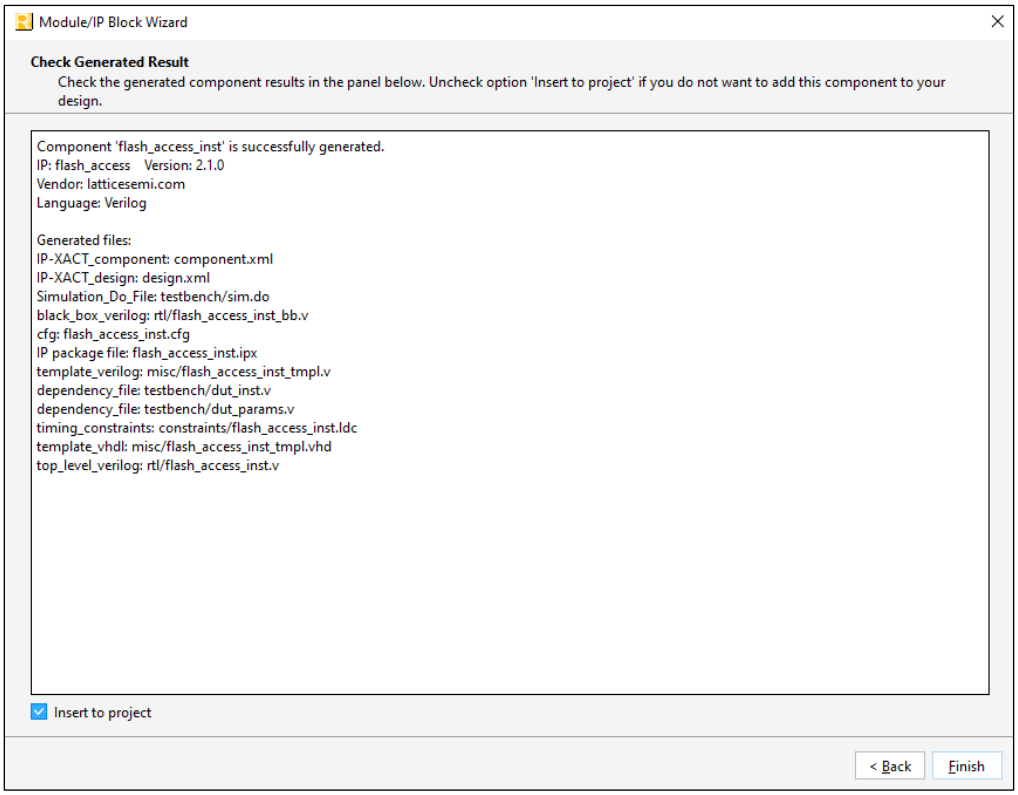


Figure 6.6. Check Generated Result

6. Click the **Finish** button. All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields shown in Figure 6.1.

6.1.1. Generated Files and File Structure

The generated Flash Access for MachXO5-NX IP Core package includes the closed-box (_bb.v) and instance templates (_tmpl.v/vhd) that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file (.v) that can be used as an instantiation template for the IP core is also provided. You may use this example as the starting template for your top-level design. The generated files are listed in Table 6.1.

Table 6.1. Generated File List

Attribute	Description
<Component name>.ipx	Contains the information on the files associated to the generated IP.
<Component name>.cfg	Contains the parameter values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Component name>.v	Provides an example RTL top file that instantiates the IP core.
rtl/<Component name>_bb.v	Provides the synthesis closed-box.
misc/<Component name>_tmpl.v misc /<Component name>_tmpl.vhd	Provide instance templates for the IP core.

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6.2. Running Functional Simulation

After the IP is generated, running functional simulation can be performed using different available simulators. The default simulator already has pre-compiled libraries ready for simulation. Choosing a non-default simulator, however, may require additional steps.

To run functional simulation using the default simulator, follow steps below.

6.2.1. Default Test Sequence

1. Click the  button located on the **Toolbar** to initiate the **Simulation Wizard** shown in Figure 6.7.

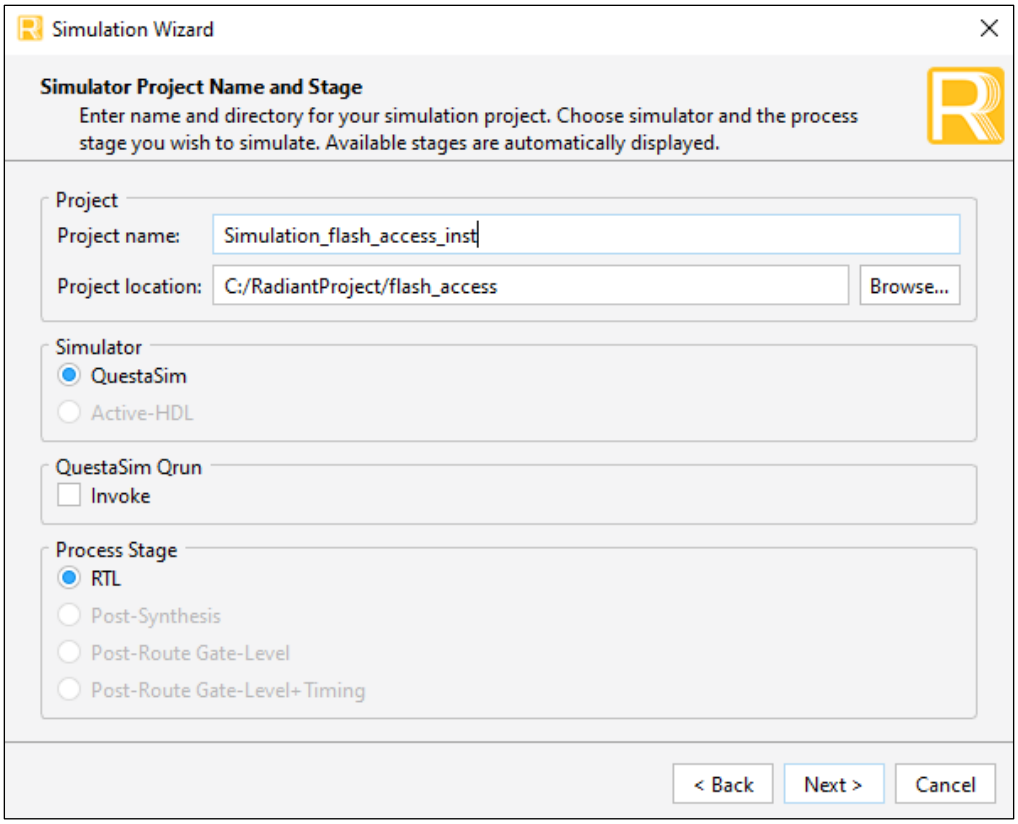


Figure 6.7. Simulation Wizard

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2. Click **Next** to open the **Add and Reorder Source** window, as shown in Figure 6.8.

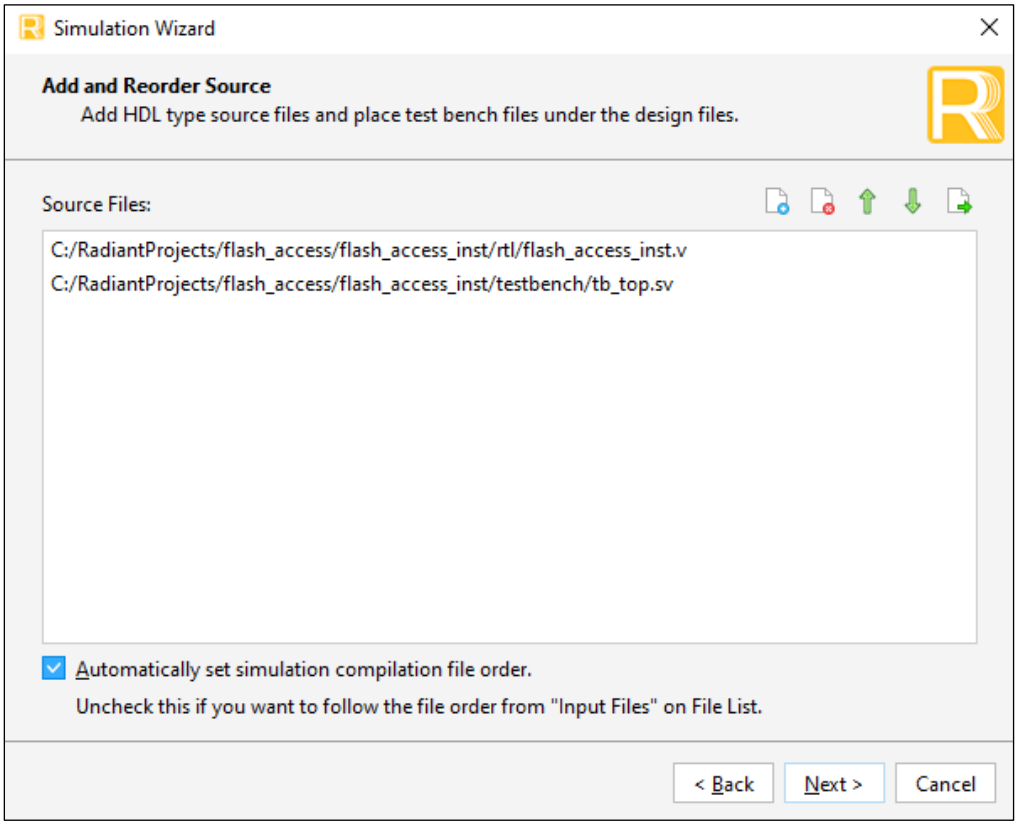


Figure 6.8. Adding and Reordering Source

3. Click **Next**. The **Summary** window is shown. Click **Finish** to run the simulation.

Note: It is necessary to follow the procedure above until it is fully automated in the Lattice Radiant software suite. The results of the simulation in our example are provided in Figure 6.9.

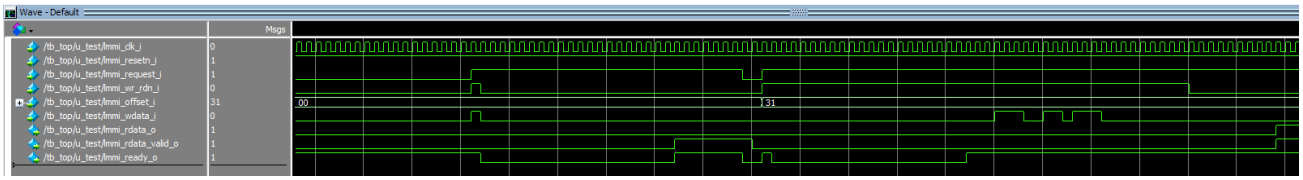


Figure 6.9. Simulation Waveform

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6.2.2. Other Test Sequence

After running the default test sequence, you can run other available test sequences. The available tests are shown in Table 6.2.

Table 6.2. Other Test Sequences

Test Name	Test Function
check_status_test	Checks the current status of the flash.
flash_erase_test	Tests the erase function.
flash_write_read_test	Tests write to and read from flash functions.

To run a test sequence:

1. Run the default test sequence described in the Default Test Sequence section.
2. Go to the project simulation directory used in running the default test sequence, it is the <Project location>/<Project name> provided in Figure 6.7. Copy the .mdo and .TXT files (Figure 6.10).

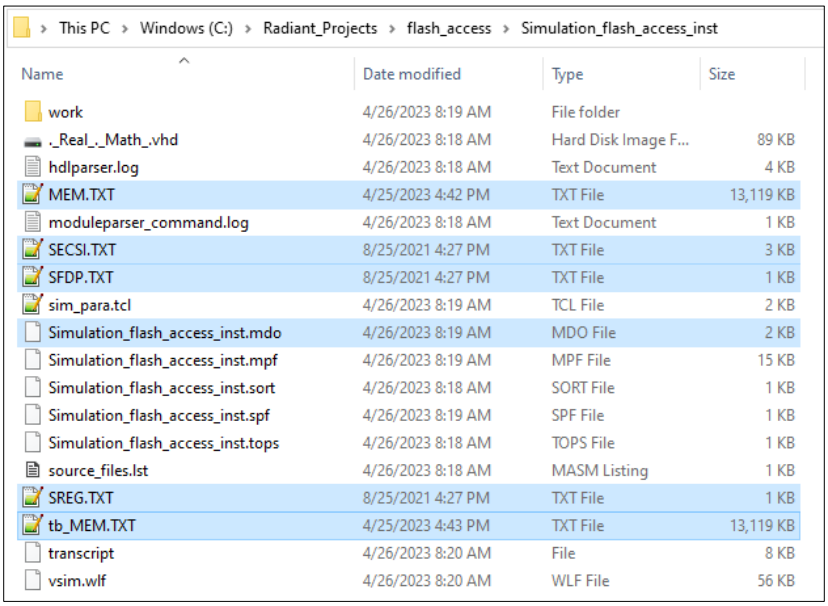


Figure 6.10. List of Files under Project Simulation Directory

3. Paste the files to a new folder, *other_tests*, for example, under the <Project Location> directory.

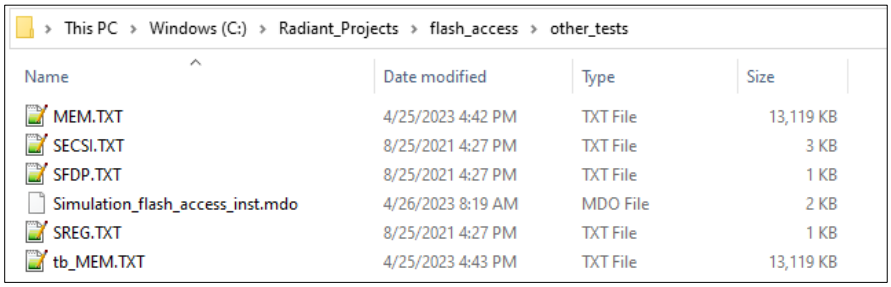


Figure 6.11. List of Files under New Directory

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4. Edit the .mdo file. Replace <project simulation name> with *other_tests.* It should be the same under the new folder name. Then, remove the first line of the .mdo file.

   Note: The **Invoke** option under **QuestaSim Qrun** must be unchecked for the .mdo file to be generated.

5. Add the following options on vsim command of the .mdo file:

   +<test name in Table 6.2>

   +iter=<# of iterations>

   Figure 6.12 shows the difference between the edited and the default .mdo file.

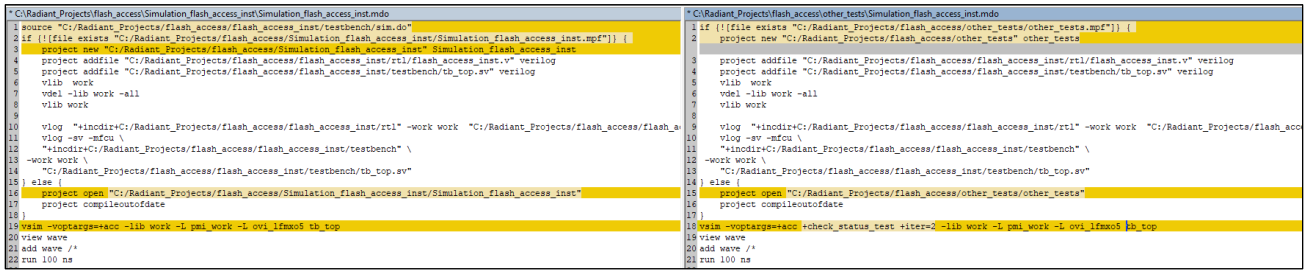


Figure 6.12. Difference of .mdo Files

6. Save the edited .mdo file.

7. Go back to the Lattice Radiant software. Click the icon located on the **Toolbar** to initiate the **ModelSim** software.

8. After opening the **ModelSim** software, run the following commands in the command line:

```
cd other_tests
do <project_name.mdo>
```

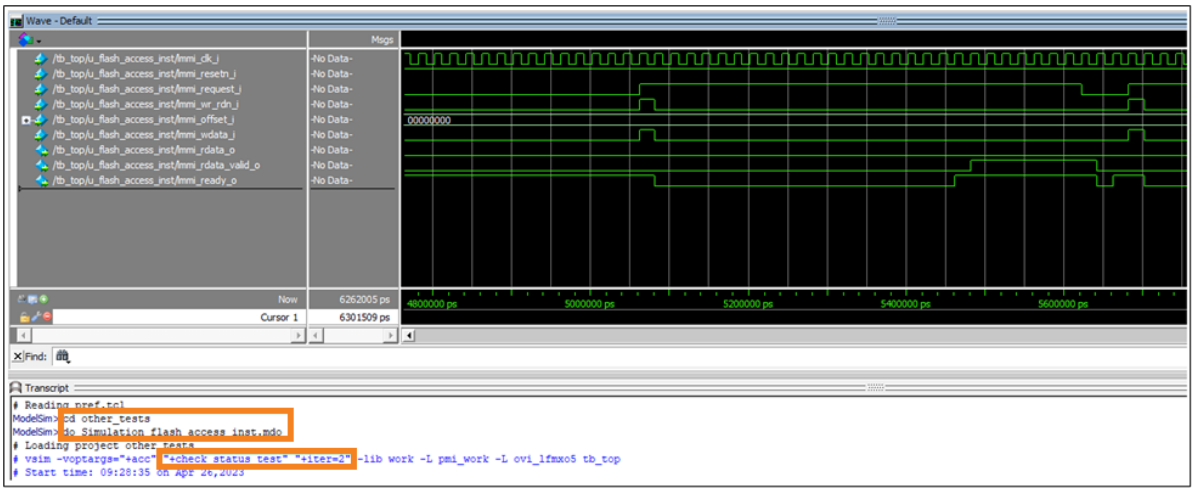


Figure 6.13. Running Other Test Sequence Output Waveform

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Appendix A. Limitations

- When target SPI port persistent mode is enabled in the user design, do not access the SSPI/JTAG port when accessing flash memory using the Flash Access IP or vice versa. The activities like driving SCSN/TMS pins low or running Reveal while accessing the flash, may result in flash access failure.
- When flash access is started by driving lmmi_request_i high, the connection of the hard JTAG TDO configuration pin becomes disconnected. Any JTAG access such as Reveal and programming/configuration cannot be done using the hard JTAG port when there is an on-going flash access operation. When flash access operation is finished and lmmi_request_i goes low, the connection to the TDO line will be restored
- The simulation/test environment does not support the optional LMMI Interface for Config Access.
- For the Flash Access IP to operate properly, the SLAVE_I2C_PORT/SLAVE_I3C_PORT option in the Device Constraint Editor of the Lattice Radiant software must be set to DISABLE.

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Appendix B. Internal Flash Memory Timing Specifications

The following table shows the internal flash memory timing specifications for supported operations.

Table B.1. Internal Flash Memory Timing Specifications for MachXO5-NX Devices

Device	Flash Size (Mb)	Operation	Typical	Maximum	Unit
LFMXO5-25, LFMXO5-25P	32	Page program	0.4	3	ms
		4 KB sector erase	45	400	ms
		32 KB sector erase	120	1600	ms
		64 KB sector erase	150	2000	ms
		Chip erase	10	50	s
LFMXO5-55T, LFMXO5-55TP, LFMXO5-100T, LFMXO5-100TP	128	Page program	0.4	3	ms
		4 KB sector erase	45	400	ms
		32 KB sector erase	120	1600	ms
		64 KB sector erase	150	2000	ms
		Chip erase	40	200	s
LFMXO5-35, LFMXO5-35T, LFMXO5-65, LFMXO5-65T	128	Page program	0.4	3	ms
		4 KB sector erase	45	400	ms
		32 KB sector erase	120	1600	ms
		64 KB sector erase	150	2000	ms
		Chip erase	40	200	s

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References

- Flash Access IP Release Notes (FPGA-RN-02064)
- sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099)
- Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039)
- MachXO5-NX web page
- Flash Access IP Core web page
- Lattice Radiant Software web page
- Lattice Solutions IP Cores web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

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Revision History

Note: In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

Document Revision 2.1, IP v2.3.0, October 2026

Section	Change Summary
All	• Made minor editorial changes. • Added LFMXO5-25P, LFMXO5-55TP, and LFMXO5-100TP devices, where appropriate.

Introduction	• In Table 1.1. Summary of the Flash Access IP Core:
	  • Updated supported devices.
	  • Updated IP core version and software version in Lattice Implementation.
	• In Table 1.2. Flash Access IP Support Readiness:
	  • Removed *Hardware Validated* column.
	• Removed the Hardware Support section.
	• In the Naming Conventions section:
	  • Added the Attribute Names section.

Document Revision 2.0, IP v2.2.0, January 2026

Section	Change Summary
All	• Added a note on the IP version in the Quick Facts and Revision History sections. • Made minor editorial changes.
Designing with the IP	• Added note on IP version in GUI. • In the Generated Files and File Structure section: • Updated descriptions in Table 6.1. Generated File List.
Appendix A. Limitations	• Added need to disable the SLAVE_I2C_PORT/SLAVE_I3C_PORT option.

Document Revision 1.9, IP v2.2.0, July 2025

Section	Change Summary

Introduction	• Updated description.
	• In Table 1.1. Summary of the Flash Access IP Core:
	  • Renamed *Supported FPGA Family* to *Supported Devices* and incorporated *Targeted Devices* information into row.
	  • Removed *Targeted Devices* row.
	  • Added IP core version to *Lattice Implementation* and made minor editorial changes.
	• In Table 1.2. Flash Access IP Support Readiness:
	  • Added LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T information.
	  • Removed *On-chip Flash* column.
	• Added LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T to supported devices in the Features section.

Functional Description	Added LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T devices to the discussion in the Clocking Overview section.

IP Parameter Description	• In Table 3.1. Attributes Table:
	  • Added selectable values and default for LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T for the attributes *Use CFG0/1/2 with size* under the CFG0/1/2 and UFM0/1/2 Settings Group sections.
	  • Added selectable values and default for LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T and updated dependency information for the attributes *Use UFM0/1/2 with size* under the CFG0/1/2 and UFM0/1/2 Settings Group sections.
	  • Added selectable values for LFMXO5-35, LFMXO5-35T, LFMXO5-65, and

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Section	Change Summary
	LFMXO5-65T for the attributes *Use USERDATA0/1/2/3/4/5/6/7/8 with size* under the USERDATA0/1/2/3/4/5/6/7/8 Settings Group sections. • Updated dependency information for the *Read Access Mode* attribute under the Access Mode section. • Added Note 1 to streamline listing of settings and default values by devices. • In Table 3.2. Attributes Description: • Updated descriptions for the attributes *Use CFG<0/1/2> with size*, *Use UFM<0/1/2> with size*, *Use USERDATA0 to USERDATA8*, *Use USERDATA<0..8> with size*, *Instantiate Internal Oscillator*, and *Read Access Mode*. • Added note regarding byte, page, sector, and block relationship to Table 3.4. Flash Memory Map LFMXO5-25. • Added Table 3.5. Flash Memory Map LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T and discussion. • In Table 3.7. Different Combinations of CFGx/UFMx Block Size: • Added LFMXO5-65T information. • In Table 3.8. Sample Settings 1: • Added LFMXO5-65T information. • In Table 3.9. Sample Settings 2: • Added LFMXO5-100T information.
Signal Description	In Table 4.1. Flash Access Module Signal Description: • Added Note 2 regarding CONFIG_IOSLEW setting in relation to lmmi_clk_i.
Designing with the IP	• Updated Figure 6.7. Simulation Wizard. • Added note to Step 4 in the Other Test Sequence section.
Appendix B. Internal Flash Memory Timing Specifications	In Table B.1. Internal Flash Memory Timing Specifications for MachXO5-NX Devices: • Added LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T information.
References	• Added Flash Access IP Core web page. • Updated listing to Lattice Radiant Software web page.

Document Revision 1.8, IP v2.1.0, January 2025

Section	Change Summary
IP Parameter Description	• In Table 3.4. Flash Memory Map LFMXO5-25: • Added *00* block start address row. • Added notes regarding primary image, golden image, and jump instruction programming. • In Table 3.5. Flash Memory Map LFMXO5-55T and LFMXO5-100T: • Updated *Contents* for *00* sector start address row. • Added notes regarding primary image, golden image, and jump instruction programming.

Document Revision 1.7, IP v2.1.0, December 2024

Section	Change Summary
Cover	Added IP version.
Introduction	• In Table 1.1. Summary of the Flash Access IP Core: • Added IP Changes row. • Removed IP Version row. • Added IP core version to *Lattice Implementation*. • Updated *Simulation* to refer to software user guide. • Added the IP Support Summary section. • Removed the IP Validation Summary section. • Updated LMMI interface for configuration access description in the Features section. • Added the Hardware Support section.

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Section	Change Summary
Functional Description	Added Figure 2.3. Flash Access Block Diagram (Config LMMI Interface Enable = Checked) and introductory sentence.

IP Parameter Description	• In Table 3.1. Attributes Table:
	  • Added *Config LMMI Interface Enable* attribute under Access Mode.
	• In Table 3.2. Attributes Description:
	  • Added *Config LMMI Interface Enable* attribute.

Designing with the IP	Updated Figure 6.1. Module/IP Block Wizard through Figure 6.8. Adding and Reordering Source.
Appendix A. Limitations	Added new section.
Appendix B. Internal Flash Memory Timing Specifications	Added new section.
References	• Updated reference names and reorganized references. • Added Flash Access IP Release Notes and sysCONFIG User Guide for Nexus Platform and Lattice Solutions IP Cores.

Document Revision 1.6, Lattice Radiant SW version 2024.1, September 2024

Section	Change Summary
All	• Revamped the document structure. • Updated the document title from *Flash Access IP Core – Lattice Radiant Software User Guide* to *Flash Access IP Core User Guide*.
Introduction	• Added the following sections: Overview of the IP, Quick Facts, Licensing and Ordering Information, IP Validation Summary, and Signal Names. • In Features, added *supports Config LMMI interface*.
Functional Description	• Changed the original subsection name of *Overview* to *IP Architecture Overview*. • In IP Architecture Overview, added the following description for the Config LMMI interface: *the IP implements the CONFIG_LMMI primitive in it to provide the Config LMMI interface that allow user logic inside the FPGA fabric to access the device configuration(CFG) functionalities. This option can be enabled by checking the Config LMMI Interface Enable option in the Flash Access IP core.* *Refer to Appendix D. Configuration Access from User Logic, in sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099) for more details.* • Newly added the Clocking, Reset, and User Interfaces sections.
IP Parameter Description	• Moved the original Table 2.2. Attributes Table and Table 2.3. Attributes Description to the General section. • In Table 3.2. Attributes Description, generally updated the language of description for the Use CFG<0/1/2> with size (blocks), Use UFM<0/1/2> with size (blocks), and Use USERDATA0 to USERDATA8 attributes. • Moved the original Table 2.9 Attributes Description to the Setting Initial Data in Flash Memory section and updated its table caption to Table 3.3. Partition Initial Value Format Attributes Description. • Moved the original Table 2.4 Flash Memory Map LFMXO5-25, Table 2.5 Flash Memory Map LFMXO5-55T and LFMXO5-100T, and Table 2.6 Different Combinations of CFGx/UFMx Block Size to the Internal Memory Block Partitioning section. • Moved the original Table 2.7. Sample Settings 1 and Table 2.8. Sample Settings 2 to the IP Parameter Settings for Example Use Cases section.
Signal Description	Moved the original Table 2.1 Flash Access Module Signal Description to this section and added the following signals to be table: *config_nflash_i*, *config_lmmi_request_i*, *config_lmmi_offset_i[7:0]*, *config_lmmi_wr_rdn_i*, *config_lmmi_wdata_i[7:0]*, *config_lmmi_ready*, *config_lmmi_rdata_valid_o*, and *config_lmmi_rdata_o[7:0]*.
Flash Access Function	Moved the original Section 2.7 Flash Functions to this section.
Designing with the IP	• Moved the original section 3.1 Generating the IP to the Generating and Instantiating the IP section.

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Section	Change Summary
	• Moved the original section 3.2 Running Functional Simulation to the Running Functional Simulation section. • Updated the following figures: Figure 6.1. Module/IP Block Wizard, Figure 6.2. Configure User Interface of Flash Access for MachXO5-NX IP Core – CFG0/1/2 and UFM0/1/2/3 Settings, Figure 6.3. Configure User Interface of Flash Access for MachXO5-NX IP Core – USERDATA0 to USERDATA8 Settings, Figure 6.4. Configure User Interface of Flash Access for MachXO5-NX IP Core – Oscillator Settings, and Figure 6.6. Check Generated Result. • Added Step 3 for Config LMMI Interface and added Figure 6.5. Configure User Interface of Flash Access for MachXO5-NX IP Core – Access Mode accordingly.

Document Revision 1.5, Lattice Radiant SW version 2023.1, March 2024

Section	Change Summary
Disclaimers	Updated disclaimers.
Acronyms in This Document	Added JTAG and SSPI.
Functional Descriptions	Added note to Overview section regarding SSPI/JTAG bus operation limitation with SSPI persistence enabled in user mode when using the Flash Access IP to access flash memory.

Document Revision 1.4, Lattice Radiant SW version 2023.1, September 2023

Section	Change Summary
Introduction	Newly added *LFMXO5-55T* and *LFMXO5-100T* as supported devices of the Flash Access IP.

Functional Descriptions	• In the Overview section, added *LFMXO5-55T* and *LFMXO5-100T* as devices in which only one Oscillator block can be instantiated.
	• Table 2.1. Flash Access Module Signal Description:
	  • added *the maximum frequency supported is 50 MHz* to the Description of the clk_i signal;
	  • added *the maximum frequency supported is 50 MHz* to the Description of the lmmi_clk_i signal;
	  • changed the Width of the lmmi_wdata_i and lmmi_rdata_o signals from *1* to *STANDARD: 1*, *QUAD: 4*;
	  • updated the Description of the lmmi_wdata_i signal to *STANDARD: serial interface for transmitting data*, *QUAD: four data input for transmitting data*;
	  • updated the Description of the lmmi_rdata_o signal to *STANDARD: serial interface for receiving data*, *QUAD: four data input for receiving data*.
	• Table 2.2. Attributes Table:
	  • for the Use CFG0 with size (blocks) Attribute, updated its Selectable Values (*LFMXO5-25: 0, 11, 15*; *LFMXO5-55T and LFMXO5-100T: 0, 33, 48*) and Default (*LFMXO5-25: 0*; *LFMXO5-55T and LFMXO5-100T: 0*);
	  • for the CFG0 Initial Value Format Attribute, changed its Default value to —;
	  • for the Use UFM0 with size (blocks) Attribute, updated its Selectable Values (*LFMXO5-25: 0, 4; LFMXO5-55T and LFMXO5-100T: 0, 15*),
	Default (*LFMXO5-25: 4*; *LFMXO5-55T and LFMXO5-100T: 15*),
	Dependency on Other Attributes (*LFMXO5-25: Use CFG0 with size (blocks) < 15*; *LFMXO5-55T and LFMXO5-100T: Use CFG0 with size (blocks) < 48*);
	  • for the UFM0 Initial Value Format Attribute, changed its Default value to *ALL 1*;
	  • for the Use CFG1 with size (blocks) Attribute, updated its Selectable Values (*LFMXO5-25: 0, 11, 15*; *LFMXO5-55T and LFMXO5-100T: 0, 33, 48*) and Default (LFMXO5-25: 0; LFMXO5-55T and LFMXO5-100T: 0);
	  • for the Use UFM1 with size (blocks) Attribute, updated its Selectable Values (*LFMXO5-25: 0, 4*; *LFMXO5-55T and LFMXO5-100T: 0, 15*),

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Section	Change Summary
	Default (*LFMXO5-25: 0*; *LFMXO5-55T and LFMXO5-100T: 0*), and Dependency on Other Attributes (*LFMXO5-25: Use CFG1 with size (blocks) < 15*; *LFMXO5-55T and LFMXO5-100T: Use CFG1 with size (blocks) < 48*); • for the Use CFG2 with size (blocks) Attribute, updated its Selectable Values (*LFMXO5-25: 0, 11, 15*; *LFMXO5-55T and LFMXO5-100T: 0, 33, 48*) and Default (*LFMXO5-25: 0*; *LFMXO5-55T and LFMXO5-100T: 0*); • for the Use UFM2 with size (blocks) Attribute, updated its Selectable Values (*LFMXO5-25: 0, 4*; *LFMXO5-55T and LFMXO5-100T: 0, 15*), Default (*LFMXO5-25: 0*; *LFMXO5-55T and LFMXO5-100T: 0*), and Dependency on Other Attributes (*LFMXO5-25: Use CFG1 with size (blocks) < 15; LFMXO5-55T and LFMXO5-100T: Use CFG1 with size (blocks) < 48*); • updated the Selectable Values to *LFMXO5-25: 1–17*; *LFMXO5-55T and LFMXO5-100T: 1-110* for the following Attributes: Use USERDATA0 with size (blocks), Use USERDATA1 with size (blocks), Use USERDATA2 with size (blocks), Use USERDATA3 with size (blocks), Use USERDATA4 with size (blocks), Use USERDATA5 with size (blocks), Use USERDATA6 with size (blocks), Use USERDATA7 with size (blocks), and Use USERDATA8 with size (blocks); • newly added the Read Access Mode Attribute under Access Mode. • Updated Figure 2.3. Sample Connection of Oscillator Soft IP to Flash Access Soft IP. • Table 2.3. Attributes Description: • updated the Description of the Use CFG<0/1/2> with size (blocks) Attribute; • updated the Description of the Use UFM<0/1/2> with size (blocks) Attribute; • changed *total number of blocks should not exceed 18 blocks* to *the total number of blocks should not exceed 17 blocks* in the Description of the Use USERDATA<0..8> with size (blocks) Attribute; • newly added the Read Access Mode Attribute and its Description. • In the Connecting an Instantiated Oscillator Soft IP to the Flash Access Soft IP section, updated that *in the LFMXO5-25, LFMXO5-55T and LFMXO5-100T devices, only one OSCILLATOR block can be instantiated*. • Table 2.4. Flash Memory Map LFMXO5-25: • changed the table caption from *Flash Memory Map* to *Flash Memory LFMXO5-25*; • changed *63 (0x3F_FFFF)* to *63 (0x3E_FFFF)* in the Block End Address (24-Bit Byte Address) column; • changed *Total ≤ 18* to *Total ≤ 17* in the Block Size column; • changed *Total ≤ 288* to *Total ≤ 272* in the Sector Size column. • Newly added description of CFG and UFM blocks in LFMXO5-55T and LFMXO5-100T devices in the Block Partitioning section. • Newly added Table 2.5. Flash Memory Map LFMXO5-55T and LFMXO5-100T and the related table note. • Updated Table 2.6. Different Combinations of CFGx/UFMx Block Size to reflect the use of different combinations of CFGx/UFMx blocks on LFMXO5-100T devices. • Updated Table 2.7. Sample Settings 1 and Table 2.8. Sample Settings 2 to reflect sample settings on LFMXO5-100T devices. • Table 2.10. Functions supported by Flash Access IP: • changed the Function of *0x30* and *0x31* to Standard Read Access; • newly added *0x34* and *0x35* as Quad Read Access and provided corresponding descriptions. • In the Read Access Sequence section: • changed *for every 1 byte received in Step 8, the read address increments* to *for every 1 byte received in Step 6, the read address increments* below the steps for performing the Standard Read Access; • newly added contents of the Quad Read Access (0x34) and Quad Read Access (0x35).
IP Generation, Simulation, and	Removed the original section 3.3 IP Evaluation.

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Section	Change Summary
Validation	
References	Newly added links to Lattice Radiant Software Web Page, MachXO5-NX Family Devices Web Page, and Lattice Insights for Training Series and Learning Plans.

Document Revision 1.3, Lattice Radiant SW version 2023.1, May 2023

Section	Change Summary
Introduction	Updated the content to specify the Flash Access is applicable for MachXO5-NX IP Core and LFMXO5-25 devices.
Functional Descriptions	• Updated the content to specify the Flash Access is applicable for MachXO5-NX IP Core and LFMXO5-25 devices. • Updated Table 2.9. Functions supported by Flash Access IP to add Access Type column.
IP Generation, Simulation, and Validation	• Changed Title from 'Flash Access IP Generation and Simulation' to 'IP Generation, Simulation, and Validation'. • Updated the entire section.
References	Removed 'AMBA 3 AHB Lite Protocol V1.0'.
Technical Support Assistance	Added reference link to the Lattice Answer Database.

Document Revision 1.2, Lattice Radiant SW version 3.2, August 2022

Section	Change Summary

Introduction	• In the Features section:
	  • updated the supported input clock frequency to 50 MHz;
	  • changed the supported device to LFMXO5-25.

Functional Descriptions	• In Table 2.2. Attributes Table:
	  • updated the Selectable Values for the Frequency of the internal LMMI CLK (MHz) Attribute;
	  • change the Default to 50 for the Frequency of the internal LMMI CLK (MHz) Attribute.
	• In Table 2.9. Functions supported by Flash Access IP:
	  • updated the Function and Description for the Read Function Group.
	• In the Read Access Sequence section:
	  • updated Figure 2.9. Sample Waveform for Read Access - lmmi_offset = 0x30;
	  • newly added Figure 2.10. Sample Waveform for Read Access - lmmi_offset_i = 0x31;
	  • updated the description for Figure 2.9. Sample Waveform for Read Access - lmmi_offset = 0x30 and Figure 2.10. Sample Waveform for Read Access - lmmi_offset_i = 0x31;
	  • deleted the original last paragraph of this section.

Document Revision 1.1, Lattice Radiant SW version 3.2, May 2022

Section	Change Summary
Functional Descriptions	• Editorial changes in Section 2.1 Overview. • Updated Figure 2.1. Flash Access Block Diagram (Use HFCLK for LMMI CLK = Unchecked), Figure 2.2. Flash Access Block Diagram (Use HFCLK for LMMI CLK = Checked), Figure 2.3. Sample Connection of Oscillator Soft IP to Flash Access Soft IP, Figure 2.6. Sample Waveform for On-chip Erase Sequence. • Updated Table 2.1. Flash Access Module Signal Description. Added rows *clk_i* and *rstn_i*. Table 2.3. Attributes Description, Table 2.4. Flash Memory Map, Table 2.5. Different Combinations of CFGx/UFMx Block Size, Table 2.6. Sample Settings 1, Table 2.7. Sample Settings 2. • Updated description of Section 2.4 Connecting an Instantiated Oscillator Soft IP to the Flash Access Soft IP.

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Section	Change Summary
	• Updated Section 2.7.3 On-chip Flash Erase Sequence. Updated the value of *Immi_offset_i* from 0x14 to 0x13. • Updated description of Section 2.7.4 Write Access Sequence.

Flash Access IP Generation and Simulation	• Updated Table 3.2. Other Test Sequences.
	  • Removed row flash_reset_test.
	  • Added rows check_status_test and flash_write_read_test.
	  • Changed row flash_sector_erase_test to flash_erase_test.

Document Revision 1.0, Lattice Radiant SW version 3.1, January 2022

Section	Change Summary
All	Initial release.

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