

Lattice Radiant Software 3.1.1 Release Notes

Welcome to Lattice Radiant® software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs).

What's New in Radiant Software 3.1.1

- ▶ **Device Support:**
 - CertusPro™-NX (LFCPNX)
 - 100K (-7/-8/-9) HP/LP 1.0 V (COM/IND) – BFG484
 - 100K (-7/-8/-9) HP/LP 1.0 V (COM/IND) – CBG256
 - Available under subscription licensing.
 - Certus™-NX-RT (UT24C)
 - 40K (-7) HP/LP 1.0 V (AUTO) – CABGA256 is license controlled.
 - CertusPro™-NX-RT (UT24CP)
 - 100K (-8) HP/LP 1.0 V (IND) – BBG484 is license controlled.
- ▶ **Tool and Other Enhancements:**
 - **Radiant Device Selector** – UT24C and UT24CP OPNs (Ordering Part Number) have been added to the Device Selector for the RT (Radiation Tested) Devices.

Support for Third-Party Synthesis and Simulator Tools

The Synopsys Synplify Pro® for Lattice synthesis tool and the Siemens ModelSim® Lattice Edition simulator tool are included in the Radiant software.

- ▶ **Synopsys Synplify Pro FPGA synthesis software version S-2021.09LR**
 - ▶ Release Notes for Synplify Pro are located in `..\<install_directory>\radiant\3.1\synpbase\doc\`. The file name is `release_notes.pdf`.
 - ▶ A full set of documents for Synplify Pro are also located in `..\<install_directory>\radiant\3.1\synpbase\doc\`.
- ▶ **Siemens ModelSim Lattice Edition 2021.4 revision 2021.10**
 - ▶ Release Notes for ModelSim Lattice Edition are located in `..\<install_directory>\radiant\3.1\modeltech\`. The file names are `RELEASE_NOTES.html` or `RELEASE_NOTES.txt`.

- ▶ A full set of documents for ModelSim Lattice Edition are located in
`..\<install_directory>\radiant\3.1\modeltech\doc\.`
- ▶ **Siemens Questa® 2020.4**
- ▶ **Cadence Xcelium® 20.09-s004**
- ▶ **Synopsys VCS® Q-2020.03**

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Radiant software, it may be necessary to re-generate some IP, per the procedures described in the following table. These procedures adapt the project for the changes in Radiant software.

Find out which version of Radiant software your project was created with. Then work through the changes for that and every later version, starting with the earliest and going to the most recent. For example, if your project was created with Radiant software 1.0, you would start with the changes for Radiant software 1.0. After completing those changes, you would work on the changes for Radiant software 2.0, and so on.

Once saved, the project will not be compatible with earlier Radiant software versions.

Versions	IP		IP Regeneration Procedures
	CrossLink-NX (LIFCL), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP)	ice40UP	
3.1.1	PLL (Phase Locked Loop) ADC (Analog to Digital Converter) ROM (Read-only Memory) MPCS (Multi-Protocol PCS) DDR_Generic (DDR Generic Interfaces) GDDR7:1 (LVDS Interface) DDR_MEM (DDR Memory Interfaces) LPDDR4_MEM (LPDDR4 Memory Interface) MIPI_DPHY (MIPI D-PHY Interface) ADC_Sequencer (Analog to Digital Converter with Sequencer)	N/A	These IP used in designs created in Radiant 3.1 must be re-generated in Radiant 3.1.1
3.1	PLL (Phase Locked Loop) DDR_Generic (DDR Generic Interfaces) GDDR7:1 (LVDS Interface) DDR_MEM (DDR Memory Interfaces) LPDDR4_MEM (LPDDR4 Memory Interface) MIPI_DPHY (MIPI D-PHY Interface) ADC_Sequencer (Analog to Digital Converter) Large_RAM_DP (Dual Port Large RAM) Large_RAM_DP_True (True Dual Port Large RAM) Large_RAM_SP (Single Port Large RAM) Large_ROM (Read-only Large Memory) FIFO_DC (Dual Clock FIFO) Complex Mult MPCS (Multi-Protocol PCS)	N/A	These IP used in designs created in Radiant 3.0 must be re-generated in Radiant 3.1
3.0	PLL (Phase Locked Loop)	N/A	

Versions	IP		IP Regeneration Procedures
	CrossLink-NX (LIFCL), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP)	iCE40UP	These IP used in designs created in Radiant 2.2.1 must be re-generated in Radiant 3.0
	DDR_Generic (DDR Generic Interfaces)		
	GDDR7:1 (LVDS Interface)		
	DDR_MEM (DDR Memory Interfaces)		
	MIPI_DPHY (MIPI D-PHY Interface)		
	LFSR (Linear Feedback Shift Register)		
	ADC_Sequencer (Analog to Digital Converter)		
	RAM_DP_True (True Dual Port RAM)		
	RAM_DQ (Single Port RAM)		
	ROM (Read-only Memory)		
	FIFO		
	FIFO_DC		
	Shift Register		
	Sine-Cosine Table		
	Convert		
2.2.1	PLL (Phase Locked Loop)	N/A	These IP used in designs created in Radiant 2.2 must be re-generated in Radiant 2.2.1
	DDR_Generic (DDR Generic Interfaces)		
	GDDR7:1 (LVDS Interface)		
	DDR_MEM (DDR Memory Interfaces)		
	MIPI_DPHY (MIPI D-PHY Interface)		
	LFSR (Linear Feedback Shift Register)		
	ADC_Sequencer (Analog to Digital Converter)		
	RAM_DP (Pseudo Dual Port RAM)		
2.2	PLL (Phase Locked Loop)	PLL (Phase Locked Loop)	These IP used in designs created in Radiant 2.1 must be re-generated in Radiant 2.2
	DDR_Generic (DDR Generic Interfaces)		
	GDDR7:1 (7:1 LVDS Interface)		
	SDR (Single Data Rate)		
	DDR_MEM (DDR Memory Interfaces)		
	ADC (Analog to Digital Converter)		
	SEDC (Soft Error Detection/Correction)		
	Sin_Cos_Table (Sine Cosine Table)		
	OSC (Oscillator)		
	RAM_DQ (Single Port RAM)		
	RAM_DP_True (True Dual Port RAM)		
	FIFO		
	FIFO_DC (FIFO Dual Clock)		
2.1	PLL (Phase Locked Loop)	N/A	These IP used in designs created in Radiant 1.0, 2.0, or 2.0 SP1 must be re-generated in Radiant 2.1
	GDDR7:1 (7:1 LVDS Interface)		
	DDR_MEM (DDR Memory Interfaces)		
	DDR_Generic (DDR Generic Interfaces)		
	MIPI_DPHY (MIPI Interface)		
	ADC (Analog to Digital Converter)		
	SEDC (Soft Error Detection/Correction)		
	OSC (Oscillator)		
All IP: <ul style="list-style-type: none"> Starting with Radiant 2.1, PMIs for any IP created in Radiant software versions 1.0, 2.0, 2.0 SP1, user must add the Family attribute in all PMI instantiations. For designs created in previous versions of Radiant software (2.0 or prior), it is necessary to re-generate PLL IP in Radiant software 2.1. Otherwise, Radiant software 2.1 will issue an error when the previous generated PLL IP is detected in the design. Designs created using Radiant Software 2.0 SP1 with PLL will work without any errors. 			

Versions	IP		IP Regeneration Procedures
	CrossLink-NX (LIFCL), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP)	iCE40UP	

- The IO_TYPE HDL attribute default value has been changed since Radiant 2.0 SP1 from LVCMOS18 to LVCMOS33.
- If a LARGE_RAM IP generated from a previous Radiant version needs to be re-configured in Radiant 2.1, the IP must be re-created.

The following server IP are not compatible with Radiant 3.0 onwards. Use the latest versions of the IP available on the IP server:

- ▶ I2C Master version 1.0.3
- ▶ UART 16550 version 1.0.4
- ▶ DDR3 SDRAM Controller version 1.1.1
- ▶ DDR3 SDRAM Controller version 1.2.1
- ▶ LPDDR2 SDRAM Controller Lite version 1.1.1
- ▶ LPDDR2 SDRAM Controller Lite version 1.2.1

Migration Changes from Earlier Release

Hold Time Calculation Issue

Bug Number: DNG-11733

There was a hold time calculation error that was existent in Radiant 3.0 and fixed in the current Radiant 3.1 in which designs from Radiant 3.0 should make note of this issue.

For example, if your design has an output delay of +1.00 ns added to the constraints (set_output_delay), during hold calculations, this delay should be ideally subtracted from the destination clock path delay. Instead in Radiant 3.0 during hold calculations, this delay was added to the destination clock path delay resulting in an erred calculation.

In Radiant 3.0, for the aforementioned example, instead of +1.00 ns, you should change the delay to -1.00ns to correct the hold calculations.

sysConfig Parameters Settings Default value Change

Bug Number: DNG-12094

Starting Radiant 3.1, the defaults for sysConfig parameter settings for JTAG_PORT, DONE_PORT, INITN_PORT and PROGRAMN_PORT are changed to ENABLE. In Prior Radiant releases, these defaults were DISABLE. Previous default settings (DISABLE) for SDM ports signals (DONE, INITN, PROGRAMN) blew fuses and were irreversible.

This new change will now preserve JTAG port and PROGRAMN port for device configuration activities by default, matching previous device behavior. The user can optionally disable the ports if explicitly desired to increase GPIO or reduce static power. Furthermore, if a design failure is encountered due to not having enough PIO, the following constraint can be added to the .pdc file to allow sysConfig shared pins to be used as GPIO.

Please change the sysConfig setting to DISABLE in Device Constraint Editor (DCE) or add the following sysConfig constraint to .pdc constraint file:

```
ldc_set_sysconfig {JTAG_PORT=DISABLE DONE_PORT=DIABLE INITN_PORT=DISABLE  
PROGRAMN_PORT=DISABLE}
```

Note: This can be manually added to the .pdc file or you can change the sysConfig settings to DISABLE in Device Constraint Editor (DCE) which adds this constraint to the .pdc file when saved.

Help Resources

Available information resources for the Radiant software include the following:

- ▶ Online Help updated with CrossLink-NX (LIFCL), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX, and CertusPro-NX-RT (UT24CP) content.
- ▶ To view the Online Help, start the Lattice Radiant software and select the  “Getting Started” icon under Information Center.

System Requirements

The following shows the basic system requirements for Radiant software:

- ▶ Intel Pentium or Pentium-compatible PC
- ▶ 64-bit OS:
 - ▶ Windows 10
 - ▶ Red Hat Enterprise Linux 7.8 or 8.2
 - ▶ Ubuntu version 18.04 LTS or 20.04 LTS
 - ▶ CentOS 7.8
- ▶ Approximately 10 GB free disk space
- ▶ Computer Memory Requirement: 16 GB Recommended for running a single project. If running multiple projects, the memory requirement will be higher.
- ▶ 1024 X 768 graphics display
- ▶ Network adapter for license and network connectivity
- ▶ A Web browser with JavaScript capability

Issues Fixed

The following known issues are fixed in this release. Their workarounds are no longer needed.

CSI-2/D-PHY Transmitter IP hangs during Post synthesis/PAR simulations.

Devices affected: CrossLink-NX (LIFCL), Certus-NX (LFD2NX)

Bug number: DNG-9697

Fixed in Radiant 3.1.1

Modify default INIT value for HardDPHY RX soft IP when running at DPHY v1.1 data rate (<=1.5 Gbps).

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-10731

Fixed in Radiant 3.1.1

When you program a target device with designs involving EBRs with initial data, the initial data programmed into the EBRs may output incorrectly.

Devices affected: CrossLink-NX (LIFCL), Certus-NX (LFD2NX), CertusPro-NX (LFPCNX)

Bug number: DNG-11514

Fixed in Radiant 3.1.1

When Reveal is used with mixed language design projects, synthesis may fail using both LSE and Synplify Pro.

Devices affected: CrossLink-NX (LIFCL), Certus-NX (LFD2NX), CertusPro-NX (LFPCNX)

Bug number: DNG-11576

Fixed in Radiant 3.1.1

ADC Soft-IP “ADC Clock Divide” value must be a string.

Devices affected: CrossLink-NX (LIFCL), Certus-NX (LFD2NX), CertusPro-NX (LFPCNX)

Bug number: DNG-12220

Fixed in Radiant 3.1.1

Reveal Eye Opening Diagram cannot be generated on Linux OS.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-12259

Fixed in Radiant 3.1.1

Known Issues for Radiant 3.1.1

The following are known issues for the Radiant Software 3.1.1.

MAP incorrectly reports number of DPHY and PCIE/ADC resources for CrossLink-NX (LIFCL) QFN72 package.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-8297

When simulating Generic DDR, there may be a mismatch in the RTL and post-route simulation. Silicon is not affected.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CrossLink-NX (LIFCL), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), CertusPro-NX-RT (UT24CP)

Bug number: DNG-9639

For some SystemVerilog designs, Synplify Pro fails to identify multi-driven nets and the flow passes with no errors.

Workaround: Check the design for multi-driven nets and run the flow using LSE to verify.

Devices affected: CrossLink-NX (LIFCL), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), CertusPro-NX-RT (UT24CP)

Bug number: DNG-10132

When Reveal Controller is used for updating the PCS register (reg80) through the controller, it will cause the PCS Register value to be stuck at a value during successive writes.

Workaround: Re-download the bitstream.

Devices affected: CertusPro-NX (LFCPNX), CertusPro-NX-RT (UT24CP)

Bug number: DNG-12235

If you have a Hard IP in the design and are controlling it with Reveal Controller, Reveal Controller logic will overwrite the user logic which controls the Hard IP.

If LMMI bus IP is used as part of your design for dynamic update, it is recommended to not use the Reveal Controller for hard IP because the user design controlling the hard IP will be overwritten by Reveal Controller Logic.

Hard IPs: DPHY, I2CFIFO, PLL, PCS, PCIELL, SGMIICDR

Devices affected: CrossLink-NX (LIFCL), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), CertusPro-NX-RT (UT24CP)

Bug number: DNG-12253