10 Gb Ethernet PCS IP Core - Lattice Radiant Software

User Guide

FPGA-IPUG-02163-1.5

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
FIFO	First In First Out
MAC	Media Access Controller
MDIO	Management Data Input/Output
PCS	Physical Coding Sublayer
PHY	Physical Layer Device
PMA	Physical Medium Attachment
SMI	Serial Management Interface
RTL	Register Transfer Language
XGMII	10 Gigabit Media Independent Interface

1. Introduction

The 10 Gigabit Media Independent Interface (XGMII) connects Ethernet Media Access Controllers (MACs) and Physical Layer Devices (PHYs). This IP core implements the Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) functionality following the IEEE 802.3 10G Base-R specification.

1.1. Quick Facts

Table 1.1 presents a summary of the 10Gb Ethernet PCS IP Core.

Table 1.1. 10 Gb Ethernet PCS IP Quick Facts

IP Requirements	Supported FPGA Families	Certus Pro™-NX
Resource Utilization	Targeted Devices	LFCPNX-100
	Supported User Interface	XGMII, APB, MDIO
	Resources	See Table A.1.
Design Tool Support	Lattice Implementation	IP Core v1.1.x – Lattice Radiant™ Software 3.0
	Synthesis	Lattice Synthesis Engine
		Synopsys® Synplify Pro® for Lattice
	Simulation	For a list of supported simulators, see the Lattice Radiant Software User Guide.

1.2. Features

The key features of the 10G Ethernet PCS IP included

- PCS/PMA functions defined in IEEE 802.3 10G Base-R
- 64b/66b encoding and decoding
- Tx phase FIFO and Rx clock compensation FIFO
- XGMII Interface: 64 bit, 156.25 MHz
- Supports APB and MDIO Interfaces for MPCS and MMD register access

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal names that end with:

- _*n* are active low (asserted when value is logic 0)
- _*i* are input signals
- _*o* are output signals

1.3.3. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

2. Functional Description

2.1. Overview

The 10 Gb Ethernet PCS IP Core provides XGMII interface to MAC and follows IEEE802.3 10G Base-R standard. It supports 64-bit of data and 8-bit of control signals for both transmit and receive path.

This IP Core instantiates MPCS Module foundation IP configured as 1-Lane 64b/66b PCS, and supports APB and MDIO access to MPCS and MMD registers.

The top-level block diagram of the 10G Ethernet PCS IP Core is shown in Figure 2.1.

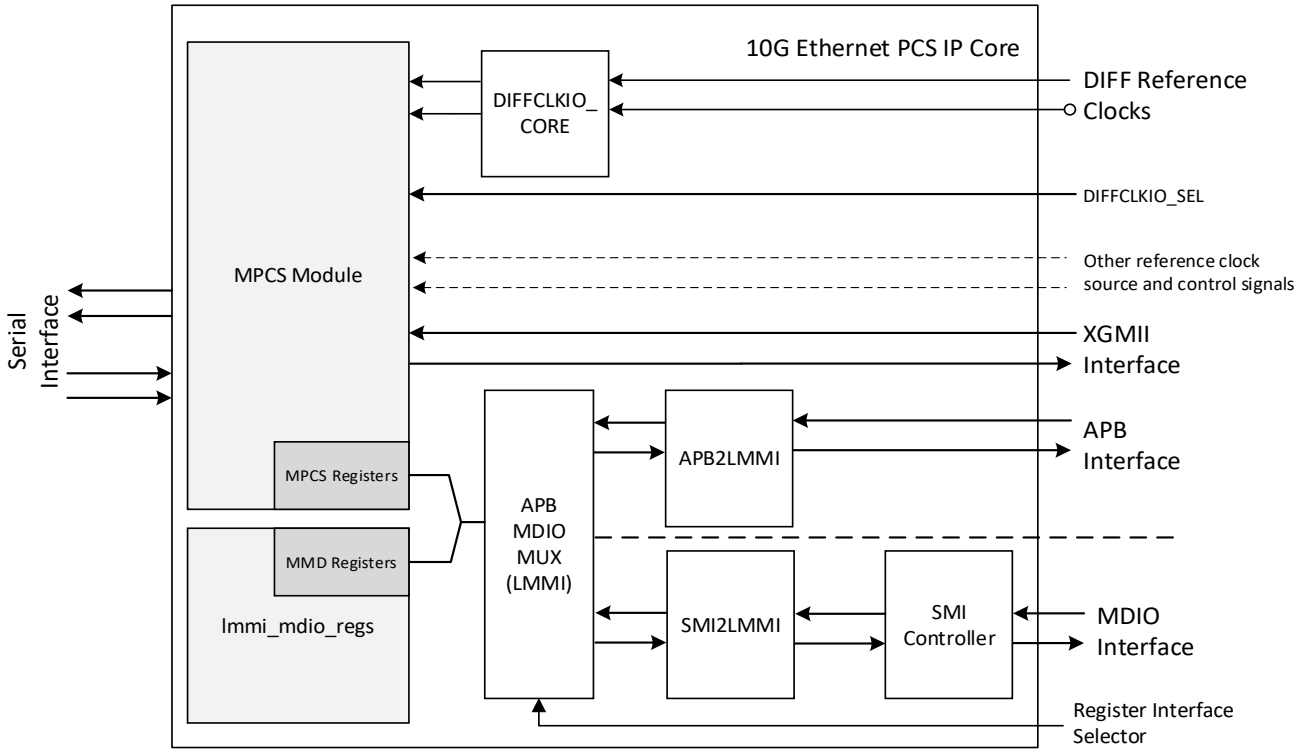

Figure 2.1. 10 Gb Ethernet PCS IP Top-Level Block Diagram

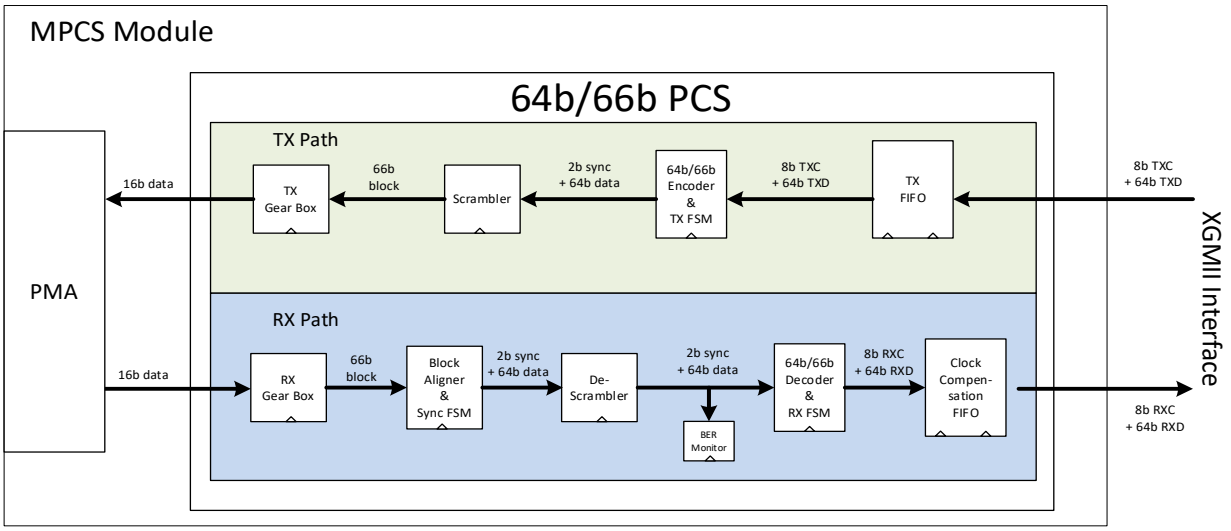

Figure 2.2. MPCS Module Configured as 64b/66b PCS Block Diagram

This MPCS Module instantiated in 10 Gb Ethernet IP Core uses 64b/66b PCS, which has the following sub-blocks:

- TX FIFO – This asynchronous FIFO is used to adapt TX path clock frequency and phase difference between 64b/66b PCS and user logic. The user logic can monitor the FIFO Almost Full and FIFO Almost Empty signals. Once FIFO almost full is detected high, to avoid FIFO overflow, user logic should pause FIFO by writing immediately, and resume writing until the status signal returns Low. The high level of FIFO almost empty indicates that user logic should write the FIFO immediately in case of FIFO underflow.
- 64b/66b Encoder – This submodule encodes 64-bit XGMII data and 8-bit XGMII control into 10GBASE-R 66-bit control or data blocks in accordance with Clause 49 of IEEE802.3-2008 specification.
- Scrambler – This submodule scrambles the 64-bit block payload data using x58 + x39 +1 polynomial specified by IEEE802.3-2008 specification.
- TX Gearbox – This submodule adapts between the 66-bit width of 64B/66B block and the 20-bit width of PMA data bus. It also generates bit sequence of square wave and PRBS pattern and sends them to PMA for transmitter or receiver tests.
- RX Gearbox – This submodule adapts between the 66-bit width of 64B/66B block and the 16-bit width of PMA. This submodule also performs PRBS32 pattern checking.
- Block Aligner – This submodule determines the block boundary of a 66-bit word received from Rx Gearbox. The incoming 66-bit data stream is slipped one bit at a time until the required number of valid synchronization header (bit 0 and 1) is detected in the received data stream.
- BER Monitor – The 10GBASE-R BER Monitor is implemented in accordance with the 10GBASE-R protocol. After block lock synchronization is achieved, the BER checker starts to count the number of invalid synchronization headers within a 125-µs period.
- 64b66b Decoder – This submodule reverses the 64B/66B encoding process. The decoder block also contains a state machine (RX SM) designed in accordance with the IEEE802.3-2008 specification.
- Clock Compensation FIFO – This submodule compensates clock frequency +/- 100 PPM difference (up to 1 clock edge difference every 5000 clock periods) in RX path by monitoring RX FIFO status and inserting or deleting characters specified by IEEE802.3-2008 if pre-defined criteria is met.

For more information regarding on how to enable or disable these submodules, refer to the Multi-Protocol PCS Module – Lattice Radiant Software (FPGA-IPUG-02118) user guide.

2.2. Signal Description

Table 2.1. 10 Gb Ethernet PCS IP Core Signal Description

Port Name	I/O	Width	Description
Serial I/O			
pad_refclkn_i	In	1	161.132812 MHz SERDES PLL Reference Clock signal (-).
pad_refclkp_i	In	1	161.132812 MHz SERDES PLL Reference Clock signal (+).
pad_rxn_i	In	1	RX- differential signal
pad_rxp_i	In	1	RX+ differential signal
pad_txn_o	Out	1	TX- differential signal
pad_txp_o	Out	1	TX+ differential signal
Other Reference Clock Source			
refclkn0_ext_i	In	1	161.132812 MHz Reference clock from external IO pad0 (-).
refclkp0_ext_i	In	1	161.132812 MHz Reference clock from external IO pad0 (+)
refclkn1_ext_i	In	1	161.132812 MHz Reference clock from external IO pad1 (-).
refclkp1_ext_i	In	1	161.132812 MHz Reference clock from external IO pad1 (+).
pll_0_refclk_i	In	1	161.132812 MHz Generated Reference clock from Left PLL.
pll_1_refclk_i	In	1	161.132812 MHz Generated Reference clock from Right PLL.
sd_pll_refclk_i	In	1	161.132812 MHz Reference Clock from fabric
Reference Clock MUX Tree Control Signals			
use_refmux_i	In	1	See Reference Clocks section.
diffioclksel_i	In	1	See Reference Clocks section.
clksel_i	In	2	See Reference Clocks section.
Clock and Reset			
xg_tx_clk_i	In	1	Tx Clock input – 156.25 MHz clock for transmit data path.
xg_tx_rst_n_i	In	1	Tx Active Low reset. Asynchronous assert, synchronous (xg_tx_clk_i) deassert.
xg_rx_clk_i	In	1	Rx Clock input – 156.25 MHz clock for receive data path.
xg_rx_rst_n_i	In	1	Rx Active Low reset. Asynchronous assert, synchronous (xg_rx_clk_i) deassert.
xg_pcs_clkin_i	In	1	Low speed clock input to PMA.
xg_tx_clk_o	Out	1	Tx Clock Output – 322.26 MHz
xg_rx_clk_o	Out	1	Rx Clock Output – 322.26 MHz
XGMII			
xg_txc_i [7:0]	In	8	8-bit Tx control signal. bit[0] is the control signal for xg_txd_i [7:0] bit[1] is the control signal for xg_txd_i [15:8] … bit[7] is the control signal for xg_txd_i [63:56] When control bit is high, indicates a control byte, otherwise it is a data byte.
xg_txd_i [63:0]	In	64	64-bit Tx data signal.
xg_rxc_o [7:0]	Out	8	8-bit Rx control signal. bit[0] is the control signal for xg_rxd_o [7:0] bit[1] is the control signal for xg_rxd_o [15:8] … bit[7] is the control signal for xg_rxd_o [63:56] When control bit is high, indicates a control byte, otherwise it is a data byte.
xg_rxd_o [63:0]	Out	64	64-bit Rx data signal.
Non-Standard Rx/Tx Signals			
xg_rxval_o	Out	1	Rx valid signal. When high, indicates that the corresponding values on signals xg_rxc_o and xg_rxd_o are valid.
xg_txval_i	In	1	Tx valid signal. When high, indicates that the corresponding values on signals xg_txc_i and xg_txd_i are valid.

Port Name	I/O	Width	Description
xg_txrdy_o	Out	1	Tx ready signal. When high, indicates that XGMII PCS is ready to accept the user data and control signal (xg_txc_i and xg_txd_i).
xg_rx_hi_ber_o	Out	1	The high level of this signal indicates high bit error rate (BER).
xg_rx_blk_lock_o	Out	1	The high level of this signal indicates the block lock is achieved.
APB Interface[1]			
apb_pclk_i	In	1	Clock.
apb_preset_n_i	In	1	Active low reset. Asynchronous assert, synchronous (apb_pclk_i) deassert.
apb_psel_i	In	1	Slave select.
apb_penable_i	In	1	Enable. This signal indicates the second and subsequent cycles of an APB transfer.
apb_paddr_i [15:0]	In	16	Address.
apb_pwdata_i [15:0]	In	16	Write Data.
apb_pwrite_i	In	1	Indicates write or read access. 0 – Read 1 – Write
apb_prdata_o [15:0]	Out	16	Read Data.
apb_pready_o	Out	1	Ready. The slave uses this signal to extend an APB transfer.
Management Data Input/Output[1]			
mdc_i	In	1	MDIO clock signal (2.5 MHz max frequency).
md_resetn_i	In	1	MDIO active low reset signal.
mdio_io	In/Out	1	MDIO bidirectional data signal.

Note:

1. Only one of the two interfaces is available as selected by *Register Interface*.

2.3. Attribute Summary

The configurable attributes of the 10G Ethernet PCS IP Core are shown in Table 2.2 and are described in Table 2.3. The attributes can be configured through the IP Catalog's Module/IP wizard of the Lattice Radiant software.

Table 2.2. Attributes Table

Attribute	Selectable Values	Default	Dependency on Other Attributes
General			
Register Interface	"APB", "MDIO"	"APB"	—
PCS Lane ID	"AUTO", "2" , "3" , "6" , "7"	"AUTO"	—
RX Adaptive Equalization			
Setting1: Enable	"Checked", "Unchecked"	"Checked"	—
Setting1: Adaptive Algorithm	"SS_LMS" , "RL2plus"	"RL2plus"	Editable if *Setting1: Enable* == "Checked"
Setting2: Enable	"Checked", "Unchecked"	"Unchecked"	—
Setting2: Adaptive Algorithm	"SS_LMS", "RL2plus"	"RL2plus"	Editable if *Setting2: Enable* == "Checked"
Setting3: Enable	"Checked", "Unchecked"	"Unchecked"	—
Setting3: Adaptive Algorithm	"SS_LMS", "RL2plus"	"RL2plus"	Editable if *Setting3: Enable* == "Checked"
Setting1/2: Preliminary Adaptive EQ	"ENABLED", "DISABLED"	"ENABLED"	Editable if *Setting1/2: Enable* == "Checked"

Attribute	Selectable Values	Default	Dependency on Other Attributes
Setting1/2: Training Phase Adaptive EQ	“ENABLED”, “DISABLED”	“ENABLED”	Editable if *Setting1/2: Enable* == "Checked"
Setting1/2: Post-Phase Adaptive EQ	“ENABLED”, “DISABLED”	“ENABLED”	Editable if *Setting1/2: Enable* == "Checked"
Setting3: Preliminary Adaptive EQ	“ENABLED”, “DISABLED”	“DISABLED”	Editable if *Setting3: Enable* == "Checked"
Setting3: Training Phase Adaptive EQ	“ENABLED”, “DISABLED”	“DISABLED”	Editable if *Setting3: Enable* == "Checked"
Setting3: Post-Phase Adaptive EQ	“ENABLED”, “DISABLED”	“DISABLED”	Editable if *Setting3: Enable* == "Checked"
Identifier			
Port Address	0–31	0	Available if *Register Interface* == “MDIO”
Device Address	—	3	Available if *Register Interface* == “MDIO”
Test Feature			
Loopback Mode	“Disabled”, “Near PMA Loopback”, “Fabric Loopback”	“Disabled”	—

Table 2.3. Attributes Descriptions

Attribute	Description
General	
Register Interface	Specifies the preferred interface for register access.
PCS Lane ID	Specifies the location of the first lane of the PCS instance.
Identifier	
Port Address	Specifies the Port Address of the IP Core.
Device Address	Specifies the Device Address of the IP Core; fixed to 3. For more details, see IEEE802.3 Clause 45.2 Table45-1.
Test Feature	
Loopback Mode	PCS loopback, refer to PCS Loopback section.

2.4. Register Description

This section provides detailed descriptions of 10G Ethernet PCS data registers.

The register address map, shown in Table 2.4, specifies the available IP Core registers.

Table 2.4. Register Address Map

APB Offset	MDIO Register Address	Register Name	Bit Width	Description
Vendor Specific MMD 1 Registers				
0x7804	0x0002	MMD1 Device Identifier 0	16	Refer to IEEE 802.3 Clause 45.2
0x7805	0x0003	MMD1 Device Identifier 1	16	Refer to IEEE 802.3 Clause 45.2
0x780A	0x0005	MMD1 Devices in Package 0	16	Refer to IEEE 802.3 Clause 45.2
0x780B	0x0006	MMD1 Devices in Package 1	16	Refer to IEEE 802.3 Clause 45.2
0x7810	0x0008	MMD1 Status Register	16	Refer to IEEE 802.3 Clause 45.2
0x781C	0x000E	MMD1 Package Identifier 0	16	Refer to IEEE 802.3 Clause 45.2
0x781D	0x000F	MMD1 Package Identifier 1	16	Refer to IEEE 802.3 Clause 45.2

APB Offset	MDIO Register Address	Register Name	Bit Width	Description
0x7A00 – 0x7AFF	0x0000 – 0x00FF	PMA Registers	16	Refer to Appendix A of the CertusPro-NX SerDes/PCS User Guide (FPGA-TN-02245).
0x7B00 – 0x7BEA	0x0100 – 0x01EA	MPCS Module Registers	16	Refer to Multi-Protocol PCS Module – Lattice Radiant Software (FPGA-IPUG-02118) user guide.

The behavior of registers to write and read access is defined by its access type, which is defined in Table 2.5.

Table 2.5. Access Type Definition

Access Type	Behavior on Read Access	Behavior on Write Access
RO	Returns register value	Ignores write access
RW	Returns register value	Updates register value
RSVD (Applicable to MMD registers only)	Ignore when read	Ignores write access

2.4.1. MMD1 Device Identifier 0

Table 2.6. MMD1 Device Identifier 0

Field	Name	Access	Width	Reset
[15:0]	mmd1_dv_id_0	RO	16	16'h0

- mmd1_dv_id_0

  MMD1 Device Identifier 0. Provides the upper 16-bit value, which constitutes to a unique identifier for a particular type of vendor-specific device. For more information regarding this register, see IEEE802.3 Clause 45.2 Table45-1.

2.4.2. MMD1 Device Identifier 1

Table 2.7. MMD1 Device Identifier 1

Field	Name	Access	Width	Reset
[15:0]	mmd1_dv_id_1	RO	16	16'h3

- mmd1_dv_id_1

  MMD1 Device Identifier 1. Provides the lower 16-bit value, which constitutes to a unique identifier for a particular type of vendor-specific device. For more information regarding this register, see IEEE802.3 Clause 45.2 Table45-1.

2.4.3. MMD1 Devices in Package 0

Table 2.8. MMD1 Devices in Package 0

Field	Name	Access	Width	Reset
[15:0]	mmd1_dv_pkg_0	RO	16	16'hA

- mmd1_dv_pkg_0

  MMD1 Devices in Package Register 0. Provides the lower 16-bit value, each bit read as one indicates which MMDs are instantiated within the same package as the MMD being accessed. PMA and PCS are bit 1 and bit 3 of this register, respectively; hence, the reset value is 16'h000A. For more details regarding this register, see IEEE 802.3 Clause 45.2 Table45-2.

2.4.4. MMD1 Devices in Package 1

Table 2.9. MMD1 Devices in Package 1

Field	Name	Access	Width	Reset
[15:0]	mmd1_dv_pkg_1	RO	16	16'h0

- mmd1_dv_pkg_1

  MMD1 Devices in Package Register 1. Provides the upper 16-bit value, each bit read as one indicates which MMDs are instantiated within the same package as the MMD being accessed. For more details regarding this register, see IEEE 802.3 Clause 45.2 Table45-2.

2.4.5. MMD1 Status Register

Table 2.10. MMD1 Status Register

Field	Name	Access	Width	Reset
[15:14]	mmd1_stat_reg	RO	2	2'h2
[13:0]	reserved	RSVD	14	14'h0

- mmd1_stat_reg

  MMD1 Status Register. Specifies if the device is present and responding at this register address or not.

  2'b10 – Device responding at this address.

  2'b11 – No device responding at this address.

  2'b01 – No device responding at this address.

  2'b00 – No device responding at this address.

2.4.6. MMD1 Package Identifier 0

Table 2.11. MMD1 Package Identifier 0

Field	Name	Access	Width	Reset
[15:0]	mmd1_pkg_id_0	RO	16	16'h0

- mmd1_pkg_id_0

  MMD1 Package Identifier 0. Provides the upper 16-bit value, which constitutes a unique identifier for a particular type of package instantiated within. The package identifier may be the same as the device identifier. For more information regarding this register, see IEEE802.3 Clause 45.2 Table45-1.

2.4.7. MMD1 Package Identifier 1

Table 2.12. MMD1 Package Identifier 1

Field	Name	Access	Width	Reset
[15:0]	mmd1_pkg_id_1	RO	16	16'h3

- mmd1_pkg_id_1

  MMD1 Package Identifier 1. Provides the lower 16-bit value, which constitutes a unique identifier for a particular type of package instantiated within. The package identifier may be the same as the device identifier. For more information regarding this register, see IEEE802.3 Clause 45.2 Table45-1.

2.5. Register Access

2.5.1. MDIO Transaction

The MDIO Interface should be driven from a STA Master according to the protocol defined in IEEE 802.3. Each transaction type is described in this section. The following abbreviations are used:

- PRE – Preamble
- ST – Start
- OP – Operation Code
- PRTAD – Port Address
- DEVAD – Device Address
- TA – Turnaround

Note: The TA field is a 2-bit turnaround time spacing between the device address field and the data field to avoid contention during a read transaction. The TA bits are treated as *don't cares* by the 10G Ethernet PCS IP Core.

Set Address Transaction

This transaction is defined by OP = 00, it is used to set the internal 16-bit address register of 10G Ethernet PCS IP Core for the data transactions.

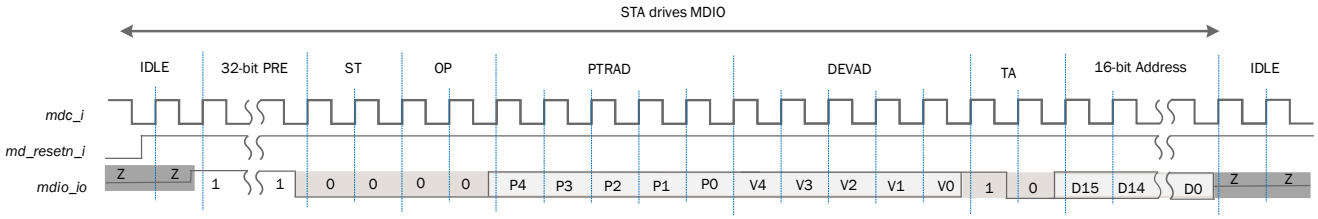

Figure 2.3. MDIO Set Address Transaction

Write Transaction

This transaction is defined by OP = 01. The 10G Ethernet PCS IP Core takes the 16-bit word in the data field and writes it to the register of the current address.

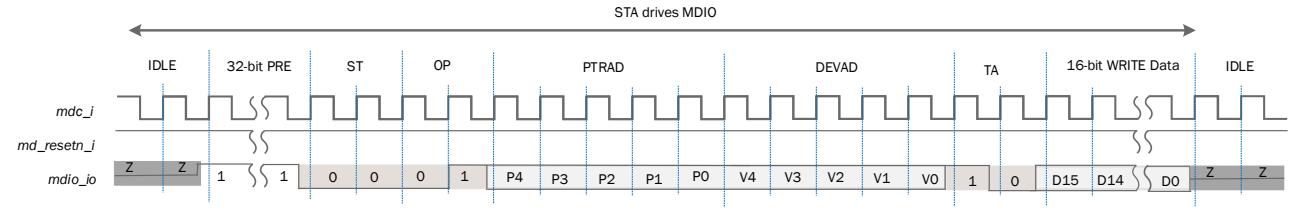

Figure 2.4. MDIO Write Transaction

Read Transaction

This transaction is defined by OP = 11. The 10G Ethernet PCS IP Core returns the 16-bit word from the register of the current address.

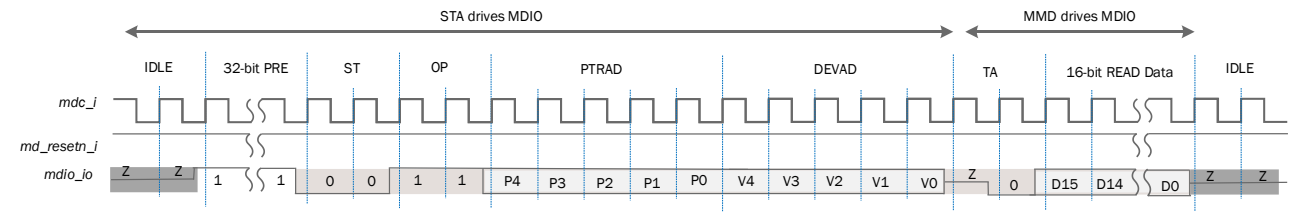

Figure 2.5. MDIO Read Transaction

2.6. Reference Clocks

The 10 Gb Ethernet PCS IP Core provides other sources of reference clocks and can be used for dynamic switching as shown in Figure 2.6. The pll_0/1_refclk_i should only be connected to PLL and should not be directly connected to fabric. To use this feature, user must set the reference clock source control signals accordingly, refer to Table 2.13.

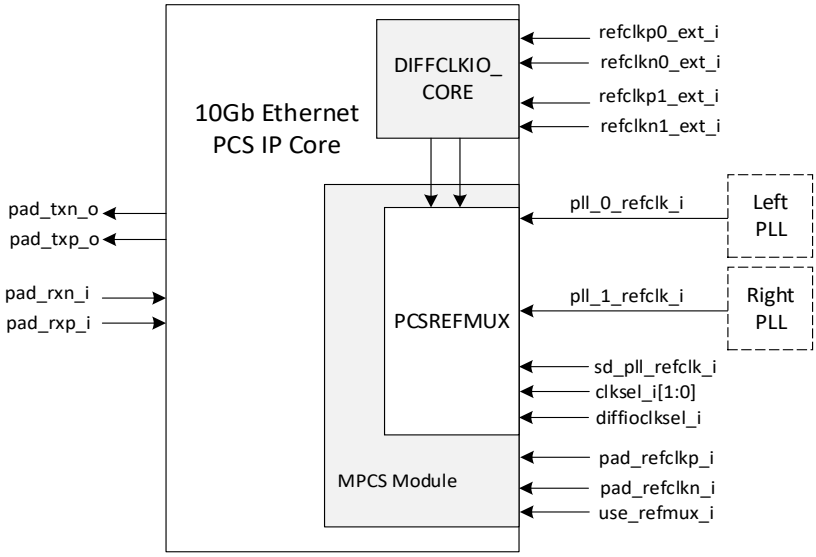

Figure 2.6. Reference Clock Block Diagram

Table 2.13. Reference Clock MUX Tree Control Signals

Reference Clock Control Signal	Usage
use_refmux_i	1'b1 – Use reference clock output from Clock MUX Tree (PCSREFMUX). 1'b0 – Use dedicated reference clocks (pad_refclkp/n_i).
diffioclksel_i	1'b1 – Use refclkp/n1_ext_i as reference clocks. 1'b0 – Use refclkp/n0_ext_i as reference clocks.
clksel_i	2'b00 – Use pll_0_refclk_i as reference clocks. 2'b01 – Use pll_1_refclk_i as reference clocks. 2'b10 – Use reference clock based on diffioclksel_i. 2'b11 – Use sd_pll_refclk_i as reference clock.

2.7. PCS Loopback

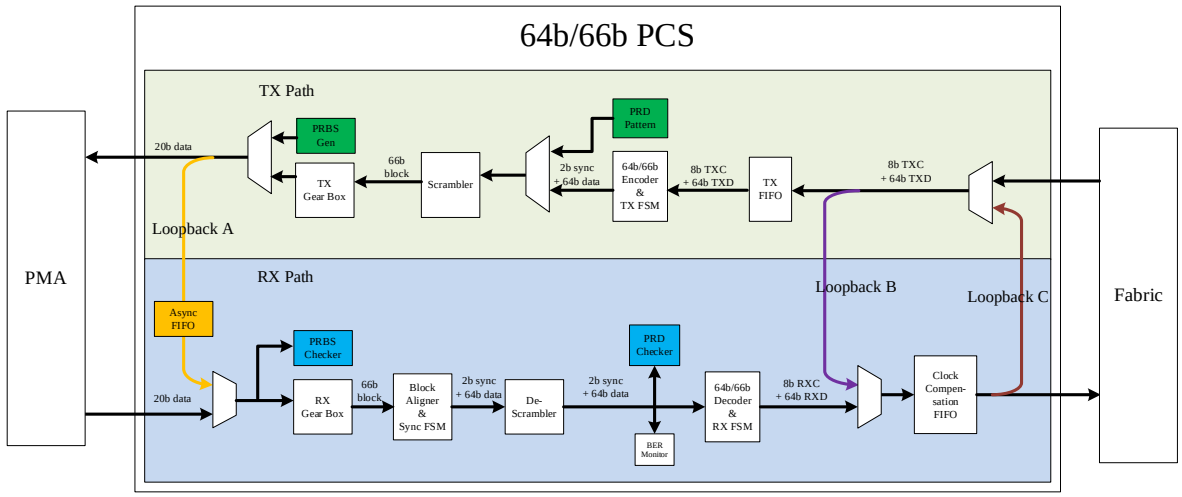

Figure 2.7. 64b66b PCS Loopback Diagram

The following are the different PCS Loopback:

- Loopback A
  This loopback can be enabled when *Loopback* = “Near PMA Loopback” or by using bit 0 of Loopback Mode Control (MPCS register).
  In this mode, the 20-bit input data of RX path comes from TX path. The TX path clock will drive both TX and RX path. The asynchronous FIFO in between TX path and RX path is for clock phase compensation.
- Loopback B
  This loopback can be enabled using bit 2 of Loopback Mode Control (MPCS register).
  In this mode, the PCS accepts data on the transmit path from the XGMII and return it on the receive path to the XGMII through RX FIFO.
- Loopback C
  This loopback can be enabled when *Loopback* = “Fabric Loopback” or by using bit 1 of Loopback Mode Control (MPCS register).
  In this mode, the received data by RX PCS is returned to TX PCS.

3. IP Generation and Evaluation

This section provides information on how to generate the 10 Gb Ethernet PCS IP Core using the Lattice Radiant software and how to run synthesis and simulation. For more details on the Lattice Radiant software, refer to the Lattice Radiant software user guide.

3.1. Licensing the IP

An IP core-specific license string is required to enable full use of the 10 Gb Ethernet PCS IP Core in a complete, top-level design.

The IP Core can be fully evaluated through functional simulation and implementation (synthesis, map, place and route) without an IP license string. This IP core supports Lattice's IP hardware evaluation capability, which makes it possible to create versions of the IP core, which operate in hardware for a limited time (approximately four hours) without requiring an IP license string. See Hardware Evaluation section for further details. However, a license string is required to enable timing simulation and to generate bitstream file that does not include the hardware evaluation timeout limitation.

3.2. Generation and Synthesis

The Lattice Radiant software allows user to customize and generate modules and IPs and integrate them into the device's architecture. The procedure for generating the 10 Gb Ethernet IP PCS Core in Lattice Radiant software is described below.

To generate the 10 Gb Ethernet PCS IP Core:

1. Create a new Lattice Radiant software project or open an existing project.
2. In the **IP Catalog** tab, double-click on **10 Gb Ethernet PCS** under **IP, Connectivity** category. The **Module/IP Block Wizard** opens as shown in Figure 3.1. Enter values in the **Instance name** and the **Create in** fields and click **Next**.

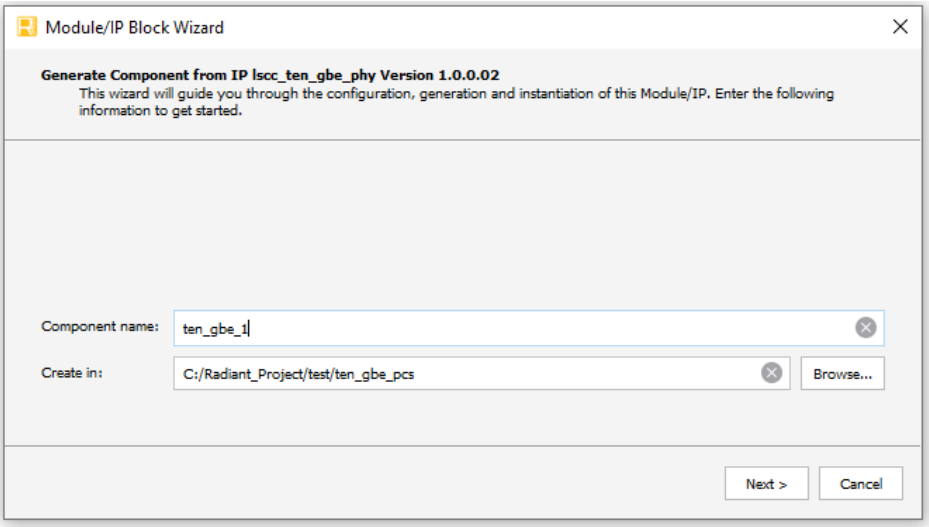

Figure 3.1. Module/IP Block Wizard

3. In the module's dialog box of the **Module/IP Block Wizard** window, customize the selected 10 Gb Ethernet PCS IP Core. As a sample configuration, see Figure 3.2. For configuration options, see the Attribute Summary section.

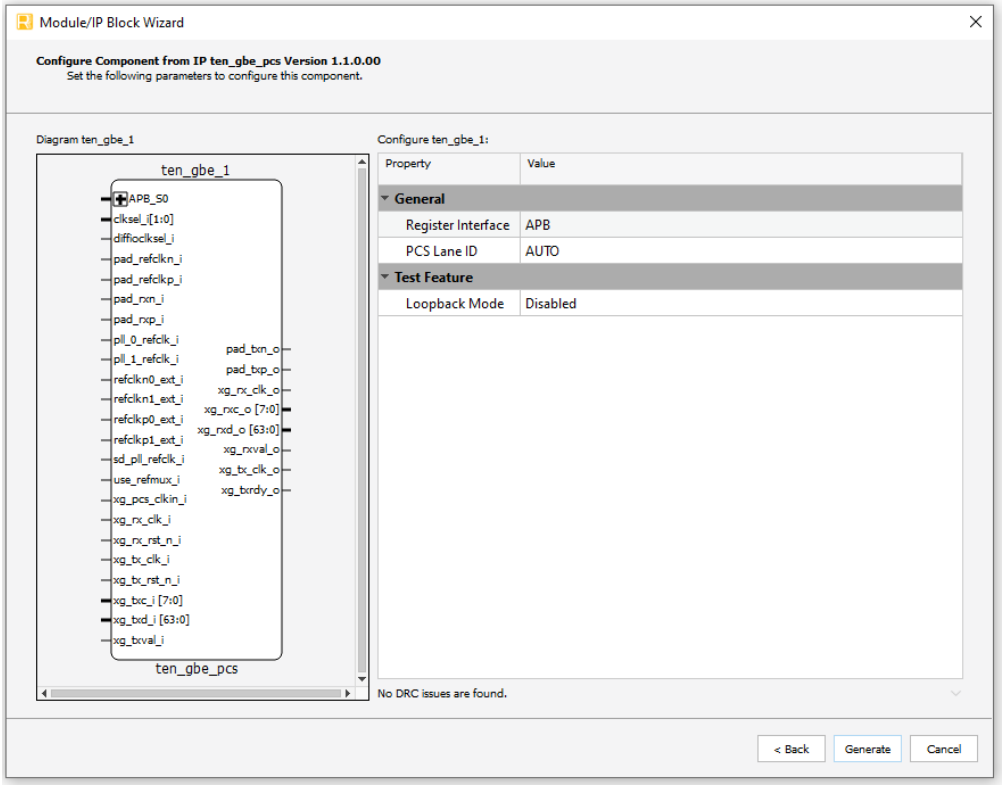

Figure 3.2. Configure User Interface of 10 Gb Ethernet PCS IP Core

4. Click **Generate**. The **Check Generating Result** dialog box opens, showing design block messages and results as shown in Figure 3.3.

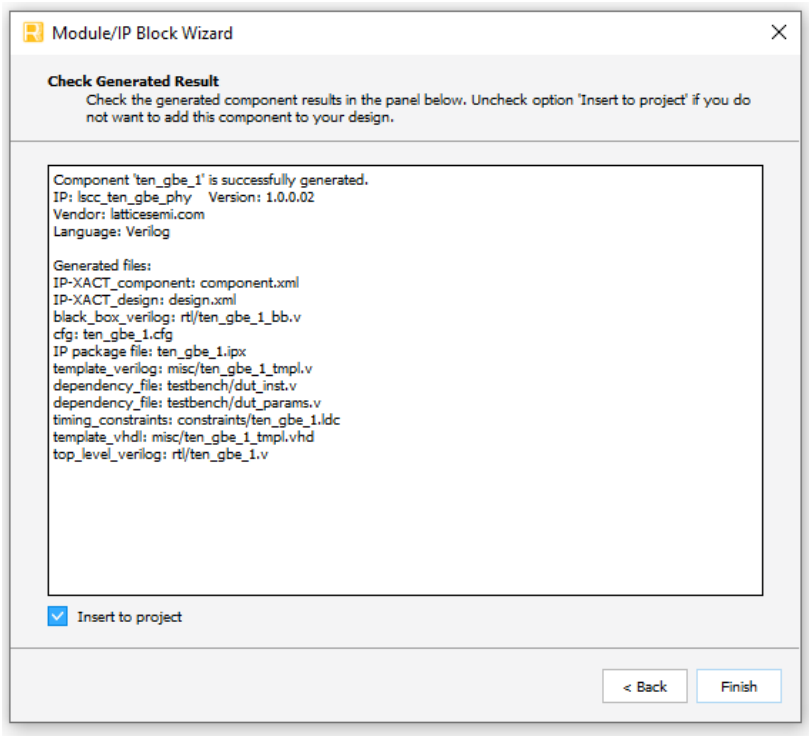

Figure 3.3. Check Generating Result

5. Click the **Finish** button. All the generated files are placed under the directory paths in the **Create in** and the **Instance name** fields shown in Figure 3.1.

The generated 10 Gb Ethernet PCS IP Core package includes the black box (<Instance Name>_bb.v) and instance templates (<Instance Name>_tmpl.v/vhd) that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file (<Instance Name>.v) that can be used as an instantiation template for the IP core is also provided. User may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 3.1.

Table 3.1. Generated File List

Attribute	Description
<Instance Name>.ipx	This file contains the information on the files associated to the generated IP.
<Instance Name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Instance Name>.v	This file provides an example RTL top file that instantiates the IP core.
rtl/<Instance Name>_bb.v	This file provides the synthesis black box.
misc/<Instance Name>_tmpl.v misc /<Instance Name>_tmpl.vhd	These files provide instance templates for the IP core.

3.3. Running Functional Simulation

Running functional simulation can be performed after the IP is generated.

To run Verilog simulation:

1. Click the  button located on the **Toolbar** to initiate the **Simulation Wizard** shown in Figure 3.4.

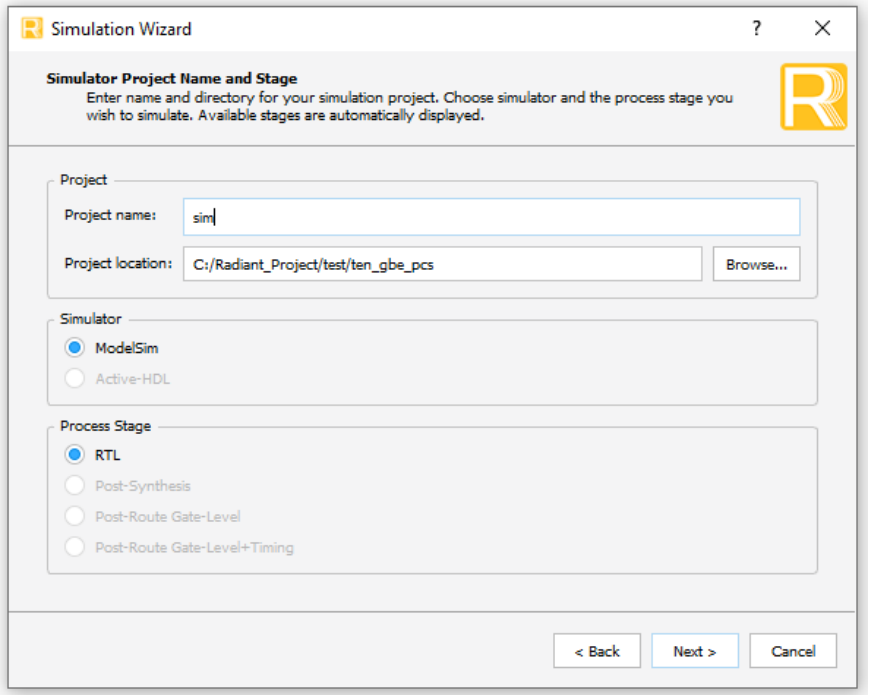

Figure 3.4. Simulation Wizard

2. Click **Next** to open the **Add and Reorder Source** window as shown in Figure 3.5.

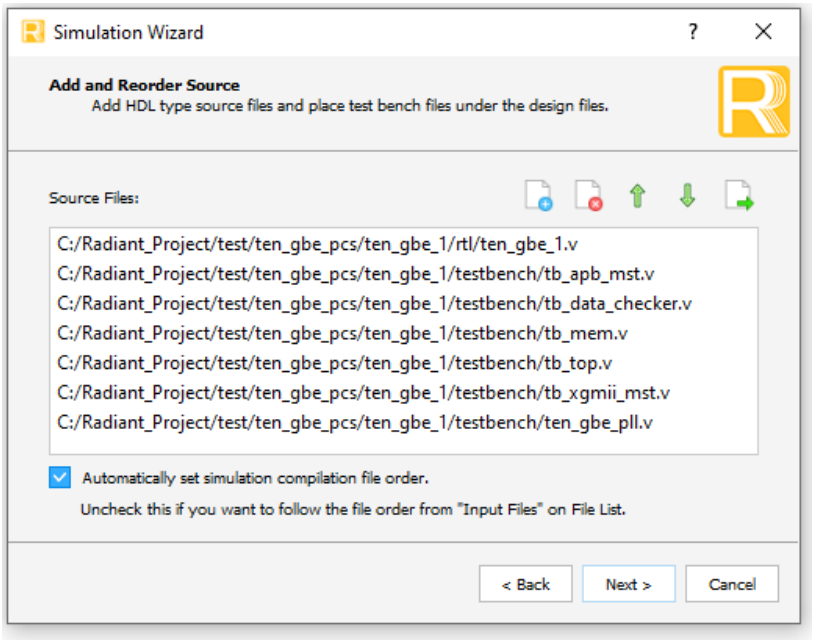

Figure 3.5. Adding and Reordering Source

3. Click **Next**. The **Summary** window is shown.
4. Click **Finish** to run the simulation.

   Note: It is necessary to follow the procedure above until it is fully automated in the Lattice Radiant Software Suite. The results of the simulation in our example are provided in Figure 3.6.

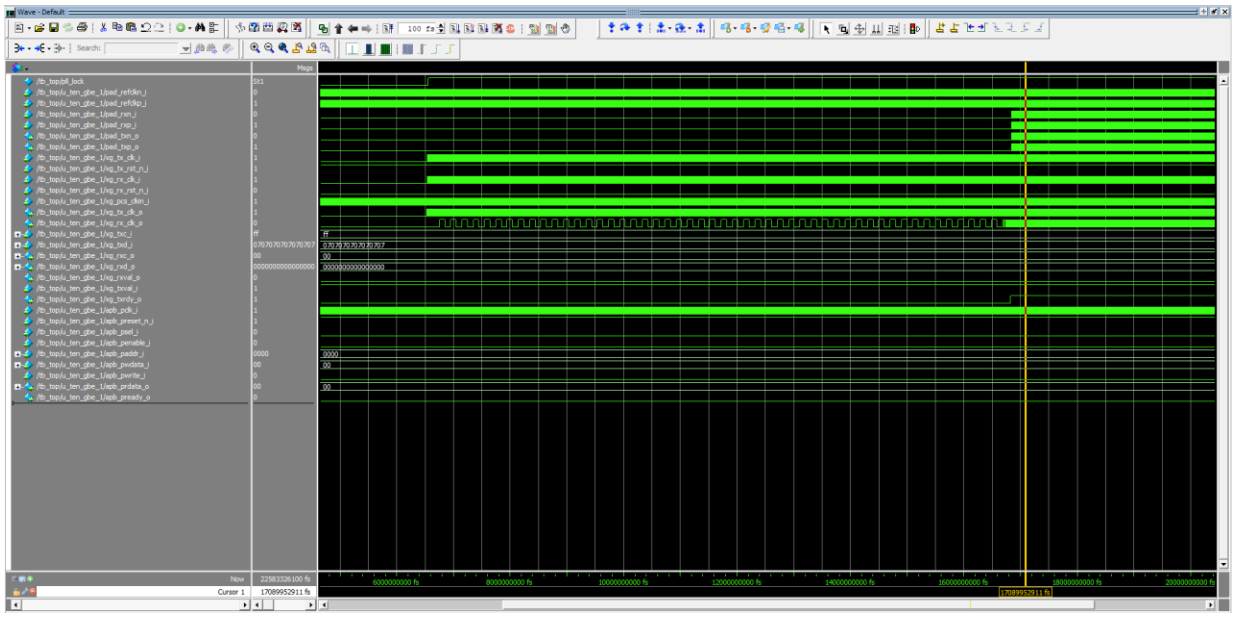

Figure 3.6. Simulation Waveform

3.4. Hardware Evaluation

The 10 Gb Ethernet PCS IP Core supports Lattice's IP hardware evaluation capability when used with LFCPNX devices. This makes it possible to create versions of the IP core that operate in hardware for a limited period of time (approximately four hours) without requiring the purchase of an IP license. It may also be used to evaluate the core in hardware in user-defined designs. The hardware evaluation capability may be enabled/disabled in the Strategy dialog box. It is enabled by default. To change this setting, go to Project > Active Strategy > LSE/Synplify Pro Settings.

4. Ordering Part Number

Table 4.1 Ordering Part Number

Device Family	Part Number	
	Single Machine Annual	Multi-Site Perpetual
CertusPro-NX	ETHER-10GEBASER-CPNX-US	ETHER-10GEBASER-CPNX-UT

Appendix A. Resource Utilization

Table A.1 shows the resource utilization for the LFCPNX-100 using the Lattice Radiant software.

For more information on Lattice Radiant software, visit the Lattice web site at www.latticesemi.com/Products/DesignSoftwareAndIP.

Table A.1. Resource Utilization

Device	Slice Registers	LUTs	EBRs
LFCPNX-100	36	52	0

Appendix B. Clock Requirement

Figure B.1 shows the suggested connection of xg_tx/rx_clk_i and xg_tx_clk_o. GPLL Module with 64/66 clock ratio is used to generate the 156.25MHz clock input to xg_tx/rx_clk_i.

GPLL Module output lock signal is also recommended to use as one of the PHY ready indicators before sending valid signals to PHY. Refer the sample code below:

```
assign sys_ready_o  = pll_lock_w & xg_rxval_o & xg_txrdy_o & xg_rx_blk_lock_o;
```

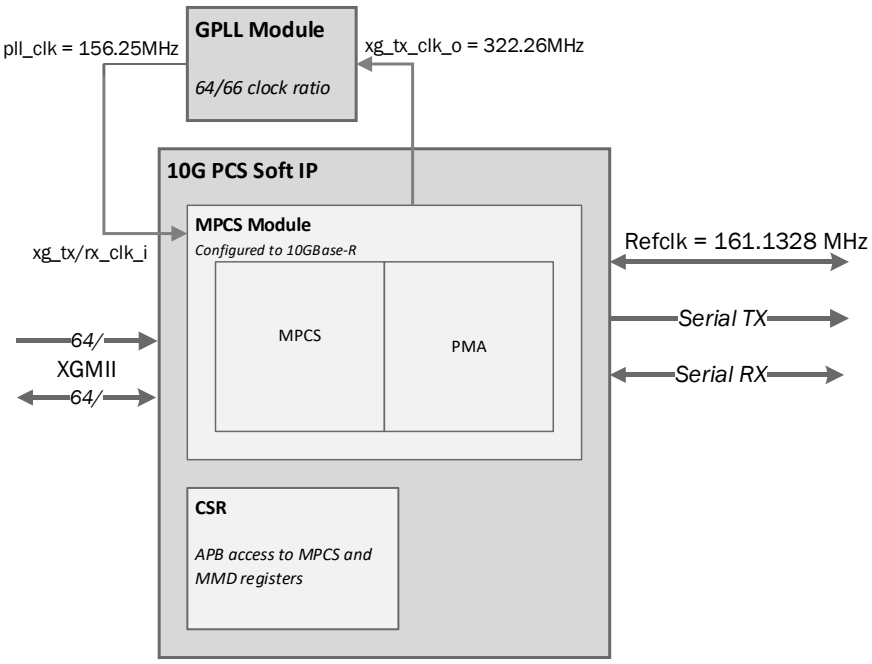

Figure B.1. 10G PCS IP Core Clock Setup

This setup is also available in the eval_top.v file under eval folder of the 10Gb Ethernet PCS IP Core Package.

References

For more information refer to:

- Lattice Sales Office
- Lattice Insights for Lattice Semiconductor training courses and learning plans
- Lattice Radiant software user guide
- Lattice Radiant FPGA design software
- Certus-NX FPGA web page
- Development Kits & Boards for Certus-NX
- IP and Reference Designs for Certus-NX
- 10Gb Ethernet PCS IP Core
- 10Gb Ethernet MAC & PCS Reference Design
- Multi-Protocol PCS Module – Lattice Radiant Software (FPGA-IPUG-02118)

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.5, October 2023

Section	Change Summary
Functional Description	Added RX Adaptive Equalization Attribute header in Table 2.2.

Revision 1.4, June 2023

Section	Change Summary
Appendix B. Clock Requirement	Newly added section.
References	Added links to the following: • Certus-NX FPGA web page • Lattice Radiant Software web page • 10Gb Ethernet PCS IP Core • 10Gb Ethernet MAC & PCS Reference Design

Revision 1.3, March 2023

Section	Change Summary
All	Minor adjustments in formatting across the document.
Functional Description	Added row for 0x7A00 – 0x7AFF in Table 2.4. Register Address Map.
Technical Support Assistance	Added reference link to Lattice Answer Database.

Revision 1.2, November 2022

Section	Change Summary
Functional Descriptions	Revised the Clock Output values for xg_tx_clk_o and xg_rx_clk_o from 161.13 MHz to 322.26 MHz in Table 2.1.

Revision 1.1, August 2021

Section	Change Summary
Introduction	Added MDIO support in Table 1.1.
Functional Descriptions	• Updated Figure 2.1 to include MDIO support. • Updated Table 2.1 to add MDIO interface. • Updated Table 2.2 to add Register interface in General group and add Identifier group. • Updated Table 2.3 to add Identifier group. • Updated Register Description section to add MMD register. • Added Register Access section.
Ordering Part Number	Added 'OPN ETHER-10GEBASER-CPNX-US - Ethernet 10GE/10G-Base R for CertusPro-NX - 1 Year Subscription License'.
Appendix A. Resource Utilization	Updated allocation to include MDIO/MMD usage.

Revision 1.0, June 2021

Section	Change Summary
All	Initial release.

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