Divider IP

IP Version: v1.6.1

User Guide

FPGA-IPUG-02130-1.7

December 2025

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Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

Figures

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
FPGA	Field Programmable Gate Array
RTL	Register Transfer Level
DSP	Digital Signal Processing
LUT	Look Up Table

1. Introduction

The Divider IP core is a one-clock divider which completes one integer division every clock. It supports signed or unsigned inputs and provides configurable output latency.

1.1. Quick Facts

Table 1.1 presents a summary of the Divider IP Core.

Table 1.1. Divider Quick Facts

IP Requirements	Supported Devices	CrossLink™-NX, Certus™-NX, Certus-NX-RT, CertusPro™-NX, CertusPro-NX-RT, MachXO5™-NX, Lattice Avant™, and Certus-N2
	IP Changes[1]	For a list of changes to the IP, refer to the Divider IP Release Notes (FPGA-RN-02090).
Resource Utilization	Resources	See Appendix A. Resource Utilization.
Design Tool Support	Lattice Implementation	IP Core v1.6.1 – Lattice Radiant™ Software 2025.2
	Synthesis	Lattice Synthesis Engine
		Synopsys® Synplify Pro® for Lattice
	Simulation	For a list of supported simulators, see the Lattice Radiant Software User Guide.

Notes:

1. In some instances, the IP may be updated without changes to the user guide. This user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

1.2. Features

The key features of Divider IP Core include:

- Supports signed or unsigned numerator and denominator
- Supports numerator and denominator data width 4-64
- Supports forced positive remainder
- Supports configurable output latency
- Optional clock enable and data valid ports

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal Names that end with:

- _*i* are input signals
- _*o* are output signals

1.3.3. Host

The logic unit inside the FPGA interacts with the Divider IP Core.

1.3.4. Attribute

The names of attributes in this document are formatted in title case and italicized (*Attribute Name*).

2. Functional Description

2.1. Overview

The Divider IP core implements integer division with the formula:

*Numerator = Denominator * Quotient + Remainder*

The Numerator and the Denominator can be signed or unsigned integers. When either the Numerator or the Denominator is a signed integer, the Quotient and the Remainder are also in signed integer format. When the Remainder is configured as *Always positive remainder*, it becomes a positive signed integer value.

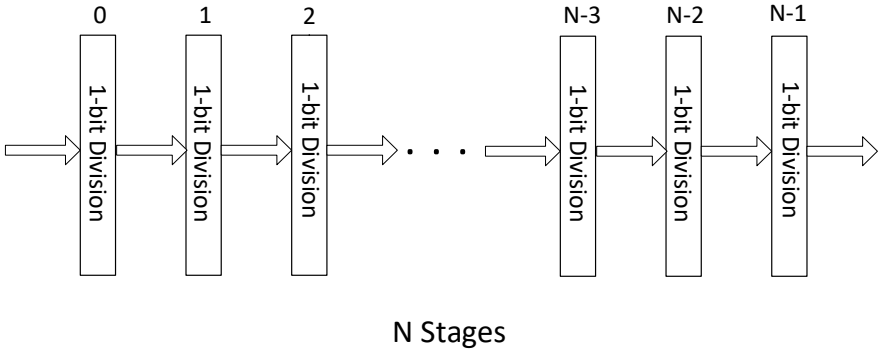

Figure 2.1. Divider IP Core Functional Diagram

2.2. Primary I/O

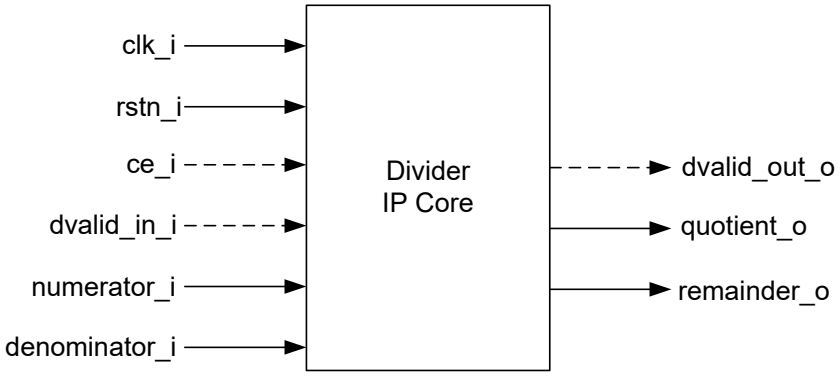

Figure 2.2. Divider IP core I/O Diagram

2.3. Signal Description

Table 2.1 lists the input and output signals for Divider IP Core.

Table 2.1. Divider IP Core Signal Description

Ports Name	Size	Direction	Description
clk_i	1	I	Input clock
rstn_i	1	I	Asynchronous active-low reset signal
numerator_i	4-64	I	Input numerator value
denominator_i	4-64	I	Input denominator value
dvalid_in_i	1	I	Optional input data valid signal, active-high
ce_i	1	I	Clock enable, active high
dvalid_out_o	1	O	Optional output data valid signal, active high
quotient_o	4-64	O	Output quotient
remainder_o	4-64	O	Output remainder

2.4. Attributes Summary

The configurable attributes of the Divider IP Core are shown in Table 2.2 and are described in Table 2.3. The attributes can be configured through the IP Catalog's Module/IP Wizard of the Lattice Radiant software.

Table 2.2. Attributes Table

Attribute	Selectable Values	Default	Dependency on Other Attributes
Structure			
Numerator data type	Unsigned, Signed	Unsigned	—
Denominator data type	Unsigned, Signed	Unsigned	—
Numerator data width	4-64	20	—
Denominator data width	4-64	10	—
Output Latency	1-64	20	Depends on Quotient width
Always positive remainder	Checked, Unchecked	Unchecked	Depends on Numerator data type
Clock enable port	Checked, Unchecked	Checked	—
Data valid ports	Checked, Unchecked	Checked	—

Table 2.3. Attributes Descriptions

Attribute	Description
Structure	
Numerator data type	Numerator data type specifies the data type of input Numerator.
Denominator data type	Denominator data type specifies the data type of input Denominator.
Numerator data width	Numerator data width specifies the data width of input Numerator.
Denominator data width	Numerator data width specifies the data width of input Denominator.
Output Latency	Output latency specifies the output latency of the Divider core. Its value can be between 1 and Numerator data width.
Always positive remainder	The Remainder is a positive signed integer value.
Clock enable port	The Clock enable port check box specifies whether the core has a clock enable port.
Data valid ports	The Data valid ports check box specifies whether the core has an input data valid and output data valid ports.

2.5. Operations Details

2.5.1. General Divider Operation

The Divider IP core uses a non-restoring division algorithm to implement the integer division operation. There are N stages of 1-bit division in an integer division operation, where N is the width of the quotient. Each stage generates a 1-bit quotient and partial-remainder. In the last stage, the final quotient and remainder are generated. 1-bit division uses an adder-subtractor to compare the partial remainder and denominator to get a new partial remainder. Quotient-digit selection is based on the sign of the partial remainder. In the last stage, the partial remainder is corrected to get the final remainder.

The Divider IP core supports configurable output latency. The latency can be any number of clock cycles from 1 to N. When latency is set to the value M, M stages of output registers are uniformly distributed into the N stages of 1-bit division operation. The final division stage always has output registers.

2.6. Timing Specifications

The Divider IP core is a one-clock divider. It can accept a numerator and denominator every clock cycle and generate a quotient and remainder every clock cycle.

When the input numerator and denominator are in an unsigned format, the output quotient and remainder are in an unsigned format. When either the numerator or denominator is in a signed format, the output quotient and remainder are always in a signed format.

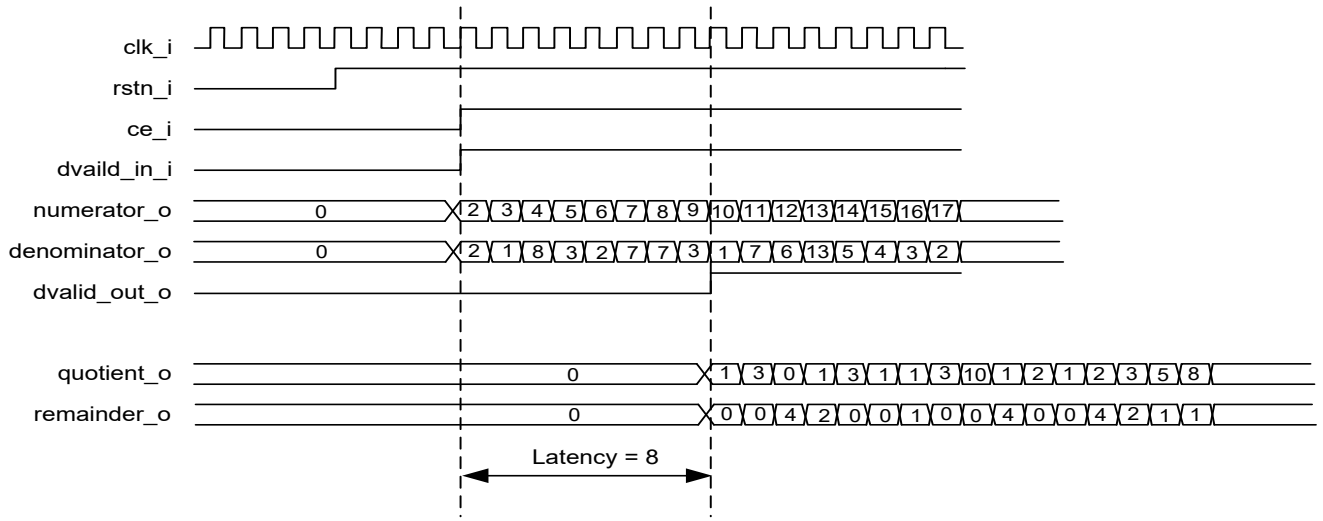

Figure 2.3. Unsigned Division for Latency 8 Diagram

3. Core Generation, Simulation, and Validation

This section provides information on how to generate the Divider IP Core using the Lattice Radiant software and how to run simulation and synthesis. For more details on the Lattice Radiant software, refer to the Lattice Radiant Software User Guide.

Note: The screenshots provided are for reference only. Details may vary depending on the version of the IP or software being used. If there have been no significant changes to the GUI, a screenshot may reflect an earlier version of the IP.

3.1. Licensing the IP

The Divider IP is provided at no additional cost with the Lattice Radiant software.

3.2. Generating and Synthesizing the IP

The Lattice Radiant software allows you to customize and generate modules and IPs and integrate them into the device's architecture. The procedure for generating the Divider IP Core in Lattice Radiant software is described below.

To generate the Divider IP Core:

1. Create a new Lattice Radiant software project or open an existing project.
2. In the **IP Catalog** tab, double-click **Divider** under **DSP** category. The **Module/IP Block Wizard** opens as shown in Figure 3.1. Enter values in the **Component name** and the **Create in** fields and click **Next**.

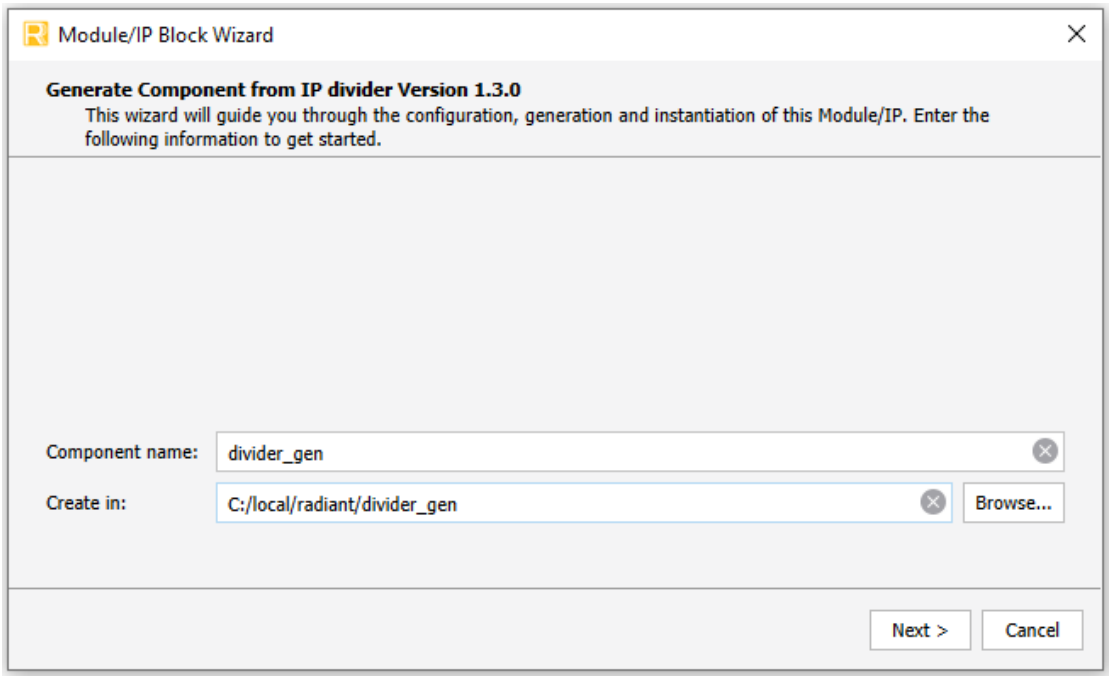

Figure 3.1. Module/IP Block Wizard

3. In the module's dialog box of the **Module/IP Block Wizard** window, customize the selected Divider IP Core using drop-down menus and check boxes. As a sample configuration, see Figure 3.2. For configuration options, see the Attributes Summary section.

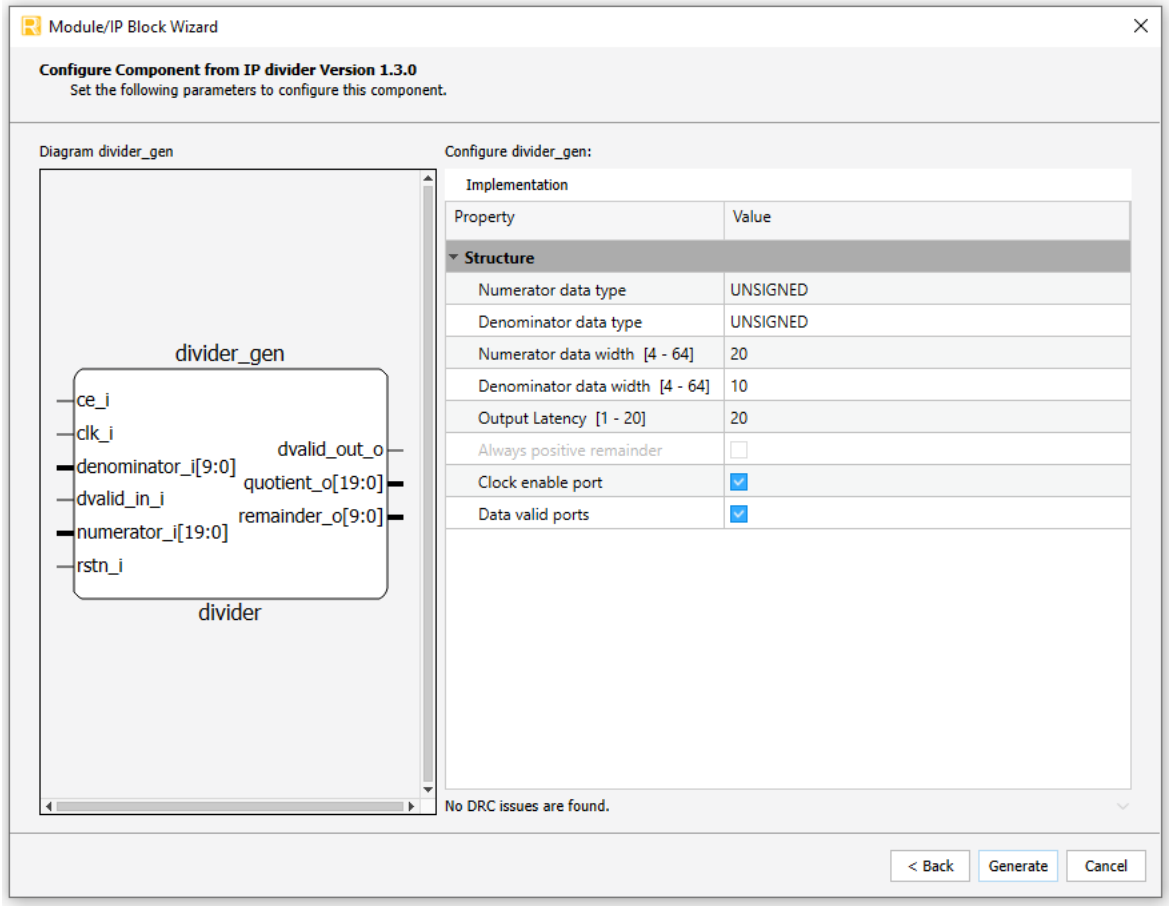

Figure 3.2. Configure User Interface of Divider IP Core

4. Click **Generate**. The **Check Generating Result** dialog box opens, showing design block messages and results as shown in Figure 3.3.

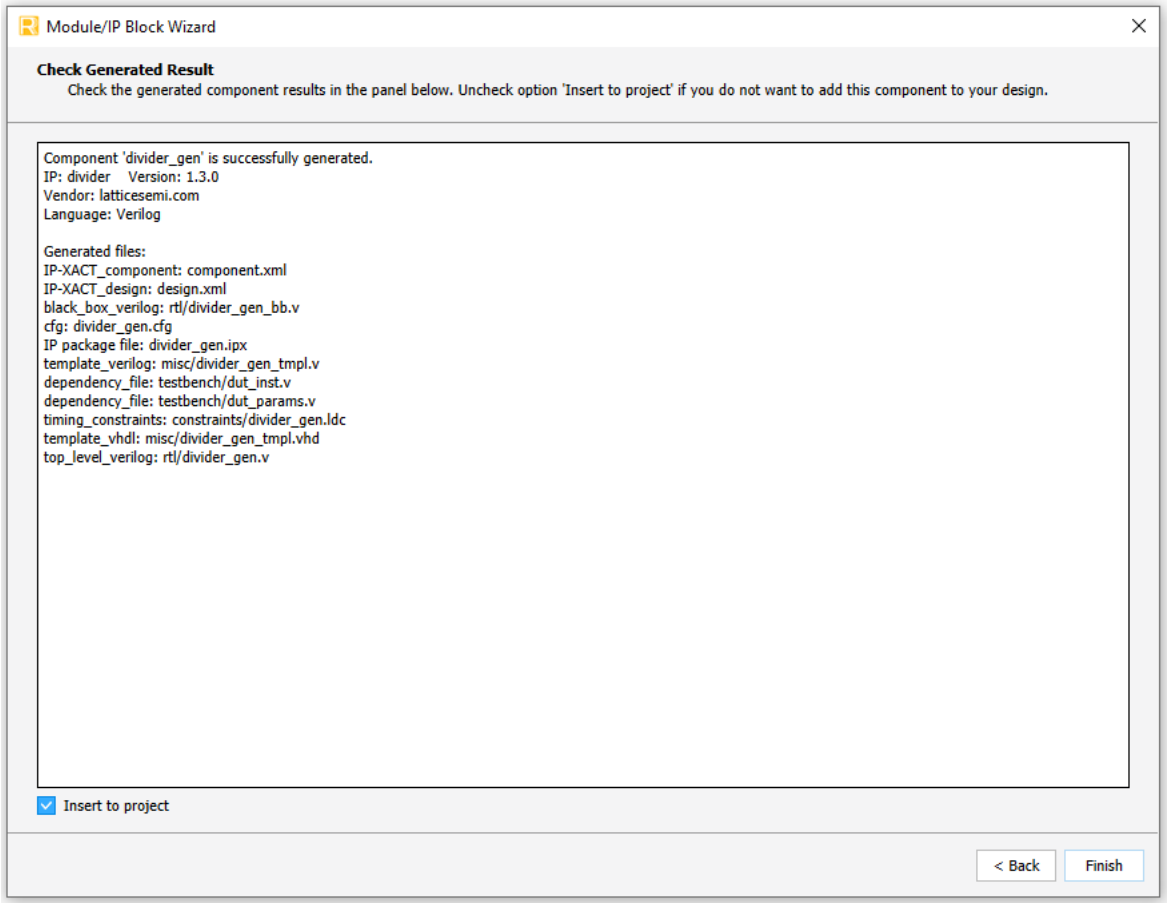

Figure 3.3. Check Generating Result

5. Click the **Finish** button.

All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields shown in Figure 3.1.

The generated Divider IP Core package includes the closed-box (<Component name>_bb.v) and instance templates (<Component name>_tmpl.v/vhd) that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file (<Component name>.v) that can be used as an instantiation template for the IP core is also provided. You may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 3.1.

Table 3.1. Generated File List

Attribute	Description
<Component name>.ipx	This file contains the information on the files associated to the generated IP.
<Component name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Component name>.v	This file provides an example RTL top file that instantiates the IP core.
rtl/<Component name>_bb.v	This file provides the synthesis closed-box.
misc/<Component name>_tmpl.v misc /<Component name>_tmpl.vhd	These files provide instance templates for the IP core.

3.3. Running Functional Simulation

To run functional simulation:

1. Click the  button located on the **Toolbar** to initiate the **Simulation Wizard** shown in Figure 3.4.

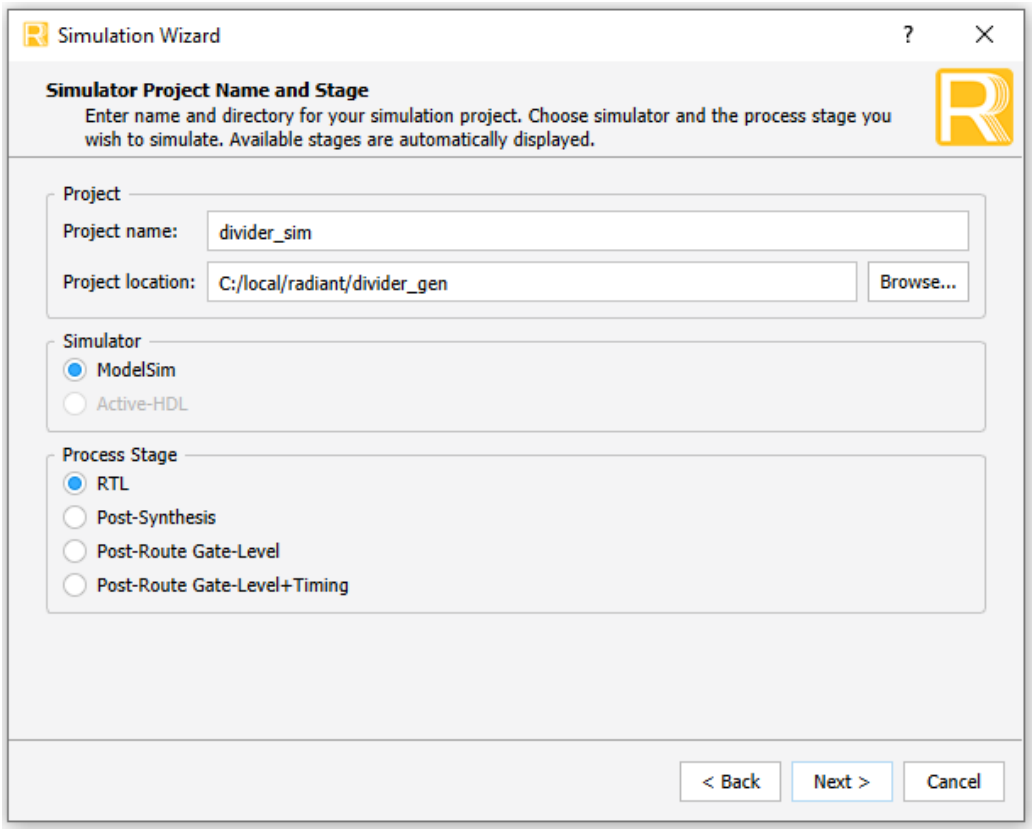

Figure 3.4. Simulation Wizard

2. Click **Next** to open the **Add and Reorder Source** window as shown in Figure 3.5.

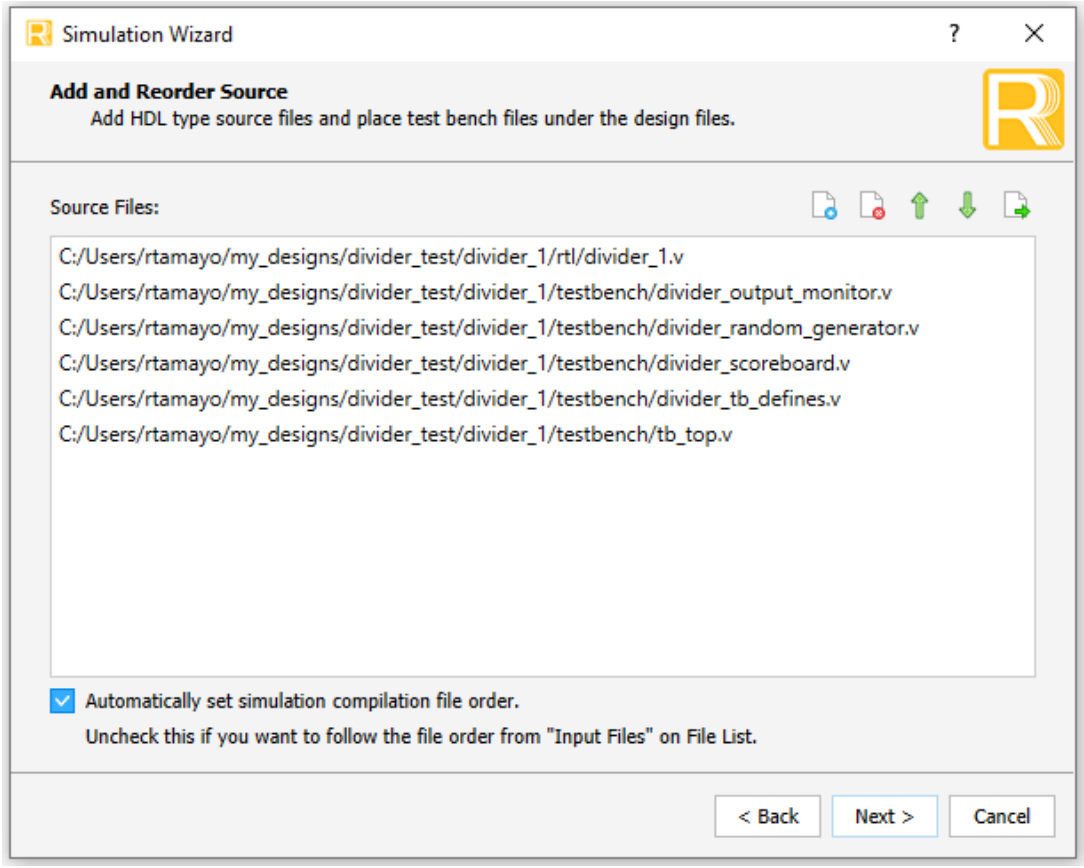

Figure 3.5. Adding and Reordering Source

3. Click **Next**. The **Summary** window is shown.
4. Click **Finish** to run the simulation.

Note: It is necessary to follow the procedure above until it is fully automated in the Lattice Radiant software suite. The results of the simulation in our example are provided in Figure 3.6.

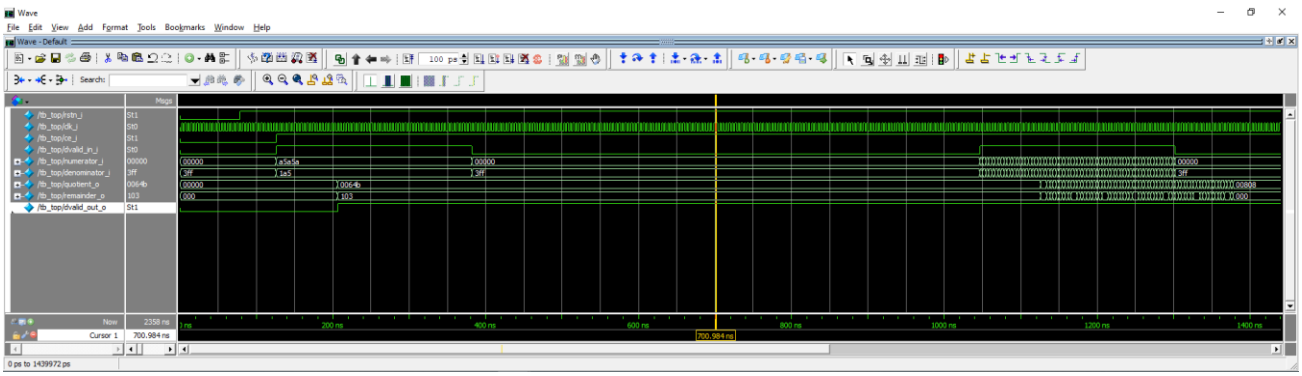

Figure 3.6. Simulation Waveform

3.4. Constraining the IP

You need to provide proper timing and physical design constraints to ensure that your design meets the desired performance goals on the FPGA device. Add the content of the following IP constraint file to your design constraints as shown in this pathway: *<IP_Instance_Path>/<IP_Instance_Name>/eval/constraint.pdc*.

The constraint file has been verified during the IP evaluation with the IP instantiated directly in the top-level module. With thorough understanding of the effect of each constraint, you can modify the constraints in the IP constraint file.

To use the IP constraint file, copy the content of *constraint.pdc* file to the top-level design constraint for post-synthesis. For details on how to constrain the user design, refer to Lattice Radiant Timing Constraints Methodology.

3.5. IP Evaluation

The Divider IP Core supports Lattice's IP hardware evaluation capability when used with Lattice FPGA devices built on the Lattice Nexus™ platform. This makes it possible to create versions of the IP core that operates in hardware for a limited period of time (approximately four hours) without requiring the purchase of an IP license. It may also be used to evaluate the core in hardware in user-defined designs. The hardware evaluation capability may be enabled/disabled in the Strategy dialog box. It is enabled by default. To change this setting, go to Project > Active Strategy > LSE/Synplify Pro Settings.

Appendix A. Resource Utilization

Table A.2 shows the resource utilization of the Divider IP Core for the LFMXO5-25-9BBG400I device using Synplify Pro of Lattice Radiant software 3.1. Default configuration is used, and some attributes are changed from the default value to show the effect on the resource utilization.

Table A.2. LFMXO5-25-9BBG400I Device Resource Utilization

Configuration	Clk Fmax (MHz)*	Registers	LUTs	EBRs
Default	200	829	341	0
Numerator Data Width: 4, Denominator Data Width: 4, Output Latency: 1, Others = Default	200	9	40	0
Numerator Data Width: 10, Denominator Data Width: 20, Output Latency: 10, Others = Default	200	499	301	0
Numerator Data Type: SIGNED, Denominator Data Type: SIGNED, Others = Default	187	821	472	0
Numerator Data Width: 64, Denominator Data Width: 64, Output Latency: 64, Others = Default	154	12540	4609	0

***Note:** Fmax is generated when the FPGA design only contains Divider IP Core, and the target Frequency is 200 MHz. These values may be reduced when user logic is added to the FPGA design.

Table A.3 shows the resource utilization of the Divider IP Core for the LFMXO5-25-7BBG400I device using Synplify Pro of Lattice Radiant software 3.1. Default configuration is used, and some attributes are changed from the default value to show the effect on the resource utilization.

Table A.3. LFMXO5-25-7BBG400I Device Resource Utilization

Configuration	Clk Fmax (MHz)*	Registers	LUTs	EBRs
Default	149	829	341	0
Numerator Data Width: 4, Denominator Data Width: 4, Output Latency: 1, Others = Default	200	9	40	0
Numerator Data Width: 10, Denominator Data Width: 20, Output Latency: 10, Others = Default	145	499	301	0
Numerator Data Type: SIGNED, Denominator Data Type: SIGNED, Others = Default	122	821	475	0
Numerator Data Width: 64, Denominator Data Width: 64, Output Latency: 64, Others = Default	97	12540	4609	0

***Note:** Fmax is generated when the FPGA design only contains Divider IP Core, and the target Frequency is 200 MHz. These values may be reduced when user logic is added to the FPGA design.

Table A.4 shows the resource utilization of the Divider IP Core for the LAV-AT-E70-3LFG1156C device using Synplify Pro of Lattice Radiant software 2023.2. Default configuration is used, and some attributes are changed from the default value to show the effect on the resource utilization.

Table A.4. LAV-AT-E70-3LFG1156C Device Resource Utilization

Configuration	Clk Fmax (MHz)*	Registers	LUTs	EBRs
Default	250	829	716	0
Numerator Data Width: 4, Denominator Data Width: 4, Output Latency: 1, Others = Default	250	9	75	0
Numerator Data Width: 10, Denominator Data Width: 20, Output Latency: 10, Others = Default	250	499	656	0
Numerator Data Type: SIGNED, Denominator Data Type: SIGNED, Others = Default	250	839	844	0
Numerator Data Width: 64, Denominator Data Width: 64, Output Latency: 64, Others = Default	250	16382	16703	0

***Note:** Fmax is generated when the FPGA design only contains Divider IP Core, and the target frequency is 200 MHz. These values may be reduced when user logic is added to the FPGA design.

Table A.5 shows the resource utilization of the Divider IP Core for the LAV-AT-G70-1LFG1156C device using Synplify Pro of Lattice Radiant software 2023.2. Default configuration is used, and some attributes are changed from the default value to show the effect on the resource utilization.

Table A.5. LAV-AT-G70-1LFG1156C Device Resource Utilization

Configuration	Clk Fmax (MHz)*	Registers	LUTs	EBRs
Default	250.0	829	716	0
Numerator Data Width: 4, Denominator Data Width: 4, Output Latency: 1, Others = Default	250.0	9	75	0
Numerator Data Width: 10, Denominator Data Width: 20, Output Latency: 10, Others = Default	250.0	499	656	0
Numerator Data Type: SIGNED, Denominator Data Type: SIGNED, Others = Default	250.0	839	844	0
Numerator Data Width: 64, Denominator Data Width: 64, Output Latency: 64, Others = Default	208.2	16382	16703	0

***Note:** Fmax is generated when the FPGA design only contains Divider IP Core, and the target frequency is 200 MHz. These values may be reduced when user logic is added to the FPGA design.

Table A.6 shows the resource utilization of the Divider IP Core for the LFD2NX-9-7MG121C device using Synplify Pro of Lattice Radiant software 2024.2. Default configuration is used, and some attributes are changed from the default value to show the effect on the resource utilization.

Table A.6. LFD2NX-9-7MG121C Device Resource Utilization

Configuration	Clk Fmax (MHz)*	Registers	LUTs	EBRs
Default	200	829	401	0
Numerator Data Width: 4, Denominator Data Width: 4, Output Latency: 1, Others = Default	200	9	56	0
Numerator Data Width: 10, Denominator Data Width: 20, Output Latency: 10, Others = Default	200	499	361	0
Numerator Data Type: SIGNED, Denominator Data Type: SIGNED, Others = Default	152.068	821	511	0
Numerator Data Width: 64, Denominator Data Width: 64, Output Latency: 64, Others = Default	Configuration does not fit in the Device.	Configuration does not fit in the Device.	Configuration does not fit in the Device.	Configuration does not fit in the Device.

***Note:** Fmax is generated when the FPGA design only contains Divider IP Core, and the target frequency is 100 MHz. These values may be reduced when user logic is added to the FPGA design.

Table A.7 shows the resource utilization of the Divider IP Core for the LFD2NX-17-7MG121C device using Synplify Pro of Lattice Radiant software 2024.2. Default configuration is used, and some attributes are changed from the default value to show the effect on the resource utilization.

Table A.7. LFD2NX-17-7MG121C Device Resource Utilization

Configuration	Clk Fmax (MHz)*	Registers	LUTs	EBRs
Default	200	829	401	0
Numerator Data Width: 4, Denominator Data Width: 4, Output Latency: 1, Others = Default	200	9	56	0
Numerator Data Width: 10, Denominator Data Width: 20, Output Latency: 10, Others = Default	200	499	361	0
Numerator Data Type: SIGNED, Denominator Data Type: SIGNED, Others = Default	152.068	821	511	0
Numerator Data Width: 64, Denominator Data Width: 64, Output Latency: 64, Others = Default	Configuration does not fit in the Device.	12540	4865	0

***Note:** Fmax is generated when the FPGA design only contains Divider IP Core, and the target frequency is 100 MHz. These values may be reduced when user logic is added to the FPGA design.

Table A.8 shows the resource utilization of the Divider IP Core for the LFD2NX-28-7MG121C device using Synplify Pro of Lattice Radiant software 2024.2. Default configuration is used, and some attributes are changed from the default value to show the effect on the resource utilization.

Table A.8. LFD2NX-28-7MG121C Device Resource Utilization

Configuration	Clk Fmax (MHz)*	Registers	LUTs	EBRs
Default	200	829	401	0
Numerator Data Width: 4, Denominator Data Width: 4, Output Latency: 1, Others = Default	200	9	56	0
Numerator Data Width: 10, Denominator Data Width: 20, Output Latency: 10, Others = Default	200	499	361	0
Numerator Data Type: SIGNED, Denominator Data Type: SIGNED, Others = Default	159.033	821	511	0
Numerator Data Width: 64, Denominator Data Width: 64, Output Latency: 64, Others = Default	157.679	12540	4865	0

***Note:** Fmax is generated when the FPGA design only contains Divider IP Core, and the target frequency is 100 MHz. These values may be reduced when user logic is added to the FPGA design.

Table A.9 shows the resource utilization of the Divider IP Core for the LFD2NX-40-7MG121C device using Synplify Pro of Lattice Radiant software 2024.2. Default configuration is used, and some attributes are changed from the default value to show the effect on the resource utilization.

Table A.9. LFD2NX-40-7MG121C Device Resource Utilization

Configuration	Clk Fmax (MHz)*	Registers	LUTs	EBRs
Default	200	829	401	0
Numerator Data Width: 4, Denominator Data Width: 4, Output Latency: 1, Others = Default	200	9	56	0
Numerator Data Width: 10, Denominator Data Width: 20, Output Latency: 10, Others = Default	200	499	361	0
Numerator Data Type: SIGNED, Denominator Data Type: SIGNED, Others = Default	159.033	821	511	0
Numerator Data Width: 64, Denominator Data Width: 64, Output Latency: 64, Others = Default	157.679	12540	4865	0

***Note:** Fmax is generated when the FPGA design only contains Divider IP Core, and the target frequency is 100 MHz. These values may be reduced when user logic is added to the FPGA design.

Table A.10 shows the resource utilization of the Divider IP Core for the LN2-CT-20-1CBG484C device using Synplify Pro of Lattice Radiant software 2024.2. Default configuration is used, and some attributes are changed from the default value to show the effect on the resource utilization.

Table A.10. LN2-CT-20-1CBG484C Device Resource Utilization

Configuration	Clk Fmax (MHz)*	Registers	LUTs	EBRs
Default	138.735	829	716	0
Numerator Data Width: 4, Denominator Data Width: 4, Output Latency: 1, Others = Default	250	9	74	0
Numerator Data Width: 10, Denominator Data Width: 20, Output Latency: 10, Others = Default	122.971	499	658	0
Numerator Data Type: SIGNED, Denominator Data Type: SIGNED, Others = Default	130.548	821	823	0
Numerator Data Width: 64, Denominator Data Width: 64, Output Latency: 64, Others = Default	159.058	16381	17019	0

***Note:** Fmax is generated when the FPGA design only contains Divider IP Core, and the target frequency is 100 MHz. These values may be reduced when user logic is added to the FPGA design.

References

- Divider IP Release Notes (FPGA-RN-02090)
- Avant-E web page
- Avant-G web page
- Avant-X web page
- Certus-N2 web page
- Certus-NX web page
- CertusPro-NX web page
- CrossLink-NX web page
- MachXO5-NX web page
- Lattice Radiant Software web page
- Lattice Solutions IP Cores web page
- Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059)
- Lattice Insights web page for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Note: In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

Revision 1.7, IP v1.6.1, December 2025

Section	Change Summary

Quick Facts	• In Table 1.1. Divider Quick Facts:
	  • Updated from *IP Core v1.6.0 to IP Core v1.6.1*.
	  • Updated from *Lattice Radiant software 2025.1* to *Lattice Radiant software 2025.2*.
	• Added note, *In some instances, the IP may be updated without changes to the user guide. This user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.*

Core Generation, Simulation, and Validation	• Added note, *The screenshots provided are for reference only. Details may vary depending on the version of the IP or software being used. If there have been no significant changes to the GUI, a screenshot may reflect an earlier version of the IP.* • Updated content of Licensing the IP: *The Divider IP is provided at no additional cost with the Lattice Radiant software.*
Ordering Part Number	Removed this section.
Revision History	Added note.

Revision 1.6, IP v1.6.0, July 2025

Section	Change Summary
Introduction	Updated Table 1.1. Divider Quick Facts: • Renamed *Table 1.1 Quick Facts* to *Table 1.1 Divider Quick Facts*. • Changed *FPGA Families Supported* to *Supported Devices* in *IP Requirements.* • Added *Certus-NX-RT* and *CertusPro-NX-RT* to *Supported Devices.* • Added *IP Changes* to *IP Requirements.* • Removed *Targeted Devices* from *Resource Utilization.* • Updated the *Lattice Implementation* information in *Design Tool Support*.
Ordering Part Number	Updated instances of *Multi-site Perpetual* to *Single Seat Perpetual*.
Core Generation, Simulation, and Validation	Minor editorial changes.
References	Added Divider IP Release Notes (FPGA-RN-02090) document.

Revision 1.5, IP v1.5.0, December 2024

Section	Change Summary
All	• Removed *Core* from the document title. • Added the IP version information on the cover page.
Introduction	Updated Table 1.1. Quick Facts: • Added the *Certus-N2* device family to *Supported FPGA Family*. • Added *LFD2NX-9*, *LFD2NX-28*, and *LN2-CT-20* devices to *Targeted Devices*. • Updated the Resources and Lattice Implementation information.
Ordering Part Number	• Updated instances of *Single Machine* to *Single Seat*. • Added the Certus-N2 OPNs.
Resource Utilization	Added resource utilizations for the Lattice Radiant software version 2024.2 and made editorial fixes.
References	• Added the *Avant-E*, *Avant-G*, *Avant-X*, *Certus-N2*, *Lattice Solutions IP Cores*, and *Lattice Insights* web pages. • Added the *Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059)* document.

Section	Change Summary
	• Removed *Lattice Avant Platform* web page. • Made editorial fixes.

Revision 1.4, December 2023

Section	Change Summary
All	• Changed the document name from *Divider IP Core – Lattice Radiant Software* to *Divider IP Core*. • Updated the device name from *LAV-AT-500E* to *LAV-AT-E70*. • Minor adjustments to ensure the document is consistent with Lattice Semiconductor's inclusive language policy.
Disclaimers	Updated boilerplate.
Inclusive Language	Added boilerplate.
Introduction	• Added trademark for Lattice Avant. • Updated the targeted devices.
Core Generation, Simulation, and Validation	• Renamed 3.2 Generating and Synthesizing the IP. • Added 3.4 Constraining the IP. • Renamed and updated the header number of 3.5 IP Evaluation.
Ordering Part Number	• Updated license type for existing Ordering Part Numbers. • Added Avant-AT-G, and Avant-AT-X Ordering Part Numbers.
Resource Utilization	• Updated from *Lattice Radiant software 2022.1* to *Lattice Radiant software 2023.2*. • Updated Table A.3 and Table A.4.
References	• Removed *in latticesemi.com* from existing references. • Added references to the MachXO5-NX, Lattice Avant Platform, Lattice Radiant Software web pages.
Technical Support Assistance	Added link to the Lattice Answer Database.

Revision 1.3, November 2022

Section	Change Summary
Introduction	Added Lattice Avant family and related device support information to Table 1.1. Quick Facts.
Core Generation, Simulation, and Validation	Updated the below figures: • Figure 3.1. Module/IP Block Wizard • Figure 3.2. Configure User Interface of Divider IP Core • Figure 3.3. Check Generating Result • Figure 3.4. Simulation Wizard • Figure 3.5. Adding and Reordering Source • Figure 3.6. Simulation Waveform
Ordering Part Number	Added Avant Ordering Part Numbers.
Resource Utilization	• Updated the titles of tables Table A.1. LFMXO5-25-9BBG400I Resource Utilization and Table A.2. LFMXO5-25-7BBG400I Resource Utilization. • Added Table A.3. LAV-AT-E70-3LFG1156C Resource Utilization and Table A.4. LAV-AT-G70-1LFG1156C Resource Utilization.

Revision 1.2, May 2022

Section	Change Summary
Disclaimer	Updated.
Introduction	Added MachXO5-NX family and related device support information to Table 1.1. Quick Facts.
Core Generation, Simulation, and Validation	• Updated Figure 3.1. Module/IP Block Wizard to reflect the most recent software update. • Updated Figure 3.2. Configure User Interface of Divider IP Core to reflect the most

Section	Change Summary
	recent software update.
Resource Utilization	• Globally updated Table A.1. Resource Utilization and Table A.2. Resource Utilization for the Divider IP update. • Removed the previous Table A.3. Resource Utilization.

Revision 1.1, June 2021

Section	Change Summary
Introduction	Updated Table 1.1. Quick Facts. • Revised Supported FPGA Families • Revised Targeted Devices • Revised Lattice Implementation
Core Generation, Simulation, and Validation	Replaced specific devices with *Lattice FPGA devices built on the Lattice Nexus platform* In the Hardware Evaluation sections.
Ordering Part Number	Added part numbers.
References	Added reference to the CertusPro-NX web page.

Revision 1.0, October 2020

Section	Change Summary
All	Initial release.

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