Lattice Diamond 3.12 Platform Designer User Guide

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Type Conventions Used in This Document

Convention	Meaning or Use
Bold	Items in the user interface that you select or click. Text that you type into the user interface.
<*Italic*>	Variables in commands, code syntax, and path names.
Ctrl+L	Press the two keys at the same time.
`Courier`	Code examples. Messages, reports, and prompts from the software.
`...`	Omitted material in a line of code.
. . .	Omitted lines in code and report examples.
`[ ]`	Optional items in syntax descriptions. In bus specifications, the brackets are required.
`( )`	Grouped items in syntax descriptions.
`{ }`	Repeatable items in syntax descriptions.
`|`	A choice between items in syntax descriptions.

Contents

Chapter 1

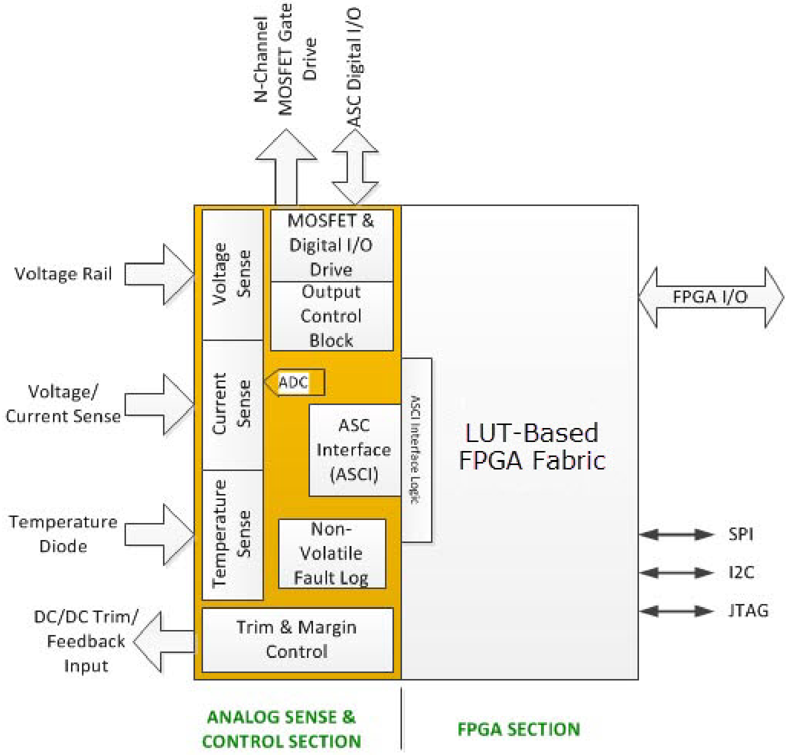
Designing with Lattice Diamond Platform Designer

Included with the Lattice Diamond software is the Platform Designer tool which enables you to build and control a complete hardware management system. With Platform Designer, you can build and control:

- Platform Manager 2
- Platform Manager 2 in a two-device (LPTM21 and LPTM21L) configuration
- Certain devices in the MachXO2HC/HE family with external Analog Sense and Control (ASC) devices
- Certain devices in the MachXO3D family with external ASC devices.
- Certain devices in the MachXO3LF family with external ASC devices.
- Certain devices in the ECP5U/UM family with external ASC devices.

The larger LPTM21 device can configure both ASC and/or LPTM21L as slave devices.

Figure 1: Platform Manager 2 Block Diagram



As shown in the previous figure, the Platform Manager 2 device is made up of an ASC block and an FPGA block. These two blocks provide the necessary programmable building blocks to enable integration of various combinations of hardware management functions into a single chip. The hardware management algorithm is implemented within the FPGA block of the Platform Manager 2. The monitoring and control resources can be scaled up, to meet application requirements, by adding an external ASC to the Platform Manager 2. Each of the ASCs provides additional monitor and control of up to ten voltage rails, two temperature sensors and two current sensors. The overall platform management algorithm that uses the inputs from the external ASC device(s) is located within the FPGA block of the Platform Manager 2. The following diagram shows how an ASC device can be connected to a Platform Manager 2 device to implement a hardware management circuit that monitors the board voltage rails (V), supply currents (**I**), and board temperatures (T).

Figure 2: ASC Device Connected to a Platform Manager 2 Device

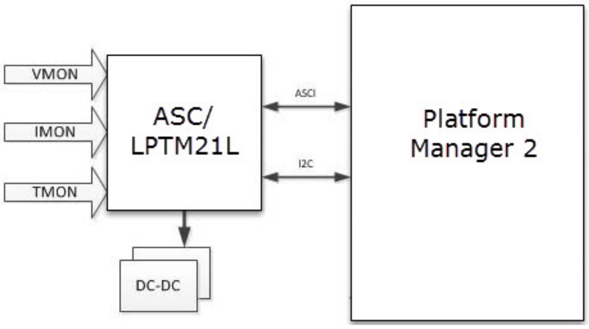
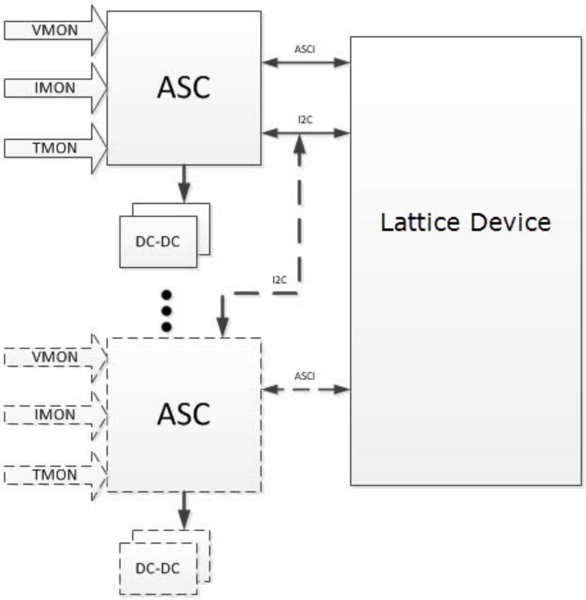


Figure 3: Connecting Multiple ASCs to Lattice Device



Multiple ASC devices can also be connected to imilar to the Platform Manager 2, to offer wider flexibility and control when implementing a complete hardware management system. Devices include:

- Certain devices in the MachXO2HC/HEHC/HE family
- Certain devices in the MachXO3D family with external ASC devices
- Certain devices in the MachXO3LF family with external ASC devices
- Certain devices in the ECP5U/UM family with external ASC devices

Unique to Platform Manager 2 is the smaller package LPTM21L device can be also configured as a slave device combining with ASC. Table 1 lists Platform Manager 2, MachXO2HC/HEHC/HE, MachXO3D, MachXO3LF and

ECP5U/UM devices that support ASCs, and also lists the maximum number of ASCs that can be used for each device.

Table 1: External ASCs/LPTM21 supported by Platform Manager 2, MachXO2HC/HEHC/HE, MachXO3D, MachXO3LF, ECP5U/UM

Family	Device	Maximum Number of External ASCs
Platform Manager 2	LPTM21	3 ASC and/or LPTM21L
Platform Manager 2	LPTM21L	3 ASC and/or LPTM21L
MachXO2HC/HEHC/HE	640HC	2
	1200HC	4
	2000HC	6
	4000HC	8
	7000HC	8
	2000HE	6
	4000HE	8
	7000HE	8
MachXO3D	4300	8
	9400	8
MachXO3LF	640E	2
	1300E/C	4
	2100E/C	6
	4300E/C	8
	6900E/C	8
ECP5U/UM	LFE5U-12F	8
	LFE5U-25F	8
	LFE5U-45F	8
	LFE5UM-25F	8
	LFE5UM-45F	8

See Also ▶“Platform Designer User Interface” on page 11

▶ “Platform Designer Flow” on page 13

About Platform Designer

Platform Designer provides an integrated design environment that enables you to configure the device, implement the hardware management algorithm, simulate, assign pins, and finally generate the JEDEC files required to program and configure the device on the circuit board. It also allows you to import other HDL files to integrate other desired functions.

See Also ▶"Launching Platform Designer" on page 15

- "Platform Designer User Interface" on page 11
- "Platform Designer Flow" on page 13

Platform Designer User Interface

Platform Designer contains separate editors for configuring global settings; current, temperature, and voltage monitors; fan controller and fault logger components; ports, nodes, and logic controls. It also provides a view for checking design rules and resources and building the design. Each editor and view is accessed from the Platform Designer menu pane on the left, which is divided into five main sections: Global, Analog, Components, Control, and Build.

Global The Global Configuration view provides global configuration options, including options for each ASC device. The global ASC Options provide access to configuration settings like the I^{2}C address and other default settings. The Device Options enable you to select the programming interface, clock source, and boot mode.

Components The Components section enables you to configure the fan, fault logging, hot swap, and PMBus Adapter. It includes the following views:

- Fan Controller – The Fan Controller allows you to add a fan, specify the fan interconnections, and configure the control parameters. The fan controller can be configured to work with 2-wire, 3-wire, or 4-wire fans, and up to sixteen fans can be controlled. The fan controller generates a pulse width modulated (PWM) signal to set fan speeds.
- Fault Logger – The Fault Logger enables you to specify and configure fault conditions that are logged to non-volatile memory. You have the option of using standard fault logging that is based on voltage, current, and temperature status; or using the full-featured fault logging.
- Hot Swap – **(Platform Manager 2, MachXO2HC/HEHC/HE, MachXO3D, and MachXO3LF only.)** The Hot Swap component enables you to configure the ASC for a hysteretic closed-loop to limit the in-rush current in an application where power is rapidly applied. Such an application can include such a line card, blade, or a PCB that is plugged into a "hot" backplane.
- PMBus Adapter – **(Platform Manager 2, MachXO2HC/HE, MachXO3D, and MachXO3LF only.)** The PMBus Adapter component allows you to configure the adapter for connecting analog Point of Load (POL) DC-DC converters to PMBus using the ASC and FPGA.

Analog The Analog section enables you to configure the settings for current, temperature, and voltage monitors. It includes the following editors:

- Current – The Current editor enables you to configure the low-voltage and high-voltage current monitors for each ASC device. Platform Designer automatically populates the current trip points available based on the sense resistor selection. You can configure the trip points and other current monitor settings here.
- Temperature – The Temperature editor enables you to configure the temperature monitors (TMON) for each ASC device. Multiple monitor levels can be selected for each TMON, with temperature values displayed in ^{o}C.
- Voltage – The Voltage editor allows you to configure voltage monitoring, trimming, margining, and voltage identification (VID) settings for each ASC device in your system. You can edit multiple settings by using the Voltage Monitor & Control dialog box. To open the dialog box, double-click an active cell in the ASC column or the Pins Monitor/Trim column on any of the three spreadsheets, or right-click the cell and choose **Edit**. You can also edit settings individually on the Voltage spreadsheet or the VID spreadsheet by single-clicking an editable cell.

Control The Control section enables you to configure signals and set the control logic. It includes the following editors:

- Ports & Nodes – The Ports & Nodes editor provides spreadsheets for viewing the internal nodes and configuring external signals (ports) of the chip set. The Ports sheet shows all physical FPGA-based PIOs that are available for use as external connections to the design and allows you to assign labels to logical ports, specify the I/O and register type, and group ports of a common type to form a bus. The Nodes sheet shows internal signals already generated to connect the implemented features of the design. The nodes sheet allows you to create additional signals for connecting different features on-chip. The GPIO sheet allows you to configure and label the ASC-based general purpose I/Os. The HV Outputs sheet allows you to label and configure the high-voltage output ports.
- Logic – The Logic editor enables you to create sequences, exception logic, supervisory equations, and timers for one or more state machines. It also allows you to import modules into your design from HDL code. The Sequence page of the Logic editor allows you to add state machines and gives you access to the Multiple State Machines dialog box for managing the state machine library.

Build The Build view enables you to check the design status, examine the amount of hardware resources consumed, run DRC check, compile the design, and generate the merged JEDEC file. The Build view includes a summary table of enabled components and programming options, and it shows the amount of hardware resources of the device that have been consumed by the current design configuration. The Build view enables you to generate a test bench, including stimulus, for simulating your design. It also allows you to export a detailed configuration report.

See Also ▶"Working with Platform Designer Editors" on page 19

Platform Designer Input Files

The input files for Platform Designer include the Platform Designer project file (.ptm) and HDL source files (.v, .vhd).

The .ptm file holds all of the Analog Sense and Control settings, as well as the logic and port information, for the active Platform Designer project. A .ptm file is generated automatically for a new project. You can also add a new or existing .ptm file, which allows you to choose from multiple project files in a single implementation.

HDL source files are not required, but you can add them to the Diamond project. Once the HDL files are added to the Diamond project, you can use Platform Designer's Logic Editor to import an HDL module into the Platform Designer project.

See Also ▶See "Working with Platform Designer Project (.ptm) Files" on page 17

▶ "Importing HDL Modules" on page 56.

▶ "Creating a New Platform Designer Project" on page 15

Platform Designer Output Files

Platform Designer automatically generates the background HDL files when you compile the design. The "Generate Jedec" process produces a merged JEDEC of the FPGA and ASC JEDEC files for programming. ECP5U/UM output file is .bit.

See Also ▶"Building the Design" on page 56

Platform Designer Flow

The number of tasks involved in the Platform Designer flow will vary, depending on the selected Platform Manager 2, or MachXO2HC/HE, MachXO3D, or MachXO3LF, or ECP5U/UM, the number of external ASC/LPTM21L (for LPTM21/LPTM21L as masters, LPTM21L and/or ASC can be slaves) devices selected, and the types of configuration needed to complete the design. The following outline shows a typical flow of required and optional tasks.

1. Create a project in Lattice Diamond. Select the base device and package; Platform Manager 2, or MachXO2HC/HE, MachXO3D, or MachXO3LF, or ECP5U/ECP5UM. Then add the number of external ASC devices needed. For Platform Manager 2 devices LPTM21 / LPTM21L selected as master devices, LPTM21L and/or ASCs can be combined as slave devices.

2. Specify global settings:

   - ASC options, including reset type, and default options for voltage, current, and temperature

- device options, including programming interface, clock source, and boot mode

3. Configure the ports and nodes:
    - ports and port groups
    - internal nodes
    - general-purpose I/Os
    - high-voltage outputs
4. Configure the analog settings:
    - Configure the voltage monitors (VMONs):
        - schematic net names and parameters
        - trim/margin parameters
        - voltage identification (VID) tables
    - Configure the current monitors (IMONs).
    - Configure the temperature monitors (TMONs).
    - Configure one or more fans:
        - fan type and pulse width modulation
        - fan interconnections
    - Configure PMBus Adapter.
    - Enable and configure fault logging.
5. Define the platform management logic, including sequencing and monitoring:
    - timers
    - sequencer instructions and exceptions for one or more state machines
    - supervisory logic equations
    - modules that are imported from HDL
6. Build the design.
    - Examine the resources consumed.
    - Run design rule check.
    - Compile the design to generate the HDL code and synthesize the logic.
    - Assign Pins in Spreadsheet View.
    - Generate the JEDEC to process the design and generate the merged JEDEC file.
7. Simulate the design.

See Also

- “Platform Designer User Interface” on page 11
- “Creating a New Platform Designer Project” on page 15
- “Working with Platform Designer Project (.ptm) Files” on page 17

Launching Platform Designer

You can launch Platform Designer by creating a new project in Diamond that targets a Platform Manager 2 LPTM21/LPTM21L device with external ASCs and/or LPTM21L devices, or a MachXO2HC/HE with external ASCs, MachXO3D with external ASCs, or MachXO3LF with external ASCs, or an ECP5U/UM with external ASCs. You can also launch Platform Designer by opening an existing Platform Designer project file (.ptm).

Platform Designer is also available from the Diamond Tools menu when you open an existing project that targets a Platform Manager 2 LPTM21/LPTM21L device with external ASCs and/or LPTM21L devices, or a MachXO2HC/HE with external ASCs, or a MachXO3D with external ASCs, or a MachXO3LF with external ASCs, or an ECP5U/UM with external ASCs.

See Also ▶“Creating a New Platform Designer Project” on page 15

- ▶ “Opening an Existing Platform Designer Project” on page 17
- ▶ “Working with Platform Designer Project (.ptm) Files” on page 17
- ▶ “Working with Platform Designer Editors” on page 19

Creating a New Platform Designer Project

When you create a new project that targets the Platform Manager 2, or a MachXO2HC/HE with external ASCs, or a MachXO3D with external ASCs, or a MachXO3LF with external ASCs, or an ECP5U/UM with external ASCs, Diamond generates a new Platform Designer project file (.ptm) and opens the Platform Designer user interface.

To create a new Platform Designer project in Diamond:

1. In Diamond, choose **File > New Project** to open the Create a Lattice Diamond Project wizard.
2. Click **Next**.
3. In the Project section, type a name for the project and use the Browse button to navigate to a location.
4. Click **Next**.
5. The Add Source section is an optional step that allows you to add HDL source files to the project or an existing Platform Designer project (.ptm) file. If you add an existing .ptm file, the default .ptm file will not be added to the project.

   To skip the Add Source step, click **Next**.

   To add source files to the project, click the **Add Source** button to navigate to the files and select them, and then click **Next**.
6. In the Select Device dialog box, do one of the following:

- Select **Platform Manager 2** in the Family section, and then select the desired LPTM device from the Device section.

  Platform Manager 2 devices contain one embedded Analog Sense and Control (ASC) device. There are 2 devices in the Platform Manager 2 family, LPTM21 and LPTM21L in a smaller package configuration. The LPTM21/LPTM21L device allows you to add up to three external ASC and/or LPTM21L devices. The LPTM20 device allows you to add one external ASC device. To add an external ASC and/or LPTM21L device, select **LPTM21/LPTM21L**. The “Select ASC Device” section will then appear near the bottom of the dialog box. You will note a 3 device radial button selection for mixing and matching selection of ASC and LPTM21L as slave devices.

- Select **MachXO2HC/HE** in the Family section, and then select the desired LCMXO2 HC device—640HC or larger—from the Device section.

  The “Select ASC Device” section appears near the bottom of the dialog box. Up to eight ASC devices can be added, depending upon the size of MachXO2HC/HE device.

- Select **MachXO3D** in the Family section, and then select the desired from the Device section.

  The “Select ASC Device” section appears near the bottom of the dialog box. Up to eight ASC devices can be added, depending upon the size of MachXO3D device.

- Select **MachXO3LF** in the Family section, and then select the desired from the Device section.

  The “Select ASC Device” section appears near the bottom of the dialog box. Up to eight ASC devices can be added, depending upon the size of MachXO3LF device.

- Select **ECP5U/UM** in the Family section, and then select the desired LFE5UM device—25F or 45F—from the Device section.

  The “Select ASC Device” section appears near the bottom of the dialog box. Up to eight ASC devices can be added.

7. In the “Select ASC Device” section, select the number of ASC devices you would like to include.

   The package type, performance grade, operating conditions, and part name are all tied to the device selection.

8. Click **Next**.

   In the Select Synthesis Tool dialog box, select the synthesis tool that you want to use. The choices are **Lattice LSE** and **Synplify Pro** and can be changed at any time.

9. Click **Next**.

   In the Project Information dialog box, the option “Create Platform Designer file” is selected by default. This will create a .ptm file using the project name shown in the File name box and cause Platform Designer to open. If desired, you can assign a different name for the .ptm file and select a different directory location.

Note

If you added an existing .ptm file to the project in Step 4, the “Create Platform Designer file” option will not be available.

10. Click **Finish**.

    Platform Designer opens within Diamond and loads the .ptm file.

See Also

- “Opening an Existing Platform Designer Project” on page 17
- “Working with Platform Designer Project (.ptm) Files” on page 17

Opening an Existing Platform Designer Project

After you have created a project in Diamond that targets a Platform Manager 2, or a MachXO2HC/HE with external ASCs, or MachXO3D with external ASCs, or MachXO3LF with external ASCs, or an ECP5U/UM with external ASCs, you can open the Platform Designer project file (.ptm) for the active implementation.

To open an existing Platform Designer project in Diamond:

1. In Diamond, choose **File > Open > Project**, and navigate to the Lattice Diamond file (.ldf) for the Platform Designer project.

   Diamond loads the file and shows the .ptm file in the File List view.

2. Do one of the following:

   - Click the Platform Designer button on the toolbar or from the Tools menu.

     Platform Designer opens and loads the active .ptm file

   - In the File List view, expand the Input Files folder and double-click the .ptm file that you want to open.

     Platform Designer opens and loads the .ptm file.

See Also

- “Working with Platform Designer Project (.ptm) Files” on page 17

Working with Platform Designer Project (.ptm) Files

The Platform Designer project file (.ptm) holds all of the Analog Sense and Control settings, as well as the logic and port information, for the active implementation. When you create a new Platform Designer project, the .ptm file is generated automatically by Diamond. You can also add a new or existing .ptm file to your project. The project's .ptm files are maintained in the Platform Design Files folder in the File List view for the active implementation, and the active .ptm file in this folder is displayed in bold. Only one .ptm file can be active for an implementation.

To add a new .ptm file to a Platform Designer project:

1. In the File List view of Diamond, right-click the name of the active implementation, and choose **Add > New File**.
2. In the dialog box, select **Source Files** from the Category list, and then select **Platform Designer File**.
3. Type a name for the new .ptm file. If desired, select a different location for the file by clicking the Browse button.
4. Click **New**.

   Diamond loads the new .ptm file and sets it as the active Platform Designer file for the current implementation.

To add an existing .ptm file to a Platform Designer project:

1. In the File List view of Diamond, right-click the name of the active implementation, and choose **Add > Existing File**.
2. In the "Files of type" list, select **Platform Designer Files** from the drop-down menu.
3. Browse to the location of the desired .ptm file, select it, and click **Add**.

   Diamond loads the .ptm file and sets it as the active Platform Designer file for the current implementation.

To change the active/inactive status of a .ptm file:

1. If the .ptm file that you want to make active or inactive is still open in Platform Designer, close it.
2. Right-click the .ptm file and choose the appropriate command: **Set as Inactive** or **Set as Active**.

Opening an Inactive .ptm File Platform Designer allows you to open an inactive .ptm file to examine the configurations. The inactive file will open in read-only mode, which will enable you to examine each view but not allow any changes. Platform Designer will close the active .ptm file, if it is open, before opening the inactive one. It will also prompt you to save any changes. You will not be able to execute any of the operations in the Build view (such as Compile, Generate JEDEC) when viewing an inactive .ptm.

Saving a .ptm File When you save an active .ptm File, Platform Designer takes all of the configuration changes that are in memory and saves them to the .ptm file. When you use the "Save as" command to save the.ptm file with a different name or to a new location, Platform Designer includes all of the collateral files for the implementation, as well as any changes in memory. You can also use the "Save as" command for an opened inactive .ptm file.

See Also ▶"Creating a New Platform Designer Project" on page 15

- "Platform Designer Flow" on page 13

Working with Platform Designer Editors

The Current, Temperature, Voltage, and Ports & Nodes editors in Platform Designer use a format that is very similar to a spreadsheet. The columns for these editors are arranged in the order of the most commonly used settings. For example, in the Voltage editor, the four most commonly used columns—ASC Device, Pins Monitor/Trim, VMON Schematic Net Name, and Nominal Profile 0—are positioned first and are locked from horizontal scrolling so that they are always visible for association with other columns and for easy access. The cells of columns that are locked from horizontal scrolling are colored with a light gray background. Columns for less frequently used settings, such as Window Mode, are positioned further to the right and are not locked from horizontal scrolling. The cells of these columns have a white background.

Platform Designer editors differ in a couple of ways from standard spreadsheet formats. In Platform Designer spreadsheets, when you click a cell to enter a value, you click only once and then choose a selection from the drop-down menu or type a value, depending on the type of cell selected. Because of this, navigating from cell to cell by keyboard is slightly different, and copying or cutting and pasting from multiple cells is not supported. The following sub-topics explain how to use the features of Platform Designer editors.

Sort by Columns You can sort the row order by a single column by clicking the column heading. An up arrow in the heading indicates that the rows are sorted in ascending order. Click the heading again to sort the list in descending order.

In the Voltage, Current, and Temperature editors, you can also sort the rows by multiple columns.

To sort by multiple columns:

1. Choose **View** > **Sort t**o open the Sort by Column(s) dialog box.
2. Select the first column to sort by from the "Sort by" drop-down menu. Click Ascending or Descending to control the order of the sorted rows.
3. Use the "Then by" boxes to select additional columns, as well as the Ascending/Descending option for each column. Click **More** to add more "Then by" menus if needed.

   The rows will be sorted first by the column specified in the "Sort by" box and then by the additional columns in the "Then by" boxes in sequence.
4. Click **OK**.

To return to the default layout:

- Right-click any column heading and choose **Default Layout** option. This returns the sorted order to the original view.

Adjust Column Width You can adjust column widths manually or choose the right-click command to fit the column to the text.

To adjust the column width manually:

- Drag the vertical border on the right of a column heading.

To fit the column width to the text, do one of the following:

- Double-click the vertical border on the right of a column heading.
- Right-click the desired column heading and choose **Fit Column**.
- Choose **View > Column > Fit All Columns** to fit all column widths to the text.

Hide and Re-display Columns You can hide a single column in the Voltage, Current, or Temperature editor or select several columns that you want displayed or hidden.

To hide a single column:

- Right-click the desired column heading and choose **Hide Column**.

To hide several columns:

1. Choose **View > Column > Visible Columns** or press Shift+F5 to open the Visible/Hide Columns dialog box.
2. Do one of the following:
   - In the “Show these Columns list,” select the columns that you want to hide, and then click the single-arrow button to move them to the “Hide these Columns” list.
   - Click the double-arrow button to move all columns to the “Hide these Columns” list, and then select those you want displayed by selecting them and moving them to the “Show these Columns” list.
3. Click **OK**.

To re-display some of the hidden columns:

- Press **Shift+F5**, and move the hidden columns back to the “Show these column(s) list.”

To re-display all columns:

- Press **Shift+F5**, and click the double-arrow button to move all hidden columns to the “Show these column(s)” list.

Edit Cell Values The editable cell values in each editor are color-coded blue or black. Blue indicates a default value, and black indicates an edited value. Values that appear in gray are values that cannot be edited, including tool calculated settings or settings that are implied by other areas of the editor.

To edit a single cell value, click once inside the editable cell and enter or select a new value. In the Voltage editor, you can use the Voltage Monitor and Control dialog box to edit the properties for an entire row. See “Setting Multiple VMON/Trim Properties” on page 26.

You can copy or cut a text entry of a single editable cell and paste it into another cell of the same type. You can do this by using the right-click menus or the standard Ctrl+C, Ctrl+X, and Ctrl+V keyboard shortcuts. Copying and pasting multiple cells is not supported.

Right-click a Text-entry Cell to Open the Complete Menu The right-click menu will sometimes vary for text-entry cells, depending on whether you have single-clicked a cell for editing or have highlighted the entire cell. For example, on the Ports sheet, when you single click a Logical Name cell, the text in the cell is highlighted so that you can type a new label. But if you right-click while only the text is highlighted, the menu will display editing commands such as cut, copy, paste, or delete, but it will not include the Add Group or Show In commands.

To access the complete right-click menu for a text-entry cell:

- Right-click a cell without clicking it to highlight the entire cell.
- If you have already single-clicked the cell, press the Enter key to highlight the entire cell.

Navigate from Cell to Cell Because of the convenient one-click access to parameters in the Current, Temperature, Voltage, and Ports & Nodes editors, navigating by keyboard from cell to cell involves an additional small step.

To enable the navigation capability, do one of the following:

- Select a cell in the ASC Device column or the Pin column by single-clicking it.
- If you have already opened an editable cell by clicking it, press **Enter** to highlight the entire cell. If the cell contains a drop-down menu, you might need to press Enter a second time to enable navigation.

Note

If you have single-clicked an editable cell in one of the columns that are locked from horizontal scrolling, you will only be able to navigate among the cells of the locked columns after you press Enter. To enable full navigation afterward, click a cell in the ASC Device column or Pin column, or click an editable cell in a column that is not locked from horizontal scrolling and press Enter.

You can then use the arrow keys to move up and down the cells of a column or across the cells in a row. You can also use the Tab key and the Shift+Tab combination to move forward and back across a row. When you have reached a targeted cell for editing, single-click the cell. To continue navigating afterward, press the Enter key.

Setting Global Options

For a new Platform Designer project, you would normally begin by using the Global Configuration view to configure those features that affect the entire design. This includes device options for operation mode and externally connected components such as dual-boot SPI flash. It includes ASC global options as well as options for each individual ASC of the target chip set.

See Also ▶"Setting ASC Options" on page 22

- "Setting Device Options" on page 23
- "Configuring a SPI Flash Model" on page 24

Setting ASC Options

The ASC options are divided into global ASC options, which affect the entire project, and specific ASC options that affect only a given ASC. Use the left portion of the ASC Options to set the values for each individual ASC, and use the Global ASC Options on the right to set global ASC values.

Options for Each ASC The following options are available for individual ASCs:

- ASC Name – labels the ASC with a unique name that will identify it globally.
- CLT Rate – sets the closed loop trim update rate, in µs or ms.
- I^{2}C Base Address (ASC0 only) – sets the 4 MSB in the 7-bit I^{2}C address of ASC0. This base 4 MSB is common for all ASCs in the system. This setting is not available for ECP5U/UM based designs. The I^{2}C base address is locked to the default value.
- I^{2}C External Resistor – displays the resistor values that are used by the ASC to set the three LSB of the I^{2}C address. See the ASC data sheet for more details.
- I^{2}C Address – displays the full address of each ASC, using the configured base address and the 3 LSB that are set by the external resistor.
- UES Bits – sets a 32-bit user electronic signature for storing unique data inside the ASC. This setting is not available for ECP5U/UM based designs.
- Reset Type – configures the reset type as mandatory or optional. For ASC0, the reset type is fixed to mandatory. Mandatory ASCs have their reset signals tied together on the board. If one of these ASCs needs to be reset, the whole system is reset. Optional ASCs are handled individually and have a dedicated reset signal.
- Reset Source – displays the port defined in the reset source for an optional reset type.

Global ASC Options The following global options affect all ASCs:

- EIA Resistor Standard – limits the resistor selection to the EIA standard selected or, if Exact is selected, calculates the exact resistor values. This value is used by the TRIM calculator in the voltage editor. It determines which resistor values will be recommended by the calculator.

- Open Resistor Threshold – sets the maximum resistor value above which the resistor is treated as an open circuit. This setting is used by the TRIM calculator.
- DC-DC Options
  - DC-DC Library Directory – sets the location for the DC-DC Library. The default directory location is inside the Diamond installation sub-directories.
  - Build DC-DC Library – opens the DC-DC Library Builder Wizard, which enables you to add or edit a DC-DC Converter model.
- VID Options
  - VID Tables Directory – sets the location for the voltage ID tables. The default directory location is inside the Diamond installation sub-directories.
  - Build VID Tables – opens the VID Table dialog box, which enables you to add or edit a VID table.
- Voltage, Current, and Temperature Options

  The Voltage, Current and Temperature monitors are populated with default trip points each time a new project is started. The ASC Global Options Default Trip Point Selections allow you to change the default trip points for each of the monitor types at the start of a new project.

See Also ▶“Configuring Voltage Identification (VID) Tables” on page 31

- “Defining DC-DC Converter Models” on page 29

Setting Device Options

Select the Device Options tab of the Global Configuration View to configure the operation mode and the external connected components.

Operation Mode Options The Operation Mode section includes the following options:

- Programming Interface:
  - Platform Manager 2 and MachXO2HC/HE, MachXO3D, and MachXO3LF: JTAG or I^{2}C
  - ECP5U/UM: JTAG only.
- Background Programming:
  - Platform Manager 2 and MachXO2HC/HE, MachXO3D, and MachXO3LF: None, I2C, or JTAG.
  - ECP5U/UM – JTAG or SPI (Background Programming Interface to SPI Flash).
- 8MHz Clock Source for Device Operation – ASC0 or Global_Clock

External Connected Components The External Connected Components section includes the following options:

- SPI Models Directory – Select a location for the SPI models directory.
- Build SPI Models – Configure a new SPI model and add it to the SPI Models Directory, or edit or delete an existing SPI model.
- Boot Mode – Normal or Dual Boot. When Dual-Boot is selected, the SPI model option will appear. Dual-boot requires that a SPI flash be specified. ECP5 only supports Normal mode - ECP5 dual boot is configured through Diamond Deployment Tool.
- ASC I^2C Write Feature – This feature allows you to configure the I^2C write access to the ASC. This feature is locked to Enabled in the ECP5 solution.
  - When "Disabled" is selected, it prevents writing to the ASC on-chip registers over the I^2C bus.
  - When "Enabled" is selected, it allows writing to the ASC on-chip registers over the I^2C bus.
  - When "Controlled by ASCx_GPIO1" is selected, the ASCx_GPIO1 input is used to control whether I^2C write access is enabled.
  - FPGA Port (External Connection) – This option appears when "Controlled by ASCx_GPIO1" has been selected. You will need to select the FPGA port that will connect to the GPIO1 on all ASCs. Afterwards, the GPIO1 will be changed to "IN" type for each ASC.

See Also "Defining DC-DC Converter Models" on page 29

- "Configuring a SPI Flash Model" on page 24

Configuring a SPI Flash Model

You can use the Global Configuration View to add and configure a new SPI flash model or edit a current one. The SPI flash models are saved in the SPI Models directory. The default directory location is inside the current project sub-directories.

To configure a SPI flash model:

1. In the Global Configuration View, select the Device Options tab.
2. In the External Connected Components section on the right, do one of the following:
   - Click **Add/Edit SPI Model** in the Value column of SPI Options.
   - If you are using Dual Boot mode, select **Add/Edit SPI Model** from the Dual-Boot SPI Flash pop-up menu in the Value column.

   The SPI Models Configuration dialog box opens and displays the library of currently available SPI models.
3. Do one of the following:
   - To edit an existing SPI model, select it from the list on the left.

- To add a new SPI flash model, click **New**, and then select the newly created model from the list.

4. Optionally, give the selected model a unique name, by single-clicking the name and typing a new one.
5. Select the desired values for the Flash Configurations and Flash Opcodes by double-clicking the value cell and choosing from the menu, and then press enter. Click **Apply** to save one or more selected values or to save all the values for a selected model.
6. If desired, select a different SPI flash model from the list, and repeat Steps 4 and 5.
7. When all options have been set for all the models you are configuring, click **OK**.

See Also
- "Setting ASC Options" on page 22
- "Setting Device Options" on page 23

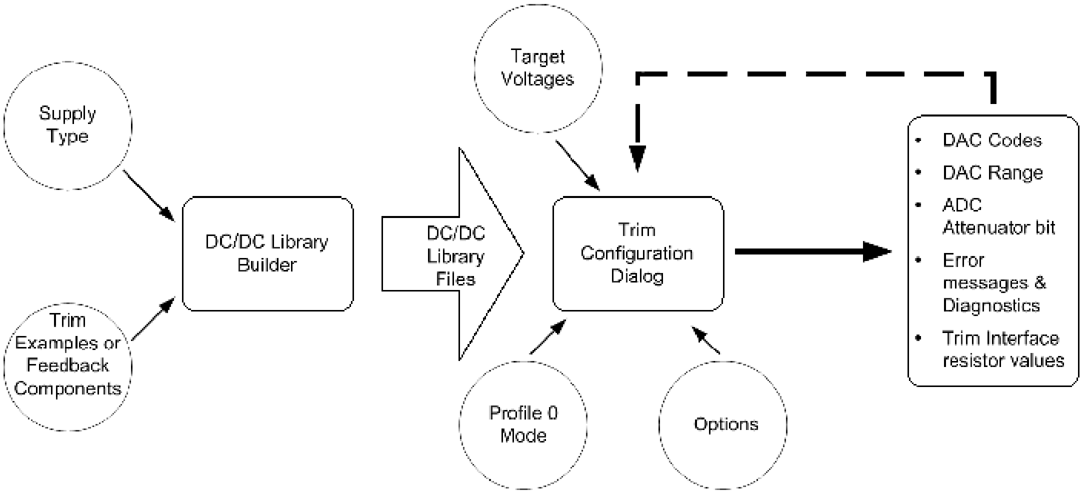
Configuring Voltage Sense (VMON) and Control (TRIM)

The Voltage editor enables you to manage voltages and settings related to voltage monitors (VMONs) and trim channels in the Platform Manager 2 or external ASC devices. You can edit a voltage property by clicking the desired cell on the Voltage spreadsheet, or you can use the Voltage Monitor and Control dialog box to edit multiple properties. Double-clicking a VMON/Trim cell in the Pins Monitor/Trim column opens the Voltage Monitor and Control dialog box. From the Voltage Monitor and Control dialog box, you can access the DC-DC Converter Library and the VID Table library.

Setting up the trim and margin capabilities involves the DC-DC Library Builder, which is used to define the voltage adjustment characteristics of the power supply or supplies that you wish to use. The Trim/Margin portion of the Voltage Monitor and Control dialog box is then used to configure each trim channel for the desired power supplies and output voltages. The following diagram illustrates this flow:

Modifications to existing DC/DC library files must be made from within the DC/DC Library Builder Wizard. The DC-DC Converter selection, as well as changes in the desired target voltages, can be made in the Trim/Margin section of the Voltage Monitor and Control dialog box. It is strongly advised that library files not be modified while trim cells are being configured, because this can create confusion and make it difficult to detect errors in your work. If a "discrete" supply is to be used at several different voltages, a separate library entry for each unique output voltage should be created.

The Trim/Margin dialog enables you to recalculate the trim with a minimum amount of parameter re-entry. Target voltages need to be re-entered only if the desired supply type is changed.



See Also ▶"Defining DC-DC Converter Models" on page 29

▶ "Setting VMON Properties" on page 27

Setting Multiple VMON/Trim Properties

The easiest way to set multiple properties for a selected voltage monitor (VMON) or high-voltage monitor (HVMON) is to use the Voltage Monitor & Control Properties dialog box. The edited settings will then be displayed in the Voltage editor.

To access the Voltage Monitor & Control Properties dialog box:

1. Select the tab in the Voltage editor for those settings that you want to configure.
2. In the Pins Monitor/Trim column, double-click the VMON that you want to configure. Alternatively, right-click and choose **Edit** from the pop-up menu.

   The Voltage Monitor & Control Properties dialog box opens and displays the Voltage, Trim/Margin, or VID section, depending on the tab you selected in the Voltage editor.

The number of tabs available in the Voltage Monitor & Control Properties will depend on whether the selected VMON supports an associated TRIM pin. Most of these properties can also be defined individually on the Voltage spreadsheet.

See Also ▶"Setting VMON Properties" on page 27

▶ "Setting Trim and Margin Properties" on page 28

▶ "Configuring Voltage Sense (VMON) and Control (TRIM)" on page 25

Setting VMON Properties

The Voltage section of the Voltage Monitor & Control Properties dialog box allows you to specify the nominal voltage and the logical names and trip points for each comparator.

- Schematic Net Name – This can consist of any combination of alphanumeric characters.
- Nominal Voltage – This defines both the nominal voltage and the closed loop trim target value for voltage profile 0. If the value is 5.7V or more and the monitor is not an HVMON, the voltage will be used to calculate an external resistor divider and select an associated trip point. A negative voltage will calculate a divider reference as well as the resistor divider. Acceptable values are from -100 volts to 100 volts.
- Logical Name – The logical names, for comparators A and B, are used in the logic builder to control the sequence and equations based on the VMON status.
- Trip Point Selection – A specific VMON trip point, for comparator A and comparator B, is associated with each logical name.
- 64 µs Glitch Filter – When selected, this option configures the comparator so that supply glitches narrower than 64 microseconds are ignored. The output will transition only if the changed status remains active for a period longer than 64 microseconds. If this option is not selected, the comparator output will toggle within 16 microseconds from the time the voltage transitions through the appropriate trip point.
- Window Mode – To use the window mode, the Comparator B threshold should be lower than the threshold setting of comparator A. The window mode output will replace the comparator A output. The window output is logical high if the Comparator B output is high and the Comparator A output is low (i.e., the voltage monitor reading is between Comparator A and Comparator B).
- External Resistor Divider – This section is used for monitoring a voltage whose highest trip point exceeds 5.70V or is a negative voltage. These values are calculated automatically when the nominal voltage specified is negative or exceeds 5.70V. You can overwrite these values to work with your preferred components.
  - Rsupply – Valid value range is 10 ohms to 10 M ohms
  - Rground – Valid value range is 10 ohms to 15 K ohms. The Rground maximum value is restricted to maintain the accuracy of the voltage monitors.
  - Divider Reference – Valid value range is 2.5 V to 6 V. The divider reference is used when monitoring voltages below ground. The external divider is connected between the negative supply being monitored and a positive reference supply.

See Also ▶“Configuring Voltage Sense (VMON) and Control (TRIM)” on page 25

Setting Trim and Margin Properties

The Trim/Margin section of the Voltage Monitor and Control dialog boxenables you to configure the trim cell operating mode and desired output voltages measured at a voltage monitor (VMON).

- Trim Schematic Net Name – This can consist of any combination of alphanumeric characters.
- Trim Configuration Mode – The Trim Calculator, which is selected by default, calculates resistor interface and DAC values from the target voltages and DC-DC converter.

  Manual trim configuration mode allows you to select the CLT loop polarity and to manually enter the DAC code for each voltage profile.
- DC-DC Converter – Select a DC-DC converter model from the drop-down menu. The menu includes all of the models that are in the DC-DC Library. To add a new model, scroll down and select **Add/Edit DC-DC** to open the DC-DC Library Builder Wizard.
- CLT Loop Polarity – If you selected Manual for the trim configuration model, select the polarity for closed loop trim.
- Voltage profile – Enter a desired output voltage for each profile. These profiles are used, along with the nominal voltage profile (profile 0), as the targets for the trim calculator.
- DAC Output Range (BPZ Voltage) – If you are using the Trim Calculator, the bipolar zero output voltage range will be calculated automatically. If you are using manual trim configuration mode, select the value from the drop-down menu.

If you have selected Trim Calculator for the trim configuration mode, click the **Calculate** button after you have made your selections. The dialog box will then provide the following information:

- the resistor values needed to interface the DAC to the TRIM pin in the DC-DC converter
- the voltage that will be achieved with each of the voltage profiles
- the DAC code needed to produce each of the desired output voltages

If a profile target voltage is outside an achievable range, it will be tagged with *Error. To resolve errors, click the **Error Details** button and follow the instructions for obtaining a possible solution.

Setting Trim Configuration Options Use the Trim Configuration Options dialog boxto adjust settings and to help resolve a target voltage error.

Click the **Options** button in the Trim/Margin Properties dialog box to set the following options:

- Maximum DAC Code Range – This setting and the Max Supply Adjustment Range work together to define the sensitivity of the trim system. The value entered defines the DAC value required to trim the supply voltage by the amount specified in the Max Supply Adjustment Range box.

- Max Supply Adjustment Range – This value defines how much the power supply output voltage will change when the DAC code is at the value in the Maximum DAC Code Range box.
- Attenuation Crossover Voltage – If the voltage in Voltage Profile 0 is greater than the voltage in the Attenuation Crossover Voltage text box, the DAC input attenuator will be enabled. The attenuation crossover voltage should be selected so that the attenuation bit is turned on if any portion of the trim range is over 2.048 volts. The default value of 1.9 volts is appropriate in most cases.
- Vbpz Selection – When Auto is selected, the bi-polar zero output voltage is calculated automatically to reach all the target voltages. Selecting one of the other voltages (0.6V, 0.8V, 1V, or 1.25V) can sometimes reduce the number of resistors.

See Also ▶"Configuring Voltage Sense (VMON) and Control (TRIM)" on page 25

Defining DC-DC Converter Models

The DC-DC Library Builder Wizard enables you to define the voltage adjustment characteristics of DC-DC converters and voltage regulators. This information is stored in a library so that any given model of DC-DC converter can be used in multiple trim cells or Platform Designer projects without having to re-enter the information each time.

You can add new DC-DC converter models to the library, delete models, or edit the parameters of a model at any time by launching the wizard. Any converter model in the library can be selected in the Trim/Margin portion of the Voltage Monitor and Control dialog box.

You can launch the DC-DC Library Builder Wizard from the Global Configuration view or from the Voltage Monitor and Control dialog box.

To launch the DC-DC Library Builder Wizard from the Global Configuration View:

1. In the Global Configuration view, select the ASC Options tab.
2. In the DC-DC Options section of Global ASC Options, click **Add/Edit DC-DC**.

To launch the DC-DC Library Builder Wizard from the Voltage Monitor and Control dialog box:

1. In the Voltage view, select the Trim/Margin tab.
2. Double-click a cell in the DC-DC Converter column or a VMON/Trim cell in the Pins Monitor/Trim column.
3. In the Voltage Monitor and Control dialog box, click the DC-DC Converter drop-down menu.
4. Scroll down and choose **Add/Edit DC-DC**.

The DC-DC Library Builder Wizard provides the option of creating a new entry in the library (using the New button) or modifying an existing entry. The flow for both operations is similar, the only exception being that when an existing entry is being edited, the previously saved parameters appear in the different dialog box sections of the Wizard.

To define a DC-DC converter model:

1. In the DC-DC Converter Model Selection, select a model from the list, or click **New** to add a new model.

   The Library Builder classifies all DC-DC converters and regulators into four different families:

   - Supplies that can be adjusted up or down a few percent about a nominal voltage by connecting a resistor between the supply's TRIM pin and its output or ground.
   - Supplies that can be adjusted over a wide range by connecting a resistor between the supply's TRIM pin and ground.
   - Supplies that can be adjusted over a wide range by connecting a resistor between the supply’s TRIM pin and Vout.
   - Supplies that use an external feedback network. The Library Builder calls this a “discrete” implementation.

2. Click **Next** to open the Select the type of DC-DC Converter section.
3. Select the type of DC-DC Converter and click **Next**.

   The wizard opens the configuration section of the dialog box, which enables you to set the parameters for the type of converter you selected.

   For the Trim-up Trim-down supply type and the Programmable supply type, the dialog box asks for several trimming examples to be entered, and the supply's adjustment characteristics are determined from the data. Many power supply data sheets provide tables of resistor values needed to achieve various different outputs. These examples can be entered directly into the dialog box.

   For discrete implementation types, the dialog box requests the values of the feedback network components and the internal reference voltage. From the data, the supply's adjustment characteristics are determined. When a specific model of voltage regulator will be used several times to produce different voltages, separate library entries will be needed for each unique set of feedback network components.

4. After setting the configuration parameters, click **Finish**.

See Also ▶“Setting Multiple VMON/Trim Properties” on page 26

- “Setting VMON Properties” on page 27
- “Setting Trim and Margin Properties” on page 28

Configuring Voltage Identification (VID) Tables

Voltage identification tables define the target voltage outputs of a DC-DC converter based on inputs of a selected bus. The VID section of the Voltage Monitor and Control dialog box enables you to select and configure a VID table for the selected voltage monitor. If your design does not yet contain VID tables, you can build them and add them to the VID Table Library.

Building VID Tables The Voltage – VID Table Library interface enables you to build a library of voltage identification tables. By default, Platform Designer stores the VID tables inside the Diamond installation sub-directories. You can specify a different location in the Global ASC Options section of the Global Configuration View.

To create a new VID table:

1. In the Voltage editor, open the VID Table library dialog box by using one of the following methods:

   - Open the Voltage Monitor & Control Properties dialog box by double-clicking the VMON/TRIM cell. Select the VID tab, and choose **Add / Edit a table** from the VID Lookup Table drop-down menu.

   - In the Global Configuration View, select the ASC Options tab. In the VID Options section on the right, click **Add / Edit a table**.

2. In the VID Table Library dialog box, click **New** to open the Create New VID Table dialog box.

3. Type a name for the VID table in the text box, and then select the table size from the drop-down menu.

4. In the Auto fill section, specify a voltage starting value and step size.

   Alternatively, you can manually enter each value in the table by double-clicking each Voltage (V) cell and typing a value. If you choose manual entry, skip Step 5.

5. Select either the Top Down or Bottom Up option, and then click **Fill**.

   Platform Designer fills in the voltage for each VID value, based on the step size and starting value. You can edit any of these values as desired.

6. Click **OK**.

   The new VID table is added to the VID Library and will be listed in the VID Table menu in the Voltage editor and in the Voltage Monitor & Control Properties dialog box.

Selecting and Configuring the VID Table The VID page of the Voltage editor enables you to select the VID lookup table from the VID Table Library and select the bus, strobe port or node, and VID strobe edge. You can also select and configure the VID table from the Voltage Monitor & Control dialog box.

Editing a VID Table To edit a VID Table, open the VID Table library dialog box by using any of the methods described in Step 1. Select a VID table and click **Edit**. In the Edit the VID Table dialog box, change the settings as desired and click **OK**.

See Also "Configuring Voltage Sense (VMON) and Control (TRIM)" on page 25

Configuring Current Sense (IMON)

The Current editor allows you to set parameters for the current monitor (IMON) and high-voltage current monitor (HIMON) for each Analog Sense and Control device. Each monitor includes settings for two precision comparators (A and B) and one fast (F) comparator.

- Schematic Net Name – Each IMON or HIMON must be identified by a unique name. The name can consist of any combination of alphanumeric characters.
- Logical Name – The monitor's comparator outputs A, B, and F must each be identified by a unique name. The name can consist of any combination of alphanumeric characters.
- Sense Resistor (Ohm) – The sense resistor value will be the same for all comparators within the monitor and can range from .0001 to 1000000.0 ohms.
- Trip Point Selection (Amps) – The selected trip point, for comparators A, B, and F, will be associated with each logical name. The trip points available are determined by the Sense Resistor value.
- Hysteresis – Hysteresis can be enabled or disabled for comparators A and B. This automatically updates the available trip point selections.
- Glitch Filter (μ) – The glitch filter can be enabled or bypassed for comparators A and B. When Yes is selected, this option configures the comparators so that supply glitches narrower than 64 microseconds are ignored.
- Window Mode – Window mode can be used for comparators A and B. To use the window mode, the Comparator B threshold should be lower than the threshold setting of comparator A. The window mode output will replace the comparator A output. The window output is logical high if the Comparator B output is high and the Comparator A output is Low.
- Low Side Sense – When Yes is selected, this sets the low voltage side sense for comparators A, B, and F. It is not available for high-voltage sense monitors.

The Programmable Gain Amplifier (PGA) Gain setting is displayed by the tool based on the selected trip points. This information is used when performing A/D measurements of the current over I^2C.

The V-Drop (V) and Peak Power (W) are calculated based on the values entered for trip point and sense resistor.

See Also

- "Configuring Voltage Sense (VMON) and Control (TRIM)" on page 25

Configuring Temperature Sense (TMON)

The Temperature editor allows you to set parameters for the external temperature sensor interfaces (TMON1, TMON2, etc) and the internal temperature sensor (TMON_Int). The temperature monitor function includes an A/D converter measurement with averaging support, as well as an alarm monitor function with programmable hysteresis and filtering. Each TMON channel includes two separate programmable comparison points. The temperature sensor hardware also supports a configurable offset and ideality factor. The parameters for each temperature monitor comparator can be set in Platform Designer's Temperature editor, as follows:

- Schematic Net Name – The schematic net name must be unique and can consist of any combination of alphanumeric characters.
- Logical Name – This must be a unique name that will identify each TMON pin and comparator output. It can consist of any combination of alphanumeric characters.
- Monitoring Type – Over temperature (OT) or under temperature (UT) monitoring can be selected.
- Trip Point Selection – This sets the trip point for the comparator in degrees Celsius.
- Hysteresis – This defines the hysteresis for updating the trip point output for the comparator.
- Monitor Alarm Filter (Depth) – This sets the number of consecutive alarms that must be detected before setting the comparator output high.
- Measurement Averaging (Filter Coefficient) – This sets the coefficient on the averaging filter implemented on the temperature sensing of the TMON.
- Offset – This calibration value is used to correct the temperature reading, in degrees Celsius for the TMON.
- Short Fault Measurement Reading – This defines the measurement reading under a short fault condition. It implies the Open fault measurement reading as well. See the Platform Manager 2, MachXO2HC/HE, MachXO3D, or MachXO3LF data sheet for more details.
- Ideality Factor – This calibration value is used to correct the diode imperfection for the TMON.
- Sensor Configuration – The external temperature monitors can be configured to interface with several different transistor circuits.

See Also ▶"Configuring Fan Control" on page 34

- "Configuring Voltage Sense (VMON) and Control (TRIM)" on page 25

Configuring Fan Control

Platform Designer's Fan Controller provides fan control for 2-wire, 3-wire, or 4-wire fans. The fan controller supports multiple fan speeds, under-speed alarm detection, and a configurable startup pulse. It enables you to set three levels of speed control through the pulse width modulated (PWM) signal. Up to 18 separate fans can be controlled.

To configure fan control:

1. Select **Fan Controller** from the menu pane, and then select a fan in the "Fan in System" list or add a new fan by clicking the add button ➕ on the lower left.
2. In the Type Setting section on the Parameters page, select the fan type from the drop-down menu.
3. If you selected 3 Wire (Low Side Drive), 3 Wire (High Side Drive), or 4 Wire, also specify the **Sense Type** for alarm detection, as follows:
   - If the fan supports a locked signal as fan feedback to indicate that the fan is locked or stuck, select **Alarm (Active High)** or **Alarm (Active Low)**.
   - If the fan includes a tachometer feedback signal, select **Tach** (2 Pulses/Rev), and then do the following:
     - In the Alarm Interval box, type a value for the number of ms that will be allowed between pulses before an under-speed violation is registered.
     - Select a value between 1 and 10 from the Alarm Filter Count. This is the number of times the alarm interval must be detected before the Alarm signal will be asserted.

     With tachometer feedback, a +/- 10% hysteresis will be applied to the corresponding assertion/de-assertion of the failure count to prevent a false alarm.
4. In the PWM Setting section, use the sliders to select a duty cycle percentage for Speed3, Speed2, and Speed1.

   Each can be set in 5% increments, ranging from 5% to 95%. The fastest speed must be assigned to Speed3, with the middle speed assigned to Speed2, and the slowest speed assigned to Speed1.
5. Use the slider to specify the PWM frequency. The frequency can be set in increments of 0.8 kHz, up to 80.0 kHz.
6. Select the polarity for the PWM signal, based on the nature of the MOSFET switch and on-board buffers.

   Refer to the fan data sheet and the board requirements for information about the correct setting of PWM polarity.
7. Optionally, enable the Startup Control and select the pulse duration, in increments of .25s for the startup period.

   When startup control is enabled, the fan controller will send a kickstart pulse of the chosen duration to the fan before switching to the selected PWM setting.

8. Select the InterConnections tab.

   The InterConnections page allows you to specify the signals that the Platform Designer will use as fan controller ports. Each fan has an independent set of interconnections.

   The PWM Out and Tach/Alarm Sense are the external connections to the fan. The other signals (Speed Sel 1 ... Alarm Out) are logical connections that set the operation of the fan controller during runtime.

9. Assign the PWM Out and Tach/Alarm Sense to external ports by dragging the desired ports from the Signal Pool.

10. Drag the desired signals from the Signal Pool to set the logical connections for Speed Sel, Run Off, Run Full, and Alarm Out.

See Also ▶“Configuring Temperature Sense (TMON)” on page 33

▶ “Configuring Voltage Sense (VMON) and Control (TRIM)” on page 25

Setting Fault Logging Options

The Fault Logger, available from the Components section of the menu pane, enables you to specify and configure fault conditions that are logged to non-volatile memory. You have the option of using standard fault logging that is based on voltage, current, and temperature status; or using the full-featured fault logging. By default, fault logging is disabled.

Each ASC device contains a block of EEPROM memory that can be used for either the V, I, T Fault Log or for User Tag Operation. The User Tag Memory is enabled automatically when fault logging is disabled or when full-featured fault logging is selected. It is disabled when V, I, T fault logging is selected.

V, I, T Fault Logging When you select this option, the Analog Sense and Control device will log the voltage (V), current (I), and temperature (T) status when a fault is detected. The V, I, T fault log supports the logging of 8 signals per Analog Sense and Control device, in addition to the V, I, T signals. These can be digital I/O or other signals.

To configure V, I, T fault logging:

1. In the Fault Logger, select **Enable V, I, T Fault Log** from the options shown at the top left.

2. Select a signal name from the Fault Logging Trigger Signal Name drop-down menu. This signal can be an output from the user logic, an external digital I/O, or a specific monitor alarm signal.

3. In the “Basic Configuration” section, select the type of memory to log to: EEPROM or SRAM. The EEPROM is non-volatile, but a log takes longer to execute. The SRAM memory is volatile but is executed more quickly.

4. The V, I, T fault log supports the logging of 8 signals per Analog Sense and Control device in addition to the V, I, T signals. These can be digital I/O or other signals. For each signal that you want to log, drag it from the “User Signals to Log” list over to a D cell of the desired ASC.

Full-Featured Fault Logging The full-featured fault logging uses either the UFM Flash memory within the device or an external SPI flash memory. Full-featured fault logging is available for Platform Manager 2 LPTM21 devices and for MachXO2HC/HE devices of 1200 and above, MachXO3D, and MachXO3LF devices. ECP5U/UM device support full-featured fault logging with external SPI flash memory only - UFM is not available in ECP5U/UM.

To configure full-featured fault logging (Platform Manager 2, MachXO2HC/HE, MachXO3D, and MachXO3LF only):

1. In the Fault Logger, select **Enable Full-Featured Fault Log** from the options shown at the top left.
2. Select a signal name from the Fault Logging Trigger Signal Name drop-down menu. This signal can be an output from the user logic, an external digital I/O, or a specific monitor alarm signal.
3. n the “Basic Configuration” section, do the following:
   a. From the drop-down menu, select the contiguous ASCs that you want logged.
   b. Select **Include Timestamp** if you want Platform Designer to include a 32-bit timestamp timer.
   c. Select a signal to be used as the busy signal name from the “Busy” Signal Name menu. This signal is an output from the fault logger and can be used to inform the user logic that a fault log recording is in progress.
   d. Select a “Log to” option: the on-chip UFM memory or external SPI flash.
   e. If you selected External SPI Flash as the “Log to” option, use the Model drop-down menu to select the external flash model to be used for fault logging.
4. In the User Log Fields menu, located above the user log table on the right, select the number of additional bits to record in the fault log.
5. For each additional signal that you want to log, drag it from the “User Signals to Log” list over to a D cell of the desired user log column.

To configure full-featured fault logging (ECP5U/UM only):

1. In the Fault Logger, select **Enable Full-Featured Fault Log** from the options shown at the top left.
2. Select a signal name from the Fault Logging Trigger Signal Name drop-down menu. This signal can be an output from the user logic, an external digital I/O, or a specific monitor alarm signal.

   Select a signal to be used as the busy signal name from the “Busy” Signal Name menu. This signal is an output from the fault logger and can be used to inform the user logic that a fault log recording is in progress.
3. In the “Basic Configuration” section, do the following:
   a. From the drop-down menu, select the contiguous ASCs that you want logged.

   b. Select either Disable Time Stamp, Internally Generated Time Stamp, or Externally Assigned Time Stamp. The internally generated timestamp option includes the 1s per bit, 32-bit timestamp. The externally assigned timestamp option will automatically update the Nodes view to include a 32-bit node group, called FL_Timestamp, which can be assigned by the user based on an external, highly accurate timestamp.

   c. In SPI Memory Configuration, select Log to Configuration SPI Memory or Log to Alternate SPI Memory.

   d. Use the Model drop-down menu to select the external flash model to be used for fault logging.

4. In the User Log Fields menu, located above the user log table on the right, select the number of additional bits to record in the fault log.

5. For each additional signal that you want to log, drag it from the “User Signals to Log” list over to a D cell of the desired user log column.

6. In the “Fault Log Memory Space” section, do the following:

   a. Enter the Start Address. This is a Hex input used by the IP to determine the starting address available to the fault logger. This setting allows the user to share the SPI memory with multiple boot images or other information. The default address is 0x030000.

   b. Enter the size in K Bytes.

   c. The End Address is automatically calculated and displayed by Platform Designer. The displayed value confirms for the user that it is safe to share the SPI memory with multiple boot images or other information.

7. The full-featured fault logger automatically adds a 16-bit node group called FL_Record_Counter to the nodes view. This nodes group can be connected to user logic to provide the number of Fault Records currently stored in memory.

See Also ▶“Configuring a SPI Flash Model” on page 24

Configuring Hot Swap

(Platform Manager 2. MachXO2HC/HE, MachXO3D, and MachXO3LF only.) Platform Designer's Hot Swap utility enables you to configure a hot swap component that will control the in-rush current in applications where power is rapidly applied, such as a circuit board that is plugged into a backplane. The Hot Swap utility contains a separate page for each of the following three tasks:

- Hot Swap – Specify the settings of a hot swap component.
- Interface – Connect the hot swap component to the Platform Manager 2 resources.
- InterConnections – Connect the hot swap component to the hardware management logic.

To specify the settings of a hot swap component:

1. Select **Hot Swap** from the Components section of the menu pane.
2. On the Hot Swap page, select a hot swap component from the list or create a new hot swap component by clicking the add button ➕ on the lower left.
3. Specify the desired options and settings:
   - Input Supply
     - V_{IN} – Input voltage. This is the supply voltage input, which is used to charge C_{LOAD}. Together with I_{MAX}, C_{LOAD} and the MOSFET SOA (Safe Operating Area) information will be used to calculate the hot swap parameters, including the number of phases, voltage and current trip points.
     - I_{MAX} – Maximum current available from the input supply.
   - MOSFET Parameters
     - Load/Supply – Allows you to place the MOSFET at either the Supply or the Load. Select the setting that matches your application.
     - MOSFET Name – Used, for informational purposes only, to track the part number of the MOSFET in your application.
     - V1/A1 – Voltage/Current data point pair from the MOSFET SOA curve found in the MOSFET datasheet.
     - V2/A2 – Voltage/Current data point pair from the MOSFET SOA curve. V1 must be greater than V2, and A1 must be less than A2.
   - Current Sensing Configuration
     - R_S – Sense Resistor used in the application. Platform Designer uses this sense resistor value to calculate available current sensing trip points.
     - Current Sense Amp choices – Determines the current sense amp circuit used in the application.

       The choice among “External and VMON,” “External and IMON,” and “IMON (Internal)” will determine whether additional current sensing circuit information is required. The choice also determines which monitor circuits are available for assignment in the Interface tab. Certain configurations of V_{IN} and Current Sense Amp are prohibited, such as using IMON (Internal) with V_{IN} voltages above 13.2V.
     - Low Side option – Determines whether the IMON is used in a near ground hot swap application (such as -48V). Selecting this option enables the Low-Side Sense feature in the IMON circuit.
   - Hot Swap Settings
     - C_{LOAD} – The load capacitor charged up during the hot swap operation. This value is used to calculate the hot swap parameters, including the number of phases and the voltage and current trip points.

- Fast Shutdown Limit – Sets the current limit for fast shutdown during hot swap. The menu is automatically populated with available current limit trip points related to the Sense Resistor and Current Sense Amp settings. If the current exceeds the selected limit during hot swap, the hot swap will be aborted and the over current error signal will be asserted. This feature can be disabled by selecting "None."
- Cooldown Period – The period used by the hot swap algorithm to ensure that the MOSFET does not overheat. Each time the hot swap algorithm detects a timeout, remaining in a phase longer than 10 ms, the cooldown period will be used as a wait time prior to resuming the hot swap operation.
- Hot Swap Name – A user-defined name for the hot swap setup.

4. After all the parameters have been selected, click the **Calculate** button.

   The V_{LOAD} and I_D graphs are updated with the estimated Voltage and current profiles based on the calculated Hot Swap algorithm and settings. The Results/Comments area is updated with information, including the number of hot swap phases and the number of VMON and IMON channels required to support the hot swap implementation.

   The hot swap calculation might not be able to provide a solution for all circuit configurations. In this case, error information is displayed in the Diamond message console.

5. If the results are not satisfactory, adjust the settings and calculate again.

To connect the hot swap component to Platform Manager 2 resources:

1. After you are satisfied with the hot swap calculation results, select the **Interface** tab.

   The Interface page consists of several menus that are used to assign VMONs, IMONs, HVOUT, GPIO and PIO channels to the different hot swap functions. When you assign VMON, IMON, and HVOUT channels in the Interface tab, their settings, such as trip point thresholds, will be updated automatically.

2. Select the desired setting from each of the drop-down menus in the gold-colored boxes, as follows:

   - V_{IN} Monitor – Associates a VMON channel with the input voltage monitoring function of a given hot swap. This VMON channel can be re-used across multiple hot swap components, if they use the same input voltage. The V_{IN} Monitor can be from any ASC in the Platform Manager 2 system.

     Selecting a V_{IN} Monitor is mandatory.

   - ASC – Specifies the ASC device to be used. The ASC menu is automatically populated with the ASCs used in the system. All channels from the drop-down menus inside the pink rectangle will be selected from the chosen ASC.

- MOSFET/Charge Pump Driver – Associates an HVOUT or GPIO with the controlled output signal used in the hot swap algorithm.

  Selecting an HVOUT or GPIO is mandatory.

- Current Sensing Monitor – Specifies the IMON or VMON channel for current sensing. The channels available are those that support the configurations that were set on the Hot Swap page.

  Selecting a current sensing monitor is mandatory.

- Fast Current Sense Monitor – Specifies an IMON or VMON channel for fast current sense. This menu is used only when a fast shutdown limit is selected on the Hot Swap page. It is used in conjunction with the fast current sense output, fast path input, and fast shutdown signal.

- Fast Current Sense Output – Specifies an HVOUT or GPIO as a fast output signal. This menu is populated with the output signals available on the ASC.

- Fast Path Input – Specifies a signal for fast path input. This menu is populated with the PIO signals from the FPGA I/O used in the Platform Manager 2 system. The signal should be externally connected to the fast current sense output signal in the application.

- Fast Shut Down Output – Specifies a signal for fast shutdown output. This menu is populated with the PIO signals from the FPGA I/O used in the Platform Manager 2 system. The signal is controlled by the hot swap IP and will perform a fast shutdown of the MOSFET when necessary.

- Load Voltage Monitor(s) – Specifies the load VMON or HVMON. This menu is populated with the voltage monitor channels from all ASCs in the Platform Manager 2 system. The number of drop-down menus available is determined by the number of phases required by the hot swap algorithm. These menus can be filled with voltage monitor channels from any ASC in the system.

  Selecting a load voltage monitor from each available menu is mandatory.

To connect the hot swap component to the hardware management logic:

1. Select the **Interconnections** tab.

   The Interconnections page includes a set of control signals that are used to connect the hot swap component to the hardware management logic. Each of these signals is typically assigned to a node.

2. Drag the desired signal from the Signal Pool over to the appropriate box, as follows:

   - Hot Swap Enable – Input signal to the hot swap component. Asserting this signal high will start the hot swap operation.

   - Over-Current Clear – Input signal to the hot swap component. This signal needs to be asserted to clear any existing Over-Current Error status.

- Hot Swap Done – Output signal from the hot swap component. This signal is asserted by the hot swap component to inform the hardware management logic that the hot swap operation was successfully completed. This signal is cleared when the hot swap enable signal is asserted again.
- Hot Swap Error – Output signal from the hot swap component. This signal is asserted by the hot swap component to inform the hardware management logic that an error occurred during the hot swap operation. This signal is cleared when the hot swap enable signal is asserted again.
- Over-Current Error – Output signal from the hot swap component. This signal is asserted by the hot swap component to inform the hardware management logic that an overcurrent error occurred during the hot swap operation. This is in addition to the fast path shutdown behavior. This signal will be cleared when the over-current clear signal is asserted.

Configuring PMBus Adapter

(Platform Manager 2, MachXO2HC/HE, MachXO3D, and MachXO3LF only.) PMBus is a serial communication bus that allows a microcontroller to configure and monitor Digital Point of Load (DPOL) DC-DC Converters. The PMBus Adapter allows the connection of analog POLs to the PMBus controller using the FPGA and ASC. Multiple POLs may be mapped to different pages configured in the PMBUS adapter. Dedicated pages for voltage, current, and temperature monitoring are provided.

The PMBus adapter supports Packet Error Checking and SMBAlert options. The PMBus adapter supports a pre-defined subset of PMBus commands.

To configure PMBus Adapter:

- In the PMBus Adapter tab, select **Enable PMBus Adapter** at the top left.

  The PMBus tab contains controls and the ASC Page Mapping table control. When **Enable PMBus Adapter** is checked, controls and the related PMBus Nodes tab are enabled. To view PMBus ports and nodes, refer to "Viewing PMBus Ports and Nodes (Platform Manager 2, MachXO2HC/HE, MachXO3D, and MachXO3LF Only)" on page 43.

The following options are available to configure PMBus Adapter:

Enable packet Error Checking (PEC) Enables/disables the packet error checking option.

Enable SMBAlert Enables/disables the SMBAlert output pin..

PMBus Bus Speed Specifies PMBus bus speed. The two available values are 100KHz and 400KHz.

PMBus Slave Address Specifies PMBus slave address. Only legal slave addresses are selectable from the drop-down list.

ASC Page Mapping Specifies the PMBus page mapping of voltage monitors (VMONs), Current Monitors (IMONs) and Temperature Monitors (TMONs) of the ASC devices in the design. The resource list view on the left contains the VMON , IMONs, and TMON signals that are part of the current design. The user can drag and drop the VMON. IMON, and TMON signals from the resource list view and assign them to PMBus pages on the right.

VMON, IMON, and TMON signals can be assigned to page numbers as follows:

- VMON - 0x00-0x2F
- IMON - 0x30-0x3F
- TMON - 0x40-0x5F

The default values on the ASC page mapping table views is None. When the user drags the VMON, IMON, or TMON signals from the resource list on the left and drops it in the table view, a dynamic design rule check (DRC) is performed in the background to verify whether the assigned page is valid or conflicts with already assigned pages.

Implementing the Platform Management Algorithm

Implementing the platform management algorithm involves labeling and configuring ports and nodes, and then building logic instructions based on these configurations. In Platform Designer, it involves the use of the Ports & Nodes editor and the Logic editor.

See Also ▶“Designing Control Sequences” on page 49

Configuring and Viewing Ports and Nodes

Use the Ports & Nodes editor to view internal nodes and configure external signals (ports) of the Platform Manager 2, MachXO3D, MachXO2HC/HE, MachXO3LF, ECP5U/UM device; configure and label the ASC-based general-purpose I/Os; view PMBus Ports and Nodes; and label and configure the high-voltage output ports. You can build control logic based on the labels you apply.

See Also ▶“Designing Control Sequences” on page 49

Configuring Ports

The Ports section of the Ports & Nodes editor shows all physical FPGA-based PIOs that are available for use as external connections to the design.

You can assign a user label to a logical port. A port requires a type: IN, OUT, INOUT or GRESET. The port also includes attributes for group, register type and reset level.

For register type, in addition to Registered or Combinatorial, you have the option of using “Registered Sync with ASC.” The MachXO2HC/HE, MachXO3D, MachXO3LF, ECP5U/UM device output is much faster than the ASC output because of the 3-wire interface propagation delay. So when you select the “Registered Sync with ASC” option, Platform Designer will add a delay for MachXO2HC/HE outputs to make sure that they are triggered in the same step.

After the design is compiled, you can cross-probe from the Ports sheet to Diamond’s Spreadsheet View or Netlist View to make pin assignments. Right-click a cell and choose **Show In > Spreadsheet View** or **Show In > Netlist View**.

Viewing PMBus Ports and Nodes (Platform Manager 2, MachXO2HC/HE, MachXO3D, and MachXO3LF Only)

The PMBus tab is enabled only if the PMBus Adapter is enabled. For information on enabling PMBus Adapter, refer to “Configuring PMBus Adapter” on page 41.

The PMbus tab lists all of the available PMBus ports/nodes that can be connected to the Logic Controls, including Sequence, Supervisory equation, and HDL Import. These nodes are managed in the user logic in order to complete the configurable PMBUS support.

The PMBus ports/nodes table view includes three read-only columns:

Logical Name/Function The node names listed in this column are the nodes that are added to the user signal pool and which connect the logic to the PMBus Adapter for support of PMBus commands..

Grouped By This column lists the PMBus status word or byte name with the correct bit index. Nodes that are not used are set to zero.

Logic Connection This column shows the node direction with respect to the user logic; In goes into the user logic and Out is driven from the user logic.

See Also ▶“Creating a Port Group” on page 43

▶ “Designing Control Sequences” on page 49

▶ “Working with Platform Designer Editors” on page 19

Creating a Port Group

The group feature allows you to combine ports of a common type, using vector notation, to form a bus. The selected ports cannot be shared among multiple groups.

To create a port group:

1. On the Ports sheet or the Nodes sheet, right-click any cell of a port or node that is not already part of a group and choose **Add Group** from the pop-up menu.
2. In the New Group dialog box, type a name for the group in the Group Name text box.
3. From the Available Ports list, select the ports that you want to include in the group, and then click the > button to place the ports in the Selected Ports list.
4. Click **Add**.

To modify a port group:

1. Right-click a cell in the Group By column that references the port group you want to edit and choose **Modify Group** from the pop-up menu.
2. In the Modify Group dialog box, use the appropriate buttons to add ports to the Selected Ports list or remove them from the list.
3. Click **Update**.

To remove a port group:

- Right-click any cell and choose **Remove Group**. From the sub-menu, select the group you want to remove.

See Also

- "Designing Control Sequences" on page 49
- "Working with Platform Designer Editors" on page 19

Configuring Nodes

The Nodes sheet enables you to add and configure internal nodes in your design. You can assign user labels to new and existing nodes and select the register type and reset level attributes.

To add a node:

1. Press the Insert key, or right click an existing node and choose **ADD NODE**.
2. Assign a unique name to the node and select the Register Type and Reset Level.

To delete one or more nodes:

- Highlight the rows you want to delete by selecting the row numbers in the first column, and then press the Delete key. Alternatively, right-click and choose **REMOVE NODE(s)**.

Nodes can also be grouped, following the same process as described in "Creating a Port Group" on page 43.

Some nodes are automatically allocated to the component logic or other features such as fault log enable and timers.

See Also

- "Designing Control Sequences" on page 49
- "Working with Platform Designer Editors" on page 19

Configuring General-Purpose I/Os

The GPIO sheet allows you to enable and assign a user label to an ASC-based general purpose I/O.

For each GPIO pin, you can specify the following:

- A unique name to identify the pin.
- The type: IN or OUT
- Reset Level: Set High or Set Low

For pins GPIO2 and GPIO3 of each ASC, you can also select the following:

- Source
- Polarity: True or Inverted

See Also

- "Designing Control Sequences" on page 49

Configuring High-Voltage Outputs

The HV Outputs sheet allows you to enable and assign a user label to a high-voltage output port.

For each HVOUT pin, you can specify the following:

- A unique logical name to identify the HVOUT pin.
- The output setting: Charge Pump or Open Drain
- The target voltage for the output (Charge Pump mode only)
- The source current in micro-amps for the output (Charge Pump mode only)
- The sink current in micro-amps for the output (Charge Pump mode only)
- The output mode: Static or Switched
- The selected frequency for the ouput in kHz (Switched mode only)
- The duty cycle for the output (Switched output mode only)
- The output source
- The output polarity: True or Inverted
- A high or low reset level

Designing with the Logic Editor

Included with the Lattice Diamond Platform Designer is the LogiBuilder™ Logic editor, which enables you to define a power supply sequence controller and monitor or other control circuits for implementing the platform management algorithm. The tools include a set of instructions for building the sequence based on conditional events and timer delays.

See Also

- "Designing Control Sequences" on page 49
- "Sequence Controller Instruction Set" on page 47

About the Logic Editor

The Logic editor simplifies the design process by allowing you to select from menus instead of writing complex code. It enables you to add and configure timers and import HDL modules. It also supports vector notation for bus structures.

After entering the set of instructions, you can compile the design and simulate the sequence or control events. When the design is compiled, synthesizable HDL code is generated based on the sequencer and supervisory logic.

- "Designing Control Sequences" on page 49
- "Sequence Controller Instruction Set" on page 47

Logic Editor User Interface

The LogiBuilder Logic editor includes separate views for building the logic instructions and exceptions, entering supervisory equations, and defining timers. An additional view is provided that allows you to import HDL modules into your design.

- Sequence – The Sequence view enables you to define the step-by-step instructions for controlling outputs for a selected state machine. When compiled, sequencer instructions implement a digital logic state machine within the PLD core.
    - Exceptions – The Exceptions section allows you to define equations that will trigger sequence controller exceptions to modify outputs and jump out to an alternative sequence step. Exceptions can be selectively applied to any sequencer step. When compiled, exception instructions are merged with the digital logic state machine of the PLD core.
    - State Machine – A tab for each state machine is shown at the bottom of the Sequence view, which allows you to select the active state machine for editing. You can also add a new state machine by clicking the **+** tab. Right-click a state machine tab to open the Multiple State Machine dialog box, which enables you to add and delete state machines.

- Supervisory – The Supervisory view enables you to define combinatorial and registered logic independent of the sequencer control logic. When compiled, supervisory equations are concurrent to the digital logic state machine of the PLD core.
- Timers – The Timers view enables you to define timers for control sequences. To add a new timer, press the Insert key or click the **Add** button.
- Imported HDL – The Imported HDL view enables you to add HDL modules from HDL source that is included in the design project.

See Also ▶"Designing Control Sequences" on page 49

- "Managing Multiple Control Sequences" on page 50.
- "Entering Supervisory Equations" on page 54
- "Defining Timers" on page 50
- "Sequence Controller Instruction Set" on page 47

Sequence Controller Instruction Set

The LogiBuilder Logic editor of Platform Designer provides the following instructions for designing control sequences:

BEGIN STARTUP SEQUENCE The BEGIN STARTUP SEQUENCE instruction signals to LogiBuilder that any instructions past this point may be interrupted by jumps specified in exceptions. This instruction may be deleted from a sequence, but not inserted.

OUTPUT The OUTPUT instruction is used to turn on or turn off the output signals. A single OUTPUT instruction can be used to simultaneously change the status of any number of output signals.

WAIT FOR <Boolean Expression> The WAIT FOR <Boolean expression> instruction suspends execution of the sequence until the specified expression becomes TRUE. Outputs can be assigned in this instruction. These outputs are asserted as soon as the sequencer enters the instruction.

WAIT FOR <Boolean Expression> with Timeout The WAIT FOR <Boolean expression> with Timeout instruction suspends execution of the sequence until the specified expression becomes TRUE or the selected timer expires. The timer is started when the sequence enters the instruction.

WAIT FOR <timeout> The WAIT FOR <timeout> instruction is used to specify a fixed delay in the execution sequence. The value of <timeout> is determined by which timer is specified. (The timer must first be configured on the Timers page).

IF <Boolean Expression> THEN GOTO <step x> ELSE GOTO <step y> The If/Then/Else instruction provides the ability to modify sequence flow depending on the state of inputs. If <Boolean expression> is TRUE, the next step in the sequence will be <step x>, otherwise the next step will be <step y>.

IF <timeout> THEN GOTO <step x> ELSE If <Boolean Expression> GOTO <step y> ELSE GOTO <step z> This instruction provides the ability to modify sequence flow depending on the state of inputs with an additional timeout feature. If Timer <n> has expired, the next step in the sequence will be <step x>; otherwise, if <Boolean expression> is TRUE, the next step will be <step y>. If <Boolean expression> is FALSE and Timer <n> has not expired, then the next step will be <step z>. This instruction only checks the values of <Boolean expression> and Timer <n>; it does not start or reset the timer.

GOTO <step x> The GOTO instruction forces the sequence to jump to <step x>.

Start Timer This instruction starts the selected timer. The status of the timer must be checked using another instruction or combinational logic.

Stop Timer This instruction stops and resets the selected timer.

NOP The NOP instruction does not affect any of the outputs or the sequence of execution. It is effectively a single-cycle delay.

HALT The HALT instruction stops execution of the sequence.

BEGIN SHUTDOWN SEQUENCE The BEGIN SHUTDOWN SEQUENCE instruction signals to LogiBuilder that any instructions past this point will not be interrupted by jumps specified in exceptions. This feature allows code used for handling exceptions not to be interfered with by other exceptions that may occur. This instruction may be deleted from a sequence, but not inserted.

General Information on Instructions

All instructions are able to assign outputs, except for NOP, BEGIN STARTUP SEQUENCE, and BEGIN SHUTDOWN SEQUENCE. The outputs are assigned immediately when the sequencer enters the instruction.

The GOTO and If/Then/Else instructions cannot jump to the Wait for (timeout value), Wait for (Boolean) with Timeout, or Start Timer instruction.

See Also ▶“Designing Control Sequences” on page 49

- ▶ “Managing Multiple Control Sequences” on page 50
- ▶ “Editing Sequence Instructions” on page 51
- ▶ “Entering Supervisory Equations” on page 54

Designing Control Sequences

The sequencer instructions define the steps for controlling selected outputs. The exceptions define the equations that will trigger sequence controller exceptions to modify outputs and jump out to an alternative sequence step. Exceptions can be selectively applied to any sequencer step. When compiled, the control sequence instructions implement a digital logic state machine within the PLD core.

To design a control sequence:

1. In the LogiBuilder Logic editor, select the **Sequence** tab. If your design uses multiple state machines, select the one that you want to use for the sequencer instructions.
2. In the sequence (upper) portion of the editor, click **Step 1 Begin Shutdown Sequence** to highlight it.
3. Double-click Step 1 or press the **Insert** key on your keyboard to open the Insert Step Dialog box.
4. In the dialog box, choose an instruction type, and click **OK**. Repeat as necessary to add sequence steps.
5. Double-click each instruction step to open the appropriate Edit Properties dialog box.
6. Select the desired instruction properties in the Edit dialog box, and click **OK**.
7. To add exceptions, do the following:
   a. Double-click ***<end-of-exception-table>*** in the exceptions (lower) portion of the editor, or highlight it and press the **Insert** key.
   b. Repeat as necessary to add additional exceptions.
   c. Double-click each exception placeholder, to open the Exception Properties dialog box. Alternatively, right-click the placeholder and choose **Properties**.
   d. Click the **Edit** button at the top right of the dialog box to open the Boolean Expression Editor. Set the expression that will trigger the exception and click **OK**.
   e. In the Exception Properties dialog box, select the desired exception properties, and click **OK**.

See Also ▶“Sequence Controller Instruction Set” on page 47

▶ “Editing Sequence Instructions” on page 51

▶ “Editing Exceptions” on page 54

▶ “Managing Multiple Control Sequences” on page 50

Managing Multiple Control Sequences

The LogiBuilder Logic editor supports multiple state machines for power-up sequence and control. The state machines are defined separately but can interact through nodes or common logic functions. Each state machine is built up in a separate tab in the Sequence section of the Logic editor.

To manage multiple control sequences:

1. In the LogiBuilder Logic editor, select the Sequence tab.

   The name of each currently defined state machine is displayed in a separate tab at the bottom. You can add a new state machine by clicking the tab that contains the **+** sign. To delete a state machine, you must use the Multiple State Machines dialog box.

2. Right-click a tab for a state machine and choose **Multiple State Machine** from the pop-up menu. Alternatively, use the **Ctrl+M** keyboard shortcut.

3. In the Multiple State Machines dialog box, do one or all of the following:

   - Select a state machine and type a unique name for it in the State Machine Name text box.
   - Delete a state machine by selecting it and clicking **Delete SM**.
   - Click **Add SM** to add a new state machine.

4. Click **OK**.

See Also ▶“Sequence Controller Instruction Set” on page 47

▶ “Designing Control Sequences” on page 49

Defining Timers

Use the LogiBuilder Logic editor to set up timers for control sequences. After you have defined timers, they will be displayed in the properties dialog boxes for sequences that include timeouts. This will allow you to select the timeout value from the list.

To define a timer:

1. In the Logic editor, select the Timers tab.

2. Click the **Add** button at the bottom or press the **Insert** key to create a new timer.

   The timer is added to the list and given a default name.

3. If desired, click the default name in the Timer Name column and type a unique name.

4. Click the Clock Source cell and select a source from the drop-down menu. ECP5U/UM only support the 62.5 kHz logic sequence clock as a timer source clock.

5. Click the Period Cell. Select a time unit from the drop-down menu, and then specify the value.

   Note

   Timer delay settings must be longer than 160 µs.

   The number of LUT resources required to generate the timer is automatically recalculated.

See Also ▶“Sequence Controller Instruction Set” on page 47

Editing Sequence Instructions

The dialog boxes provided by the Logic editor enable you to set up and edit sequence instruction properties, Boolean expressions, and exceptions. The appropriate dialog box automatically opens when you double-click an inserted step or exception for editing.

See Also ▶“Sequence Controller Instruction Set” on page 47

Editing Boolean Instruction Properties

When you double-click a Boolean step for editing, the appropriate properties dialog box opens. Each Boolean instruction’s properties dialog box allows you to define output control properties, specify whether the instruction is interruptible by an exception, edit the Boolean expression, and enter descriptive comments. Boolean expressions such as conditional branches, also allow you to specify “timeout” and “goto” properties.

Edit “Wait for Bool” Properties This dialog box allows you to define a “wait for” Bool statement and specify output signal values.

Edit “Wait for Bool With Timeout” Properties This dialog box allows you to set up a “wait for” Boolean statement with an auto timeout. If the Boolean condition is met before the selected timer expires, the sequencer will continue to the next step. If the condition is not met and the timer expires, the sequencer will go to the specified step. The timer is started when the sequence enters this instruction step. The “with output” option specifies output signals that occur after the timer expires and transitions to the “Then Goto” step.

Conditional Branch (IfThenElse) This dialog box enables you to set up a conditional statement that checks a Boolean condition and then branches to an instruction step.

- The sequence will jump to the selected “Then Goto” step if the condition is true. The “With Output” option specifies output signal values that occur after the “Then Goto” transition.
- The sequence will jump to the selected “Else Goto” step if the expression is false. The “With Output” option specifies output signal values that occur after the “Else Goto” transition.

Edit “IfThenElse with Timeout” Properties This dialog box allows you to set up a conditional statement that checks a Boolean condition and the status of a timer.

- If the timer has expired, the sequencer will go to the “On Timeout Goto Sequencer step.” The “with Output” option specifies output signal values that occur after the step transition.
- If the Boolean condition is met before the selected timer expires, the sequencer will go to the selected “Goto Sequencer step if no timeout and the Boolean expression is satisfied” step. The “With Output” option specifies output signal values that occur after the step transition.
- If neither the Boolean condition is met nor the selected timer has expired, the sequencer will go to the “Else Goto Sequencer step.”

Note

This instruction checks the selected timer but does not start it. The timer must be started using a “Start Timer” instruction or supervisory logic.

See Also ▶“Sequence Controller Instruction Set” on page 47

Editing Boolean Expressions

The Boolean Expression Editor allows you to set up a Boolean expression using logic operators and a list of available inputs. You can enter the expression manually in the Expression text box at the top or select from the Logic Signal Pool and operators.

To edit a Boolean expression:

1. On the Sequence page, double-click the Boolean instruction that you want to edit.
2. In the Edit properties dialog box, click **Edit Boolean Expression**.

   You can enter the Boolean expression manually, if desired, by typing it into the Expression text box at the top and clicking OK. Otherwise, proceed with Steps 3-5.
3. Double-click a signal or bus from the Logic Signal Pool to add it to the expression.

   You can use the Filter input box below the signal pool to reduce the number of signals available. The signal pool only displays signals with the character string contained in the filter box.
4. Click the desired operator to add it to the expression.

   The following special vector operator is available for comparisons between buses and single-bit signals:

   - BITEXTEND (#) – Extends single bit to <wide> type vector. The BITEXTEND operator is only valid for single-bit signals.
5. Click **OK**.

The Boolean Expression Editor checks the expression for correctness and will issue a message if an error is encountered.

See Also ▶"Sequence Controller Instruction Set" on page 47

Editing Timeout Properties

The properties dialog boxes for "Wait for Timeout," "Start Timer," and "Stop Timer" enable you to select a defined timer, specify outputs, and specify whether the step can be interrupted by an exception.

All properties dialog boxes for sequence instructions that include timeouts—for example, the "Wait for Bool with Timeout"—allow you to select from a "Timeout" list of timers that have been defined. The properties dialog boxes for these instructions do not allow you to change the clock source and period for a selected timer. To do this, you must use the Timers sheet.

See Also ▶"Defining Timers" on page 50.

Editing Goto, NOP, and Halt Properties

The Edit "Goto" instruction properties dialog box allows you to specify the destination step for a GOTO (or branch) type of instruction, set the output signal values, enter a comment, and specify whether the instruction is interruptible by an exception.

The Edit NOP Properties dialog box allows you to enter a comment and specify that the NOP instruction is interruptible by an exception. A NOP step is essentially a single-cycle delay; it does not affect any of the outputs or the sequence of execution.

The Edit Halt Properties dialog box allows you to specify output values, enter a comment, and specify that the instruction is interruptible by an exception. A Halt step stops the execution of the sequence.

See Also ▶"Sequence Controller Instruction Set" on page 47

Editing Outputs

The Edit Output Properties dialog box enables you to select the outputs for a sequence instruction. It is immediately available when you double-click an Outputs instruction. For other instructions, it is accessible through the "Output Control" button or "With Output" button of the properties dialog box for the selected sequence.

Any single signal can be set to "Do not Modify," which preserves the signal value; or it can be set to a binary, hexadecimal, or decimal literal value.

Port groups can also be set to Increment, Decrement, Increment with Saturation, or Decrement with Saturation. These operations support counter implementations in the logic. The "with Saturation" instructions will saturate at all 0s (decrement) or all 1s (increment). The decrement and increment operations will roll over.

See Also ▶"Creating a Port Group" on page 43

Editing Exceptions

You can add an exception for use in a control sequence by double-clicking the <end-of-exception-table> line in the Exceptions section of the Sequence page or selecting it and pressing the Insert key. Afterwards, double-click the inserted exception placeholder to set the properties.

In the Exception Properties dialog box, you can type the expression that will trigger the exception in the Expression text box at the top. Alternatively, click the **Edit** button to open the Boolean Expression Editor and select the signals and operators for the expression.

Select the step that the sequence will go to when the exception is encountered.

Then, in the Logic Signal Pool, you can select output signals or groups that will be modified when the exception occurs.

Note

Any output signals that are controlled by the exception expression are active at all times. These outputs will be modified, even if the sequence is currently in a non-interruptible step.

See Also ▶"Designing Control Sequences" on page 49

▶ "Editing Boolean Expressions" on page 52

▶ "Sequence Controller Instruction Set" on page 47

Entering Supervisory Equations

The supervisory equations define combinatorial and registered logic independent of the sequencer control logic. The supervisory equations are always active and execute in parallel to the sequencer logic.

To enter supervisory equations:

1. In the LogiBuilder Logic editor, select the **Supervisory** tab.
2. Insert an equation placeholder by double-clicking the **<end-of-supervisory-logic-table>** marker. Alternatively, highlight the marker and press the Insert key on your keyboard.
3. Double-click the equation placeholder to open the Supervisory Logic Equation Entry dialog box.

4. Select the output signal of the Supervisory equation. The output signal is chosen from the available pool, which can be reduced using the filter input. Output signal groups can also be assigned.
5. Choose the assignment type. A signal can be assigned combinatorially, as D flip-flop, or as asynchronous set or reset. Only signals that are already assigned in the sequence, or assigned as D flip-flop in other equations, can be assigned as asynchronous set or reset.
6. Edit the expression either directly in the expression or click Edit to use the Boolean Expression editor.
7. Click **OK** to complete the equation definition.

Note

The sequencing, exceptions, and supervisory equations are combined together during the compilation process. Outputs that are already assigned in the sequence cannot be assigned as D type in the logic equations. They can only be accessed by asynchronous reset or preset equations.

See Also ▶“Editing Boolean Expressions” on page 52

Copying and Pasting Sequences and Equations

The LogiBuilder Logic editor allows you to copy, cut, and paste control sequences, exceptions, and supervisory equations. If you are copying multiple instructions, they must be contiguous.

To copy or cut and paste in the Logic editor:

1. Select the sequences, exceptions, or equations that you want to copy or cut.

   Note

   The Begin Startup Sequence, Halt (end of program), <end of exceptions table>, and <end of supervisory table> cannot be included in your selection. If you include them, you will receive an error message.

2. Choose **Edit > Copy** or **Edit > Cut** or use the Ctrl+C or Ctrl+X keyboard shortcut.
3. Select the step, exception ID, or equation, where you wish to insert the copied items.
4. Choose **Edit > Paste** or use the Ctrl+V keyboard shortcut.

   The copied items are pasted before the selected step, exception, or equation. Branch targets will not be pasted along with the instruction or equation. These need to be re-entered manually.

   If you need to undo the action, chose **Edit > Undo** or use the Ctrl+Z keyboard shortcut.

See Also ▶“Sequence Controller Instruction Set” on page 47

Importing HDL Modules

The LogiBuilder Logic editor enables you to add an HDL module to a Platform Designer project. You must first add the source file to your Diamond project. Only one module can be imported into a Platform Designer project. To include multiple modules, you must structure a top-level module that you will pass to Platform Designer.

To import an HDL Module:

1. In Diamond’s main window, choose **File > Add > Existing File**.
2. Navigate to the directory that contains the Verilog or VHDL source file, select the file and click **Add**.

   Diamond adds the file to the project and displays it in the Input Files folder of the File List view.
3. In Platform Designer, open the Logic editor and select the **Imported HDL** tab.
4. Select the **Enable Imported HDL** option. This will parse the input files for modules available to import.
5. Select the module from the Module Name menu.

   Platform Designer populates the File Location of the chosen module automatically. It also populates the Instance Name text box with the name of the module and adds the “Inst” extension. The left portion of the screen will be populated with any parameters available for definition in the imported HDL, as well as port information from the module.
6. If desired, rename the module instance by typing a new name in the Instance Name text box.
7. Assign values to the available HDL parameters.
8. For each port of the imported module, drag the desired signal from the Logic Signal Pool over to the Signal Name cell. The Logic editor’s DRC checking will inform you if the signal you are trying to map is not compatible.

Building the Design

The Build view enables you to do a final design rule check, examine resource utilization, compile the design, assign pins, implement the design, and generate the merged JEDEC file. This view enables you to generate a test bench, including stimulus, for simulating your design. It also enables you to export a detailed configuration report.

Checking Design Rules

Design rules are checked automatically each time you issue a save command or run synthesis. Automatic design rule checking also prohibits you from entering or pasting invalid data into cells that have pre-defined ranges or numeric data types.

You can also use the Build view to run manual design rule check at any time.

To run manual design rule check:

- Click the **DRC** button at the top of the Build view.

  The results are displayed in the Output view of Diamond's main window.

Examining Resource Utilization

The Build view of Platform Designer displays a summary of the hardware resources that are being used by the current design configuration. It provides estimates of the consumption of device resource logic, major blocks, and I/Os of the current design. The Look Up Tables, Embedded Block RAM, and Programmable IOs area of the resource summary are updated after you run the Generate JEDEC step.

The Component Summary table at the top of the Build view indicates the status of the design components and programming options. The lower portion of the view provides a list of resources used in the design and the percentage of each resource consumed. At the bottom left corner, a green check mark or red X indicates the status of the implementation. When any options have been changed that affect the build output, the status will be marked "Not Current." You will then need to click the Compile button, to update the output, and complete the Pin Assignment and Generate JEDEC steps. If the implementation is successful, with no errors, the status will change to Current.

Compiling the Design

When you compile the design, Platform Designer generates the HDL code and synthesizes the logic design.

To compile the design:

- In the Build view of Platform Designer, click the **Compile** button.

  If you have unsaved changes in your design, the Save Modified Files dialog box will open. Select the .ptm file in the Modified File list and any others that you want to save and click **OK**.

  Platform Designer compiles the design and takes it through the synthesis and translation processes.

See Also ▶"Examining Resource Utilization" on page 57

- "Exporting a Detailed Configuration Report" on page 58

Assigning Pins

After compiling the design in Platform Designer, you can open Diamond's Spreadsheet View to assign pins.

To assign pins:

1. In the Build view, click **Pin Assignments**.

   Spreadsheet View opens to the Port Assignments sheet.
2. Select the pin cells in the Pin column for the signals you want to assign.
3. Right-click the selected cells and choose **Assign Pins**.
4. Make your selections in the Assign Pins dialog box, and click **Assign Pins**.

See Also ▶"Assigning Signals in Spreadsheet View" on page 465 in Diamond online help.

Generating the JEDEC

The Build view enables you to generate a merged JEDEC file after pin assignment. This process merges the JEDEC of the FPGA with the ASC JEDECs.

To generate the merged JEDEC file:

▶ In the Build view, click **Generate Jedec**.

When the process is completed, the Summary Status at the bottom of the Build view will be set to Current.

Exporting a Detailed Configuration Report

After the design has been successfully compiled and implemented, the Build view shows a green check mark, indicating that the status is current. This allows you to export a detailed report of the design's configuration.

To export a detailed configuration report:

▶ Select the Build view and click the **Export Configuration Report** button.

Platform Designer automatically exports the report, named <project_name>_report.txt, to your project directory. You can view the report by following the link displayed after the report is exported.

The report lists the components utilized in the design, along with the component settings for each feature. The report also includes full configuration information for the analog portion of the design.

Simulating the Design

After the design has been compiled successfully, you can perform functional simulation using Platform Designer and the Diamond Simulation Wizard. Platform Designer enables you to create a test bench file, based on the ASC configurations and specified connections, and it generates a stimulus file based on clock and non-clock data signals that you specify.

Generating a Stimulus and Test Bench File

After the design has been compiled successfully, you can specify the connections and signals for functional simulation. Platform Designer uses this information, plus the port-related information from the FPGA top-level HDL and the ASC configuration files, to generate a stimulus file and a test bench file.

To generate a stimulus file and a test bench file:

1. In the Build view of Platform Designer, click the **Generate Stimulus** button.

   The dialog box opens to the “Connections between FPGA and ASCs” page. The “From” and “To” sections, at the top, list all the FPGA ports and ASC signals that you can use to establish new board-level connections. The “Connection” section, at the bottom, displays the default hardware connections between the FPGA and all ASC devices in the design. These cannot be edited or removed.

2. Click the “**add connection**” button ➕ on the bottom left.

   A new row is added at the bottom of the Connection section.

3. Scroll down to the newly added row, and then do the following:

   a. Select the desired signal in the “From” column in the top section and drag it to the “From Signal” cell in the newly created row at the bottom.

   b. Likewise, select the desired signal in the “To” column in the top section and drag it to the “To Signal” cell in the newly created row at the bottom.

   c. Type a name for the new net in the Net Name cell of the newly created row.

   Only a connection’s Net Name can be edited after you have selected the signals. To change the signals of a connection, you must remove the connection and replace it. To remove a connection, click any cell in the connection, and then click the X button.

4. Repeat Step 3 for each new connection you want to add.

5. Select the **Stimulus** tab, and then do the following:

   a. Select the **Clock** tab on the left to edit the stimulus of clock signals.

- Click the "**add clock stimulus**" button on the bottom left to add a clock. The system clock signal, ASC0_CLK, will be shown when this tab is opened, and it cannot be edited.
- Select the desired clock signal from the Signal Name drop-down menu, and then select an initial value, 1 or 0, from the Initial Value menu.
- In the Frequency or Period cell, type a value, select the measurement unit, and press **Enter**. The period is calculated automatically when you enter the frequency and vice versa.

b. Select the **Data** tab on the left to add stimulus for non-clock signals.

- Click the "**add data stimulus**" button on the bottom left to add a new row.
- Click inside the Signal Name column and choose a signal from the drop-down menu.
- The column following the Signal Name specifies the initial value. Click inside the cell and select the numerical type—Bin, Hex, or Dec—and then enter a value. Enter a value in each subsequent cell where the signal changes.

  You do not need to enter a value for each signal in each cell. Enter a value in a cell only when the value changes. The input value will be held at the last entered value if no entry is made in a cell.

  You can also select a bus and enter the values. The values can be entered as Binary, Decimal, or Hexadecimal for bus signals.
- Repeat the above steps to add stimulus for more non-clock signals.
- Add time entries for the additional columns in the top row of the display. You can select the time base to use as you enter each time value. The time entries are absolute time references rather than relative to each other. Therefore, the time values must be increasing from left to right.

  When you add a time entry in the last column on the right, a new column gets added on the right, allowing you to enter an additional time value if desired.

  To add or remove a column, right-click the time entry top row where you want to insert or remove a column and choose Insert Before, Insert After, or Remove. Make sure that the time entry cell is not open for editing before you right-click. If it is open for editing, press the Enter key, and then right-click to access the pop-up menu.

6. Click **OK**.

Simulating the Design

When you generate the stimulus for the design, the following four files are automatically created:

<project_name>_design.v This file serves as a wrapper of the MachXO2HC/HE, MachXO3D, MachXO3LF, ECP5U/UM and ASC for functional simulation

<project-name>_test.v This file serves as the top-level file for functional simulation

<project-name>_design_post.v This file serves as a wrapper of the MachXO2HC/HE, MachXO3D, MachXO3LF, and ASC for timing simulation.

<project-name>_test_post.v This file serves as the top-level file for timing simulation

You can use Diamond's Simulation Wizard to create the simulation project for the Platform Manager 2 or MachXO2HC/HE, MachXO3D, MachXO3LF, ECP5U/UM design and export the simulation project into ModelSim Lattice FPGA Edition or Aldec Active-HDL full version. After opening the Simulation Wizard, follow the on-screen prompts to create the simulation script.

When you create the simulation project in the Diamond Simulation Wizard and click **Finish**, the ModelSim software will start automatically. If "Run Simulation" (the default value) was selected in the Simulation Wizard, the project will be loaded into the simulator. The project files will be compiled, and the simulation waveform window will open with all the top-level signal names. You can add signal names from within the design to the waveform window if you wish to see other signals from your design. See the ModelSim documentation for more information about adding signal names to the waveform window.

The simulation will run for a period of 1 µs after it is loaded and compiled. You can run it for additional time by using the Run command in the ModelSim console. To run the simulation for 100 µs, type the command `<run 100 us>` and press the Enter key. The length of time to run your simulation will depend upon the design and the stimulus file you created.

For each ASC configuration, the Simulation Wizard will copy the following files to the simulation folder:

- cfg_eeprom.hex
- flut_eeprom.hex
- i2caddress.hex
- trim_eeprom.hex

The Simulation Wizard will also copy the memory file (.mem) for the "VID table" and the MICO "scratchpad" and "prom" files.

The Simulation Wizard will not copy any memory or data file from an imported HDL module. If you have imported an HDL module into your Platform Designer project, you will need to copy it manually into the simulation folder.

See Also ▶"Simulation in Diamond" on page 307 in Diamond online help.

Working with Power Calculator

When using Platform Designer with Power Calculator, the most accurate power calculation is accomplished when using Power Calculator in integrated mode within your projects.

When calculating power for Platform Manager 2 and MachXO2HC/HE, MachXO3D, MachXO3LF, ECP5U/UM designs using an ASC device, the Diamond integrated Power Calculator tool imports a data file generated by the Platform Designer software. This data file is generated in the current implementation directory and should not be edited by the user.

Platform Designer calculates the power mode for each ASC used and generates a data file containing each ASC, the power used by that ASC, and the power supply used (if relevant). Refer to the description of the "ASC" on page 766 page in Diamond Power Calculator online help. The data file contains both external ASC devices used and the ASC internal component in the Platform Manager 2 device.

The power consumed by an ASC device is determined by the number of HVOUTs used in the design. The data file, which is generated from Platform Designer and which has an .apw suffix, includes the number of HVOUTs used and the power model equation. The data file lists all ASCs and the power used by each and is located in the design implementation directory. This file is read by Power Calculator and then the additional power from the ASC devices is added to the total power displayed. This data is displayed in the Power Calculator Power Summary tab, Power by Block (W) section and the ASC page.

Power calculation for ASCs is different than for other Lattice devices. To calculate power consumption for ASCs, the following equations are used:

$$Current = I_O + I_{HVOUT} \times \#HVOUT$$

$$Power = V_{CC} \times Current$$

$$Power = V_{CC} \times (I_O + I_{HVOUT} \times \#HVOUT)$$

There are four variables:

$$V_{CC} = 3.6V$$

$$I_O = 23mA$$

$$I_{HVOUT} = 2mA$$

$\#HVOUT =$ Number of HV Outputs used

The above calculations are only used when Power Calculator is used in the integrated mode or used with a PCF file generated in this mode. To understand the different methods power is calculated refer to the list below.

Power Calculator Integrated mode

- Calculates power from multiple ASC devices for Platform Manager 2, or MachXO2HC/HE with external ASCs, MachXO3D with external ASCs, MachXO3LF with external ASCs, or ECP5U/UM with external ASCs.

Power Calculator standalone mode

- Calculates power only from the internal ASC in the Platform Manager 2 device. ASC power is estimated as a fixed value, not a variable amount based on the number of HVOUTs used.
- Can correctly calculate ASC power based on HVOUTs used only if opened with a PCF file generated by Power Calculator in integrated mode instead of loading NGD database.

Power Estimator standalone mode

- Calculates power only from the internal ASC in the Platform Manager 2 device. ASC power is estimated as a fixed value, not a variable amount based on the number of HVOUTs used.
- Can correctly calculate ASC power based on HVOUTs used only if opened with a PCF file generated by Power Calculator in integrated mode.

See Also ▶“Analyzing Power Consumption” on page 755 in Diamond online help.

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