

Lattice Radiant Software 2.2 Release Notes

Welcome to Lattice Radiant® software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs).

What's New in Radiant Software 2.2

▶ Device Support:

- CrossLink™-NX Device Family (LIFCL):
 - 17K and 40K devices bitstream enabled.
- Certus™-NX Device Family (LFD2NX):
 - 40K (-7/-8/-9) HP/LP 1.0V (COM/IND) - CABGA196
 - 40K (-7/-8/-9) HP/LP 1.0V (COM/IND) - CSFBGA121
 - 40K devices bitstream enabled.

▶ Tool and Other Enhancements:

- **Programmer** – Supports full encryption and authentication.
- **Simulation tool change** – Mentor ModelSim® Lattice Edition is the new OEM simulation tool included with Radiant software. ModelSim replaces Aldec-Active HDL™.

NOTE: For post-routing simulation, please use a full version of ModelSim PE. The OEM version will be addressed in an upcoming software release.

- **Reveal** – Reveal Analyzer/Controller support for CrossLink-NX (LIFCL) and Certus-NX device families.
- **Soft Error Injection** – Soft Error Injection (SEI) Editor allows you to generate single-bit errors, insert them into a bitstream, and detect them for analysis, simulating the effect of radiation damage on the device's configuration memory.

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Radiant software, start with the following procedures. These procedures adapt the project for the changes in Radiant software.

Find out which version of Radiant software your project was created with. Then work through the changes for that and every later version, starting with the earliest and going to the most recent. For example, if your project was created with Radiant software 1.0, you would start with the changes for Radiant software 1.0. After completing those changes, you would work on the changes for Radiant software 2.0, and so on.

Once saved, the project will not be compatible with earlier Radiant software versions

The following IP for iCE40UP must be regenerated in Radiant software v2.2:

- ▶ PLL (Phase Locked Loop)

The following IP for CrossLink-NX (LIFCL) and Certus-NX (LFD2NX) must be regenerated in Radiant software v2.2:

- ▶ DDR_Generic (DDR Generic Interfaces)
- ▶ GDDR7:1 (7:1 LVDS Interface)
- ▶ SDR (Single Data Rate)
- ▶ DDR_MEM (DDR Memory Interfaces)
- ▶ ADC (Analog to Digital Converter)
- ▶ SEDC (Soft Error Detection/Correction)
- ▶ Sin_Cos_Table (Sine Cosine Table)
- ▶ OSC (Oscillator)
- ▶ RAM_DQ (Single Port RAM)
- ▶ RAM_DP_True (True Dual Port RAM)
- ▶ FIFO
- ▶ FIFO_DC (FIFO Dual Clock)

The following is a list of IP for CrossLink-NX (LIFCL) and Certus-NX (LFD2NX) that must be regenerated in Radiant software v2.1:

- ▶ PLL (Phase Locked Loop)

The following IPs use PLL; therefore, these IPs need be re-generated to update the PLL:

- GDDR7:1 (7:1 LVDS Interface)
- DDR_MEM (DDR Memory Interfaces)
- DDR_Generic (DDR Generic Interfaces)
- MIPI_DPHY (MIPI Interface)
- ▶ ADC (Analog to Digital Converter)
- ▶ SEDC (Soft Error Detection/Correction)
- ▶ OSC (Oscillator)

Migrating IPs – When an older version IP is migrated to Radiant software 2.1, observe the following:

- ▶ For PMIs, user must add the Family attribute in all PMI instantiations (Radiant software 2.0, 2.0 SP1, and 2.1).
- ▶ Phase Locked Loop (PLL) IP has been enhanced since Radiant software 2.0 SP1 released. For designs created in previous versions of Radiant software (2.0 or prior), it is necessary to re-generate PLL IP in Radiant software 2.1. Otherwise, Radiant software 2.1 will issue an error when

the previous generated PLL IP is detected in the design. Designs created using Radiant Software 2.0 SP1 with PLL will work without any errors.

Update to IO_Type HDL attribute default value – The IO_TYPE HDL attribute default value has been changed since Radiant 2.0 SP1 from LVCMOS18 to LVCMOS33.

Oscillator Frequency Range change in iCE40UP – The “Fast” setting for “Oscillator Frequency Range” in Bitstream Strategy options has been removed in Radiant 2.1. There are two settings only - “Medium” and “Slow.” If you have an earlier project using the “Fast” setting, it will be defaulted to “Slow” in Radiant 2.1. You will need to change it to “Medium” if you want a faster configuration speed.

Large_RAM – If a LARGE_RAM IP generated from a previous Radiant version needs to be re-configured in Radiant 2.1, the IP must be re-created.

Help Resources

Available information resources for the Radiant software include the following:

- ▶ Online Help updated with CrossLink-NX and Certus-NX content.
 - ▶ To view the Online Help, start the Lattice Radiant software and select the  “Getting Started” icon under Information Center.
- ▶ Installation:
 - ▶ *Lattice Radiant Software 2.2 Installation Guide for Windows*
This document provides installation instructions for Windows OS.
 - ▶ *Lattice Radiant Software 2.2 Installation Guide for Linux/Ubuntu*
This document provides installation instructions for Linux/Ubuntu OS.

System Requirements

The following shows the basic system requirements for Radiant software:

- ▶ Intel Pentium or Pentium-compatible PC
- ▶ 64-bit OS:
 - ▶ Windows 7, Windows 8 and 8.1, or Windows 10. (ModelSim Lattice Edition requires Windows 10)
 - ▶ Red Hat Enterprise Linux 6.9 or 7.4
 - ▶ Ubuntu version 16.04 LTS
- ▶ Approximately 3 GB free disk space
- ▶ Computer Memory Requirement: 8 GB Recommended for running a single project. If running multiple projects, the memory requirement will be higher.
- ▶ 1024 X 768 graphics display

- ▶ Network adapter for license and network connectivity
- ▶ A Web browser with JavaScript capability
- ▶ Acrobat Reader

Support for Third-Party Synthesis and Simulator Tools

In addition to the Synopsys Synplify Pro® for Lattice and ModelSim Lattice Edition tools included with Radiant software suite, the following 3rd-party synthesis and simulator tools are supported by Radiant software:

- ▶ **Synthesis Tools:**
 - ▶ Synopsys Synplify Pro FPGA synthesis software version Q-2020.03LR
- ▶ **Simulator Tools:**
 - ▶ Aldec Active-HDL v11.1 or later
 - ▶ Mentor Questa® Sim v10.4g or later
v10.6b or later (supports IP encryption)

Known Issues for Radiant Software 2.2

The following are known Issues for the Radiant software 2.2.

MAP incorrectly reports number of DPHY and PCIE/ADC resources for CrossLink-NX QFN72 package.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CrossLink-NX

Bug number: DNG-8297

When simulating Generic DDR, there may be a mismatch in the RTL and post-route simulation. Silicon is not affected.

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CrossLink-NX, Certus-NX

Bug number: DNG-9639

CSI-2/D-PHY Transmitter IP hangs during Post synthesis/PAR simulations.

For some configurations of CSI-2/DSI D-PHY-TX IP, post-synthesis and post-PAR simulation hangs (runs indefinitely without stopping) when LSE is used.

Workaround: Use Synplify Pro for synthesis and generating the post-PAR netlist if you run into this issue.

Devices affected: CrossLink-NX, Certus-NX

Bug number: DNG-9697

For some SystemVerilog designs, Synplify Pro fails to identify multi-driven nets and the flow passes with no errors

Workaround: Check the design for multi-driven nets and run the flow using LSE to verify.

Devices affected: CrossLink-NX, Certus-NX

Bug number: DNG-10132

ModelSim requires installation of Visual C++ 2013

In order for the ModelSim simulation tool to function correctly on a freshly configured machine, Visual C++ 2013 must also be installed to ensure all the correct DLLs are present.

Workaround: On newly configured PCs, install Visual C++ 2013 to ensure necessary DLLs are included. (msvcr120.dll)

Devices affected: All

Bug number: DNG-10282

PLL Soft IP

There are two issues that require a manual workaround until it is addressed in the next Radiant release.

Issue#1 – DIV_DEL attribute is not set by the PLL Soft IP

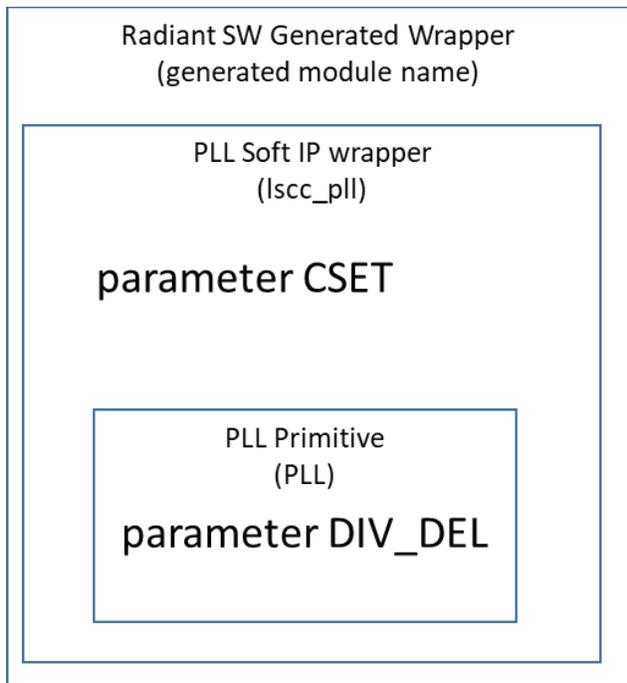
The PLL can be unstable for certain configurations and not be able to produce correct frequencies.

Workaround: Set DIV_DEL parameter

DIV_DEL parameter

- This parameter is not visible in the wrapper.
- Search the PLL primitive module instance and assign a value to the DIV_DEL parameter.
- DIV_DEL should have the same value as the output divider of the clock selected as feedback (in 7bit binary format).
- For example, if CLKOP is selected as feedback clock and the CLKOP output divider is 1 (DIVOP_ACTUAL_STR == "1"), then DIV_DEL should be set to "0b0000001"

.DIV_DEL() → .DIV_DEL("0b0000001")



Issue#2 – CSET attribute value mapping is reversed by the PLL primitive

The PLL will produce a higher than expected jitter.

Workaround: Manually set CSET's value properly after PLL is generated.

CSET parameter

- The CSET parameter will have its value calculated by the IP Generation script and assigned at the Generated wrapper.
- Replace the CSET value in the Generated wrapper according to the mapping shown on the left.
- Example:
.CSET("16P") → .CSET("60P")

Devices affected: All

Bug number: N/A

CSET	
Old	New
"8P"	"68P"
"12P"	"64P"
"16P"	"60P"
"20P"	"56P"
"24P"	"52P"
"28P"	"48P"
"32P"	"44P"
"36P"	"40P"
"40P"	"36P"
"44P"	"32P"
"48P"	"28P"
"52P"	"24P"
"56P"	"20P"
"60P"	"16P"
"64P"	"12P"
"68P"	"8P"