Mach-NX Hardware Checklist

Technical Note

FPGA-TN-02235-1.3

October 2025

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This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
I2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
LVDS	Low-Voltage Differential Signaling
PCB	Printed Circuit Board
PLD	Programmable Logic Device
SFB	SoC Function Block
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSPI	Slave Serial Peripheral Interface

1. Introduction

When designing complex hardware using the Mach-NX™ PLD, you must pay special attention to critical hardware configuration requirements. This technical note steps through these critical hardware requirements related to the Mach-NX devices. This document does not provide detailed step-by-step instructions but gives a high-level summary checklist to assist in the design process.

Hardware checklists are developed after evaluation boards and incorporate optimized designs that improve upon the circuitry of the evaluation boards. If you copy circuits from evaluation boards, ensure to optimize your designs according to the hardware checklists.

The Mach-NX PLDs are low power, instant-on, Flash based devices with high integration and on-board System-on-Chip SoC Function Block (SFB) features. This technical note assumes that the reader is familiar with the Mach-NX device features as described in the Mach-NX Family Data Sheet (FPGA-DS-02084).

The critical hardware areas covered in this technical note include:

- Power supplies as they relate to the Mach-NX supply rails and how to connect them to the PCB and the associated system.
- Configuration and how to connect the configuration mode selection for proper power up configuration.
- Device I/O interface and critical signals.

Important: Refer to the following documents for detailed recommendations.

- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- Mach-NX sysI/O Usage Guide (FPGA-TN-02233)
- Implementing High-Speed Interfaces with Mach-NX Devices (FPGA-TN-02234)
- Mach-NX Programming and Configuration Usage Guide (FPGA-TN-02231)
- Mach-NX SFB Hardware Usage Guide (FPGA-TN-02222)

2. Power Supply

The V_{CC} and V_{CCIO0} power supplies determine the Mach-NX internal *power good* condition. These supplies need to be at a valid and stable level before the device can become operational. In addition, there are six (V_{CCIO1} to V_{CCIO6}) supplies that power the remaining I/O banks, and two auxiliary supplies, V_{CCAUX} and V_{CCB}. Table 2.1 shows the power supplies and the appropriate voltage levels for each.

Refer to the Mach-NX Family Data Sheet (FPGA-DS-02084) for more information on the voltage levels.

Table 2.1. Power Supply Description and Voltage Levels

Supply	Voltage (Nominal Value)	Description
V_{CC}	1.0 V	Core power supply
V_{CCIO0}	2.5 V or 3.3 V	Power supply pins for I/O Bank 0. banks.
V_{AUX}	1.8 V	Auxiliary power supply pin for internal analog circuitry.
V_{CCB}	1.8 V	Power supply for auxiliary core functions.
V_{CCIO1}, V_{CCIO2}, V_{CCIO5}, V_{CCIO6}	1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V	Power Supply pins for I/O Banks 1, 2, 5 and 6
V_{CCIO3}, V_{CCIO4}	1.0 V, 1.2 V, 1.35 V, 1.5 V, or 1.8 V	Power Supply pins for I/O Banks 3 and 4

2.1. Power Noise

The power rail voltages of the FPGA allow for a worst-case normal operating tolerance of ±5% of these voltages. The 5% tolerance includes any noise.

2.2. Power Source

It is recommended that the designed voltage regulator's are accurate to within 3% of the optimum voltage to allow power noise design margin.

When calculating the voltage regulator total tolerance, include:

- Regulator voltage reference tolerance
- Regulator line tolerance
- Regulator load tolerance
- Tolerances of any resistors connected to the regulator's feedback pin, which sets the regulator's output voltage
- Expected voltage drops due to power filtering the ferrite bead's ESR * expected current draw
- Expected voltage drops due to the current measuring resistor's ESR * expected current draw

With a 3% tolerance allocated to the voltage source, the design has a remaining 2% tolerance for noise, and layout related issues. The 1.0 V rail is especially sensitive to noise as every 10 mV is 1% of the rail voltage.

3. Power Supply Fitering

Providing a quiet, filtered supply is important for all rails and critical for the analog rails. Supplies should be decoupled with adequate power filters. Bypass capacitors must be located close to the device package pins with very short traces to keep inductance low.

For the best performance, use careful pin assignments to keep noisy I/O pins away from sensitive functional pins. The leading causes of PCB related crosstalk with sensitive blocks are related to FPGA outputs located in close proximity to the sensitive power supplies. These supplies require cautious board layout to ensure noise immunity to the switching noise generated by FPGA outputs. Guidelines are provided to build quiet filtered supplies for the analog supplies; however, robust PCB layout is required to ensure that noise does not infiltrate into these analog supplies.

3.1. Recommended Power Filtering Groups and Components

Table 3.1. Recommended Power Filtering Groups and Components

Power Input	Recommended Filter	Notes
V_{CC}	10 µF x 2 + 100 nF per pin	Core and clock logic. 1.0 V
V_{CCAUX}	120 Ω FB + 10 µF + 100 nF per pin	Auxillary power supply pin for internal analog circuitry. 1.8 V
V_{CCB}	120 Ω FB + 10 µF + 100 nF per pin	Power supply for auxillary core functions. 1.8 V
$V_{CCIO[6:0]}$	10 µF + 100 nF per pin for each V_{CCIOX}	Bank I/O. Unused banks can use a single 1.0 µF. For banks with lots of outputs or large capacitive loading, replace the 10 µF with a 22 µF (or use two 10 µF). Bank 0: 2.5 V or 3.3 V only. Banks 1, 2, 5, 6: 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V. Banks 3, 4: 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V.

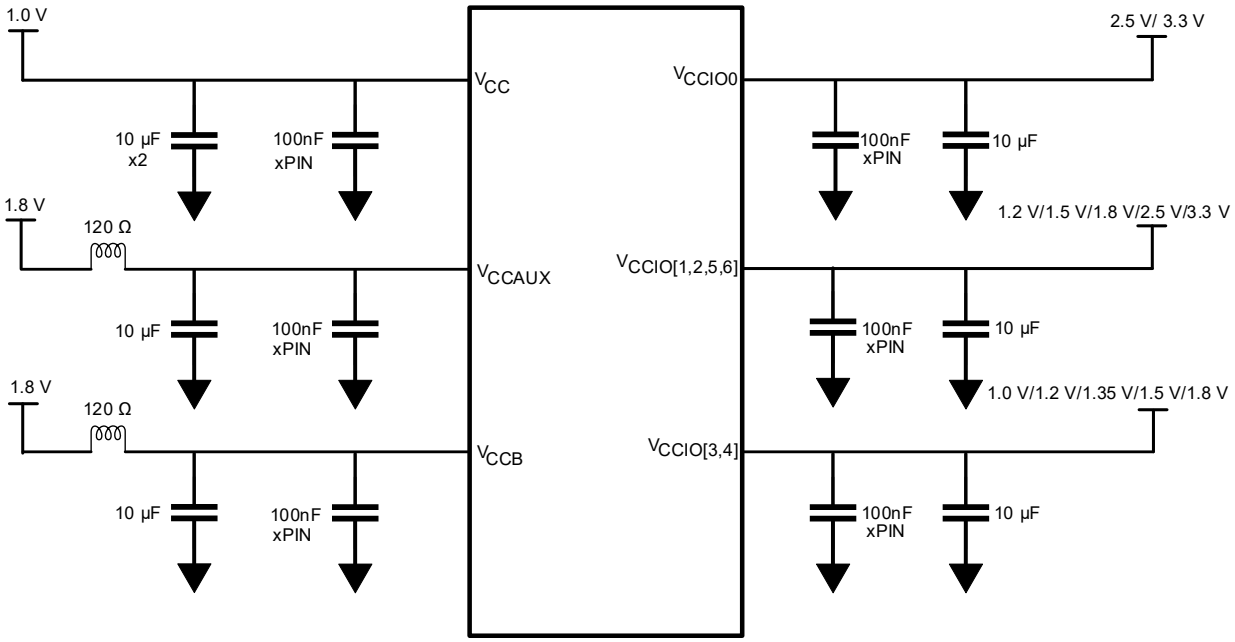

Figure 3.1. Recommended Power Filter

3.2. Ground Pins

All ground pins need to be connected to the board's ground plate.

3.3. Unused Bank V_{CCIOX}

Connect the unused V_{CCIOX} pins to a power rail. Do not leave them open.

3.4. Clock Oscillator Supply Filtering

When providing an external reference clock to the FPGA from, for example, a single-ended or differential clock oscillator, proper power supply isolation and decoupling of the clock oscillator are recommended.

When specifying components, choose good quality ceramic capacitors in small packages and place them as close to the clock oscillator supply pins as practically possible. Good quality capacitors for bypassing generally meet the following requirements:

3.5. Ferrite Bead Selection

- Most designs work well using ferrite beads between 120 Ω at 100 MHz and 240 Ω at 100 MHz.
- Ferrite bead induced noise voltage from ESR * CURRENT should be < 1% of rail voltage for non-analog rails and < 0.25% for sensitive rails.
- Non-PLL rails should use ferrite beads with an ESR between 0.025 Ω and 0.10 Ω, depending on the current load.
- PLL rails draw low current, which allows ferrite beads with an ESR ≤ 0.3 Ω.
- Small package size ferrite beads have a higher ESR than large package size ferrite beads of the same impedance.
- High-impedance ferrite beads have a higher ESR than low-impedance ferrite beads in the same package size.

3.6. Capacitor Selection

When specifying components, choose good quality ceramic capacitors in small packages and place them as close to the power supply pins as practically possible. Good quality capacitors for bypassing generally meet the requirements discussed in the following sections.

3.6.1. Capacitor Dielectric

Use dielectrics such as X5R, X7R, and similar that have good capacitance tolerance (≤ ±20%) over a temperature range. Avoid Y5V, Z5U, and similarly poor capacitance-controlled dielectrics.

3.6.2. Voltage Rating

Capacitor working capacitance decreases non-linearly with a higher voltage bias. To maintain capacitance, the capacitor voltage rating should be at least 80% higher than the voltage rail (maximum). Example: 3.3 V rail bypass capacitors should use the commonly available 6.3 V rating as a minimum.

3.6.3. Size

Smaller body capacitors have lower inductance, work at higher frequencies, and improve board layout. For a given voltage rating, smaller body capacitors tend to cost more than larger body capacitors. Optimizing between market pricing and size related inductance, the following capacitor sizes are recommended:

Table 3.2. Recommended Capacitor Sizes

Capacitance	Preferred Size	Next Best Size
0.1 µF	0201	0402
1.0 µF, 2.2 µF	0402	0201
4.7 µF	0402	0603
10 µF	0402	0603
22 µF	0805	0603

4. Power Sequencing

There is no power-up sequence required for the Mach-NX device.

5. Power Estimation

Once the Mach-NX device density, package, and logic implementation are determined, power estimation can be performed using the Power Calculator tool, which is provided as part of the Lattice Diamond™ design software. While performing power estimation, you should keep two specific goals in mind.

- Power supply budgeting should be considered based on the maximum power-up in-rush current, configuration current, or maximum DC and AC current for a given system environmental condition.
- The ability of the system environment and Mach-NX device packaging to support the specified maximum operating junction temperature.

By determining these two criteria, system design planning can take the Mach-NX power requirements into consideration early in the design phase.

6. Configuration Considerations

Mach-NX devices contain two types of memory, SRAM and Flash. SRAM is volatile memory and contains the active configuration. Flash is non-volatile memory that provides on-chip storage for SRAM configuration data. Additional external Flash memory is required for SoC Function Block configuration data and code storage and must be connected to SoC Function Block QSPI Monitor Channel 0 (refer to the SoC Function Block section).

The Mach-NX device includes multiple programming and configuration interfaces:

- 1149.1 JTAG
- Self-download
- Slave SPI
- Dual Boot
- I²C

For ease of prototype debugging, it is recommended that every PCB have easy access to the programming and configuration pins.

The configuration logic arbitrates access from the interfaces by the following priority. When higher priority ports are enabled, Flash access by lower priority ports will be blocked.

- JTAG Port
- Slave SPI Port (SN low activates the SPI port)
- I²C Primary Port

Note: Erased devices have all programming and configuration ports enabled by default. When the device is erased, ensure that SN and PROGRAMN are not driven low.

For a detailed description of the programming and configuration interfaces, refer to the Mach-NX Programming and Configuration Usage Guide (FPGA-TN-02231).

The use of external resistors is always needed if the configuration signals are being used to handshake with other devices. Pull-up and pull-down resistor (4.7 kΩ) recommendations on different configuration pins are listed below.

Table 6.1. Default State of the sysCONFIG™ Pins[1]

Pin Name	Pin Function (Configuration Mode)	Pin Direction (Configuration Mode)	Default Function (User Mode)
PROGRAMN	PROGRAMN	Input with weak pull-up, external pull-up to V_{CCIO0}.	PROGRAMN
INITN	I/O	I/O with weak pull-up, external pull-up to V_{CCIO0}	User-defined I/O
DONE	I/O	I/O with weak pull-up, external pull-up to V_{CCIO0}.	User-defined I/O
CCLK	SSPI	Input with weak pull-up.	User-defined I/O
SN	SSPI	Input with weak pull-up, external pull-up to V_{CCIO2}.	User-defined I/O
SI/SPISI	SSPI	Input	User-defined I/O
SO/SOSPI	SSPI	Output	User-defined I/O
CSSPIN	I/O	I/O with weak pull-up, external pullup to V_{CCIO2}.	User-defined I/O
SCL	I²C	Bi-Directional open drain, external pull-up.	User-defined I/O
SDA	I²C	Bi-Directional open drain, external pull-up.	User-defined I/O
TDI	TDI	Input with weak pull-up.	TDI
TDO	TDO	Output with weak pull-up.	TDO
TCK	TCK	Input. Recommended 4.7 kΩ pull-down.	TCK
TMS	TMS	Input with weak pull-up.	TMS
JTAGENB	I/O	Input with weak pull-down.	I/O

Note:

1. Leave the unused configuration ports open.

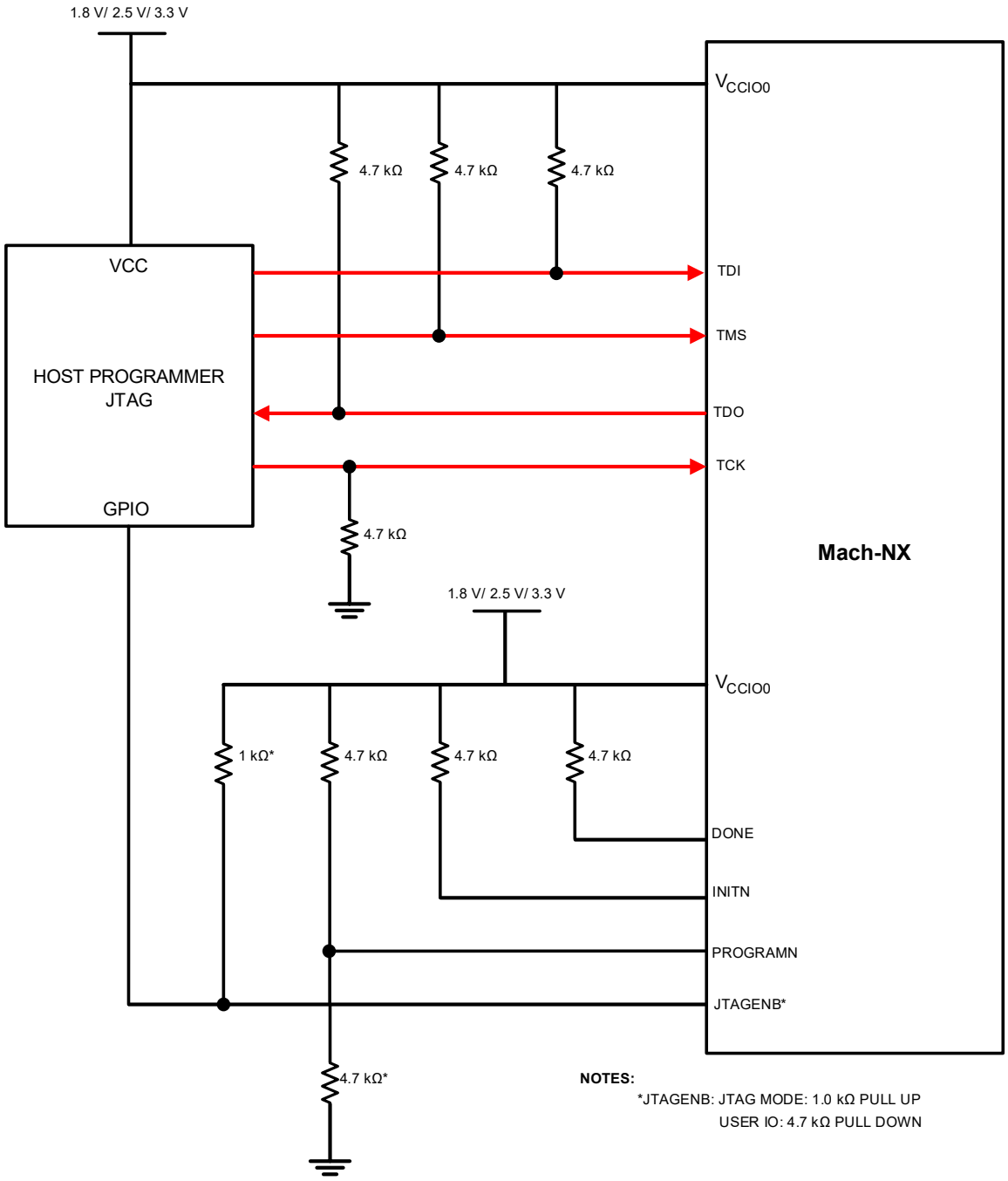

Figure 6.1. Typical Connections for Programming SRAM or Internal Flash via JTAG

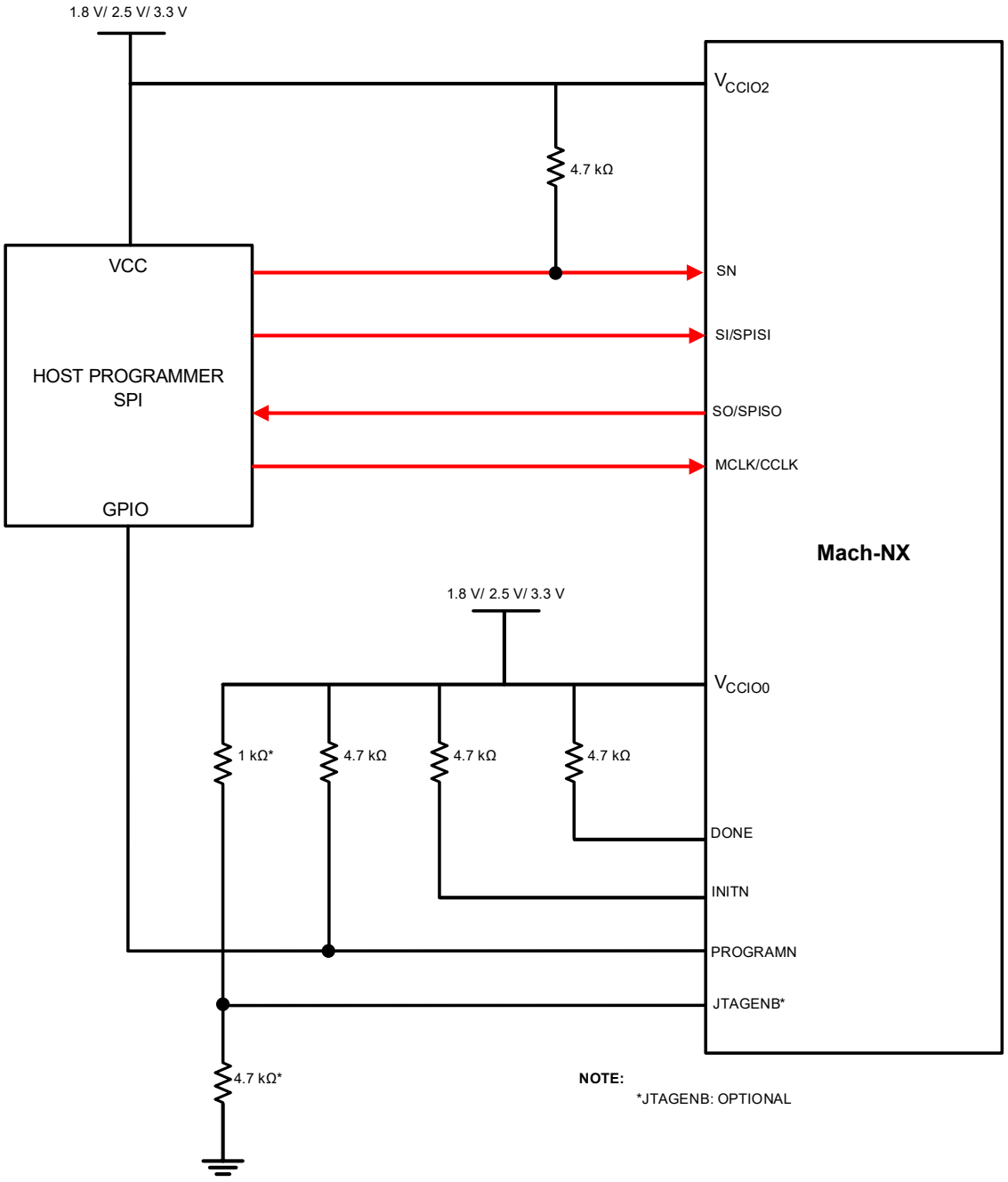

Figure 6.2. Typical Connections for Programming SRAM or Internal Flash via SSPI

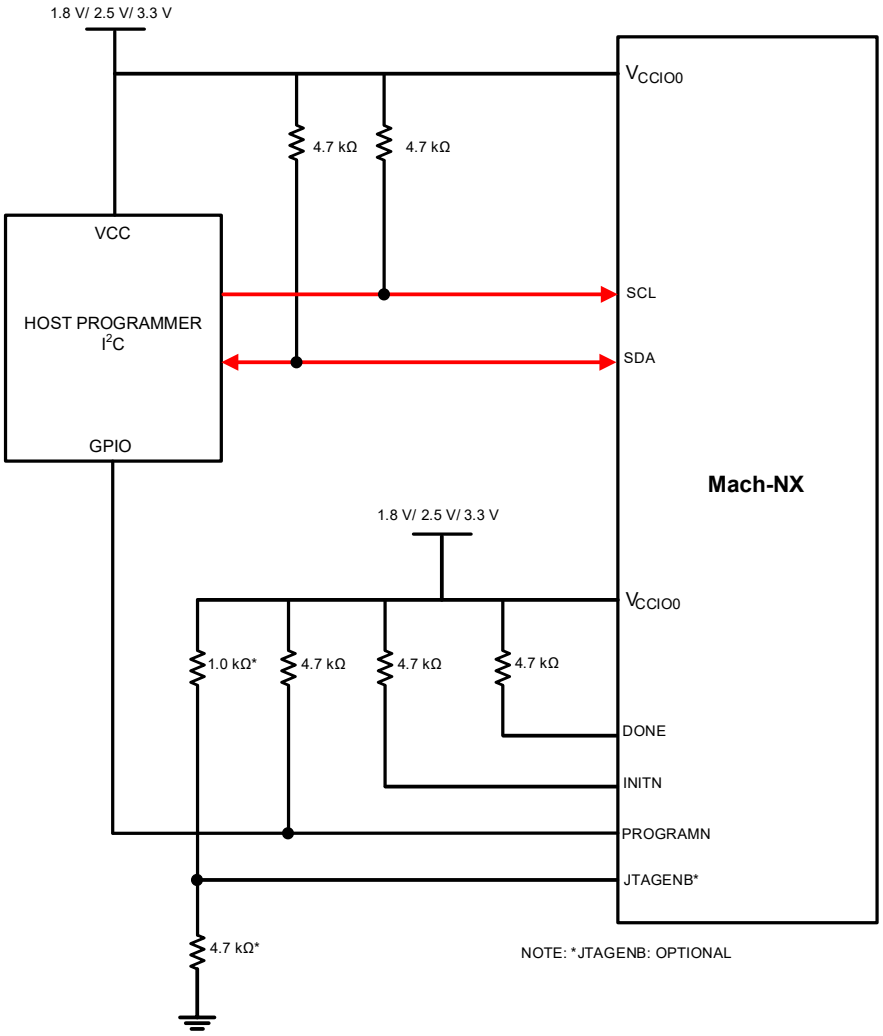

Figure 6.3. Typical Connections for Programming SRAM or Internal Flash via I²C

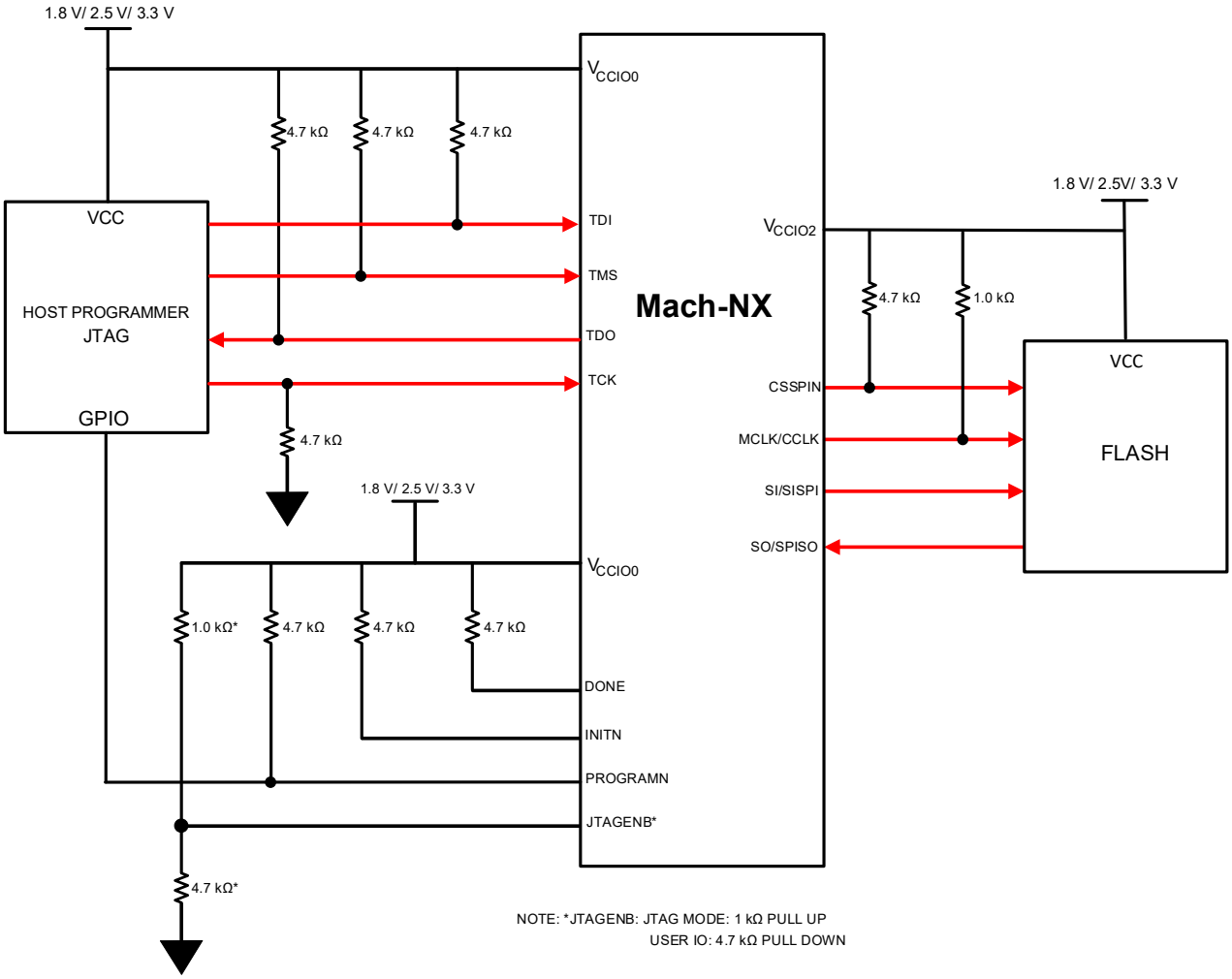

Figure 6.4. Typical Connections for Programming External Flash via JTAG

7. SoC Function Block

7.1. Platform Firmware Resiliance (PFR) Application

The SoC Function Block supports PFR applications. Supported hardware configurations and external circuits are described in the Mach-NX PRF and SoC Function Block Architecture User Guide (FPGA-TN-02230).

7.2. External SPI Flash

External Flash memory is required for SoC Function Block configuration data and firmware storage and must be connected to SoC Function Block QSPI Monitor Channel 0. Ensure that the external SPI Flash V_{CC} and the Mach-NX V_{CCIO0} are at the same level. Ensure that the SPI Flash V_{CC} is at the recommended operating level.

QSPI Monitor Channel 0 can be connected in either SPI or QSPI mode. See Table 5.1 below. After SoC Function Block configuration, QSPI_Monitor Channel 0 is used by the SoC Function Block for SPI/QSPI bus monitoring.

Table 5.1. SoC Function Block Configuration Pin Connection

Pin Name	Pin Function (Configuration Mode)	Pin Direction (Configuration Mode)	Pin Function (Monitor Mode)
QSPI_MON0_CLK	Clock	Output	QSPI_MON0_CLK
QSPI_MON0_CSN	Chip Select	Output	QSPI_MON0_CSN
QSPI_MON0_DQ0	MOSI/SIO0	Output / Bidirectional	QSPI_MON0_DQ0
QSPI_MON0_DQ1	MISO/SIO1	Input / Bidirectional	QSPI_MON0_DQ1
QSPI_MON0_DQ2	SIO2	Bidirectional	QSPI_MON0_DQ2
QSPI_MON0_DQ3	SIO3	Bidirectional	QSPI_MON0_DQ3

It is recommended to use an SPI Flash Device that is supported in Radiant Programmer. To see the supported list of devices, go to the Diamond Programmer, under the Help menu, choose **Help**, then search for **SPI Flash support**.

For SPI Flash devices that are not listed in the **SPI Flash Support**, using the custom flash option may allow a non-supported device to work.

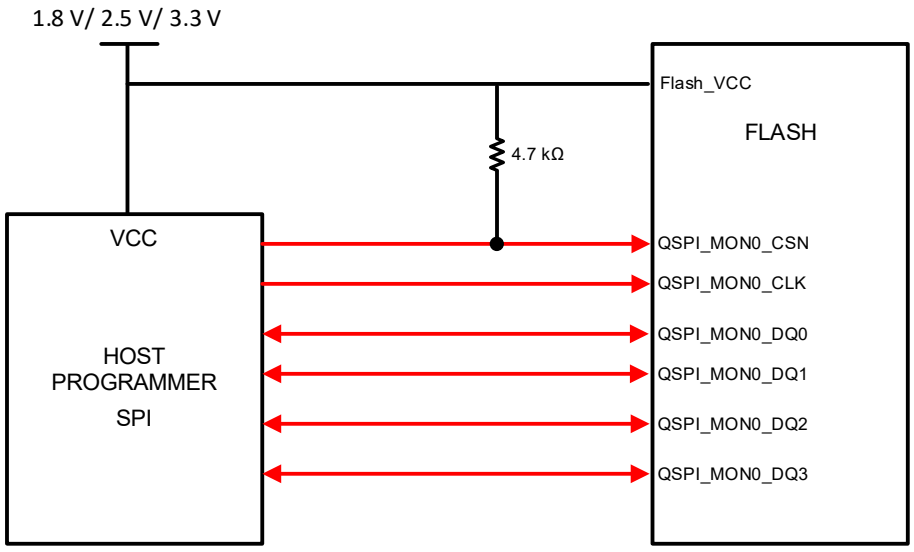

Figure 7.1. Typical Connections for Programming SoC External Flash

8. PROGRAMN Initial Power Considerations

The Mach-NX PROGRAMN is permitted to become a generalpurpose I/O. The PROGRAMN only becomes a general purpose I/O after the configuration bitstream is loaded. When power is applied to the Mach-NX device, the PROGRAMN input performs the PROGRAMN function. It is critical that any signal input to the PROGRAMN have a high-to-low transition period that is longer than the V_{CC} (min) to INITN rising edge time period. Transitions faster than this time period prevent the Mach-NX device from becoming operational. Refer to the description of PROGRAMN in the Mach-NX Programming and Configuration Usage Guide (FPGA-TN-02231).

9. Pinout Considerations

The Mach-NX PLDs support many applications with high-speed interfaces. These include various rule-based pin-outs that need to be understood prior to the implementation of the PCB design. The pin-out selection must be completed with an understanding of the interface building blocks of the FPGA fabric. These include IOLOGIC blocks such as DDR, clock resource connectivity, and PLL usage. Refer to Implementing High-Speed Interfaces with Mach-NX Devices (FPGA-TN-02234) for rules pertaining to these interface types.

10. Clock Inputs

The Mach-NX device provides certain pins for use as clock inputs in each I/O bank. These pins are shared and can alternately be used for General Purpose I/O.

When these pins are used for clocking purposes, you need to pay attention to minimize signal noise on these pins. Refer to Implementing High-Speed Interfaces with Mach-NX Devices (FPGA-TN-02234).

These shared clock input pins, typically named GPLL and PCLK, can be found under the Dual Function column of the pin-list .csv file. High-speed differential interfaces (such as MIPI) received by the FPGA must route their differential clock pair into a pair of inputs that support differential clocking, labeled PCLKTx_y (+true) and PCLKCx_y (-complement).

Note: For single-ended I/Os, use only PCLKT pins as primary CLK pads.

When providing an external reference clock to the FPGA, ensure that the oscillator's output voltage to the FPGA does not exceed the bank's voltage. Good power supply decoupling of the clock oscillator is required to reduce clock jitter. A typical bypassing circuit is shown in Figure 10.1

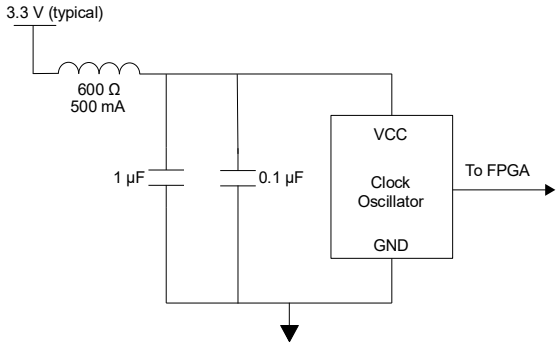

Figure 10.1. Clock Oscillator Bypassing

For differential clock inputs to banks with a V_{CCIO} voltage of 1.5 V or lower, it is recommended to use an HCSL oscillator to keep the clock voltage less than or equal to the bank's V_{CCIO}. An LVDS oscillator can also be used if AC is coupled and then DC is biased at half the V_{CCIO} voltage. Example dual footprint design supporting HCSL and LVDS is shown below in Figure 10.2

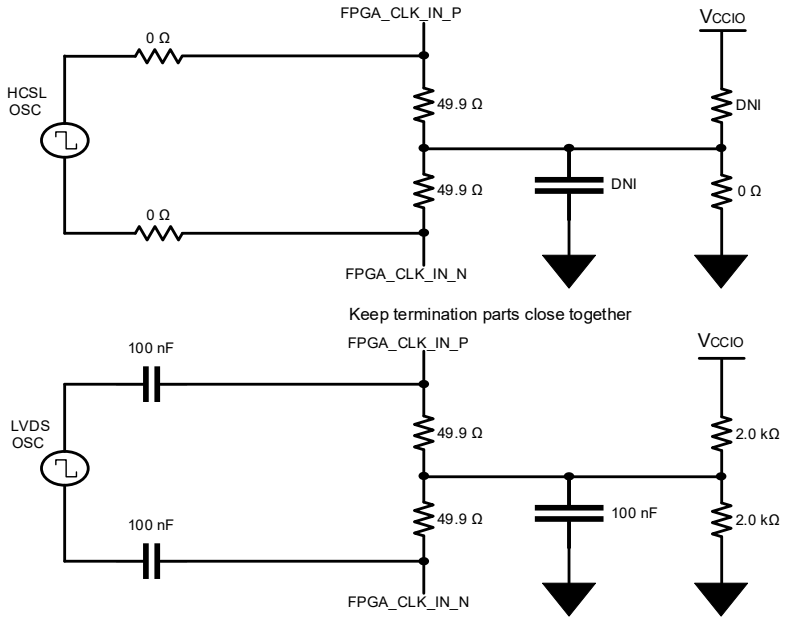

Figure 10.2. PCB Dual Footprint Supporting HCSL and LVDS Oscillators

11. True-LVDS Output Pin Assignments

True-LVDS outputs are on Bank 0 of the Mach-NX devices. When using the LVDS outputs, a 2.5 V or 3.3 V supply needs to be connected to the Bank 0 V_{CCIO} supply rails. Refer to Mach-NX sysI/O Usage Guide (FPGA-TN-02233) for more information.

12. Layout Recommendations

A good design from a schematic should also reflect a good layout for the system design to work without any issues with noise or power distribution. Below are some of the recommended layouts in general.

1. All power should come from power planes. This is to ensure good power delivery and thermal stability.
2. Each power pin has its own decoupling capacitor, typically 100 nF, that should be placed as close as possible to each other.
3. The placement of analog circuits must be away from digital circuits or high-switching components.
4. High-speed signals should have a clearance of five times the trace width of other signals.
5. High-speed signals that transition from one layer to another should have a corresponding transition ground if both reference planes are grounded. If the reference on the other layer is a V_{CC} plane, then a stitching capacitor should be used (ground to V_{CC}).

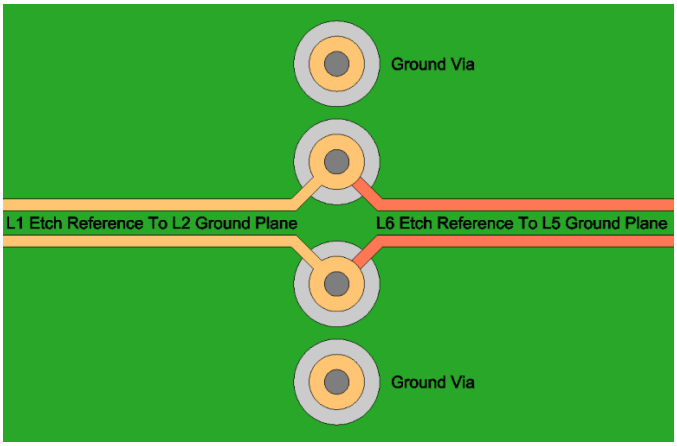

Figure 12.1. Ground Vias Implementation

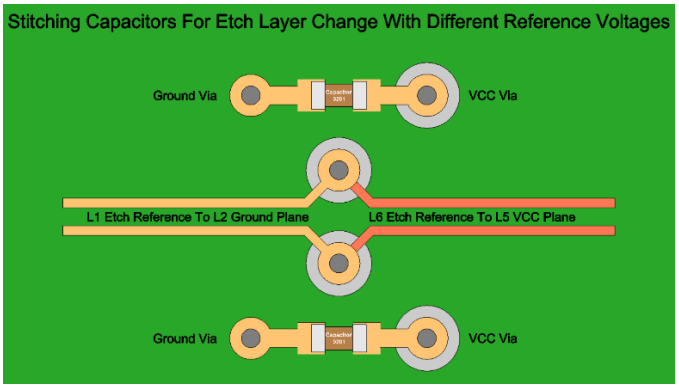

Figure 12.2. Stitching Vias Implementation

6. High-speed signals have a corresponding impedance requirement. Calculate the necessary trace width and trace gap (differential gap) according to the desired stack-up. Verify trace dimensions with the PCB vendor.
7. For differential pairs, be sure to match the length as closely as possible. A good rule of thumb is to match up to ±5mils.

For further information on layout recommendations, refer to:

- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)

13. Checklist

Table 13.1. Hardware Checklist

	Item	OK	N/A
1	Power supply		
1.1	Core supply V_{CC} at 1.0 V		
1.2	I/O power supply V_{CCIO0} at 2.5 V or 3.3 V		
1.3	Auxiliary power supplies V_{AUX} and V_{CCB} at 1.8 V		
1.4	I/O power supplies V_{CCIO1}, V_{CCIO2}, V_{CCIO5}, V_{CCIO6} at 1.2 V to 3.3 V		
1.5	I/O power supplies V_{CCIO3}, V_{CCIO4} at 1.0 V to 1.8 V		
1.6	Power estimation		
2	Configuration		
2.1	Configuration options		
2.2	Pull-up on PROGRAMN, INITN, DONE		
2.3	Pull-up on SSPI mode pins		
2.4	Pull-up on I^2C mode pins		
2.5	JTAG default logic levels		
2.6	PROGRAMN high-to-low transition time period is larger than the $V_{CC\ (min)}$ to INITN rising edge time period		
3	SoC Function Block External SPI flash		
4	I/O pin assignment		
4.1	True LVDS pin assignment considerations		
5	External Flash for PFR		
5.1	Flash voltage should match V_{CCIO0} voltage.		
6	Critical Pinout Selection		
6.1	Pinout is chosen to address FPGA resource connections to I/O logic and clock resources per Implementing High Speed Interfaces with Mach-NX (FPGA-TN-02234).		
6.2	Shared general purpose I/O are used as inputs for FPGA PLL and Clock inputs.		
6.3	Differential pair I/O polarity: I/O are named P[T/B/L/R] [Number]_[A/B] Diff pair positive signal connects to name ending in A, Negative connects to name endng in B.		
6.4	Use a PCLK pin pair for differential clock inputs to ensure the clock signal is routed directly to the edge clock tree.		
6.5	Connect single-ended clock inputs to the FPGA using the PCKLTx_y pins, which supports low skew routing throughout the FGPA fabric. For single-ended I/Os, use only PCLKT pins as primary CLK pads.		
7	Layout Recommendations		
7.1	Power should come from power planes to ensure good power delivery and thermal stability.		
7.2	Placement of analog circuits must be away from digital circuits or high switching components.		
7.3	High speed signals should target clearance of five times trace width from other signal.		
7.4	High speed signals that transition from one layer to another should have a corresponding transition ground if both reference planes are ground, else a stitching capacitor should be used.		
7.5	High speed signals have a corresponding impedance requirement, calculate the necessary trace width and trace gap (differential gap) according to the desired stack-up. Verify trace dimensions with PCB vendor.		

References

- Mach-NX web page
- Mach-NX Family Data Sheet (FPGA-DS-02084)
- Mach-NX sysI/O Usage Guide (FPGA-TN-02233)
- Mach-NX Programming and Configuration Usage Guide (FPGA-TN-02231)
- Mach-NX SFB Hardware Usage Guide (FPGA-TN-02222)
- Mach-NX PRF and SoC Function Block Architecture User Guide (FPGA-TN-02230)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- Implementing High-Speed Interfaces with Mach-NX Devices (FPGA-TN-02234)
- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)
- Electrical Recommendations for Lattice SERDES (FPGA-TN-02077)
- Lattice Radiant FPGA design software
- Lattice Diamond FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at https://www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.3, October 2025

Section	Change Summary
All	Minor editorial fixes.
Disclaimers	Updated this section.
Introduction	Added, *Hardware checklists are developed after evaluation boards and incorporate optimized designs that improve upon the circuitry of the evaluation boards. If you copy circuits from evaluation boards, ensure to optimize your designs according to the hardware checklists,* after the first paragraph of this section.
Clock Inputs	Added note, *For single-ended I/Os, use only PCLKT pins as primary CLK pads.*
Layout Recommendations	Replaced Figure 12.1 PCB Layout Recommendation with Figure 12.1. Ground Vias Implementation and Figure 12.2. Stitching Vias Implementation.
Checklists	• Added item 6 Critical Pinout Section. • Added item 7 Layout Recommendations.

Revision 1.2, March 2024

Section	Change Summary
All	Minor editorial fixes.
Disclaimers	Updated this section.
Power Supply	• Reworked the subsection contents of Subsection 2.1 Power Noise. • Added Subsection 2.2 Power Source.
Power Supply Filtering	• Changed the section title from *Power Estimation* to *Power Supply Filtering*. • Reworked section contents.
Power Sequencing	Added this section.
Power Estimation	Added this section.
Configuration Considerations	• Moved this section to section 6. • Updated the Pin Direction of pin INITN to *I/O with weak pull-up, external pull-up to* V_{CCIO0}, in Table 6.1. Default State of the sysCONFIG™ Pins[1]. • Added Figure 6.1. Typical Connections for Programming SRAM or Internal Flash via JTAG, Figure 6.2. Typical Connections for Programming SRAM or Internal Flash via SSPI, Figure 6.3. Typical Connections for Programming SRAM or Internal Flash via I^2C and Figure 6.4. Typical Connections for Programming External Flash via JTAG.
SoC Function Block	Reworked this section and added Figure 7.1. Typical Connections for Programming SoC External Flash.
Pinout Considerations	Removed subsection 9.1 Clock Inputs.
Clock Inputs	Reworked old Subsection 9.1 Clock Inputs and converted to this main section.
Back Leakage Consideration	Removed this section.
Layout Recommendations	Added this section.
Checklist	Added item no. 5 External Flash for PFR.
References	Added this section.
Technical Support Assistance	Added reference to the Lattice Answer Database on the Lattice website.

Revision 1.1, February 2021

Section	Change Summary
Acronyms in This Document	Added SFB.
All	Changed *SoC* to *SoC Function Block (SFB)*.

Revision 1.0, November 2020

Section	Change Summary
All	Initial release.

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