Lattice Radiant Software 2.1 Release Notes

Welcome to Lattice Radiant® software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs).

What's New in Radiant Software 2.1

- **Device Support:**
  - Certus™-NX Device Family (LFD2NX) offers the following 40K device:
    - 40K (-7/-8/-9) HP/LP 1.0V (COM/IND) – Bitstream Disabled
      - CABGA256

    Note: Bitstream generation is disabled for CrossLink-NX devices for this release, but bitstream for LIFCL-40K is expected to be enabled in the upcoming Service Pack (Radiant 2.1 SP1).

- **Tool and Other Enhancements:**
  - **Physical Designer** – The Physical Designer provides a central location where a user can do all the floor-planning and be able to view the physical layout of the design.
  - **FPGA Libraries -- New Primitives**:
    - CRE (LFD2NX) only. License controlled.)
    - FIFO16K
  - **Pin Migration** - This release adds Pin Migration support, allowing user to view devices that are of the same family and package as your current device and view incompatible pins.
  - **Security** – The LFD2NX device supports user mode Cryptographic Engine (CRE).
  - **SystemVerilog Support** – as follows**:**
    - **Lattice Synthesis Engine** – The ability to read and synthesize SystemVerilog.
    - **File Hierarchy View** – The ability to read and produce a hierarchical file view of design.
    - **Hierarchy Viewer** – The ability to read and produce hierarchical view in Design Constraint Editor, Netlist Analyzer, Floorplan View.
    - **Reveal** – support for SystemVerilog for Reveal Controller, Reveal Analyzer, and Reveal Inserter.

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Radiant software, start with the following procedures. These procedures adapt the project for the changes in Radiant software.

Find out which version of Radiant software your project was created with. Then work through the changes for that and every later version, starting with the earliest and going to the most recent. For example, if your project was created with Radiant software 1.0, you would start with the changes for Radiant software 1.0. After completing those changes, you would work on the changes for Radiant software 2.0, and so on.

Once saved, the project will not be compatible with earlier Radiant software versions.

The following is a list of IP for CrossLink-NX (LIFCL) and Certus-NX (LFD2NX) that must be regenerated in Radiant software v2.1:

- PLL (Phase Locked Loop)

  The following IPs use PLL; therefore, these IPs need be re-generated to update the PLL:

  - GDDR7:1 (7:1 LVDS Interface)
  - DDR_MEM (DDR Memory Interfaces)
  - DDR_Generic (DDR Generic Interfaces)
  - MIPI_DPHY (MIPI Interface)
- ADC (Analog to Digital Converter)
- SEDC (Soft Error Detection/Correction)
- OSC (Oscillator)

Migrating IPs – When an older version IP is migrated to Radiant software 2.1, observe the following:

- For PMIs, user must add the Family attribute in all PMI instantiations (Radiant software 2.0, 2.0 SP1, and 2.1).
- Phase Locked Loop (PLL) IP has been enhanced since Radiant software 2.0 SP1 released. For designs created in previous versions of Radiant software (2.0 or prior), it is necessary to re-generate PLL IP in Radiant software 2.1. Otherwise, Radiant software 2.1 will issue an error when the previous generated PLL IP is detected in the design. Designs created using Radiant Software 2.0 SP1 with PLL will work without any errors.

Update to IO_Type HDL attribute default value – The IO_TYPE HDL attribute default value has been changed since Radiant 2.0 SP1 from LVCMOS18 to LVCMOS33.

Oscillator Frequency Range change in iCE40UP – The “Fast” setting for “Oscillator Frequency Range” in Bitstream Strategy options has been removed in Radiant 2.1. There are two settings only - “Medium” and “Slow.” If you have an earlier project using the “Fast” setting, it will be defaulted to “Slow” in Radiant 2.1. You will need to change it to “Medium” if you want a faster configuration speed.

Large_RAM – If a LARGE_RAM IP generated from a previous Radiant version needs to be re-configured in Radiant 2.1, the IP must be re-created.

Help Resources

Available information resources for the Radiant software include the following:

- Online Help updated with CrossLink-NX and Certus-NX content.
  - To view the Online Help, start the Lattice Radiant software and select the  "Getting Started" icon under Information Center.
- Installation:
  - *Lattice Radiant Software 2.1 Installation Guide for Windows*

    This document provides installation instructions for Windows OS.
  - *Lattice Radiant Software 2.1 Installation Guide for Linux/Ubuntu*

    This document provides installation instructions for Linux/Ubuntu OS.

System Requirements

The following shows the basic system requirements for Radiant software:

- Intel Pentium or Pentium-compatible PC
- 64-bit OS:
  - Windows 7, Windows 8 and 8.1, or Windows 10
  - Red Hat Enterprise Linux 6.9 or 7.4
  - Ubuntu version 16.04 LTS
- Approximately 3 GB free disk space
- Computer Memory Requirement: 8 GB Recommended for running a single project. If running multiple projects, the memory requirement will be higher.
- 1024 X 768 graphics display
- Network adapter for license and network connectivity
- A Web browser with JavaScript capability
- Microsoft Internet Explorer 8 or higher (required for Aldec Active-HDL Lattice Edition simulator)
- Acrobat Reader 5.0 or later

Support for Third-Party Synthesis and Simulator Tools

In addition to the Synopsys Synplify Pro® for Lattice and Aldec Active-HDL™ Lattice Edition tools included with Radiant software suite, the following 3rd-party synthesis and simulator tools are supported by Radiant software:

- **Synthesis Tools:**
  - Synopsys Synplify Pro FPGA synthesis software version Q-2020.03LR
- **Simulator Tools:**
  - Aldec Active-HDL v11.1 or later
  - Mentor Questa® Sim v10.4g or later
    v10.6b or later (supports IP encryption)

Known Issues for Radiant Software 2.1

The following are known Issues for the Radiant software 2.1.

ActiveHDL crashes or errors out unexpectedly with syn.vo file for LSE flow

In some cases, ActiveHDL will crash when trying to compile the syn.vo file and cause whole compile flow failure.
For assistance with this issue, please contact Lattice Technical Support.
Devices affected: CrossLink-NX
Bug number: DNG-8143

MAP incorrectly reports number of DPHY and PCIE/ADC resources for CrossLink-NX QFN72 package.

For assistance with this issue, please contact Lattice Technical Support.
Devices affected: CrossLink-NX
Bug number: DNG-8297

Some IO constraints may not work as expected when designed with SystemVerilog

For assistance with this issue, please contact Lattice Technical Support.
Devices affected: CrossLink-NX, Certus-NX
Bug number: DNG-9019

When Synplify Pro is used for SystemVerilog based designs, some cases may fail when Reveal is inserted.

For assistance with this issue, please contact Lattice Technical Support.
Devices affected: CrossLink-NX, Certus-NX
Bug number: DNG-9103

When simulating Generic DDR, there may be a mismatch in the RTL and post-route simulation. Silicon is not affected.

For assistance with this issue, please contact Lattice Technical Support.
Devices affected: CrossLink-NX, Certus-NX
Bug number: DNG-9639

For SystemVerilog designs using LSE, synthesis fails when "default_nettype" is set to none.

Workaround: Attempt one of the following:

- Do not set "default_nettype none" in RTL.
- Set the top level unit as follows: In Radiant, choose **Project > Active Implementation > Set Top-level Unit.**

Devices affected: CrossLink-NX, Certus-NX
Bug number: DNG-9710