FIR Filter IP

IP Version: v2.3.1

User Guide

FPGA-IPUG-02095-1.6

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Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviations	Definition
DSP	Digital Signal Processing
EBR	Embedded Block RAM
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
IP	Intellectual Property
LSE	Lattice Synthesis Engine
LUT	Look Up Table

1. Introduction

The Lattice Finite Impulse Response (FIR) Filter IP Core is implemented using high performance Digital Signal Processing (DSP) blocks available in Lattice devices. The input data, coefficient, and output data widths are configurable over a wide range. The IP core uses full internal precision while allowing variable output precision with several choices for saturation and rounding. The coefficients of the filter can be specified at generation time and/or reloadable during run-time through input ports.

1.1. Quick Facts

Table 1.1 presents a summary of the FIR filter.

Table 1.1. FIR Filter Quick Facts

IP Requirements	Supported Devices	CrossLink™-NX, Certus™-NX, Certus-NX-RT, CertusPro™-NX, CertusPro-NX-RT, MachXO5™-NX, Lattice Avant™, and Certus-N2
	IP Changes[1]	For a list of changes to the IP, refer to the FIR Filter IP Release Notes (FPGA-RN-02025).
Resource Utilization	Supported User Interface	Native interface, see the Signal Description section.
	Resources	See Appendix A. Resource Utilization
Design Tool Support	Lattice Implementation	IP Core Version 2.3.1 – Lattice Radiant Software 2025.2
	Synthesis	Lattice Synthesis Engine (LSE)
		Synopsys Synplify Pro® for Lattice
	Simulation	For a list of supported simulators, see the Lattice Radiant Software User Guide.

Notes:

1. In some instances, the IP may be updated without changes to the user guide. This user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

1.2. Features

The key features of the FIR Filter include:

- Variable number of taps up to 1024
- Input data and coefficient widths of 4 to 16 bits
- Multi-channel support for up to 64 channels
- Signed or unsigned input data and coefficients
- Coefficients symmetry and negative symmetry optimization
- Re-loadable coefficients support
- Full precision arithmetic
- Selectable output width and precision
- Selectable overflow: wrap-around or saturation
- Selectable rounding: rounding up, round away from zero, round towards zero and convergent rounding
- Width and precision specified using fixed point notations

1.3. Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal names that end with:

- _n are active low, asserted when value is logic 0.
- _i are input signals.
- _o are output signals.
- _io are bi-directional input/output signals.

1.3.3. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

2. Functional Descriptions

2.1. Overview

A top-level block diagram of the FIR Filter IP core is shown in Figure 2.1.

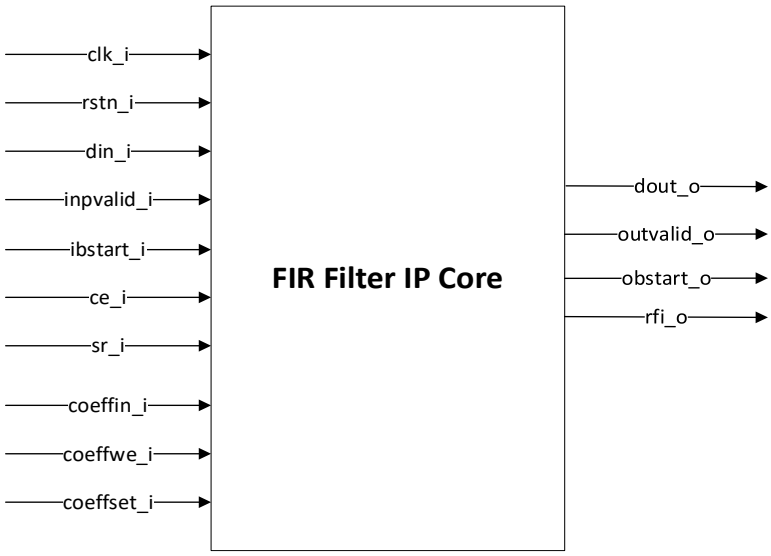

Figure 2.1. FIR Filter IP Core Block Diagram

The functional diagram is shown in Figure 2.2. The data and coefficients are stored in different memories shown as the tap memory and coefficients memory. The symmetry adder, multiplier array and adder tree are implemented using DSP blocks. The symmetry adder is used if the coefficients are symmetric. The adder tree performs the sum of the products. Depending on the configuration, the adder tree, or a part of it, is implemented inside the DSP blocks. The output processing block performs the output width reduction and precision control. This also contains logic to support different types of rounding and overflow. The control logic block manages the scheduling of data and arithmetic operations based on the type of filter.

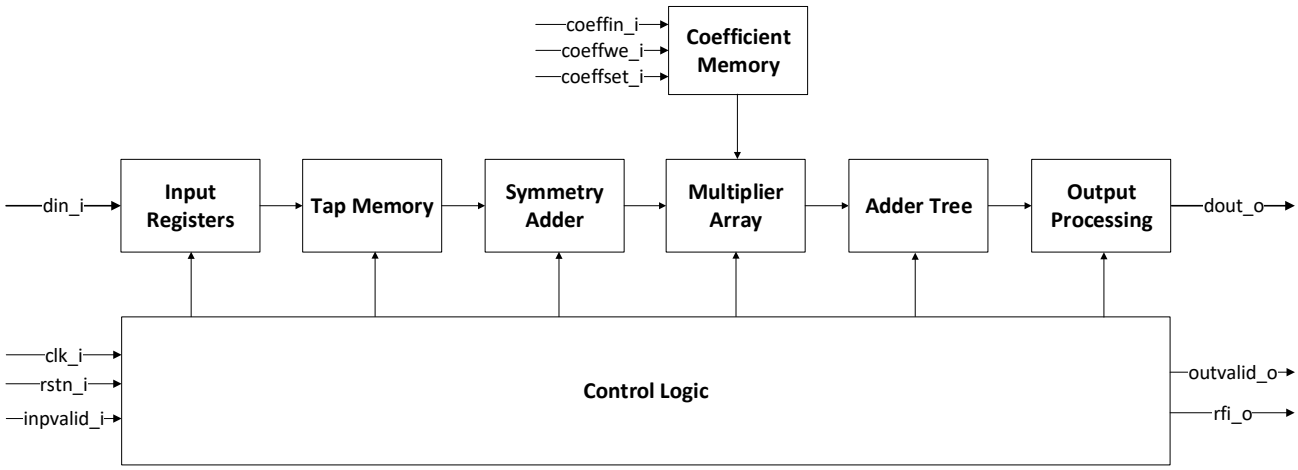

Figure 2.2. FIR Filter IP Core Functional Diagram

2.2. FIR Filter IP Core Architecture

FIR Filter operation on data samples can be described as a sum-of-products operation. For an N-tap FIR filter, the current input sample and (N-1) previous input samples are multiplied by N filter coefficients and the resulting N products are added to give one output sample as shown below:

$$y_n = \sum_{i=0}^{N-1} x_{n-i}h_i = x_n h_0 + x_{n-1}h_1 + \ldots + x_{n-N+1}h_{N-1}$$

wherein: h_n, where n = 0,1,…, N-1, is the impulse response;

x_n, where n = 0,1,…,∞ is the input;

y_n, where *n* = 0,1,…,∞ is the output;

N-1, number of delay elements, represents the order of the filter;

N, the number of current and previous input data samples used for one output sample represents the number of filter taps ().

2.2.1. Direct-form

In the direct-form implementation shown in Figure 2.3, the input samples are shifted into a shift register queue and each shift register is connected to a multiplier. The products from the multipliers are added to get the output sample of the FIR filter.

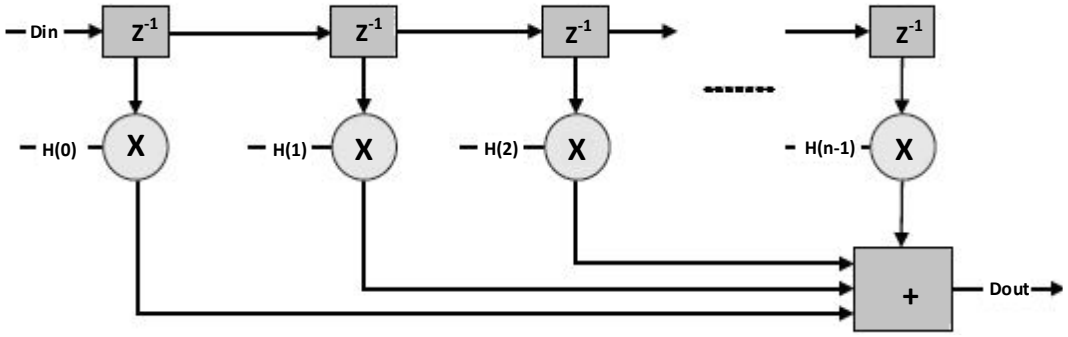

Figure 2.3. Direct-form FIR Filter Implementation

2.2.2. Symmetric

The impulse response for most FIR filters is symmetric. This symmetry can generally be exploited to reduce the arithmetic requirements and produce area-efficient filter realizations. It is possible to use only one half of the multipliers for symmetric coefficients compared to that used for a similar filter with non-symmetric coefficients. An implementation for symmetric coefficients is shown in Figure 2.4.

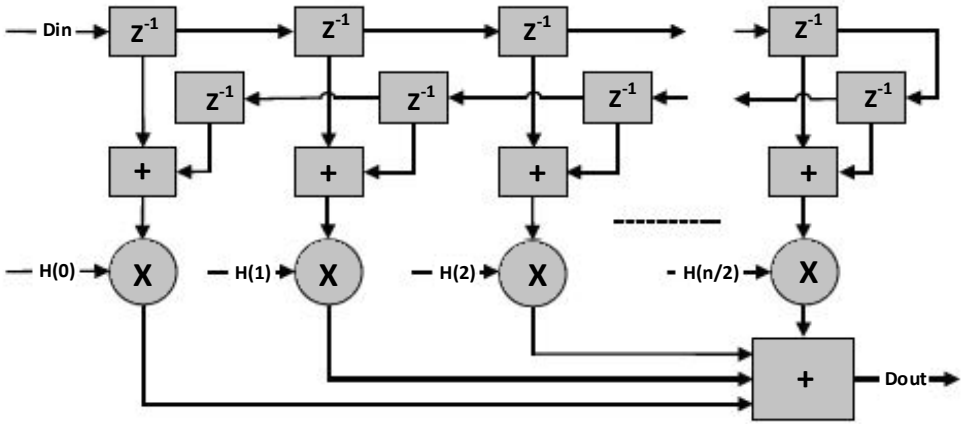

Figure 2.4. Symmetric Coefficients FIR Filter Implementation

2.2.3. Multi-Channel FIR Filter

To implement a multi-channel FIR Filter, the same DSP resources are used in a time-multiplexed way. This uses independent tap and coefficient memories to feed each DSP block. It is also possible to use the same coefficient set for all channels, which in turn required less memory usage.

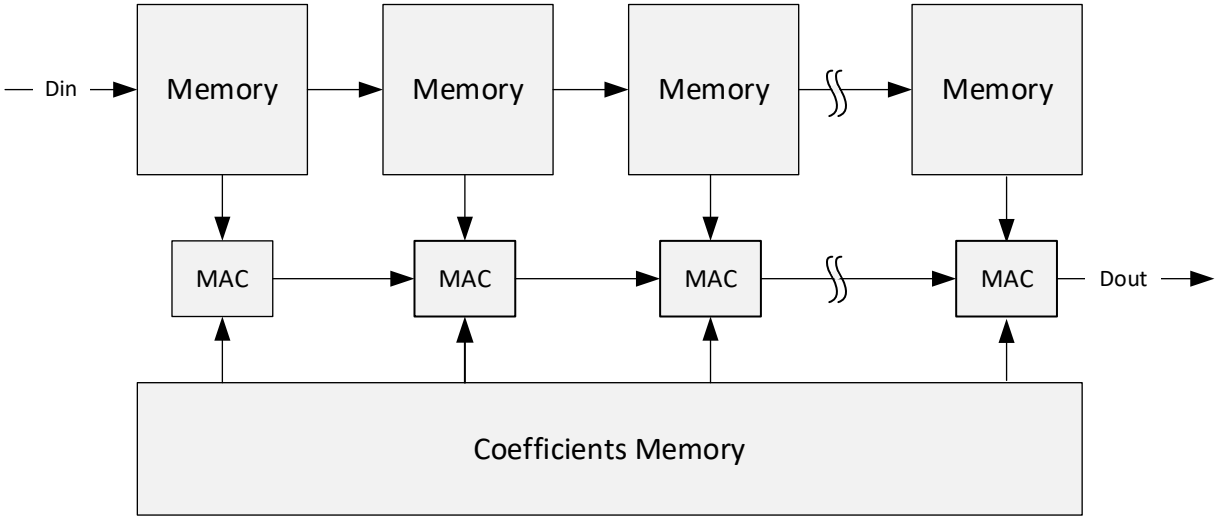

Figure 2.5. Multi-Channel FIR Filter Implementation

2.3. Signal Description

Table 2.1 lists FIR Filter IP Core top-level input and output signals and their descriptions.

Table 2.1. FIR Filter IP Core Signal Description

Port Name	Direction	Bits	Description
Clocks and Reset			
clk_i	Input	1	System clock for data and control inputs and outputs.
rstn_i	Input	1	System wide asynchronous active-low reset signal.
General			
din_i	Input	*Input Data Width*	Input data
inpvalid_i	Input	1	Input valid signal. The input data din_i is read-in only when inpvalid_i is high.
dout_o	Output	*Output Width*	Output data
outvalid_o	Output	1	Output data qualifier. Output data dout_o is valid only when this signal is high.
rfi_o	Output	1	Ready for input. This output, when high, indicates that the IP core is ready to receive the next input data. A valid data may be applied at din only if rfi_o is high during the previous clock cycle.
When *Reloadable coefficients* is selected			
coeffin_i	Input	*Coefficient Width*	Coefficients input. The coefficients have to be loaded through this port in a specific order. All the coefficients need to be loaded in one batch, while keeping the signal coeffwe_i high during the entire duration of loading. After all the coefficients are loaded, the input signal coeffset_i must be pulsed high for one clock cycle for the new coefficients to take effect.
coeffwe_i	Input	1	When asserted, the value on bus coeffin_i is written into coefficient memories.

Port Name	Direction	Bits	Description
coeffset_i	Input	1	This input is used to signal the filter to use the recently loaded coefficient set. This signal must be pulsed high for one clock cycle after the loading the entire coefficient set using coeffin_i and coeffwe_i.
When *Number of Channels* is greater than 1			
ibstart_i	Input	1	Input block start. For multi-channel configurations, this input identifies channel 0 of the input.
obstart_o	Output	1	Output block start. For multi-channel configurations, this output identifies channel 0.
Optional			
ce_i	Input	1	Clock Enable. While this signal is de-asserted, the core ignores all other synchronous inputs and maintain its current state
sr_i	Input	1	Synchronous Reset. When asserted for at least one clock cycle, all the registers in the IP core are initialized to reset state.

2.4. Attribute Summary

Table 2.2 provides the list of user selectable and compile time configurable parameters for the FIR Filter IP Core. The parameter settings are specified using the FIR Filter user interface in Lattice Radiant software.

Table 2.2. Attributes Table

Attribute	Selectable Values	Default	Dependency on Other Attributes
Number of Channels	For the Avant devices: 1–64 For the Nexus devices: Only single channel is supported	1	—
Number of Taps	For the Avant devices: • 1–2048 if *Symmetric Coefficients* is enabled; otherwise, it is 1–1024 • 1–512 if *Number of Channels > 1* For the Nexus devices: 1–64 if *Symmetric Coefficients* is enabled; otherwise, it is 1–32 (depending on the device used)	16	*Symmetric Coefficients == True; Number of Channels > 1*
Reloadable Coefficients	Checked, Unchecked	Unchecked	—
Symmetric Coefficients	Checked, Unchecked	Unchecked	—
Negative Symmetry	Checked, Unchecked	Unchecked	*Symmetric Coefficients == Checked*
Coefficients Set	Common, Separate	Common	Number of Channels > 1
Coefficients Radix	Binary, Hex, Decimal, Floating Point	Decimal	*Reloadable Coefficients == Unchecked*
Coefficients File	Browser Window	None	*Reloadable Coefficients == Unchecked*
Input Data Type	Signed, Unsigned	Signed	—
Input Data Width	4–16	16	—
Input Data Binary Point Position	–2 to *Input Data Width* + 2	0	—
Coefficients Type	Signed, Unsigned	Signed	—
Coefficients Width	4–16	16	—
Coefficients Binary Point Position	–2 to *Coefficients Width* + 2	0	—

Attribute	Selectable Values	Default	Dependency on Other Attributes
Output Width	4 to *Input Data Width* + *Coefficients Width* + ceil ($\log_2$ (*Number of Taps*))	36	—
Output Binary Point Position	4 + *Input Data Binary Point Position* + *Coefficients Binary Point Position* – *Output Width Full Precision* to *Output Width* + *Input Data Binary Point Position* + *Coefficients Binary Point Position* – 4	0	—
Output Width Full Precision	Calculated	36	Display information only
Output Binary Point Position Full Precision	Calculated	0	Display information only
Overflow	Saturation, Wrap Around	Saturation	*Output Width != Output Width Full Precision*
Rounding	None, Rounding Up, Rounding away from zero, Rounding towards zero, Convergent rounding	None	*Output Width != Output Width Full Precision*
Data Memory Type	EBR, Distributed, Auto	EBR	—
Coefficients Memory Type	EBR, Distributed, Auto	EBR	—
Output Buffer Type	EBR, Distributed, Auto	EBR	—
Synchronous Reset (sr_i)	Checked, Unchecked	Unchecked	—
Clock Enable (ce_i)	Checked, Unchecked	Unchecked	—

Table 2.3. Attribute Description

Attribute	Description
General Tab	
Filter Specifications	
Number of Channels	Specifies the number of channels.
Number of Taps	Specifies the number of taps.
Coefficients Specifications	
Reloadable Coefficients	Indicates whether the coefficients are fixed or reloadable. If checked, the coefficients can be reloaded during core operation using the input port coeffin_i. With this option, the desired coefficients must be loaded before the operation of the filter.
Symmetric Coefficients	Indicates that the coefficients are used in symmetric form. If this is checked, the number of taps expected is twice the number of coefficients on the coefficient file.
Negative Symmetry	If this is checked, the coefficients are considered to be negative symmetric. The second half of coefficients are made equal to the negative of the coefficients on the coefficient file.
Coefficients Set	• If *Separate* is selected, each channel has a unique set of coefficients. As an example for Direct-form filter, the required number of coefficients is calculated as Number of Taps × Number of Channels. • If *Common* is selected, all channels use the same set of coefficients given, requiring only one set of coefficients for any number of channels.
Coefficients Radix	This option allows you to specify the radix for the coefficients in the coefficients file with the following considerations: • For decimal radix, the negative values have a preceding unary minus sign. • For hexadecimal (Hex) and binary radices, the negative values must be written in 2's complement form using exactly as many digits as specified by the *Coefficients Width* parameter. • The floating-point coefficients are specified in the form <nn…n>.<dd…d>, where the digits 'n' denote the integer part and the digits 'd' the decimal part. The values of the floating-point coefficients must be consistent with the *Coefficients width* and

Attribute	Description
	Coefficients Binary Point Position parameters. For example, if <nn...n>.<dd...d> is 8.4 and *Coefficients Type* is unsigned, the value of the coefficients should be between 0 and 11111111.1111 (255.9375).
Coefficients File	Indicates the name and location of the coefficients file. This text file has one coefficient per line. If *Coefficients File* is not specified, the filter is initialized with a default coefficient set consisting of 16 coefficients.
I/O Specifications Tab	
Data	
Input Data Type	Shows whether input data type to be used is signed or unsigned. The input data is interpreted as a 2's complement number if the type is signed.
Input Data Width	Specifies the input data width.
Input Data Binary Point Position	This number specifies the bit position of the binary point from the LSB of the input data. If the number is zero, the point is right after LSB; if the number is positive, the point is to the left of LSB; and if the number is negative, the point is to the right of LSB.
Coefficients	
Coefficients Type	This option allows you to specify the coefficients type as signed or unsigned. The coefficient data is interpreted as a 2's complement number if the type is signed.
Coefficients Width	Specifies the coefficients width.
Coefficients Binary Point Position	This number specifies the bit position of the binary point from the LSB of the coefficients. If the number is zero, the point is right after LSB; if the number is positive, the point is to the left of LSB and if the number is negative, the point is to the right of LSB.
Output	
Output Width	Specifies the output data width. The output of the core is usually a part of the full precision output equal to the *Output Width* and extracted based on the different *Output Binary Point Position* parameters. The format for the internal full precision output is displayed as static text next to *Output Width Full Precision*.
Output Binary Point Position	Specifies the bit position of the binary point from the LSB of the actual core output. If the number is zero, the point is right after LSB; if the number is positive, the point is to the left of LSB; and if the number is negative, the point is to the right of LSB. This number, together with the parameter *Output Width*, determines how the actual core output is extracted from the true full precision output. The precision control parameters *Overflow* and *Rounding* are applied respectively when MSBs and LSBs are discarded from the true full precision output.
Output Width Full Precision	Shows the full precision of the output width when the resulting value is not rounded.
Output Binary Point Position Full Precision	Shows the binary point position of the output when the resulting value is not rounded.
Precision Control	
Overflow	This can be used whenever there is a need to drop some of the MSBs from the true output. The following options are supported: • Saturation: The output value is clipped to the maximum if positive or minimum if negative, while discarding the MSBs. • Wrap-around: The MSBs are simply discarded without making any correction.
Rounding	This option allows you to specify the rounding method when there is a need to drop one or more LSBs from the true output. The following five options are supported for rounding: • None: Discards all bits to the right of the output least significant bit and leaves the output uncorrected. • Rounding up – Rounds up to nearest positive number. • Rounding away from zero – Rounds away from zero if the fractional part is exactly one-half. • Rounding towards zero – Rounds towards zero if the fractional part is exactly one-half. • Convergent rounding – Rounds to the nearest even value if the fractional part is exactly one-half.

Attribute	Description
Implementation Tab	
Memory Type	
Data Memory Type	Specifies the type of memory that is used for storing the input data. The following options are supported: • EBR: EBR memories are used for storing the data. • Distributed: Look up table based distributed memories are used for storing data. • Auto: EBR memories are used for memory sizes deeper than 128 locations and distributed memories are used for all other memories.
Coefficients Memory Type	Specifies the type of memory that is used for storing the coefficients. The following options are supported: • EBR: EBR memories are used for storing the data. • Distributed: Look up table based distributed memories are used for storing data. • Auto: EBR memories are used for memory sizes deeper than 128 locations and distributed memories are used for all other memories.
Output Buffer Type	Indicates the memory type for the output buffer.
Optional Ports	
Synchronous Reset (sr_i)	When enabled, this signal resets all the registers in the FIR filter IP core.
Clock Enable (ce_i)	When enabled, this can be used for power saving when the core is not being used. Use of clock enable port increases the resource utilization and may affect the performance due to the increased routing congestion.

2.5. Coefficients Specification

By default, the Reloadable Coefficients is disabled and the coefficients of the filter are specified using a coefficients file. The coefficients file is a text file with one coefficient data per line.

The coefficient values in the file can be in *Binary*, *Decimal*, or *Hexadecimal* radix. *Floating Point* is also supported for decimal values with fractional part, or values less than 1. This can be selected through the *Coefficients Radix* attribute.

For Signed values, Binary and Hexadecimal should be in 2's complement to represent negative values. While for Decimal and Floating Point, the negative unary operator (–) can be used.

The following is an example of a Coefficient File for a 16-tap Direct-form FIR Filter:

- In Binary:
  1111110100000010
  1111100111110010
  0000011101100011
  0000100100011111
  1111001000110010
  1110101100000001
  0010010101011110
  0111001010110001
  0111001010110001
  0010010101011110
  1110101100000001
  1111001000110010
  0000100100011111
  0000011101100011
  1111100111110010
  1111110100000010
- As Floating Point:
  –0.011688232421875

–0.023651123046875
0.0288543701171875
0.0356292724609375
–0.053924560546875
–0.0820159912109375
0.145965576171875
0.4480133056640625
0.4480133056640625
0.145965576171875
–0.0820159912109375
–0.053924560546875
0.0356292724609375
0.0288543701171875
–0.023651123046875
–0.011688232421875

The required number of lines is also dependent on the number of taps, filter architecture, and the number of channels:

- For a Single Channel – Direct-form Filter, the number of coefficients required is the number of taps specified.
- For a Single Channel – Symmetric Filter, the number of coefficients required is half of the number of taps specified (Even Symmetric). If the number of taps is an odd number (Odd Symmetric), the number of coefficients required is half of the number of taps + 1.
- For a multi-channel filter (Number of Channels > 1) and Coefficients Set = *Separate*, the number of coefficients required is the number of coefficients for a Single Channel × the number of channels. As an example for Direct-form Filter, it is calculated as Number of Taps x Number of Channels.
- For a multi-channel filter (Number of Channels > 1) and Coefficients Set = *Common*, the number of coefficients required is the same as for a Single Channel.

When Reloadable Coefficients is enabled, additional ports are used to dynamically write the coefficients into memory. The number of coefficient data loaded is based on the number of required coefficients. Refer to Figure 2.8 for the timing specifications when using dynamic coefficients reloading.

2.6. Timing Specifications

The timing specifications for the FIR Filter IP are as follows:

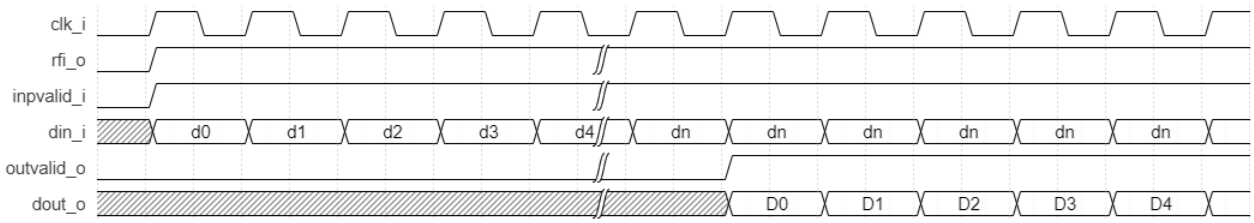

Figure 2.6. Single-Channel FIR Filter with Continuous Input

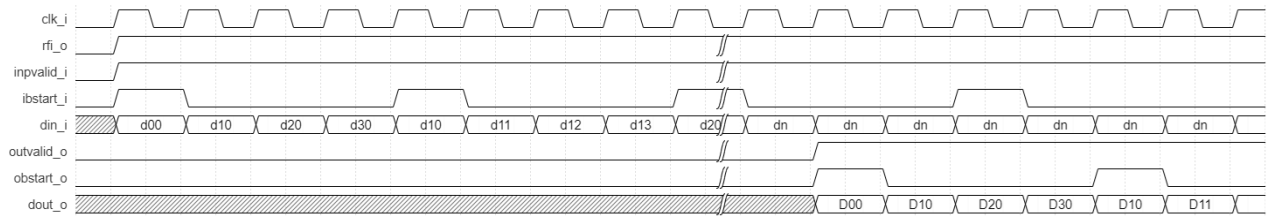

Figure 2.7. Multi-Channel FIR Filter with Continuous Input

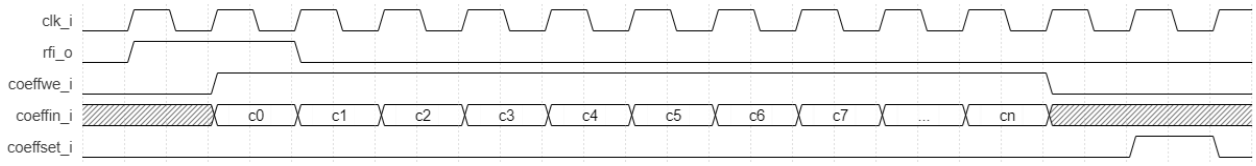

Figure 2.8. Coefficients Reloading

3. IP Generation and Evaluation

This section provides information on how to generate and synthesize FIR Filter IP Core using Lattice Radiant Software, as well as on how to run simulation, synthesis and hardware evaluation. For more details on the Lattice Radiant Software, refer to the Lattice Radiant Software User Guide.

Note: The screenshots provided are for reference only. Details may vary depending on the version of the IP or software being used. If there have been no significant changes to the GUI, a screenshot may reflect an earlier version of the IP.

3.1. Licensing the IP

The FIR Filter IP is provided at no additional cost with the Lattice Radiant software.

3.2. Generation and Synthesis

The Lattice Radiant Software allows you to customize and generate modules and IPs and integrate them into the device architecture. The procedure for generating FIR Filter IP Core in Lattice Radiant Software is described below.

To generate the FIR Filter IP Core:

1. Create a new Lattice Radiant Software project or open an existing project.
2. In the **IP Catalog** tab, double-click on **FIR Filter** under **IP-> DSP** category. The **Module/IP Block Wizard** opens, as shown in Figure 3.1. Enter values in the **Instance name** and the **Create in** fields and click **Next**.

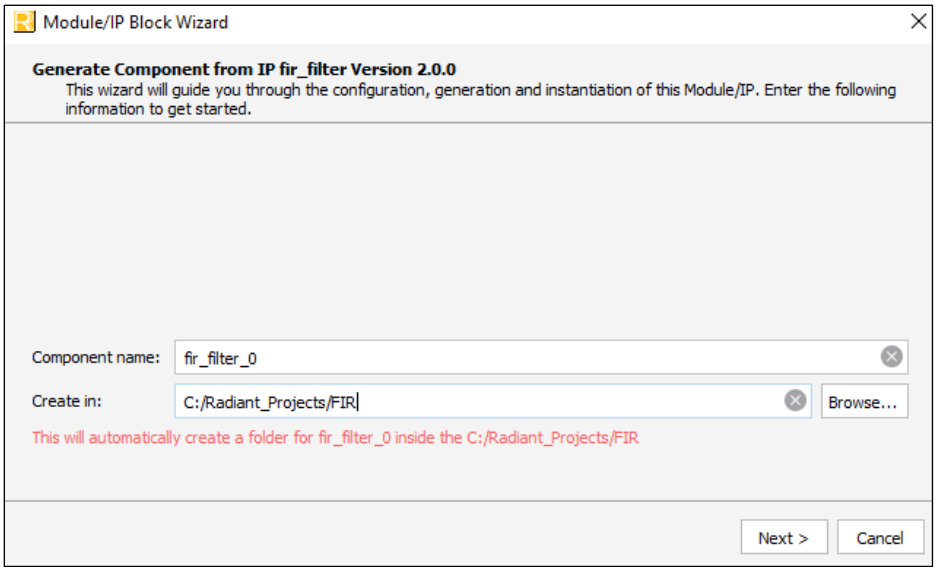

Figure 3.1. Module/IP Block Wizard

3. In the **Module/IP Block Wizard** GUI, customize the selected FIR Filter IP Core using drop-down menus and check boxes. As a sample configuration, see Figure 3.2. For configuration options, see the
4. Attribute Summary section.

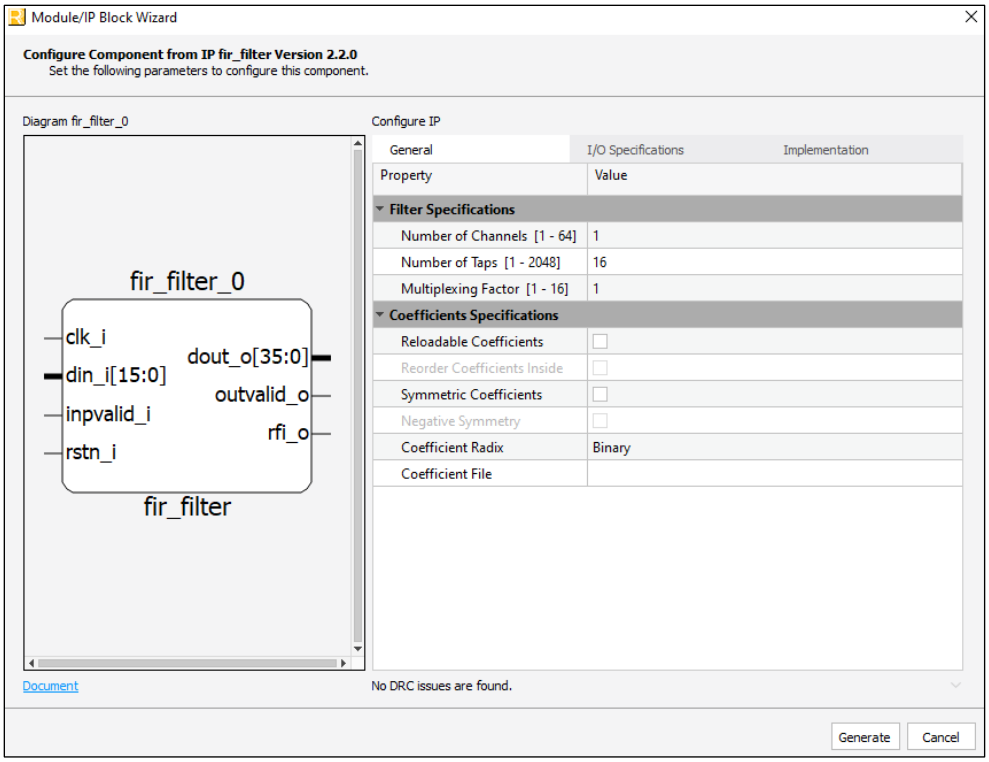

Figure 3.2. Configure User Interface of FIR Filter IP Core

5. Click **Generate**. The **Check Generating Result** dialog box opens, showing design block messages and results as shown in Figure 3.3.

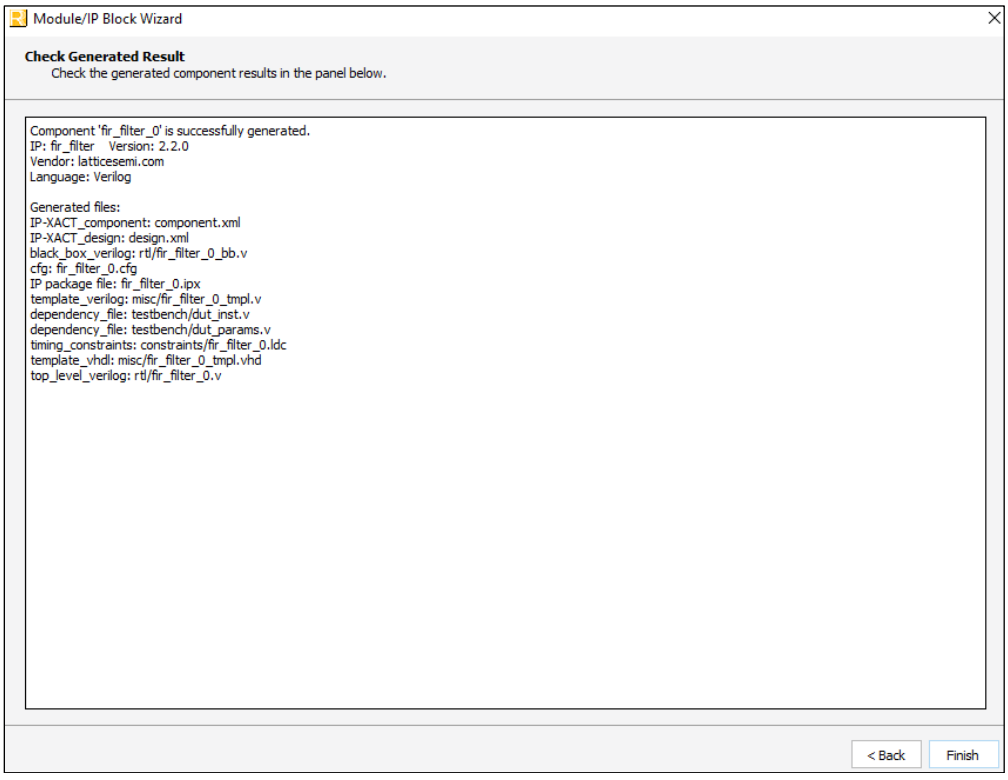

Figure 3.3. Check Generated Result

6. Click the **Finish** button. All the generated files are placed under the directory paths in the **Create in** and the **Instance name** fields shown in Figure 3.1.

The generated FIR Filter IP Core package includes the closed-box (<Instance Name>_bb.v) and instance templates (<Instance Name>_tmpl.v/vhd) that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file (<Instance Name>.v) that can be used as an instantiation template for the IP core is also provided. You may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 3.1.

Table 3.1. Generated File List

Attribute	Description
<Instance Name>.ipx	This file contains the information on the files associated to the generated IP.
<Instance Name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Instance Name>.v	This file provides an example RTL top file that instantiates the IP core.
rtl/<Instance Name>_bb.v	This file provides the synthesis closed-box.
misc/<Instance Name>_tmpl.v misc /<Instance Name>_tmpl.vhd	These files provide instance templates for the IP core.

3.3. Running Functional Simulation

After the IP is generated, running functional simulation can be performed using different available simulators. The default simulator already has pre-compiled libraries ready for simulation. Choosing a non-default simulator, however, may require additional steps.

To run functional simulation using the default simulator:

1. Click the  button located on the **Toolbar** to initiate the **Simulation Wizard**, as shown in Figure 3.4.

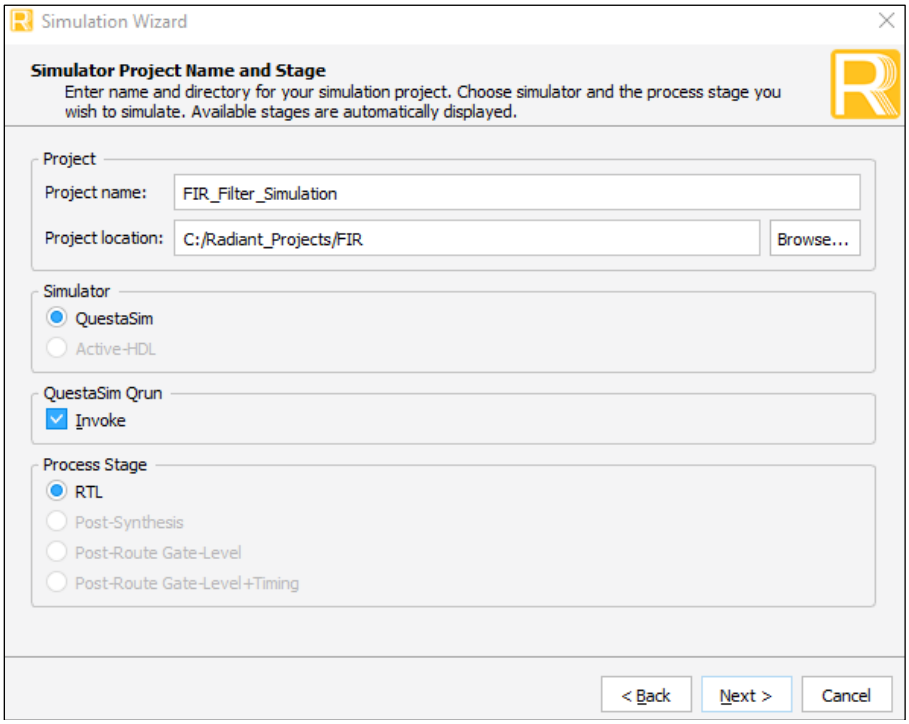

Figure 3.4. Simulation Wizard

2. Click **Next** to open the **Add and Reorder Source** window, as shown in Figure 3.5.

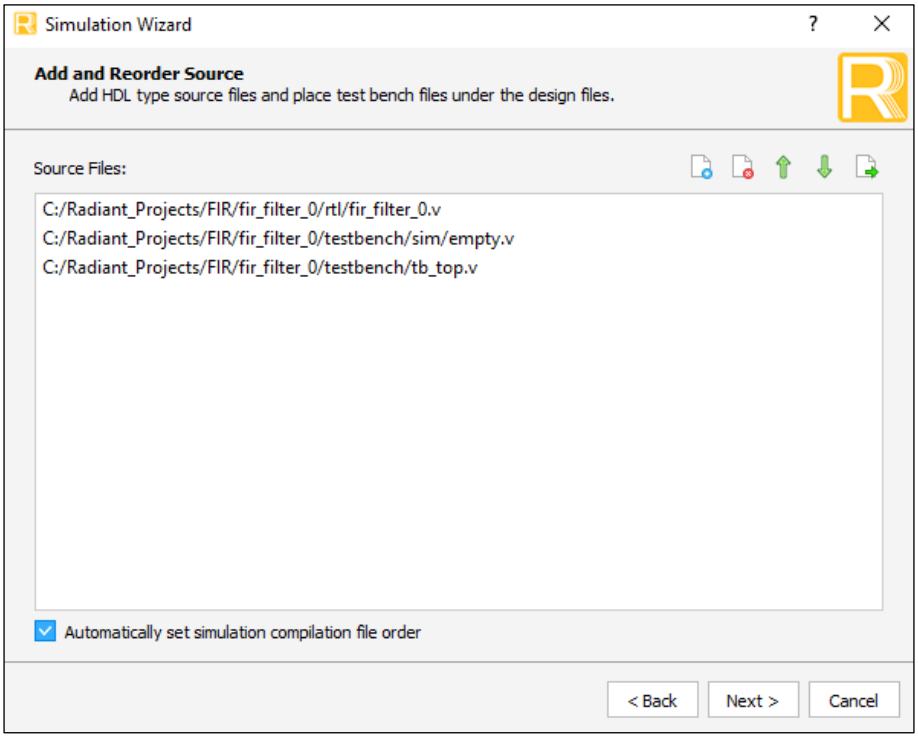

Figure 3.5. Adding and Reordering Source

3. Click **Next**. The **Summary** window is shown. Click **Finish** to run the simulation.

   Note: It is necessary to follow the procedure above until it is fully automated in the Lattice Radiant Software Suite.

   The result of the simulation in our example is provided in Figure 3.6.

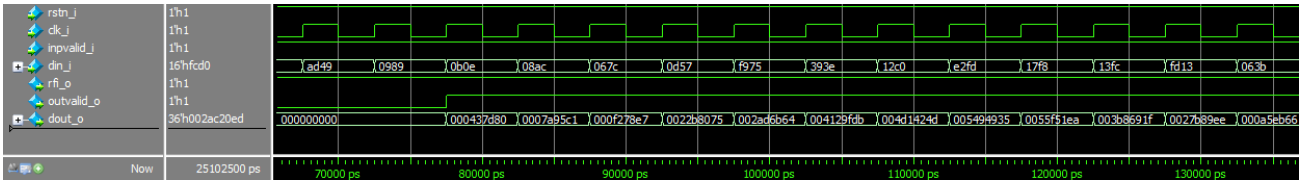

Figure 3.6. Simulation Waveform

3.3.1. Functional Simulation Results

The included testbench simulates a basic FIR Filter operation by generating a sample noisy signal from IP generation, then using the same filter coefficients to calculate the expected outputs given the FIR Filter configuration. The sample noisy signal is created by mixing a high frequency signal with varying amplitude to a lower frequency sinusoidal signal.

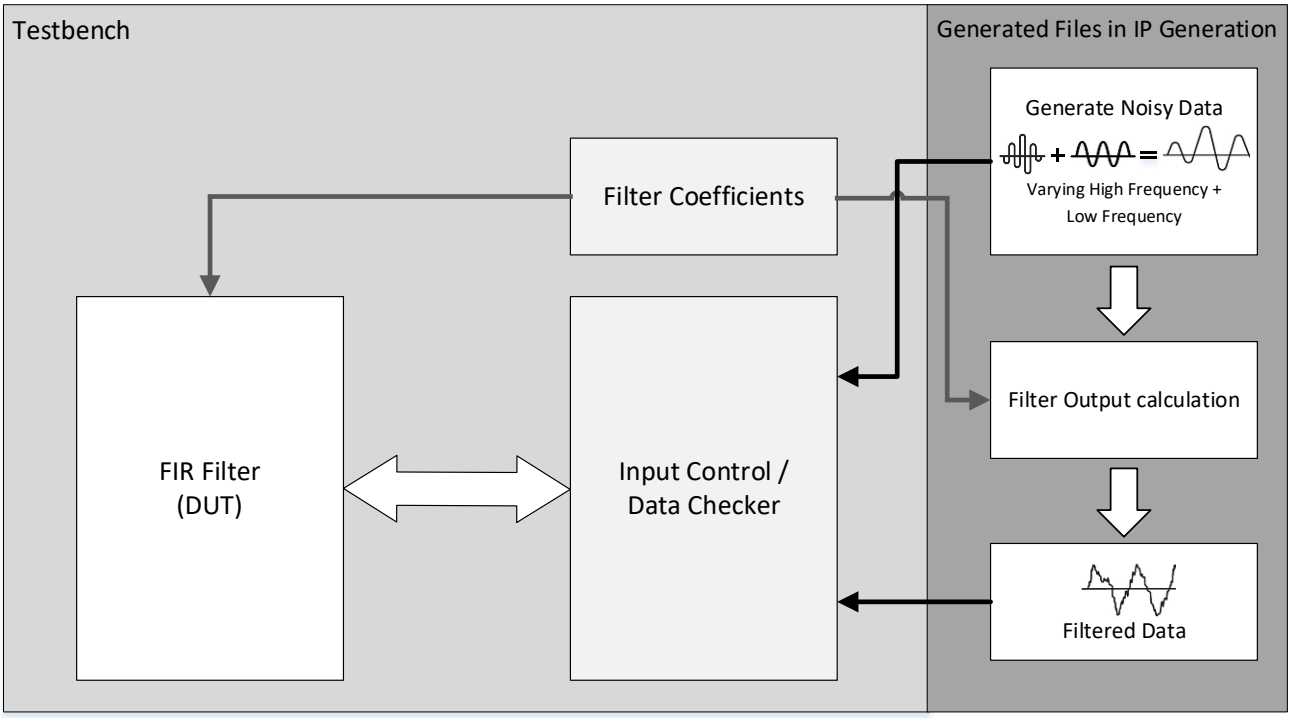

Figure 3.7. Simulation Testbench Diagram

Upon IP Generation, memory files containing the stream of input data, and the expected output data are generated. If Reloadable Coefficients are enabled, it also generates the applicable Coefficients Memory file. The expected simulation results output a 'SIMULATION PASSED' message in the logs, and the input noisy signal and expected output can be observed in simulation if Analog formatting is set.

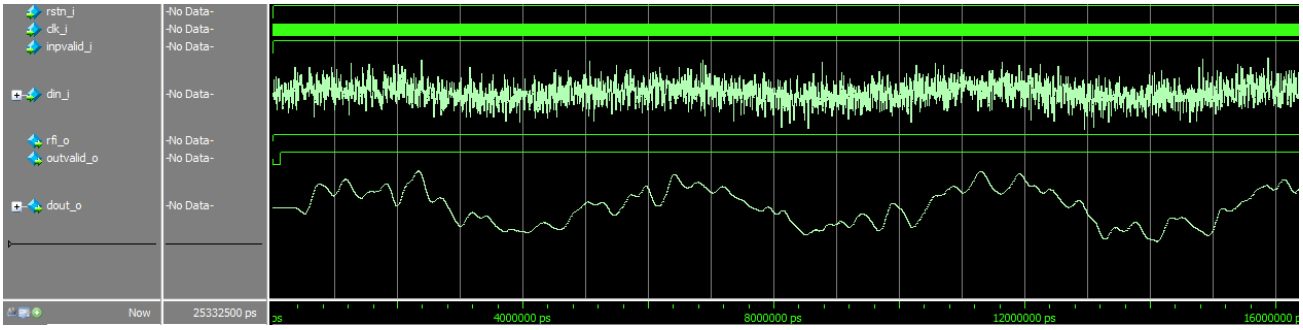

Figure 3.8. Sample Simulation Results (Symmetric, 64-tap Filter)

3.4. Hardware Evaluation

The FIR Filter IP Core supports Lattice's IP hardware evaluation capability. This makes it possible to create versions of the IP core that operates in hardware for approximately four hours without requiring the purchase of an IP license. It may also be used to evaluate the core in hardware in user-defined designs. The hardware evaluation capability may be enabled/disabled in the Strategy dialog box. It is enabled by default. To change this setting, go to Project > Active Strategy > LSE/Synplify Pro Settings.

Appendix A. Resource Utilization

Table A.1 shows the resource utilization of the FIR Filter IP Core for the LIFCL-33-8USG84C device using Synplify Pro of the Lattice Radiant Software 2024.2. Default configuration is used, and some attributes are changed from the default value to show the effect on the resource utilization.

The default configurations are: Number of Taps=16, Reloadable Coefficients = False, Symmetric Coefficients = False, Input/Coefficients Type = Signed, Input/Coefficients Width = 16, Output Width = 36

Table A.1. LIFCL-33-8USG84C Device Resource Utilization

Configuration	Clk Fmax (MHz)[1]	Registers	LUTs	EBRs	DSPs[2]
Default	200.000	100	103	0	16
Reloadable Coefficients: true, Reorder Coefficients Inside: true, Others = Default	200.000	686	135	0	16
Number of Taps: 32 Symmetric Coefficients: true Others: Default	200.000	100	103	0	16
Number of Taps: 28 Input Data Type: Unsigned Overflow: Saturation Rounding: Rounding up Others: Default	200.000	100	103	0	28
Number of Taps: 32 Symmetric Coefficients: true Coefficient Radix: Floating Point Coefficient File: provided Coefficients Binary Point Position: 4 Output Binary Point Position: 4	200.000	100	103	0	16

Notes:

1. Fmax is generated when the FPGA design only contains FIR Filter IP Core, and the target frequency is 200 MHz. These values may be reduced when user logic is added to the FPGA design.
2. Values are based on the number of 18X18 Multipliers.

Table A.2 shows the resource utilization of the FIR Filter IP Core for the LFMXO5-25-7BBG400C device using Synplify Pro of the Lattice Radiant Software 2024.2. Default configuration is used, and some attributes are changed from the default value to show the effect on the resource utilization.

The default configurations are: Number of Taps=16, Reloadable Coefficients = False, Symmetric Coefficients = False, Input/Coefficients Type = Signed, Input/Coefficients Width = 16, Output Width = 36

Table A.2. LFMXO5-25-7BBG400C Device Resource Utilization

Configuration	Clk Fmax (MHz)[1]	Registers	LUTs	EBRs	DSPs[2]
Default	200.000	100	103	0	16
Reloadable Coefficients: true, Reorder Coefficients Inside: true, Others = Default	200.000	686	135	0	16
Number of Taps: 32 Symmetric Coefficients: true Others: Default	200.000	100	103	0	16
Number of Taps: 28 Input Data Type: Unsigned Overflow: Saturation Rounding: Rounding up Others: Default	200.000	100	103	0	28
Number of Taps: 32	200.000	100	103	0	16

Configuration	Clk Fmax (MHz)[1]	Registers	LUTs	EBRs	DSPs[2]
Symmetric Coefficients: true Coefficient Radix: Floating Point Coefficient File: provided Coefficients Binary Point Position: 4 Output Binary Point Position: 4					

Notes:

1. Fmax is generated when the FPGA design only contains FIR Filter IP Core, and the target frequency is 200 MHz. These values may be reduced when user logic is added to the FPGA design.
2. Values are based on the number of 18X18 Multipliers.

Table A.3 shows the resource utilization of the FIR Filter IP Core for the LAV-AT-G70-1LFG676C device using Synplify Pro of the Lattice Radiant Software 2024.2. Default configuration is used, and some attributes are changed from the default value to show the effect on the resource utilization.

The default configurations are: Number of Taps=16, Reloadable Coefficients = False, Symmetric Coefficients = False, Input/Coefficients Type = Signed, Input/Coefficients Width = 16, Output Width = 36

Table A.3. LAV-AT-G70-1LFG676C Device Resource Utilization

Configuration	Clk Fmax (MHz)	Registers	LUTs	EBRs	DSPs
Default (Coefficients file provided)	250.000	63	13	0	16
Reloadable Coefficients: true Others = Default	250.000	608	112	1	16
Number of Taps: 255 Symmetric Coefficients: true Reloadable Coefficients: true Others: Default	151.217	4225	630	1	128
Number of Taps: 512 Coefficient Radix: Floating Point Coefficients Binary Point Position: 16 Output Binary Point Position: 16 Output Data Width: 40	91.988	477	95	3	512
Number of Taps: 64 Number of Channels: 4	183.925	57	75	64	64
Number of Taps: 300 Number of Channels: 8 Reloadable Coefficients: true Output Data Width: 38	154.440	9960	163	301	300

Table A.4 shows the resource utilization of the FIR Filter IP Core for the LAV-AT-E70-3LFG676C device using Synplify Pro of the Lattice Radiant Software 2024.2. Default configuration is used, and some attributes are changed from the default value to show the effect on the resource utilization.

The default configurations are: Number of Taps=16, Reloadable Coefficients = False, Symmetric Coefficients = False, Input/Coefficients Type = Signed, Input/Coefficients Width = 16, Output Width = 36

Table A.4. LAV-AT-E70-3LFG676C Device Resource Utilization

Configuration	Clk Fmax (MHz)	Registers	LUTs	EBRs	DSPs
Default (Coefficients file provided)	250.000	63	13	0	16
Reloadable Coefficients: true Others = Default	250.000	608	112	1	16
Number of Taps: 255 Symmetric Coefficients: true	188.182	4225	630	1	128

Configuration	Clk Fmax (MHz)	Registers	LUTs	EBRs	DSPs
Reloadable Coefficients: true Others: Default					
Number of Taps: 512 Coefficient Radix: Floating Point Coefficients Binary Point Position: 16 Output Binary Point Position: 16 Output Data Width: 40	121.286	477	95	3	512
Number of Taps: 64 Number of Channels: 4	234.522	57	75	64	64
Number of Taps: 300 Number of Channels: 8 Reloadable Coefficients: true Output Data Width: 38	171.262	9960	163	301	300

References

- FIR Filter IP Release Notes (FPGA-RN-02025)
- Avant-E web page
- Avant-G web page
- Avant-X web page
- Certus-N2 web page
- Certus-NX web page
- CertusPro-NX web page
- CrossLink-NX web page
- MachXO5-NX web page
- Lattice Radiant Software web page
- Lattice Solutions IP Cores web page
- Lattice Insights web page for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Note: In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

Revision 1.6, IP v2.3.1, December 2025

Section	Change Summary
Abbreviations in This Document	Removed *OPN*.

Quick Facts	• In Table 1.1. FIR Filter Quick Facts:
	  • Updated from *IP Core v2.3.0* to *IP Core v2.3.1*.
	  • Updated from *Lattice Radiant software 2025.1* to *Lattice Radiant software 2025.2*.
	• Added note, *In some instances, the IP may be updated without changes to the user guide. This user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.*

IP Generation and Evaluation	• Added note, *The screenshots provided are for reference only. Details may vary depending on the version of the IP or software being used. If there have been no significant changes to the GUI, a screenshot may reflect an earlier version of the IP.* • Updated content of Licensing the IP: *The FIR Filter IP is provided at no additional cost with the Lattice Radiant software.*
Ordering Part Numbers	Removed this section.
Revision History	Added note.

Document Revision 1.5, IP v2.3.0, July 2025

Section	Change Summary

Introduction	Table 1.1. FIR Filter Quick Facts:
	• IP Requirements
	  • Changed *FPGA Families Supported* to *Supported Devices*.
	  • Removed *CrossLinkU-NX* from *Supported Devices*.
	  • Added *Certus-NX-RT* and *CertusPro-NX-RT* to *Supported Devices*.
	• Resource Utilization
	  • Removed *Targeted Devices*.
	• Lattice Implementation
	  • Updated *IP* and the *Lattice Radiant Software* version.

Functional Descriptions	• Updated Figure 2.5. Multi-Channel FIR Filter Implementation. • Removed *Frequency Constraint (MHz)* from Table 2.2. Attributes Table. • Removed *Synthesis Options* from Table 2.3. Attribute Description.
IP Generation and Evaluation	3.3 Running Functional Simulation: • Updated Figure 3.6. Simulation Waveform. • Added sub-chapter Functional Simulation Results.
Ordering Part Numbers	Updated instance of *Multi-site Perpetual* to *Single Seat Perpetual*.

Document Revision 1.4, IP v2.2.0, December 2024

Section	Change Summary
All	• Updated the document title from FIR Filter IP Core – Lattice Radiant Software to FIR Filter IP. • Added the IP version information on the cover page. • Made editorial fixes.
Inclusive Language	Added boilerplate.

Introduction	• In Table 1.1. FIR Filter Quick Facts:
	  • Added *Certus-N2* to *FPGA Families Supported*.
	  • Added the *LFD2NX-9*, *LFD2NX-28*, and *LN2-CT-20* devices to *Targeted Devices*.
	  • Add *IP Changes*.

Section	Change Summary
	• Updated *Resources* and *Lattice Implementation*. • Updated the Features section.

Functional Descriptions	• Added Figure 2.5. Multi-Channel FIR Filter Implementation.
	• In Table 2.1. FIR Filter IP Core Signal Description:
	  • Updated the *Bits* column for *coeffin_i*.
	  • Added information for *When Number of Channels is greater than 1*.
	  • Removed *Notes*.
	• Added the Number of Channels and Coefficients Set attributes and removed the Multiplexing Factor, Reorder Coefficients Inside and Half Band attributes from Table 2.2. Attributes Table and Table 2.3. Attribute Description.
	• In Table 2.2. Attributes Table, updated the Selectable Values for the following attributes:
	  • *Number of Taps* (updated *Dependency on Other Attributes* as well)
	  • *Input Data Width*
	  • *Coefficients Width*
	  • *Frequency Constraint (MHz)*
	• Added the Coefficients Specification and Timing Specifications sections.

IP Generation and Evaluation	• Updated Figure 3.2. Configure User Interface of FIR Filter IP Core and Figure 3.3. Check Generated Result. • Updated black box to closed-box in the Generation and Synthesis section.
Ordering Part Numbers	Added the *Certus-N2* OPNs and updated the *Bundled* OPNs.
Appendix A. Resource Utilization	Updated resource utilizations for the Lattice Radiant software version 2024.2.
References	Updated this section.

Document Revision 1.3, Lattice Radiant SW Version 2024.1, June 2024

Section	Change Summary
Disclaimers	Updated this section.
Acronyms in This Document	Updated this section.

Introduction	• Table 1.1. FIR Filter Quick Facts:
	  • added *Lattice Avant* and *CrossLinkU-NX* to FPGA Families Supported;
	  • added *LAV-AT-E70*, *LAV-AT-G70*, *LAV-AT-X70*, *LFMXO5-55T*, *LFMXO5-100T*, *LIFCL-33*, *LIFCL-33U*, and *LFCPNX-50* to Targeted Devices;
	  • updated Resource to *See Table A.1, Table A.2, Table A.3, and Table A.4*;
	  • updated Lattice Implementation to *IP Core Version 2.0.0 – Lattice Radiant Software 2.2 or later.*
	• Features:
	  • Changed *Variable number of taps up to 56* to *Variable number of taps*.

Functional Descriptions	Table 2.2. Attributes Table: • updated Selectable Values of the Number of Taps attribute to *1–56 if Half Band == True or Symmetric Coefficients = True otherwise, it is 1–28 (depending on device used)*; • added the default value of the Output Width attribute: *36*; • updated Selectable Values of the Output Binary Point Position attribute *to 4 + Input Data Binary Point Position + Coefficients Binary Point Position – Output Width Full Precision to Output Width + Input Data Binary Point Position + Coefficients Binary Point Position – 4*.
IP Generation and Evaluation	Updated Figure 3.1. Module/IP Block Wizard, Figure 3.2. Configure User Interface of FIR Filter IP Core, Figure 3.3. Check Generated Result, and Figure 3.4. Simulation Wizard.
Ordering Part Numbers	Updated the OPNs for the FIR Filter IP core.
Resource Utilization	• Replaced the original Table A.1 with Table A.1. Resource Utilization (LIFCL-33-8USG84C) and updated corresponding description for the table.

Section	Change Summary
	• Replaced the original Table A.2 with Table A.2. Resource Utilization (LFMXO5-25-7BBG400C) and updated corresponding description for the table. • Added Table A.3. Resource Utilization (LAV-AT-E70-3LFG676C), Table A.4. Resource Utilization (LAV-AT-G70-1LFG676C), and corresponding descriptions for each table.
References	• Added links to Avant-E Family Devices web page, MachXO5-NX Family Devices web page, CrossLink-NX Family Devices web page, CertusPro-NX Family Devices web page, Certus-NX Family Devices web page, and Lattice Insights for Lattice Semiconductor Training Series and Learning Plans.
Technical Support Assistance	Added the link to Lattice Answer Database.

Document Revision 1.2, Lattice Radiant SW Version 3.2, May 2022

Section	Change Summary
Introduction	Updated Table 1.1. FIR Filter Quick Facts: • Added MachXO5-NX to FPGA Families Supported • Added LFMXO5-25 to Targeted Devices • Added Table A.2. Resource Utilization (LFMXO5-25-7BBG400I) to Resources
IP Generation and Evaluation	Updated Figure 3.1. Module/IP Block Wizard, Figure 3.2. Configure User Interface of FIR Filter IP Core and Figure 3.3. Check Generated Result.
Ordering Part Numbers	Added the following part numbers: • FIR-COMP-XO5-U - FIR Filter Generator for MachXO5-NX - Single Design License • FIR-COMP-XO5-UT - FIR Filter Generator for MachXO5-NX - Site License • FIR-COMP-XO5-US - FIR Filter Generator for MachXO5-NX - 1 Year Subscription License
Appendix A. Resource Utilization	Updated resource utilization for *LFMXO5-25-9BBG400I* and *LFMXO5-25-7BBG400I*.

Document Revision 1.1, Lattice Radiant SW Version 3.0, June 2021

Section	Change Summary

Introduction	• Removed last paragraph.
	• Updated Table 1.1. FIR Filter Quick Facts.
	  • Revised Supported FPGA Families
	  • Revised Targeted Devices
	  • Revised Lattice Implementation.

Ordering Part Numbers	Added part numbers.

Document Revision 1.0, Lattice Radiant SW Version 2.2, October 2020

Section	Change Summary
All	Initial release.

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