MIPI CSI-2 Virtual Channel Aggregation with CrossLink-NX Devices

Reference Design

FPGA-RD-02148-1.2

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Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AP	Application Processor
CSI-2	Camera Serial Interface 2
DDR	Double Data Rate
EBR	Embedded Block RAM
ECC	Error Correction Code
HS	High Speed
ID	Identification Data
LP	Low Power
LUT	Look Up Table
MIPI	Mobile Industry Processor Interface
PLL	Phase Locked Loop
GPLL	General Purpose PLL
RX	Receiver
TDM	Time Domain Multiplexing
TX	Transmitter
VC	Virtual Channel

1. Introduction

The majority of image sensors and application processors (AP) in the consumer market use the Mobile Industry Processor Interface (MIPI®) Camera Serial Interface 2 (CSI-2) as a video signal interface. In some cases, the AP has to take multiple image data for various applications without increasing the physical interface signals.

The Lattice Semiconductor MIPI CSI-2 virtual channel aggregation reference design with CrossLink™- NX devices offers up to eight-channel aggregation. A different virtual channel identification (ID) is assigned to each receiver (RX) channel. CrossLink-NX devices have two MIPI hard macro IPs which can be used as MIPI TX or RX module (D-PHY Hard IP). The RX module can also be realized by a soft macro utilizing general DDR modules (D-PHY Soft IP).

The reference design is available on the MIPI CSI-2 Virtual Channel Aggregation Reference Design web page.

1.1. Supported Device and IP

This reference design supports the following devices with IP versions.

Table 1.1. Supported Device and IP

Device Family	Part Number	Compatible IP
CrossLink-NX	LIFCL-40 LIFCL-17	D-PHY Receiver IP version 2.0.0 D-PHY Transmitter IP version 2.3.0

The IPs above are supported by the Lattice Radiant™ software version 2025.1 or later.

1.2. Features List

- Two to eight independent RX channels can be aggregated.
- You can assign a unique virtual channel ID (0 to 15) to each RX channel.
- Each RX channel can have one, two, or four lanes.
- Number of TX lanes can be one, two, or four.
- Maximum RX bandwidth is 1.5 Gbps per lane.
- Maximum TX bandwidth is 2.5 Gbps per lane by using Hard D-PHY.
- Non-continuous clock mode on RX channels is possible as long as the continuous byte clock with the same frequency as the stoppable byte clock can be obtained internally or fed directly from the pin. Each RX clock can be independent and does not have to come from the same clock source.

1.3. Block Diagram

Figure 1.1 shows the block level diagram of the MIPI CSI-2 virtual channel aggregation reference design with eight RX channels.

As TX D-PHY PLL has an input clock frequency requirement of between 24 MHz and 200 MHz, another on-chip GPLL may have to be used to create an appropriate clock.

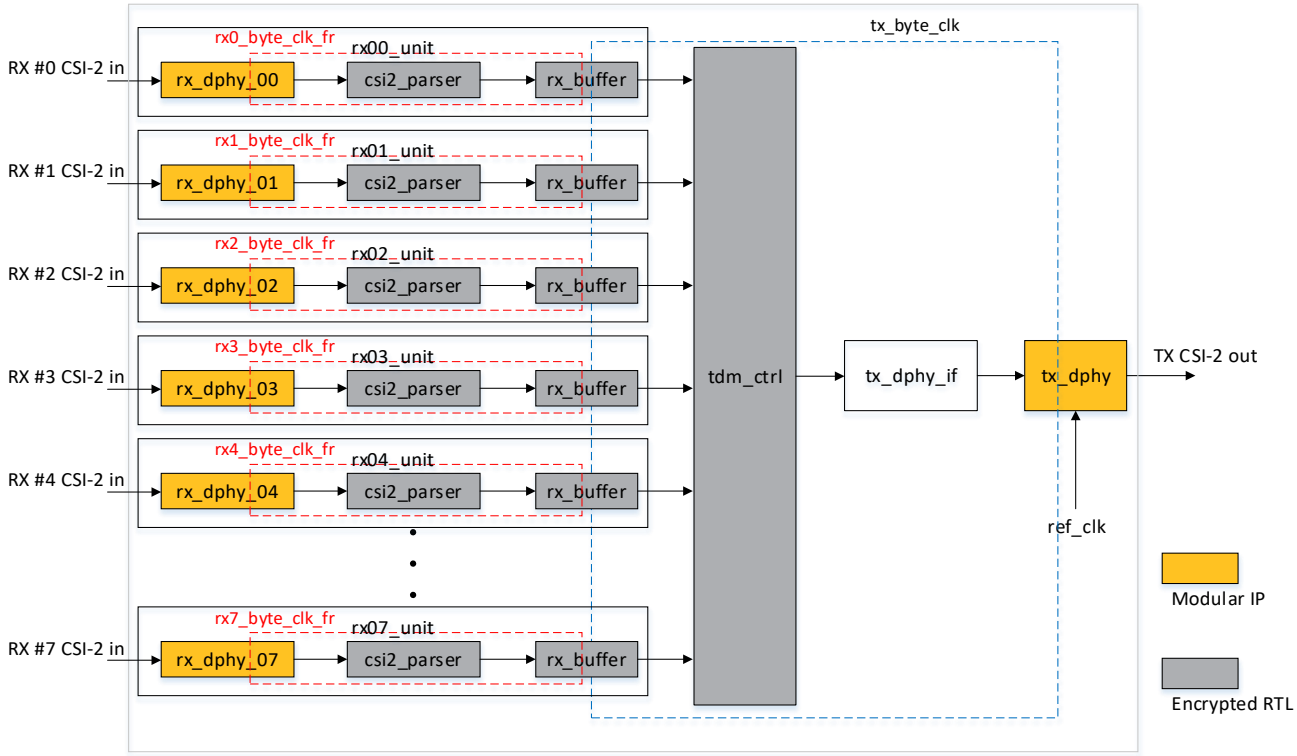

Figure 1.1. CSI-2 Virtual Channel Aggregation Block Diagram

Figure 1.2. shows a clocking scheme example. In this example, RX channel #0 is in continuous clock mode and all other RX channels are in non-continuous clock mode. Sync clock (> 60 MHz) is required for RX Soft D-PHY IP and a clock to drive LP (Low Power) HS (High Speed) mode detection logic is required in non-continuous clock mode. The internal oscillator is used to generate ~75 MHz clock for these purposes. GPLL generates four continuous byte clocks for the four RX channels with non-continuous clock mode utilizing the continuous byte clock that comes from rx_dphy_00 as a reference clock.

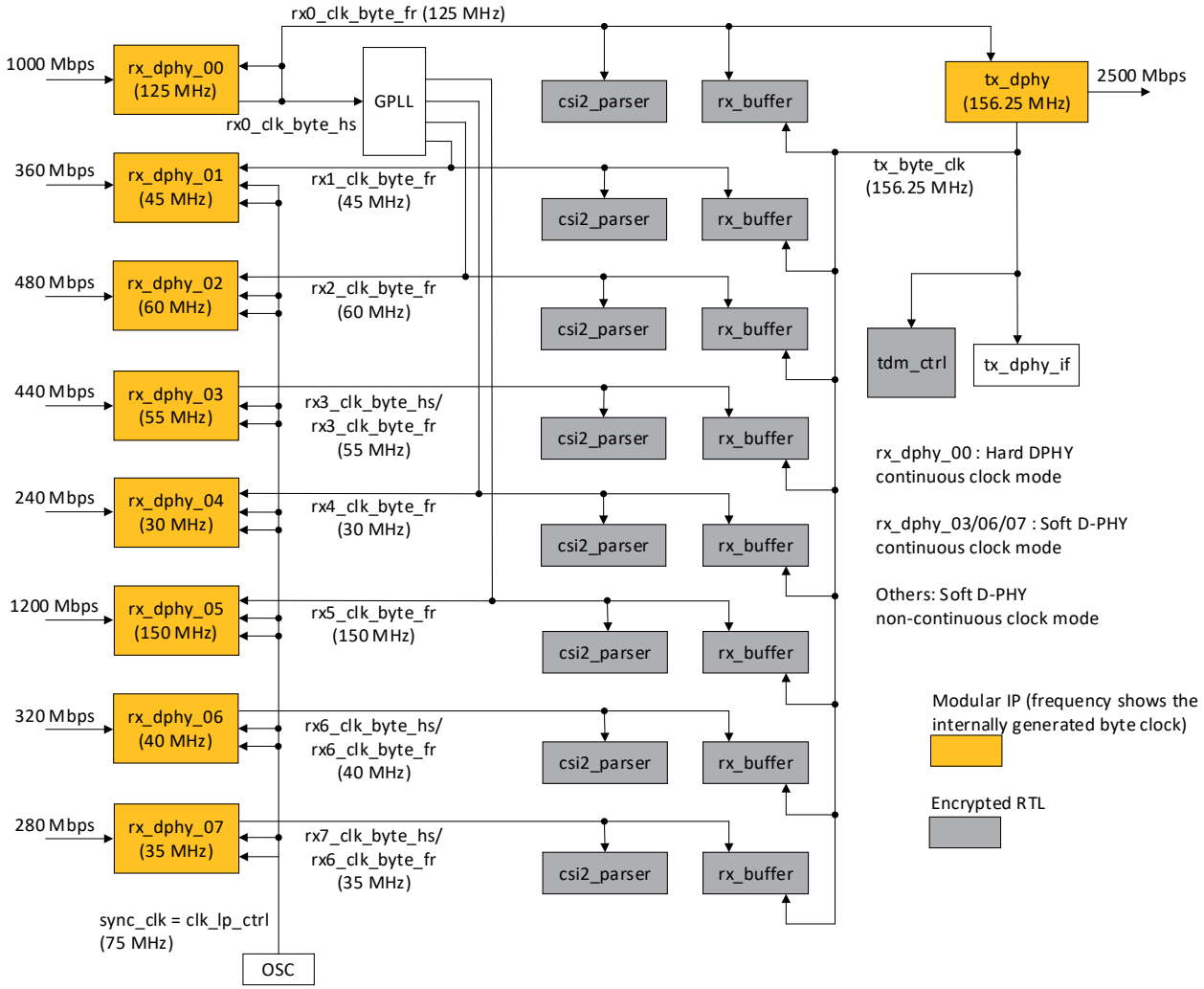

Figure 1.2. Clocking Scheme Example

1.4. RX and TX Permutations

This design allows all RX channels to be independent on number of lanes, bandwidth, and clock mode as long as the total RX bandwidth (plus some overhead) does not exceed the TX capability of 2.5 Gbps per lane. The amount of overhead varies by the number of RX channels, the horizontal blanking period of each RX channels, the active line period, etc., but less than 5% is enough for ordinary cases.

The Microsoft® Excel calculator (*docs/vc_aggr_NX_clock.xlsx*) included in the reference design package is for you to get the byte clock and number of required Embedded Block RAM (EBR) for the design. This calculator is useful to estimate the required TX bandwidth and configure D-PHY RX and TX IP. A sample entry is shown in Figure 1.3. The setting in the calculator is matched the configuration shown in Figure 1.2.. By entering the values and modes indicated by the boxes, you can get the byte clock frequency and number of required EBR. Refer to RX FIFO section for details. Also, refer to the rx_buffer section to select the value of *actual RX Buffer Depth*.

Note that some permutations may not be feasible by LIFCL-17 because of limited I/O and resources.

Virtual Channel Aggregation with CrossLink-NX RD Frequency Calculator											
Number of RX Channels	8	CH #0	CH #1	CH #2	CH #3	CH #4	CH #5	CH #6	CH #7		
DPHY IP		HARD	SOFT	SOFT	SOFT	SOFT	SOFT	SOFT	SOFT		
RX Rate per lane (Mbps)		1000	360	480	440	240	1200	320	280		
RX DPHY Clock Frequency (MHz)		500	180	240	220	120	600	160	140		
RX DPHY Clock Period (ps)		2000	5555.555556	4166.666667	4545.454545	8333.333333	1666.666667	6250	7142.857143		
Number of RX Lanes		4	4	2	1	1	1	2	2	10	total EBR for soft lane aligner
RX Gear (fixed to 8)		8	8	8	8	8	8	8	8		
RX Data Type		RAW10	RAW12	RAW14	RAW8	RGB888	YUV420_10	YUV420_8	YUV422_10		
Horizontal Resolution		720	480	480	1920	240	480	480	240		
Word Count		900	720	840	1920	720	1200	960	600		
min. RX Buffer Depth		112.5	90	105	240	90	150	120	75		
actual RX Buffer Depth		1024	1024	512	512	1024	1024	512	512		
actual EBR used for RX Buffer		4	4	2	2	4	4	2	2	24	total EBR for RX Buffer
RX Byte Clock Frequency		125	45	60	55	30	150	40	35		
RX DPHY Clock Mode		continuous	non-continuous	non-continuous	continuous	non-continuous	non-continuous	continuous	continuous		
source of continuous byte clock		self	GPLL_op	GPLL_os	self	GPLL_os2	GPLL_os3	self	self		
Recommended RX FIFO type		SINGLE	SINGLE	SINGLE	OFF	SINGLE	SINGLE	OFF	OFF		
Recommended RX FIFO depth		8	16	16	NA	16	16	NA	NA		
Recommended RX FIFO delay		1	4	4	NA	4	4	NA	NA		
# of EBR used for RX FIFO		1	1	1	0	1	1	0	0	5	total EBR for RX FIFO
Number of TX Lanes	4									39	Total EBR used (max. 84)
TX Gear	16										
min. TX Rate per lane (Mbps)	2370	Note: Only modify the boxed cells									
min. TX DPHY Clock Frequency (MHz)	1185	Note : "source of continuous byte clock" are informative and do not affect clock frequency or EBR count.									
min. TX Byte Clock Frequency (MHz)	148.125										
actual TX Rate per lane (Mbps)	2500										
actual TX DPHY Clock Frequency (MHz)	1250										
actual TX Byte Clock Frequency (MHz)	156.25										
TX DPHY CLK PERIOD	800										

Figure 1.3. Microsoft Excel Calculator

2. Parameters and Port List

There are two directive files for this reference design:

- *synthesis_directives.v* – used for design compilation by the Lattice Radiant software and for simulation.
- *simulation_directives.v* – used for simulation.

You can modify these directives according to your own configuration. The settings in these files must match RX and TX D-PHY IP settings created by the Lattice Radiant software.

2.1. Synthesis Directives

Table 2.1 shows the synthesis directives that affect this reference design. These are used for both synthesis and simulation. As shown in Table 2.1 and Table 2.2, some parameter selections are restricted by other parameter settings.

Table 2.1. Synthesis Directives

Category	Directive	Remarks
External reference clock	EXT_REF_CLK	Enable this when the reference clock is fed from a pin.
RX channel count	NUM_RX_CH_2	Number of RX channels aggregated. Only one of these four directives must be defined.
	NUM_RX_CH_3	
	NUM_RX_CH_4	
	NUM_RX_CH_5	
	NUM_RX_CH_6	
	NUM_RX_CH_7	
	NUM_RX_CH_8	
RX channel lane count	NUM_RX0_LANE_1	Number of lanes in RX channel 0. Only one of these three directives must be defined.
	NUM_RX0_LANE_2	
	NUM_RX0_LANE_4	
	NUM_RX1_LANE_1	Number of lanes in RX channel 1. Only one of these three directives must be defined.
	NUM_RX1_LANE_2	
	NUM_RX1_LANE_4	
	NUM_RX2_LANE_1	Number of lanes in RX channel 2. Only one of these three directives must be defined. Effective when RX channel count is 3 or more.
	NUM_RX2_LANE_2	
	NUM_RX2_LANE_4	
	NUM_RX3_LANE_1	Number of lanes in RX channel 3. Only one of these three directives must be defined. Effective when RX channel count is 4 or more.
	NUM_RX3_LANE_2	
	NUM_RX3_LANE_4	
	NUM_RX4_LANE_1	Number of lanes in RX channel 4. Only one of these three directives must be defined. Effective when RX channel count is 5 or more.
	NUM_RX4_LANE_2	
	NUM_RX4_LANE_4	
	NUM_RX5_LANE_1	Number of lanes in RX channel 4. Only one of these three directives must be defined. Effective when RX channel count is 6 or more.
	NUM_RX5_LANE_2	
	NUM_RX5_LANE_4	
	NUM_RX6_LANE_1	Number of lanes in RX channel 4. Only one of these three directives must be defined. Effective when RX channel count is 7 or more.
	NUM_RX6_LANE_2	
	NUM_RX6_LANE_4	
	NUM_RX7_LANE_1	Number of lanes in RX channel 4. Only one of these three directives must be defined. Effective when RX channel count is 8.
	NUM_RX7_LANE_2	
	NUM_RX7_LANE_4	
RX D-PHY Clock Gear	RX0_GEAR_8	Only one of these directives must be selected. Gear 16 can be used for only 1- and 2-lane configurations of Hard D-PHY.
	RX0_GEAR_16	
	RX1_GEAR_8	Only one of these directives must be selected. Gear 16 can be used

Category	Directive	Remarks
	RX1_GEAR_16	for only 1- and 2-lane configurations for Hard D-PHY.
	RX2_GEAR_8	Only one of these directives must be selected. Gear 16 can be used for only 1- and 2-lane configurations for Hard D-PHY.
	RX2_GEAR_16	
	RX3_GEAR_8	Only one of these directives must be selected. Gear 16 can be used for only 1- and 2-lane configurations for Hard D-PHY.
	RX3_GEAR_16	
	RX4_GEAR_8	Only one of these directives must be selected. Gear 16 can be used for only 1- and 2-lane configurations for Hard D-PHY.
	RX4_GEAR_16	
	RX5_GEAR_8	Only one of these directives must be selected. Gear 16 can be used for only 1- and 2-lane configurations for Hard D-PHY.
	RX5_GEAR_16	
	RX6_GEAR_8	Only one of these directives must be selected. Gear 16 can be used for only 1- and 2-lane configurations for Hard D-PHY.
	RX6_GEAR_16	
	RX7_GEAR_8	Only one of these directives must be selected. Gear 16 can be used for only 1- and 2-lane configurations for Hard D-PHY.
	RX7_GEAR_16	
RX Hard D-PHY channel	RX0_DPHY_HARD	Specify RX channel that uses Hard D-PHY. Only one of these eight directives must be defined. If none of these is defined, all RX channels use Soft D-PHY.
	RX1_DPHY_HARD	
	RX2_DPHY_HARD	
	RX3_DPHY_HARD	
	RX4_DPHY_HARD	
	RX5_DPHY_HARD	
	RX6_DPHY_HARD	
	RX7_DPHY_HARD	
RX D-PHY Clock Mode[1]	RX0_CLK_MODE_HS_ONLY	RX D-PHY Clock mode on channel 0. Only one of these two directives must be defined.
	RX0_CLK_MODE_HS_LP	
	RX1_CLK_MODE_HS_ONLY	RX D-PHY Clock mode on channel 1. Only one of these two directives must be defined.
	RX1_CLK_MODE_HS_LP	
	RX2_CLK_MODE_HS_ONLY	RX D-PHY Clock mode on channel 2. Only one of these two directives must be defined.
	RX2_CLK_MODE_HS_LP	
	RX3_CLK_MODE_HS_ONLY	RX D-PHY Clock mode on channel 3. Only one of these two directives must be defined.
	RX3_CLK_MODE_HS_LP	
	RX4_CLK_MODE_HS_ONLY	RX D-PHY Clock mode on channel 4. Only one of these two directives must be defined.
	RX4_CLK_MODE_HS_LP	
	RX5_CLK_MODE_HS_ONLY	RX D-PHY Clock mode on channel 5. Only one of these two directives must be defined.
	RX5_CLK_MODE_HS_LP	
	RX6_CLK_MODE_HS_ONLY	RX D-PHY Clock mode on channel 6. Only one of these two directives must be defined.
	RX6_CLK_MODE_HS_LP	
	RX7_CLK_MODE_HS_ONLY	RX D-PHY Clock mode on channel 7. Only one of these two directives must be defined.
	RX7_CLK_MODE_HS_LP	
VC ID pass through[2]	RX0_VC_PASS_THROUGH	Enable when VC ID is passed through without change.
	RX1_VC_PASS_THROUGH	Enable when VC ID is passed through without change.
	RX2_VC_PASS_THROUGH	Enable when VC ID is passed through without change.
	RX3_VC_PASS_THROUGH	Enable when VC ID is passed through without change.
	RX4_VC_PASS_THROUGH	Enable when VC ID is passed through without change.
	RX5_VC_PASS_THROUGH	Enable when VC ID is passed through without change.
	RX6_VC_PASS_THROUGH	Enable when VC ID is passed through without change.
	RX7_VC_PASS_THROUGH	Enable when VC ID is passed through without change.

Category	Directive	Remarks
RX channel VC value[3]	RX0_NEW_VC {value}	Channel 0 Virtual Channel ID; 0 – 15
	RX1_NEW_VC {value}	Channel 1 Virtual Channel ID; 0 – 15
	RX2_NEW_VC {value}	Channel 2 Virtual Channel ID; 0 – 15
	RX3_NEW_VC {value}	Channel 3 Virtual Channel ID; 0 – 15
	RX4_NEW_VC {value}	Channel 4 Virtual Channel ID; 0 – 15
	RX5_NEW_VC {value}	Channel 5 Virtual Channel ID; 0 – 15
	RX6_NEW_VC {value}	Channel 6 Virtual Channel ID; 0 – 15
	RX7_NEW_VC {value}	Channel 7 Virtual Channel ID; 0 – 15
RX Channel Frame Counter[4]	RX0_FRAME_COUNT	Enable when Data Field of Frame Start/End Short Packet is replaced with the Frame Counter value.
	RX1_FRAME_COUNT	Enable when Data Field of Frame Start/End Short Packet is replaced with the Frame Counter value.
	RX2_FRAME_COUNT	Enable when Data Field of Frame Start/End Short Packet is replaced with the Frame Counter value.
	RX3_FRAME_COUNT	Enable when Data Field of Frame Start/End Short Packet is replaced with the Frame Counter value.
	RX4_FRAME_COUNT	Enable when Data Field of Frame Start/End Short Packet is replaced with the Frame Counter value.
	RX5_FRAME_COUNT	Enable when Data Field of Frame Start/End Short Packet is replaced with the Frame Counter value.
	RX6_FRAME_COUNT	Enable when Data Field of Frame Start/End Short Packet is replaced with the Frame Counter value.
	RX7_FRAME_COUNT	Enable when Data Field of Frame Start/End Short Packet is replaced with the Frame Counter value.
Maximum value of the frame counter	RX0_FRAME_COUNT_MAX {value}	Frame counter value goes back to 1 after it reaches this value. Effective when RX0_FRAME_COUNT is defined. Must be 2 – 65535.
	RX1_FRAME_COUNT_MAX {value}	Frame counter value goes back to 1 after it reaches this value. Effective when RX1_FRAME_COUNT is defined. Must be 2 – 65535.
	RX2_FRAME_COUNT_MAX {value}	Frame counter value goes back to 1 after it reaches this value. Effective when RX2_FRAME_COUNT is defined. Must be 2 – 65535.
	RX3_FRAME_COUNT_MAX {value}	Frame counter value goes back to 1 after it reaches this value. Effective when RX3_FRAME_COUNT is defined. Must be 2 – 65535.
	RX4_FRAME_COUNT_MAX {value}	Frame counter value goes back to 1 after it reaches this value. Effective when RX4_FRAME_COUNT is defined. Must be 2 – 65535.
	RX5_FRAME_COUNT_MAX {value}	Frame counter value goes back to 1 after it reaches this value. Effective when RX4_FRAME_COUNT is defined. Must be 2 – 65535.
	RX6_FRAME_COUNT_MAX {value}	Frame counter value goes back to 1 after it reaches this value. Effective when RX4_FRAME_COUNT is defined. Must be 2 – 65535.
	RX7_FRAME_COUNT_MAX {value}	Frame counter value goes back to 1 after it reaches this value. Effective when RX4_FRAME_COUNT is defined. Must be 2 – 65535.
RX Buffer Depth[5]	RX0_BUFFER_DEPTH_*	RX channel 0 FIFO Depth. * must be 512, 1024, 2048, or 4096.
	RX1_BUFFER_DEPTH_*	RX channel 1 FIFO Depth. * must be 512, 1024, 2048, or 4096.
	RX2_BUFFER_DEPTH_*	RX channel 2 FIFO Depth. * must be 512, 1024, 2048, or 4096.
	RX3_BUFFER_DEPTH_*	RX channel 3 FIFO Depth. * must be 512, 1024, 2048, or 4096.
	RX4_BUFFER_DEPTH_*	RX channel 4 FIFO Depth. * must be 512, 1024, 2048, or 4096.
	RX5_BUFFER_DEPTH_*	RX channel 5 FIFO Depth. * must be 512, 1024, 2048, or 4096.
	RX6_BUFFER_DEPTH_*	RX channel 6 FIFO Depth. * must be 512, 1024, 2048, or 4096.
	RX7_BUFFER_DEPTH_*	RX channel 7 FIFO Depth. * must be 512, 1024, 2048, or 4096.
TX channel lane count	NUM_TX_LANE_1	Number of lanes in TX channel. Only one of these three directives must be defined.
	NUM_TX_LANE_2	
	NUM_TX_LANE_4	

Category	Directive	Remarks
TX D-PHY Clock Gear	TX_GEAR_8	TX D-PHY Clock Gear. Only one of these two directives must be defined.
	TX_GEAR_16	
TX D-PHY Clock Mode	TX_CLK_MODE_HS_ONLY	TX D-PHY Clock mode. Only one of these two directives must be defined.
	TX_CLK_MODE_HS_LP	

Notes:

1. HS_LP mode means *non-continuous clock mode* and HS_ONLY means *continuous clock mode*. HS_LP mode works only if RX continuous byte clock (clk_byte_fr_i) for corresponding RX channel can be generated internally or directly fed from I/O pin with the same frequency as the stoppable byte clock (clk_byte_hs_o).
2. You cannot assign the same VC value on different RX channels when this is defined.
3. Incoming VC values on RX CSI-2 data are overwritten by these VC values when RX*_VC_PASS_THROUGH is not defined. Values 4 and above are only supported by CSI-2 version 2.0 and above. If the opponent device supports only CSI-2 version 1.1, VC values of 4-15 must not be used.
4. When this is defined, the Data Field is replaced with the 16-bit counter value which begins with 1 after power on/reset and goes back to 1 after it reaches RX*_FRAME_COUNT_MAX. The Data Field is passed through when this is not defined.
5. This value affects the necessary EBR used in the device. Number of necessary EBR per RX channel is
   (BUFFER_DEPTH/512) × 2 (in case of NUM_TX_LANE_4 and TX_GEAR_16), or
   (BUFFER_DEPTH/512) × 1 (others).
   Total number of EBR used in this design must not exceed 84 for LIFCL-40 and 24 for LIFCL-17.

2.2. Simulation Directives

Table 2.2 shows the simulation directives for this reference design.

Table 2.2. Simulation Directives

Category	Directive	Remarks
Reference clock period	REF_CLK_PERIOD {value}	Reference clock period in ps
RX D-PHY clock period	RX0_DPHY_CLK_PERIOD {value}	RX D-PHY clock period on Channel 0 in ps
	RX1_DPHY_CLK_PERIOD {value}	RX D-PHY clock period on Channel 1 in ps
	RX2_DPHY_CLK_PERIOD {value}	RX D-PHY clock period on Channel 2 in ps
	RX3_DPHY_CLK_PERIOD {value}	RX D-PHY clock period on Channel 3 in ps
	RX4_DPHY_CLK_PERIOD {value}	RX D-PHY clock period on Channel 4 in ps
	RX5_DPHY_CLK_PERIOD {value}	RX D-PHY clock period on Channel 5 in ps
	RX6_DPHY_CLK_PERIOD {value}	RX D-PHY clock period on Channel 6 in ps
	RX7_DPHY_CLK_PERIOD {value}	RX D-PHY clock period on Channel 7 in ps
RX Byte clock frequency	RX0_FREQ_TGT {value}	RX byte clock frequency on Channel 0 in MHz
	RX1_FREQ_TGT {value}	RX byte clock frequency on Channel 1 in MHz
	RX2_FREQ_TGT {value}	RX byte clock frequency on Channel 2 in MHz
	RX3_FREQ_TGT {value}	RX byte clock frequency on Channel 3 in MHz
	RX4_FREQ_TGT {value}	RX byte clock frequency on Channel 4 in MHz
	RX5_FREQ_TGT {value}	RX byte clock frequency on Channel 5 in MHz
	RX6_FREQ_TGT {value}	RX byte clock frequency on Channel 6 in MHz
	RX7_FREQ_TGT {value}	RX byte clock frequency on Channel 7 in MHz
TX byte clock frequency	TX_FREQ_TGT {value}	TX byte clock frequency in MHz
TX D-PHY clock period	TX_DPHY_CLK_PERIOD {value}	TX D-PHY clock period in ps
Frame Start Detection	TX_WAIT_LESS_15MS	Always enable this directive.
VC value on RX channel	VC_CH0 {value}	VC value on incoming RX Channel 0; 0 – 15
	VC_CH1 {value}	VC value on incoming RX Channel 1; 0 – 15
	VC_CH2 {value}	VC value on incoming RX Channel 2; 0 – 15
	VC_CH3 {value}	VC value on incoming RX Channel 3; 0 – 15
	VC_CH4 {value}	VC value on incoming RX Channel 4; 0 – 15
	VC_CH5 {value}	VC value on incoming RX Channel 5; 0 – 15
	VC_CH6 {value}	VC value on incoming RX Channel 6; 0 – 15
	VC_CH7 {value}	VC value on incoming RX Channel 7; 0 – 15
Frame Number in Frame Start/End Short Packets	CH0_FNUM_EMBED	Frame number is embedded in Data Field of Frame Start/End Short packet. The value “0” is filled when undefined.
	CH1_FNUM_EMBED	Frame number is embedded in Data Field of Frame Start/End Short packet. The value “0” is filled when undefined.
	CH2_FNUM_EMBED	Frame number is embedded in Data Field of Frame Start/End Short packet. The value “0” is filled when undefined.
	CH3_FNUM_EMBED	Frame number is embedded in Data Field of Frame Start/End Short packet. The value “0” is filled when undefined.
	CH4_FNUM_EMBED	Frame number is embedded in Data Field of Frame Start/End Short packet. The value “0” is filled when undefined.
	CH5_FNUM_EMBED	Frame number is embedded in Data Field of Frame Start/End Short packet. The value “0” is filled when undefined.
	CH6_FNUM_EMBED	Frame number is embedded in Data Field of Frame Start/End Short packet. The value “0” is filled when undefined.
	CH7_FNUM_EMBED	Frame number is embedded in Data Field of Frame Start/End Short packet. The value “0” is filled when undefined.
Maximum value of Frame Number	CH0_FNUM_MAX {value}	The maximum value of the frame number; 2 - 65535
	CH1_FNUM_MAX {value}	The maximum value of the frame number; 2 – 65535

Category	Directive	Remarks
	CH2_FNUM_MAX {value}	The maximum value of the frame number; 2 – 65535
	CH3_FNUM_MAX {value}	The maximum value of the frame number; 2 – 65535
	CH4_FNUM_MAX {value}	The maximum value of the frame number; 2 - 65535
	CH5_FNUM_MAX {value}	The maximum value of the frame number; 2 - 65535
	CH6_FNUM_MAX {value}	The maximum value of the frame number; 2 - 65535
	CH7_FNUM_MAX {value}	The maximum value of the frame number; 2 - 65535
Initial delay on RX channel	CH0_DELAY {value}	Initial delay to activate RX Channel 0 in ps
	CH1_DELAY {value}	Initial delay to activate RX Channel 1 in ps
	CH2_DELAY {value}	Initial delay to activate RX Channel 2 in ps
	CH3_DELAY {value}	Initial delay to activate RX Channel 3 in ps
	CH4_DELAY {value}	Initial delay to activate RX Channel 4 in ps
	CH5_DELAY {value}	Initial delay to activate RX Channel 5 in ps
	CH6_DELAY {value}	Initial delay to activate RX Channel 6 in ps
	CH7_DELAY {value}	Initial delay to activate RX Channel 7 in ps
Gap (LP) time between active lines on RX Channel	CH0_DPHY_LPS_GAP {value}	Gap time on RX Channel 0 in ps
	CH1_DPHY_LPS_GAP {value}	Gap time on RX Channel 1 in ps
	CH2_DPHY_LPS_GAP {value}	Gap time on RX Channel 2 in ps
	CH3_DPHY_LPS_GAP {value}	Gap time on RX Channel 3 in ps
	CH4_DPHY_LPS_GAP {value}	Gap time on RX Channel 4 in ps
	CH5_DPHY_LPS_GAP {value}	Gap time on RX Channel 5 in ps
	CH6_DPHY_LPS_GAP {value}	Gap time on RX Channel 6 in ps
	CH7_DPHY_LPS_GAP {value}	Gap time on RX Channel 7 in ps
Gap (LP) time between Frame End and Frame Start on RX Channel	CH0_DPHY_FRAME_GAP {value}	Gap time on RX Channel 0 in ps
	CH1_DPHY_FRAME_GAP {value}	Gap time on RX Channel 1 in ps
	CH2_DPHY_FRAME_GAP {value}	Gap time on RX Channel 2 in ps
	CH3_DPHY_FRAME_GAP {value}	Gap time on RX Channel 3 in ps
	CH4_DPHY_FRAME_GAP {value}	Gap time on RX Channel 4 in ps
	CH5_DPHY_FRAME_GAP {value}	Gap time on RX Channel 4 in ps
	CH6_DPHY_FRAME_GAP {value}	Gap time on RX Channel 4 in ps
	CH7_DPHY_FRAME_GAP {value}	Gap time on RX Channel 4 in ps
Video data configuration on RX Channel 0	CH0_NUM_FRAMES {value}	Number of frames to feed
	CH0_NUM_LINES {value}	Number of active lines per frame
	CH0_NUM_PIXELS {value}	Number of pixels per line
	CH0_DT_*	Data Type; * must be RAW8, RAW10, RAW12, RAW14, RGB888, YUV420_10, YUV420_8, YUV422_10, or YUV422_8.
Video data configuration on RX Channel 1	CH1_NUM_PIXELS {value}	Number of pixels per line
	CH1_NUM_LINES {value}	Number of active lines per frame
	CH1_NUM_PIXELS {value}	Number of pixels per line
	CH1_DT_*	Data Type; * must be RAW8, RAW10, RAW12, RAW14, RGB888, YUV420_10, YUV420_8, YUV422_10, or YUV422_8.
Video data configuration on RX Channel 2	CH2_NUM_FRAMES {value}	Number of frames to feed
	CH2_NUM_LINES {value}	Number of active lines per frame
	CH2_NUM_PIXELS {value}	Number of pixels per line
	CH2_DT_*	Data Type; * must be RAW8, RAW10, RAW12, RAW14, RGB888, YUV420_10, YUV420_8, YUV422_10, or YUV422_8.
Video data configuration on RX Channel 3	CH3_NUM_FRAMES {value}	Number of frames to feed
	CH3_NUM_LINES {value}	Number of active lines per frame
	CH3_NUM_PIXELS {value}	Number of pixels per line

Category	Directive	Remarks
	CH3_DT_*	Data Type; * must be RAW8, RAW10, RAW12, RAW14, RGB888, YUV420_10, YUV420_8, YUV422_10, or YUV422_8.
Video data configuration on RX Channel 4	CH4_NUM_FRAMES {value}	Number of frames to feed
	CH4_NUM_LINES {value}	Number of active lines per frame
	CH4_NUM_PIXELS {value}	Number of pixels per line
	CH4_DT_*	Data Type; * must be RAW8, RAW10, RAW12, RAW14, RGB888, YUV420_10, YUV420_8, YUV422_10, or YUV422_8.
Video data configuration on RX Channel 5	CH5_NUM_FRAMES {value}	Number of frames to feed
	CH5_NUM_LINES {value}	Number of active lines per frame
	CH5_NUM_PIXELS {value}	Number of pixels per line
	CH5_DT_*	Data Type; * must be RAW8, RAW10, RAW12, RAW14, RGB888, YUV420_10, YUV420_8, YUV422_10, or YUV422_8.
Video data configuration on RX Channel 6	CH6_NUM_FRAMES {value}	Number of frames to feed
	CH6_NUM_LINES {value}	Number of active lines per frame
	CH6_NUM_PIXELS {value}	Number of pixels per line
	CH6_DT_*	Data Type; * must be RAW8, RAW10, RAW12, RAW14, RGB888, YUV420_10, YUV420_8, YUV422_10, or YUV422_8.
Video data configuration on RX Channel 7	CH7_NUM_FRAMES {value}	Number of frames to feed
	CH7_NUM_LINES {value}	Number of active lines per frame
	CH7_NUM_PIXELS {value}	Number of pixels per line
	CH7_DT_*	Data Type; * must be RAW8, RAW10, RAW12, RAW14, RGB888, YUV420_10, YUV420_8, YUV422_10, or YUV422_8.
Internal signal monitoring	MISC_ON	Enables internal signal monitored by the testbench. Always enable this directive.

2.3. Top-Level I/O

Table 2.3 shows the top-level I/O of this reference design. Actual I/O depend on your channel and lane configurations. All necessary I/O ports are automatically declared by compiler directives.

Table 2.3. CSI-2 VC Aggregation Top-Level I/O

Port Name	Direction	Description
Clocks and Resets		
ref_clk_i (optional)	I	Input reference clock. This port is declared only when EXT_REF_CLK is defined in *synthesis_directives.v*.
reset_n_i	I	Asynchronous active low system reset
CSI-2 RX Interface		
rx0_clk_p_i	I	Positive differential RX Ch0 D-PHY input clock
rx0_clk_n_i	I	Negative differential RX Ch0 D-PHY input clock
rx0_d0_p_i	I	Positive differential RX Ch0 D-PHY input data 0
rx0_d0_n_i	I	Negative differential RX Ch0 D-PHY input data 0
rx0_d1_p_i	I	Positive differential RX Ch0 D-PHY input data 1 (in case of 2-lane or 4-lane configuration)
rx0_d1_n_i	I	Negative differential RX Ch0 D-PHY input data 1 (in case of 2-lane or 4-lane configuration)
rx0_d2_p_i	I	Positive differential RX Ch0 D-PHY input data 2 (in case of 4-lane configuration)
rx0_d2_n_i	I	Negative differential RX Ch0 D-PHY input data 2 (in case of 4-lane configuration)
rx0_d3_p_i	I	Positive differential RX Ch0 D-PHY input data 3 (in case of 4-lane configuration)
rx0_d3_n_i	I	Negative differential RX Ch0 D-PHY input data 3 (in case of 4-lane configuration)
rx1_clk_p_i	I	Positive differential RX Ch1 D-PHY input clock
rx1_clk_n_i	I	Negative differential RX Ch1 D-PHY input clock
rx1_d0_p_i	I	Positive differential RX Ch1 D-PHY input data 0
rx1_d0_n_i	I	Negative differential RX Ch1 D-PHY input data 0
rx1_d1_p_i	I	Positive differential RX Ch1 D-PHY input data 1 (in case of 2-lane or 4-lane configuration)
rx1_d1_n_i	I	Negative differential RX Ch1 D-PHY input data 1 (in case of 2-lane or 4-lane configuration)
rx1_d2_p_i	I	Positive differential RX Ch1 D-PHY input data 2 (in case of 4-lane configuration)
rx1_d2_n_i	I	Negative differential RX Ch1 D-PHY input data 2 (in case of 4-lane configuration)
rx1_d3_p_i	I	Positive differential RX Ch1 D-PHY input data 3 (in case of 4-lane configuration)
rx1_d3_n_i	I	Negative differential RX Ch1 D-PHY input data 3 (in case of 4-lane configuration)
rx2_clk_p_i	I	Positive differential RX Ch2 D-PHY input clock
rx2_clk_n_i	I	Negative differential RX Ch2 D-PHY input clock
rx2_d0_p_i	I	Positive differential RX Ch2 D-PHY input data 0
rx2_d0_n_i	I	Negative differential RX Ch2 D-PHY input data 0
rx2_d1_p_i	I	Positive differential RX Ch2 D-PHY input data 1 (in case of 2-lane or 4-lane configuration)
rx2_d1_n_i	I	Negative differential RX Ch2 D-PHY input data 1 (in case of 2-lane or 4-lane configuration)
rx2_d2_p_i	I	Positive differential RX Ch2 D-PHY input data 2 (in case of 4-lane configuration)
rx2_d2_n_i	I	Negative differential RX Ch2 D-PHY input data 2 (in case of 4-lane configuration)
rx2_d3_p_i	I	Positive differential RX Ch2 D-PHY input data 3 (in case of 4-lane configuration)
rx2_d3_n_i	I	Negative differential RX Ch2 D-PHY input data 3 (in case of 4-lane configuration)
rx3_clk_p_i	I	Positive differential RX Ch3 D-PHY input clock
rx3_clk_n_i	I	Negative differential RX Ch3 D-PHY input clock
rx3_d0_p_i	I	Positive differential RX Ch3 D-PHY input data 0
rx3_d0_n_i	I	Negative differential RX Ch3 D-PHY input data 0
rx3_d1_p_i	I	Positive differential RX Ch3 D-PHY input data 1 (in case of 2-lane or 4-lane configuration)
rx3_d1_n_i	I	Negative differential RX Ch3 D-PHY input data 1 (in case of 2-lane or 4-lane configuration)
rx3_d2_p_i	I	Positive differential RX Ch3 D-PHY input data 2 (in case of 4-lane configuration)
rx3_d2_n_i	I	Negative differential RX Ch3 D-PHY input data 2 (in case of 4 lane configuration)

Port Name	Direction	Description
rx3_d3_p_i	I	Positive differential RX Ch3 D-PHY input data 3 (in case of 4 lane configuration)
rx3_d3_n_i	I	Negative differential RX Ch3 D-PHY input data 3 (in case of 4 lane configuration)
rx4_clk_p_i	I	Positive differential RX Ch4 D-PHY input clock
rx4_clk_n_i	I	Negative differential RX Ch4 D-PHY input clock
rx4_d0_p_i	I	Positive differential RX Ch4 D-PHY input data 0
rx4_d0_n_i	I	Negative differential RX Ch4 D-PHY input data 0
rx4_d1_p_i	I	Positive differential RX Ch4 D-PHY input data 1 (in case of 2-lane or 4-lane configuration)
rx4_d1_n_i	I	Negative differential RX Ch4 D-PHY input data 1 (in case of 2-lane or 4-lane configuration)
rx4_d2_p_i	I	Positive differential RX Ch4 D-PHY input data 2 (in case of 4-lane configuration)
rx4_d2_n_i	I	Negative differential RX Ch4 D-PHY input data 2 (in case of 4-lane configuration)
rx4_d3_p_i	I	Positive differential RX Ch4 D-PHY input data 3 (in case of 4-lane configuration)
rx4_d3_n_i	I	Negative differential RX Ch4 D-PHY input data 3 (in case of 4-lane configuration)
rx5_clk_p_i	I	Positive differential RX Ch5 D-PHY input clock
rx5_clk_n_i	I	Negative differential RX Ch5 D-PHY input clock
rx5_d0_p_i	I	Positive differential RX Ch5 D-PHY input data 0
rx5_d0_n_i	I	Negative differential RX Ch5 D-PHY input data 0
rx5_d1_p_i	I	Positive differential RX Ch5 D-PHY input data 1 (in case of 2-lane or 4-lane configuration)
rx5_d1_n_i	I	Negative differential RX Ch5 D-PHY input data 1 (in case of 2-lane or 4-lane configuration)
rx5_d2_p_i	I	Positive differential RX Ch5 D-PHY input data 2 (in case of 4-lane configuration)
rx5_d2_n_i	I	Negative differential RX Ch5 D-PHY input data 2 (in case of 4-lane configuration)
rx5_d3_p_i	I	Positive differential RX Ch5 D-PHY input data 3 (in case of 4-lane configuration)
rx5_d3_n_i	I	Negative differential RX Ch5 D-PHY input data 3 (in case of 4-lane configuration)
rx6_clk_p_i	I	Positive differential RX Ch6 D-PHY input clock
rx6_clk_n_i	I	Negative differential RX Ch6 D-PHY input clock
rx6_d0_p_i	I	Positive differential RX Ch6 D-PHY input data 0
rx6_d0_n_i	I	Negative differential RX Ch6 D-PHY input data 0
rx6_d1_p_i	I	Positive differential RX Ch6 D-PHY input data 1 (in case of 2-lane or 4-lane configuration)
rx6_d1_n_i	I	Negative differential RX Ch6 D-PHY input data 1 (in case of 2-lane or 4-lane configuration)
rx6_d2_p_i	I	Positive differential RX Ch6 D-PHY input data 2 (in case of 4-lane configuration)
rx6_d2_n_i	I	Negative differential RX Ch6 D-PHY input data 2 (in case of 4-lane configuration)
rx6_d3_p_i	I	Positive differential RX Ch6 D-PHY input data 3 (in case of 4-lane configuration)
rx6_d3_n_i	I	Negative differential RX Ch6 D-PHY input data 3 (in case of 4-lane configuration)
rx7_clk_p_i	I	Positive differential RX Ch7 D-PHY input clock
rx7_clk_n_i	I	Negative differential RX Ch7 D-PHY input clock
rx7_d0_p_i	I	Positive differential RX Ch7 D-PHY input data 0
rx7_d0_n_i	I	Negative differential RX Ch7 D-PHY input data 0
rx7_d1_p_i	I	Positive differential RX Ch7 D-PHY input data 1 (in case of 2-lane or 4-lane configuration)
rx7_d1_n_i	I	Negative differential RX Ch7 D-PHY input data 1 (in case of 2-lane or 4-lane configuration)
rx7_d2_p_i	I	Positive differential RX Ch7 D-PHY input data 2 (in case of 4-lane configuration)
rx7_d2_n_i	I	Negative differential RX Ch7 D-PHY input data 2 (in case of 4-lane configuration)
rx7_d3_p_i	I	Positive differential RX Ch7 D-PHY input data 3 (in case of 4-lane configuration)
rx7_d3_n_i	I	Negative differential RX Ch7 D-PHY input data 3 (in case of 4-lane configuration)
CSI72 TX Interface		
tx_clk_p_o	O	Positive differential TX D-PHY output clock
tx_clk_n_o	O	Negative differential TX D-PHY output clock
tx_d0_p_o	O	Positive differential TX D-PHY output data 0
tx_d0_n_o	O	Negative differential TX D-PHY output data 0

Port Name	Direction	Description
tx_d1_p_o	O	Positive differential TX D-PHY output data 1 (in case of 2-lane or 4-lane configuration)
tx_d1_n_o	O	Negative differential TX D-PHY output data 1 (in case of 2-lane or 4-lane configuration)
tx_d2_p_o	O	Positive differential TX D-PHY output data 2 (in case of 4-lane configuration)
tx_d2_n_o	O	Negative differential TX D-PHY output data 2 (in case of 4-lane configuration)
tx_d3_p_o	O	Positive differential TX D-PHY output data 3 (in case of 4-lane configuration)
tx_d3_n_o	O	Negative differential TX D-PHY output data 3 (in case of 4-lane configuration)

3. Design and Module Description

The top-level design (*csi2_aggr_vc_NX.v*) consists of the following modules:

- rx0*_unit (* is 0 - 7)
  - rx_dphy_0* (* is 0 - 7)
  - csi2_parser
  - rx_buffer
- tdm_ctrl
- tx_dphy_if
- tx_dphy
- int_osc
- int_gpll

The top-level design has a reset synchronization logic. In addition, GPLL may be added if necessary, according to RX and TX configurations.

3.1. rx0*_unit

This module is instantiated for each RX channel as a wrapper module to include rx_dphy, csi2_parser, and rx_buffer modules.

3.1.1. rx_dphy_0*

This module must be created for each RX channel according to channel conditions, such as the number of lanes, bandwidth, and others. Figure 3.1 shows an example of IP interface settings in the Lattice Radiant software for the CSI-2/DSI D-PHY Receiver Submodule IP. Create a separate rx_dphy IP for each RX channel even though their configurations are same. Refer to the CSI-2/DSI D-PHY Rx IP User Guide (FPGA-IPUG-02081) for details.

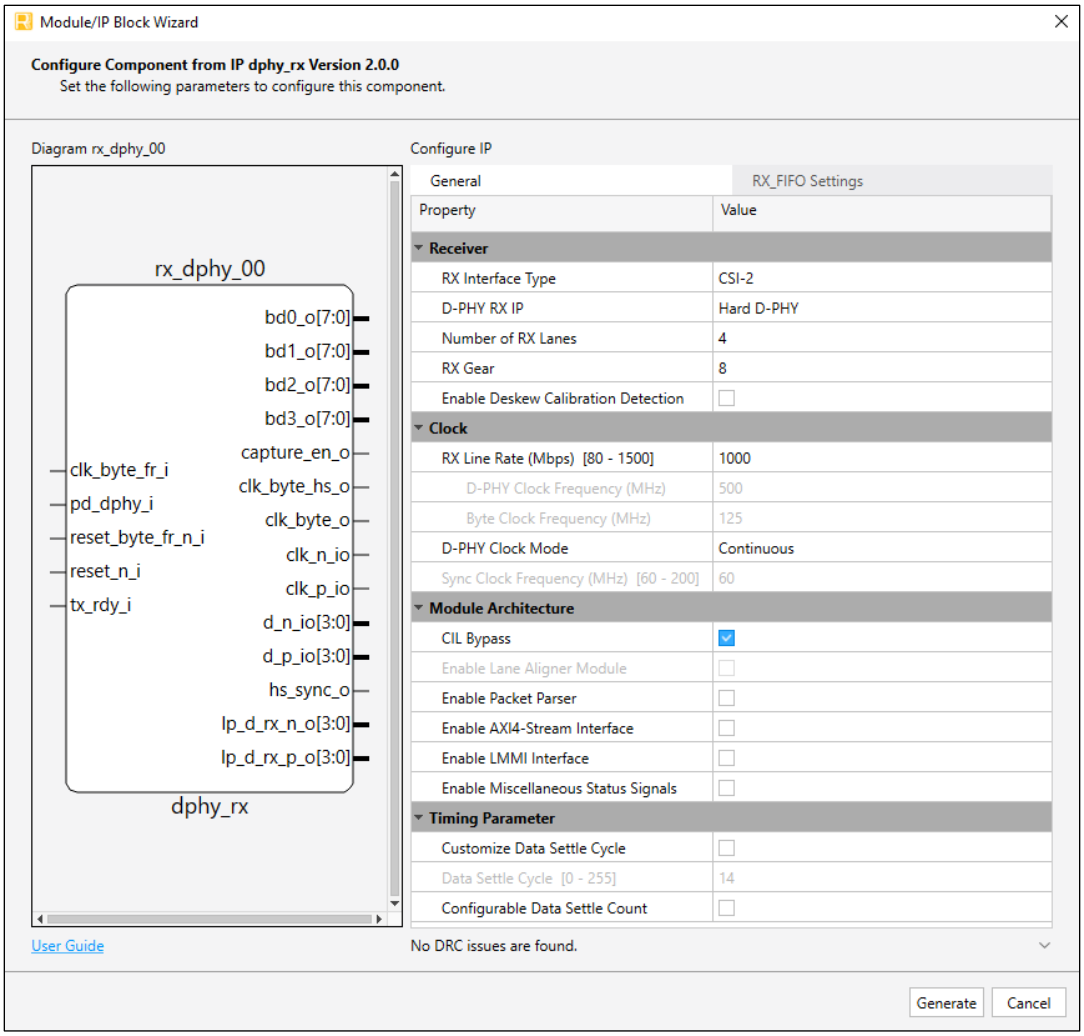

Figure 3.1. rx_dphy_0* IP Creation in the Lattice Radiant Software

The following shows guidelines and parameter settings required for this reference design.

General tab

- **RX Interface Type** – Select CSI-2.
- **D-PHY RX IP** – Select Hard D-PHY only for one RX channel, others must be Soft D-PHY. The setting must match RX*_D-PHY_HARD setting.
- **Number of RX Lanes** – Set according to channel configuration. The value must match NUM_RX*_LANE_* setting.
- **RX Gear** – Fixed to Gear 8 for this reference design.
- **Enable Deskew Calibration Detection** – Select disabled (unchecked).
- **RX Line Rate** – Set according to channel configuration. 1500 is the maximum for Soft D-PHY and Hard D-PHY with 4-lane configuration.
- **D-PHY Clock Mode** – Select Continuous or Non-continuous. This setting must match the RX*_CLK_MODE_* setting (Continuous = HS_ONLY, Non-continuous = HS_LP).
- **CIL Bypass** – For Hard D-PHY only, select enabled (checked).
- **Enable Lane Aligner Module** – Select Enabled for Soft D-PHY with 2-lane and 4-lane configurations.
- **Enable LMMI Interface** – Select disabled (unchecked).
- **Enable AXI4-Stream Interface** – Select disabled (unchecked).
- **Enable Packet Parser** – Select disabled (unchecked).
- **Enable Miscellaneous Status Signals** – Select disabled (unchecked).

- **Customize Data Settle Cycle** – Select Disabled (unchecked) to use the default pre-calculated tHS-Settle value by the IP.
- **Configurable Data Settle Count** – Select disabled (unchecked).

RX_FIFO Settings tab

- **RX_FIFO Enable** – Select disabled (unchecked) for continuous clock mode with Soft D-PHY, select enabled (checked) for all other modes.
- **Implementation** – Select LUT if **RX_FIFO Enable** is enabled (checked).
- **Depth** – For Hard D-PHY with continuous clock mode, select 8. For non-continuous clock mode, select 16.
- **Type** – Select SINGLE for Hard D-PHY or non-continuous clock mode with Soft D-PHY.
- **Packet Delay** – Set 1 for continuous clock mode with Hard D-PHY. For non-continuous clock mode, select 4.
- **Clock Mode** – Select DC (dual clock).
- **Misc Signals** – Select disabled (unchecked).

This module takes serial CSI-2 data and outputs byte data after de-serialization in CSI-2 High Speed mode. It is recommended to set the design name to *rx_dphy_00, rx_dphy_01, … , rx_dphy_07* so that you do not need to modify the instance names of these IPs in *rx_0*_unit.v* and the simulation setup file. Otherwise, you have to modify the names accordingly.

3.1.1.1. RX FIFO

RX FIFO is used as an elastic buffer, absorbing any PPM or phase differences between the continuous byte clock (clk_byte_fr_i) and the stoppable byte clock (clk_byte_hs_o). RX FIFO is mainly used in the non-continuous clock mode where the continuous byte clock is required to be generated externally. For continuous clock mode with Hard D-PHY, the IP automatically enables the FIFO. This FIFO resides after the word aligner for the Hard D-PHY RX IP and resides before the word aligner for the Soft D-PHY RX IP.

Hard D-PHY in Continuous Clock Mode

In this mode, the minimum configuration of RX FIFO is recommended as mentioned above (**Implementation** = LUT, **Depth** = 8, **Type** = SINGLE, **Packet Delay** = 1, **Clock Mode** = DC).

Soft D-PHY in Continuous Clock Mode

In this mode, RX FIFO is not necessary, and **RX_FIFO Enable** must be disabled (unchecked).

Non-Continuous Clock Mode

In this mode, the continuous byte clock (clk_byte_fr_i) must be generated with the same frequency as the stoppable byte clock (clk_byte_hs_o). The IP RX FIFO can be set at depth of 16 and delay the read by 4 to absorb any phase or small ppm differences.

3.1.2. csi2_parser

This module is instantiated for each RX channel to handle CSI-2 protocol decoding and VC overwrite. Upon receiving byte data from rx_dphy_0*, csi2_parser detects short and long packet headers. When RX*_VC_PASS_THROUGH is not defined, it replaces VC values with the value specified by RX*_NEW_VC and calculates ECC value based on this new VC value and other packet data. As a result, VC value and ECC are replaced with new values and sent to the next module (rx_buffer). As VC values of 4 and above are only supported by CSI-2 version 2.x, using 0 to 3 is safe in case of 2-to-4-channel aggregation. The downstream device must support CSI-2 version 2.x in case that VC = 4 or above is used. On the other hand, packet header data including VC values are not changed and passed through when RX*_VC_PASS_THROUGH is defined.

Figure 3.2 shows short packet capture and a new VC assignment when RX*VC_PASS_THROUGH is not defined, with 4 lanes RX D-PHY. The original VC=0 is replaced with VC=1 along with new ECC value calculated applying the new VC. 16-bit Data Field ({bd2_i, bd1_i}) is replaced with the frame counter value if RX*_FRAME_COUNT is defined. If not, the Data Field is passed through.

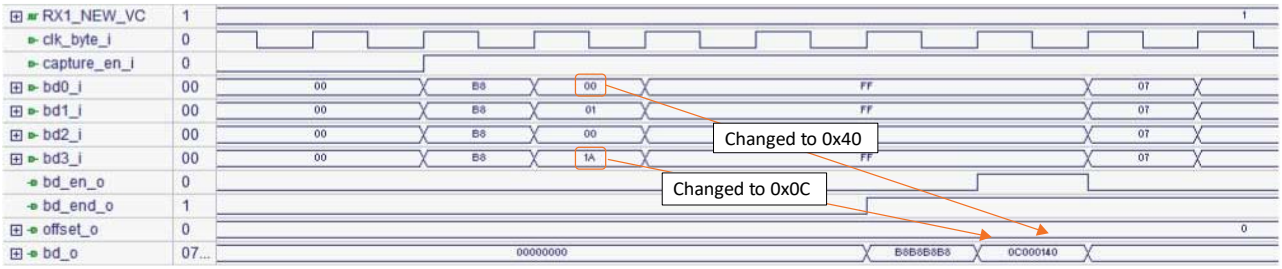

Figure 3.2. Short Packet Detection and VC Replacement

It is possible to do 16:1 aggregation using three CrossLink-NX devices with two CrossLink-NX devices in the first stage, both taking 8 RX channels and the third CrossLink-NX device takes the output of two CrossLink-NX to do 2:1 aggregation as the second stage. In this case RX*_VC_PASS_THROUGH must be defined in the second stage CrossLink-NX as each first stage TX output contains 8 channel data aggregated.

This module also detects the end of the current High Speed transmission by detecting the trailer byte and asserts the end flag sent to rx_buffer along with the offset info. Offset is a 3-bit data that indicates the number of remaining bytes in the final data transmission. This is modulo of 8 considering 64-bit transmission in case of four lanes with Gear 16 on TX side. Figure 3.3 and Figure 3.4 show the beginning and the end of long packet capture and transfer for 4 lanes RX D-PHY.

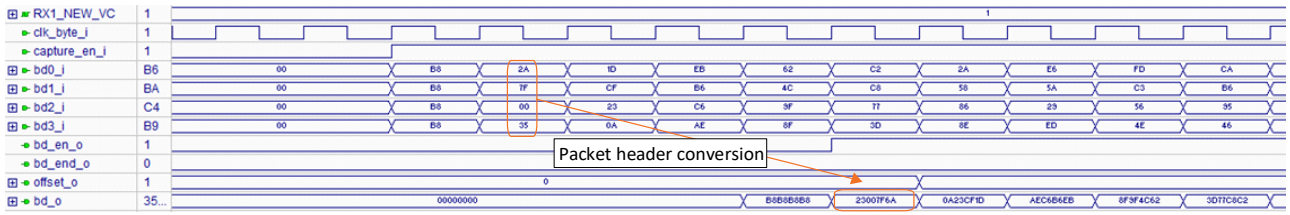

Figure 3.3. Long Packet Detection and VC Replacement

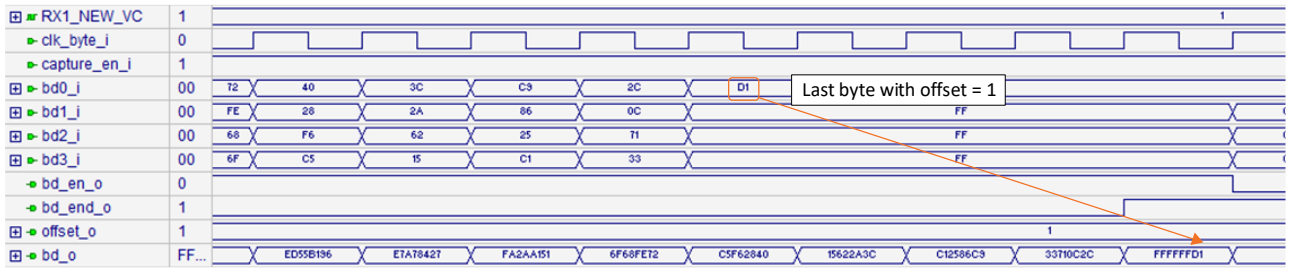

Figure 3.4. End of Long Packet with Trailer Bytes

3.1.3. rx_buffer

This module is instantiated for each RX channel to store HS transmission data to be read out by tdm_ctrl. Default buffer depth is 512, which means the buffer can store 512 × 64 bytes (NUM_TX_LANE_4 and TX_GEAR_16) or 512 × 32 bytes (others). 512 × 64 bytes FIFO requires two EBRs, therefore at least 16 EBRs are required for 8:1 aggregation with 4-lane TX and TX Gear 16 configuration. Buffer depth of 1024 or deeper is possible as long as the total number of EBR does not exceed 84 for LIFCL-40 and 24 for LIFCL-17. Data size of one HS transmission must not exceed FIFO size (for example, 1920 pixels of RAW10 makes 1920 × 5/4 = 2400 bytes, which is less than 1024 × 32, but more than 512 × 32). In case the data transfer to tdm_ctrl of the RX channel in question is in a queue and needs to wait for the completion of other channel data transmission, the FIFO has to begin storing the next line data. Therefore, it is safer to make the FIFO depth cover close to two HS transmission data. The first FIFO data is read out by this module with ready flag assertion, which happens at least 5 TX byte clock cycles after the data end flag (bd_end_i) assertion. The FIFO has extra data width to contain data end flag and offset data. This FIFO is a boundary between RX byte clock (write side) and TX byte

clock (read side) domain. The write side input ports are generated from the csi2_parser modules, while the read side input and output ports establish handshake with the tdm_ctrl module.

Figure 3.5 shows an example of short packet write transaction. An extra data write happens after the completion of every HS data transmission. This dummy write is necessary to ease the FIFO read timing to quit HS data read when it gets the end data flag. tdm_ctrl can stop fifo_re_i assertion in the next cycles when it sees bd_end_o =1. This module automatically reads the first data of each HS transmission. Along with ready flag (bd_rdy_o) assertion, it notifies tdm_ctrl that HS data is ready to be acquired from this channel. In this example, the offset is 4 as TX Gear is 16, which means 8 bytes are passed to tdm_ctrl in a single read cycle.

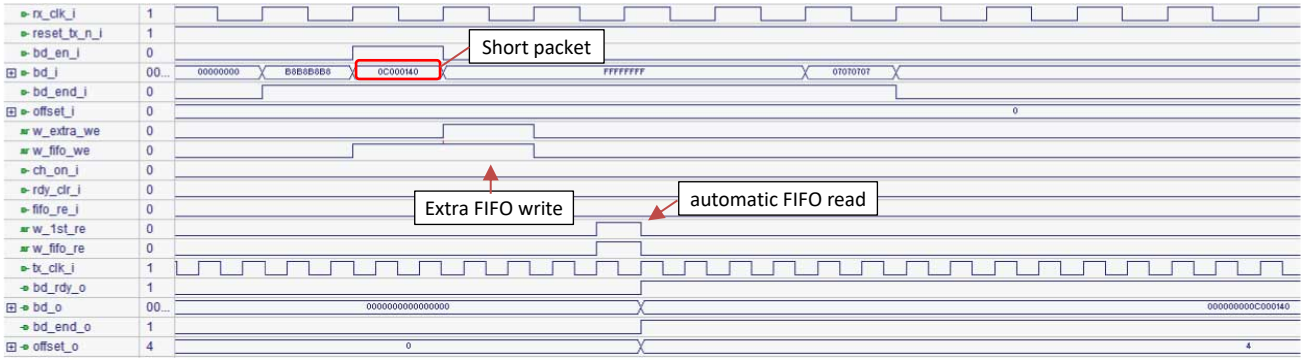

Figure 3.5. Short Packet Write

Figure 3.6 and Figure 3.7 show the beginning and end of long packet write transaction. In case of TX Gear 16, write happens every two cycles to form 64-bit byte data. Upon the detection of bd_end_i, an extra write enable is generated to write dummy data followed by the automatic first data read with bd_rdy_o assertion.

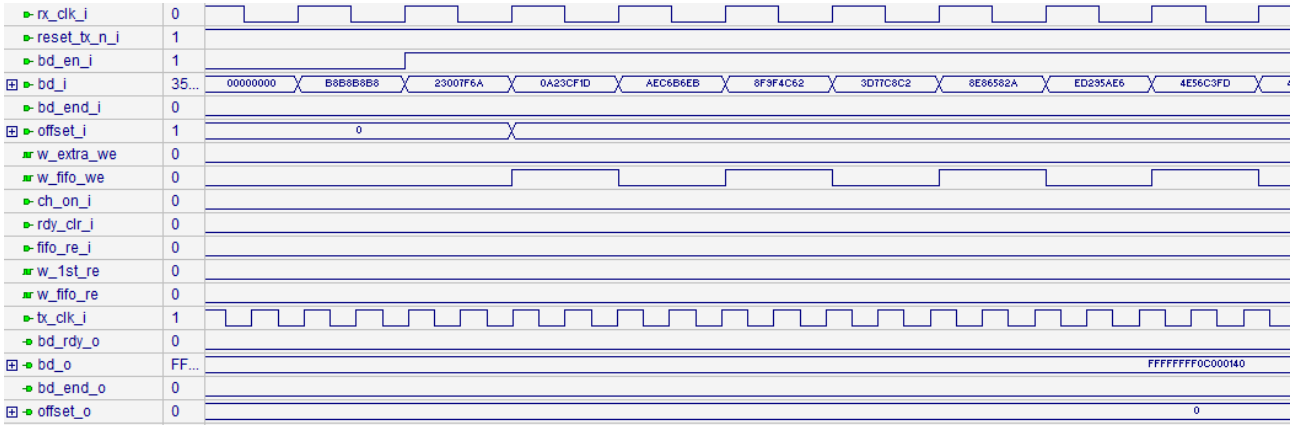

Figure 3.6. Beginning of Long Packet Write

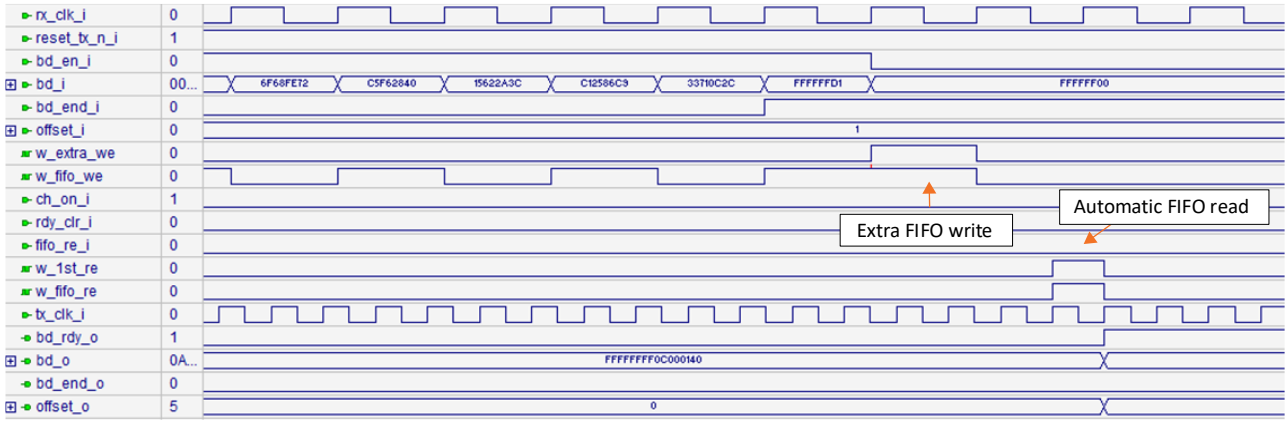

Figure 3.7. End of Long Packet Write

Figure 3.8 shows short packet read transaction. rdy_clr_i comes from tdm_ctrl to clear bd_rdy_o. The valid data (0x0c000140) is already on bd_o when fifo_re_i is asserted because of the automatic first data read. Therefore, this fifo_re_i reads an extra dummy data and discarded by tdm_ctrl. bd_end_o is used to terminate fifo_re_i by tdm_ctrl.

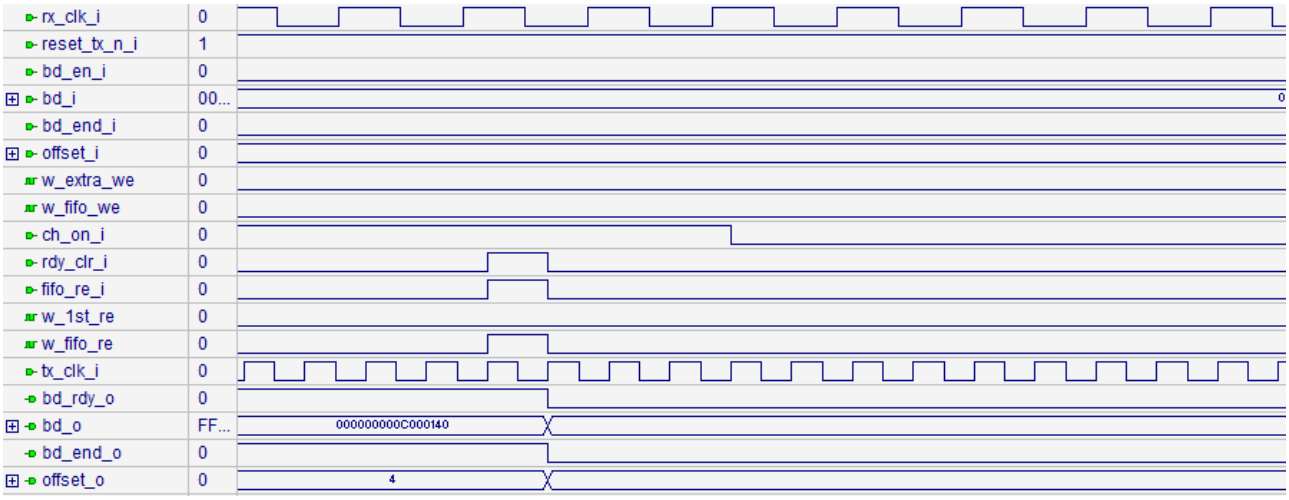

Figure 3.8. Short Packet Read

Figure 3.9 shows end of long packet read. Upon the detection of bd_end_o, fifo_re_i is de-asserted. In this example, the last data is “0xD133710C2C” as offset_o is 5.

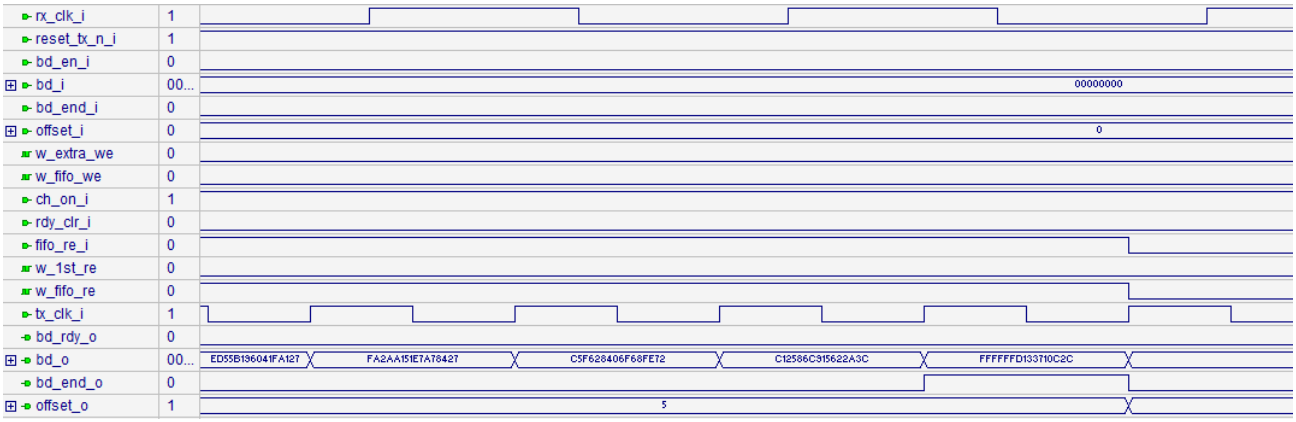

Figure 3.9. End of Long Packet Read

3.2. tdm_ctrl

This module monitors the ready flags of the RX channels and takes the HS transmission data of the selected channel. TX D-PHY data lane goes into LP mode after every HS data transfer of a single RX channel and come back to HS mode when the next HS transmission begins with the new RX channel data. The channel selection is based on a round robin fashion when multiple RX channel data are available signified by the assertion of the ready flags. Incoming data width is either 32 or 64, but the outgoing data width is adjusted to TX Lane count * TX_GEAR, which means 8, 16, 32, or 64. In case of 8 or 16, FIFO read enable is asserted once every 4 or 2 TX byte clock cycles. When the data end flag is detected, the trailer bytes are appended. The beginning of trailer byte within 16/32/64 bytes is judged by offset data obtained from rx_buffer when the end flag is detected.

Figure 3.10 shows an example of a 4-channel aggregation global sequence of tdm_ctrl. tdm_ctrl monitors all ready signals (rx0_rdy_i, … rx3_rdy_i) and decides which RX channel data is aggregated for the next transmission. In this example, channel 0 is selected as ready flag is asserted only on channel 0. tdm_bgn_i is a trigger signal to begin reading FIFO data from rx_buffer. rx0_rdy_clr_o is asserted to clear rx0_rdy_i and rx0_fifo_re_o is asserted to begin reading FIFO data from rx0_buffer. Read data are sent to the next module (tx_dphy_if) for transmission. Other channel data are also transferred in the same manner.

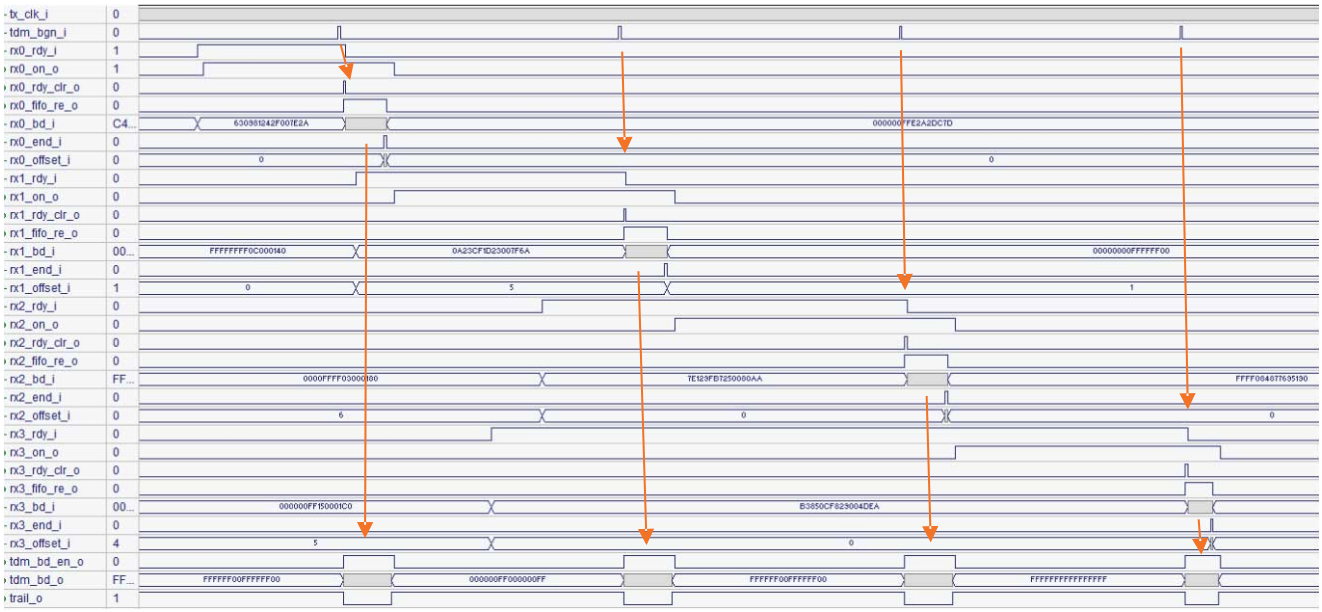

Figure 3.10. Global Sequence of tdm_ctrl

Trailer byte appending is another important feature of tdm_ctrl in addition to TDM of RX channel data. Figure 3.11 shows an example. The last valid data is 0x0C07D0 (rx3_offset_i = 3 when rx3_end_i = 1). Trailer bytes against these are 0xFFFF00. MSByte of the previous data is 0x59 and trailer byte against this is 0xFF. Therefore, 0xFFFFFF00FF is appended as trailer bytes, which appears as upper 5 bytes with the last valid data (0x0C07D0) followed by two sets of 0xFFFFFF00 along with trail_o assertion.

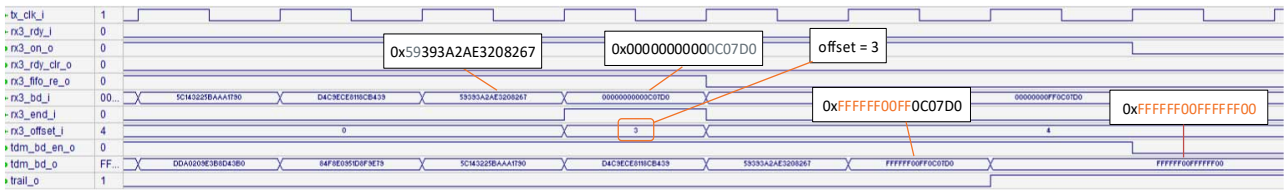

Figure 3.11. Trailer Byte Appending

3.3. tx_dphy_if

This module reallocates byte data coming from tdm_ctrl and sends to tx_dphy according to TX lane and TX Gear value. In addition, it monitors ready flag from rx_buffer modules and ready flag from tx_dphy to control tdm_bgn_o that triggers TDM operation in tdm_ctrl. Figure 3.12 shows global operation of tx_dphy_if including tx_dphy signals. tx_dphy_if asserts clk_hs_en_o and d_hs_en_o to make both clock and data lane from LP mode to HS mode. After that d_hs_rdy_i is asserted by tx_dphy. Confirming at least one of ready flags from rx_buffer is asserted, tdm_bgn_o is asserted to let tdm_ctrl begins a new HS data transmission.

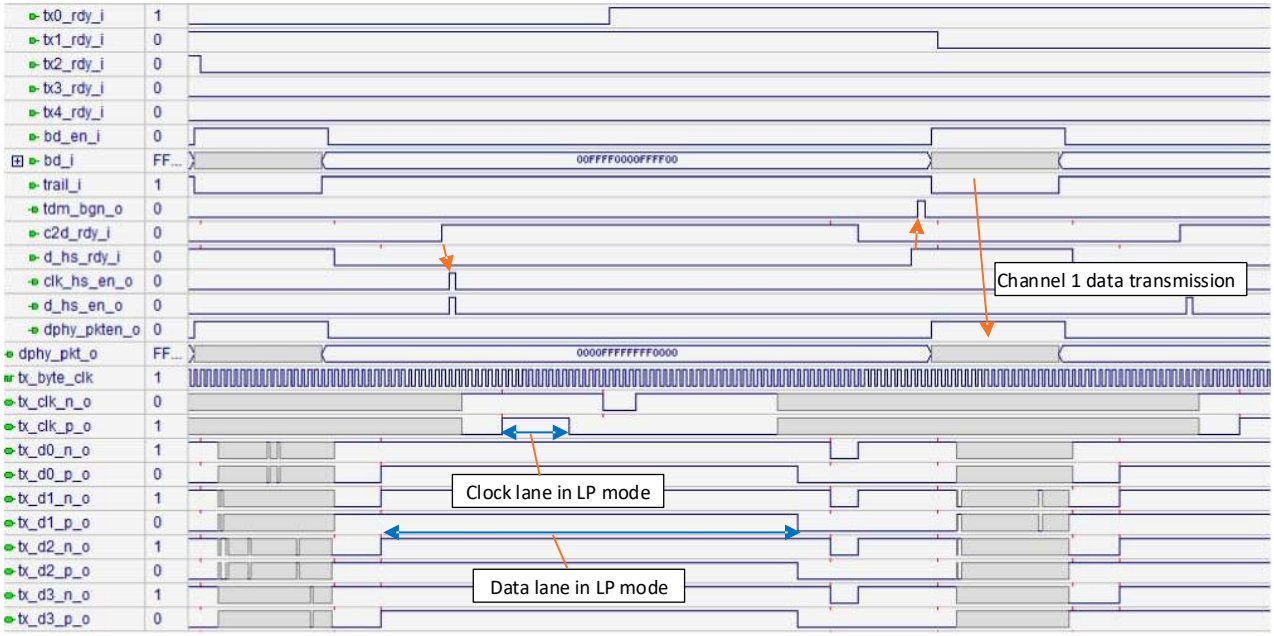

Figure 3.12. Global Operation of tx_dphy_if

3.4. tx_dphy

You must create this module according to channel conditions, such as number of lanes, bandwidth, and others. Figure 3.13 shows an example IP interface setting in the Lattice Radiant software for the CSI-2/DSI D-PHY Transmitter Submodule IP. Refer to the CSI-2/DSI D-PHY Tx IP User Guide (FPGA-IPUG-02080) for details.

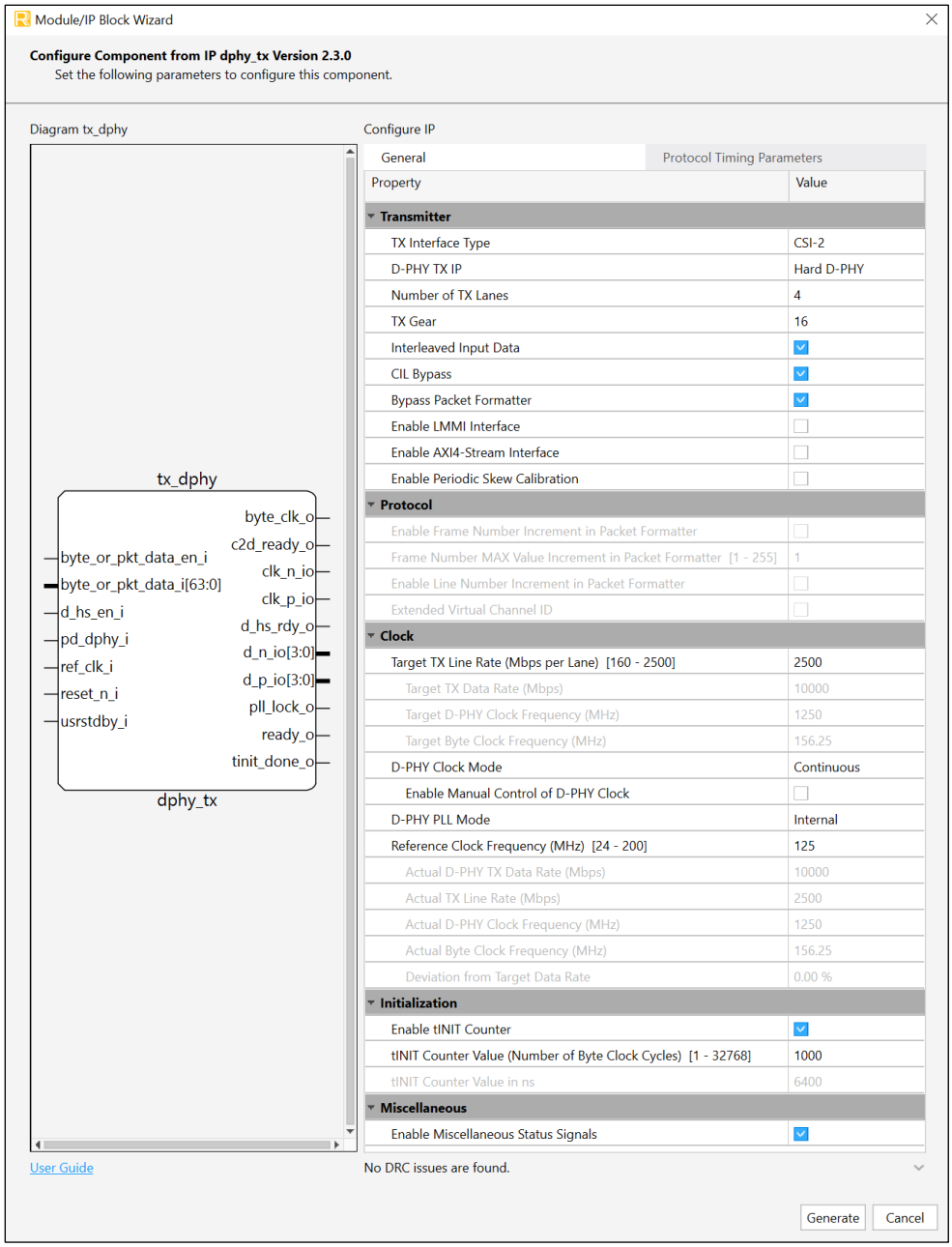

Figure 3.13. tx_dphy IP Creation in the Lattice Radiant Software

The following shows guidelines and parameter settings required for this reference design.

- **TX Interface Type** – Select CSI-2.
- **D-PHY TX IP** – Select Hard D-PHY.
- **Number of TX Lanes** – Set according to channel configuration. Must match NUM_TX_LANE_* setting.
- **TX Gear** – Set to 16 if the **Target TX Line Rate** is higher than 1500 Mbps, otherwise set to 8.
- **Interleaved Input Data** – Select checkbox to enable (checked).
- **CIL Bypass** – Select checkbox to enable (checked).
- **Bypass Packet Formatter** – Select checkbox to enable (checked).
- **Enable LMMI Interface** – Select disabled (unchecked).
- **Enable AXI4-Stream Interface** – Select disabled (unchecked).
- **Enable Periodic Skew Calibration** – Select disabled (unchecked).

- **Target TX Line Rate** – Set according to channel configuration. Total bandwidth must be fast enough to aggregate all RX channel data with extra overhead for the transitions between HS and LP modes.
- **D-PHY Clock Mode** – Set according to channel configuration. Select Continuous when the TX bandwidth margin is small. This setting must match the TX*_CLK_MODE_* setting (Continuous = HS_ONLY, Non-continuous = HS_LP).
- **Enable Manual Control of D-PHY Clock** – Select checkbox to disable (unchecked).
- **D-PHY PLL Mode** – Select Internal.
- **Reference Clock Frequency** – Set the appropriate value which can be obtained from the ref_clk_i pin, one of the continuous rx*_byte_clk, or on-chip GPLL. This clock frequency must be in the range of 20 MHz – 200 MHz.
- **Enable tINIT Counter** – Enabled (checked) is recommended.
- **tINIT Counter Value** – 1000 (default) is recommended.
- **Enable Miscellaneous Status Signals** – Must be set to enabled (checked).
- **Protocol Timing Parameters** tab – Default values are recommended.

This module takes the byte data and outputs CSI-2 data after serialization in CSI-2 High Speed mode. It is recommended to set the design name to *tx_dphy* so that you do not need to modify the instance name of this IP in the top-level design and simulation setup file. Otherwise, you need to modify the names accordingly.

TX Gear 8 is automatically selected by the Lattice Radiant software when the lane bandwidth is less than 1500 Mbps, which means TX byte clock can be ~187.5 MHz.

TX Line Rate setting is one of the key factors in this reference design. Calculating the required TX lane bandwidth is derived from the following equation:

$$TX\_lane\_bandwidth = \frac{1}{m}\sum_{k=0}^{n-1} number\_of\_lanes\_in\_RX[k] \ * lane\_bandwidth\_in\_RX[k]$$

where *m* is number of TX lanes and *n* is number of RX channels.

Example: 8 to 1 aggregation with the following configuration

RX0: 4 lanes, 1000 Mbps / lane,

RX1: 4 lanes, 360 Mbps / lane,

RX2: 2 lanes, 480 Mbps / lane,

RX3: 1 lane, 440 Mbps / lane,

RX4: 1 lane, 240 Mbps / lane,

RX5: 1 lane, 1480 Mbps / lane,

RX6: 2 lanes, 320 Mbps / lane,

RX7: 2 lanes, 280 Mbps / lane,

TX: 4 lanes

Then TX lane bandwidth = (4 x 1000 + 4 x 360 + 2 x 480 + 1 x 440 + 1 x 240 + 1 x 1480 + 2 x 320 + 2 x 280) / 4 = 2.44 Gbps.

The above configuration does not work if RX channels do not have enough length of blanking (LP) periods. The TX bandwidth is fast enough to cover all of RX channel HS data transmissions, but transition time going back and forth between HS and LP mode cannot be proportionally shrunk by increasing TX bandwidth. The guideline of minimum blanking period per active line is (500 ns x number of RX channels) if the above equation is used to get TX lane bandwidth, assuming continuous clock (HS_ONLY mode) is set in TX D-PHY. In case of non-continuous clock (HS_LP mode), the required blanking period is doubled. TX lane bandwidth has to be raised from the above value in case that RX channel cannot have enough blanking periods. Increasing RX FIFO size can be an alternative option in some cases, but most likely this is not as effective.

You must monitor FIFO overflow flags of all rx_buffer modules (rx*_fifo_full) instantiated and increase the TX bandwidth if any of rx_buffer FIFO overflow happens.

3.5. int_osc

This module generates ~75 MHz clock used for sync clock and rx*_clk_lp_ctrl. sync clock is used by Soft D-PHY RX IP and rx*_clk_lp_ctrl is used by all RX D-PHY IP, which are in non-continuous clock mode. If a continuous clock above 60 MHz is available, you can use that without instantiating this module.

3.6. int_gpll

This module generates continuous byte clock(s) used for RX channels in non-continuous clock mode. If all RX channels are in continuous clock mode or continuous byte clock(s) for RX channels in non-continuous clock mode are already available, this module is not necessary.

In case of non-continuous clock (HS_LP) mode in RX, each RX channel requires two clock trees (non-continuous RX byte clock and continuous RX byte clock) in CrossLink-NX device. As CrossLink has 32 primary clock trees, it is possible to use HS_LP mode in all RX channels when appropriate continuous byte clocks are obtained for all RX channels. Therefore, you have to make sure that the continuous clock can be obtained to set the non-continuous clock mode in RX D-PHY on RX channels. The following are possible candidates of the continuous clock:

- GPLL outputs driven by the external reference clock or a continuous byte clock from other channels
- Continuous byte clock from other channels (either directly or after divider)
- Continuous clock fed from I/O pin (either directly or after divider)

The sample design (*csi2_aggr_vc_NX.v*) assumes that RX channel #0 is in HS_ONLY mode and other RX channels are in HS_LP mode. In this example, the continuous byte clock for RX channel #1-7 and TX byte clock are generated by the on-chip GPLL taking the external clock as a reference clock. The code snippets are shown below. *int_gpll* is the name used in this top-level design. This name has to be changed if the different name is used.

```
////////////////////////////////////////////////////////////////////////////////
///// Reference Clock generation to TX D-PHY                                /////
///// Customer has to modify here according to the available clock for TX-DPHY /////
///// tx_refclk must be in the range of 20-200 MHz.                         /////
////////////////////////////////////////////////////////////////////////////////

wire gpll_refclk;

`ifdef EXT_REF_CLK
       assign tx_refclk = ref_clk_i;
       assign gpll_refclk = ref_clk_i;
`else
       assign tx_refclk = rx0_clk_byte_fr; // could be from other channels
       assign gpll_refclk = rx0_clk_byte_fr; // could be from other channels
`endif

////////////////////////////////////////////////////////////////////////////////
///// below is just a reference only and to be modified according to the   /////
///// customer's application                                             //////
////////////////////////////////////////////////////////////////////////////////

//assign gpll_lock = 1;       // when GPLL is not in use


//// CrossLink-NX GPLL
int_gpll pll_inst (
       .rstn_i (reset_n_i),
       .clki_i (gpll_refclk),
       .clkop_o       (gpll_clk_op),
       .clkos_o       (gpll_clk_os),
       .clkos2_o      (gpll_clk_os2),
```

```
        .clkos3_o       (gpll_clk_os3),
        .lock_o (gpll_lock)
);
```

On TX side, using continuous or non-continuous clock mode does not affect the number of necessary clock trees (always use one clock tree). To feed a clock to TX D-PHY IP, the external clock is necessary if continuous RX byte clocks are not appropriate to generate the desired clock for TX D-PHY. The clock to TX D-PHY must be continuous and in the range of 24 – 200 MHz.

4. Design and File Modifications

This reference design is based on RX D-PHY IP v2.0.0 and TX D-PHY IP v2.3.0. Some modifications are required depending on your configuration in addition to two directive files (*synthesis_directives.v*, *simulation_directives.v*). To modify the reference design, follow these steps:

1. Determine the configuration to modify such as number of sensors, lanes, bitrates, and clock modes.
2. Determine the FIFO depths, RX D-PHY, and Tx D-PHY configurations using the Microsoft Excel calculator (*docs/vc_aggr_NX_clock.xlsx*).
   - For non-continuous clock mode, use the calculator to determine if the continuous byte clock with the same frequency as the stoppable byte clock can be generated. For example, to use GPLL to generate those continuous byte clocks, use the IP GUI for GPLL to determine the feasibility.
3. Launch the Lattice Radiant software and open the project (*fpga_lifcl/radiant/csi2_aggr_vc_RD_NX.rdf*).
4. Configure and generate the IPs per the configurations.
5. Modify the *synthesis_directives.v* file as described in Synthesis Directives section.
6. Modify the *simulation_directives.v* file as described in the Simulation Directives section and run the RTL simulation to ensure the modifications are correct.
   - To speed up the RTL simulation, reduce the number of lines or frames (CH*_NUM_LINES and CH*_NUM_FRAMES in the *simulation_directives.v* file).
7. Modify the post synthesis constraint file to define the design pins placement, and define the external clocks for timing analysis as described in the Post Synthesis Constraint File section.

4.1. Top-Level RTL

The GPLL setting in the current top-level file (*csi2_aggr_vc_NX.v*) is based on the configuration shown in Figure 1.2. and Figure 1.3. According to the configuration you use, you have to modify the GPLL instantiation as described in int_gpll section. You can also remove the int_osc module if the appropriate sync clock and r*_clk_lp_ctrl are already available. You may have to change the continuous byte clock (clk_byte_fr_i) connections for each rx_dphy_0* to match to the intended clock source.

In addition, an instance name of IP modules (tx_dphy, rx_dphy_0*) have to be modified if you create this IP with a different name.

4.2. rx0*_unit

An instance name of RX D-PHY (rx_dphy_0*) has to be modified if you create this IP with a different name.

4.3. Post Synthesis Constraint File

The provided constraint file (*csi2_aggr_vc_NX.pdc*) contains the timing constraints used in this design. You may need to change the variable DPHY*_CLK_PER to match the period of each of the D-PHY RX channels, in nanoseconds.

If you source the reference clock via external pin instead of reusing the continuous byte clock from rx_dphy_00, you need to add the following timing constraints:

```
create_clock -name {ref_clk_i} -period <Reference Clock Period in ns> [get_ports ref_clk_i]
```

If all the external clocks are properly defined, the other constraints from the IPs such as byte clocks or PLL output clocks definition are automatically propagated. You can check the timing reports to ensure the constraint coverage is sufficient (more than 90%), and all the target clocks frequency are correct.

You may also add the physical constraints into this file to assign each of the design ports according to your boards and devices.

5. Design Simulation

The script file (*fpga_lifcl/sim/questa/run_sim.do*) and testbench files are provided to run the functional simulation by QuestaSim®. If you follow the naming recommendations regarding design name and instance name when RX and TX D-PHY IPs are created by the Lattice Radiant software, you can follow the steps to run the simulation as follows:

1. Launch QuestaSim using the Lattice Radiant software.
2. Execute the following command in the QuestaSim terminal.

```
cd ../sim/questa
source run_sim.do
```

You need to modify *simulation_directives.v* according to your configuration (refer to the Simulation Directives section for details). By executing the script in QuestaSim, compilation and simulation are executed automatically. The testbench takes all data comparison between the expected data and output data from the reference design, including VC and ECC data modifications. The QuestaSim terminal shows the following statements while running and doing data comparison:

```
…
# [163857056470][DPHY_CHK] payload data = 18 62 b3 74 --- Data matches ch5 : 18 62 b3 74
# [163857376470][DPHY_CHK] payload data = 66 fa c5 03 --- Data matches ch5 : 66 fa c5 03
# [163857696470][DPHY_CHK] payload data = f8 58 4f 27 --- Data matches ch5 : f8 58 4f 27
# [163858016470][DPHY_CHK] payload data = 7e 8c e6 21 --- Data matches ch5 : 7e 8c e6 21
# [163858336470][DPHY_CHK]CRC = dfdf
#         163858336500 Data matches ch5 : df df
# [163868376470][DPHY_TX_HS_LP_CHK] HS to LP11 Transition on D0 lane with HS-TRAIL period = 100 ns
#         164286352800 DPHY CH 5 CLK : Driving HS-CLK-RQST
#         164291352800 DPHY CH 5 CLK : Driving HS-Prpr
#         164295152800 DPHY CH 5 CLK : Driving HS-Go
#         164321352800 DPHY CH 5 CLK : Driving HS-0/HS-1
#         164322020000 DPHY CH 5 DATA : Driving HS-RQST
#         164327020000 DPHY CH 5 DATA : Driving HS-Prpr
#         164331353600 DPHY CH 5 CLK : Driving HS-Go
#         164342452300 DPHY CH 5 CLK : Driving SYNC Data
#         164342452300 DPHY CH 5 Lane 0 : Driving with data = b8
#         164343161100 DPHY CH 5 Driving Data header
#         164343161100 DPHY CH 5 Driving Data header for data = 59
#         164343161100 DPHY CH 5 Lane 0 : Driving with data = 59
#         164343828300 DPHY CH 5 Driving Data header for data = 58
#         164343828300 DPHY CH 5 Lane 0 : Driving with data = 58
#         164344495500 DPHY CH 5 Driving Data header for data = 02
#         164344495500 DPHY CH 5 Lane 0 : Driving with data = 02
#         164345162700 DPHY CH 5 Driving Data header for data = a9
#         164345162700 DPHY CH 5 Lane 0 : Driving with data = a9
#         164345829900 DPHY CH 5 Driving Data
#         164345829900 DPHY CH 5 Lane 0 : Driving with data = a9
#         164346497100 DPHY CH 5 Driving Data
#         164346497100 DPHY CH 5 Lane 0 : Driving with data = 6f
#         164347164300 DPHY CH 5 Driving Data
#         164347164300 DPHY CH 5 Lane 0 : Driving with data = 75
#         164347831500 DPHY CH 5 Driving Data
#         164347831500 DPHY CH 5 Lane 0 : Driving with data = 16
#         164348498700 DPHY CH 5 Driving Data
#         164348498700 DPHY CH 5 Lane 0 : Driving with data = 2a
#         164349165900 DPHY CH 5 Driving Data
#         164349165900 DPHY CH 5 Lane 0 : Driving with data = 45
#         164349833100 DPHY CH 5 Driving Data
#         164349833100 DPHY CH 5 Lane 0 : Driving with data = 20
```

```
#         164350500300 DPHY CH 5 Driving Data
#         164350500300 DPHY CH 5 Lane 0 : Driving with data = 9f
#         164351167500 DPHY CH 5 Driving Data
#         164351167500 DPHY CH 5 Lane 0 : Driving with data = 88
#         164351834700 DPHY CH 5 Driving Data
#         164351834700 DPHY CH 5 Lane 0 : Driving with data = 11
#         164352501900 DPHY CH 5 Driving Data
#         164352501900 DPHY CH 5 Lane 0 : Driving with data = 02
#         164353169100 DPHY CH 5 Driving Data
#         164353169100 DPHY CH 5 Lane 0 : Driving with data = d1
#         164353836300 DPHY CH 5 Driving Data
#         164353836300 DPHY CH 5 Lane 0 : Driving with data = 25
#         164354503500 DPHY CH 5 Driving Data
…
```

An example of the statements at the end of simulation is as follows:

```
…
# [165387096470][DPHY_TX_HS_LP_CHK] HS to LP11 Transition on D0 lane with HS-TRAIL period = 103 ns
#         167452855200 DPHY CH 5 CLK CONT : Driving CLK-Trail
#         167458838400 TEST END
#
# CH #0 (VC = 0) : 51 / 51 HS transmission completed successfully
# CH #1 (VC = 1) : 51 / 51 HS transmission completed successfully
# CH #2 (VC = 2) : 51 / 51 HS transmission completed successfully
# CH #3 (VC = 3) : 14 / 14 HS transmission completed successfully
# CH #4 (VC = 5) : 36 / 36 HS transmission completed successfully
# CH #5 (VC = 9) : 160 / 160 HS transmission completed successfully
# CH #6 (VC = 11) : 51 / 51 HS transmission completed successfully
# CH #7 (VC = 15) : 36 / 36 HS transmission completed successfully
#
### Simulation Completed ###
```

One HS transmission is either Frame Start/End short packet or long packet of one active video line. The result is fine if the numerator is equal to the denominator in the statements.

You must set small values in CH*_NUM_LINES and CH*_NUM_PIXELS directives in the *simulation_directives.v* file, especially in the first simulation trial to minimize simulation time. On the other hand, it makes sense to set the actual value to CH*_NUM_PIXELS directives and CH*_DPHY_LPS_GAP directives when TX bandwidth cannot have extra margin against total RX bandwidth. By setting realistic values, FIFO overflow can be detected when the margin is not large enough.

Figure 5.1. shows an example of 4-channel aggregation. tx*_bd_rdy = 1 indicates the waiting period from the completion of one HS transmission data write (to rx_buffer) to the start of FIFO read by tdm_ctrl. This waiting period gets longer when the channel in question is in a cue to be read by tdm_ctrl.

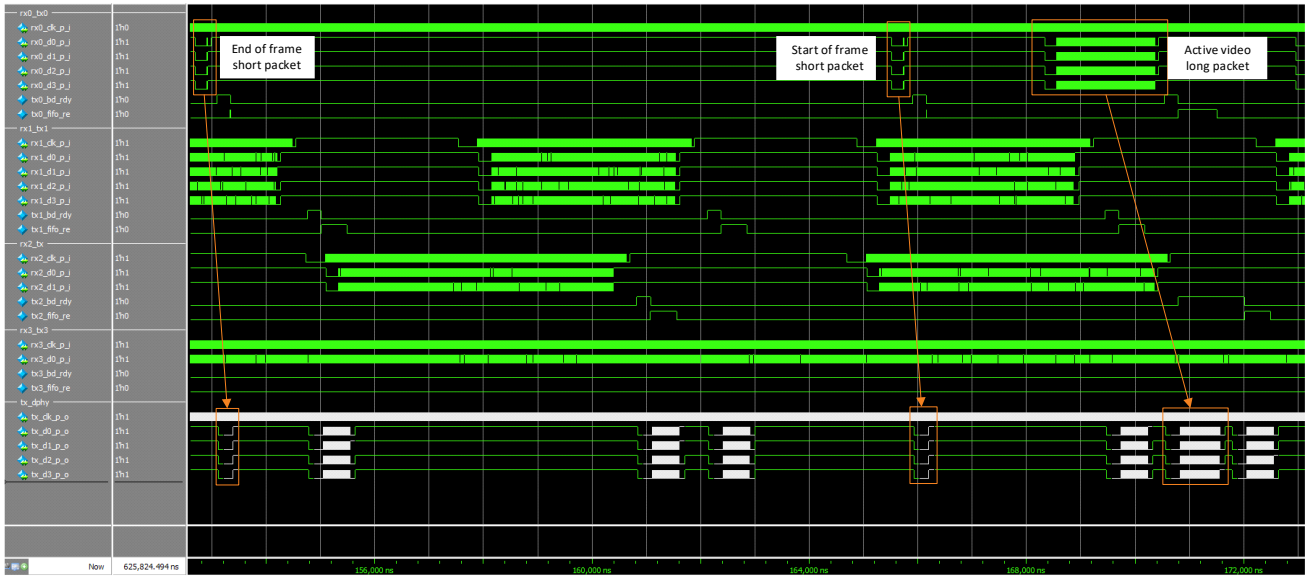

Figure 5.1. Functional Simulation Example

Figure 5.2. shows an example of FIFO overflow in rx_buffer. The active video line is too long and cannot be accomodated by the FIFO in the rx_buffer, causing the buffer to overflow. Simulation automatically stops when FIFO overflow happens.

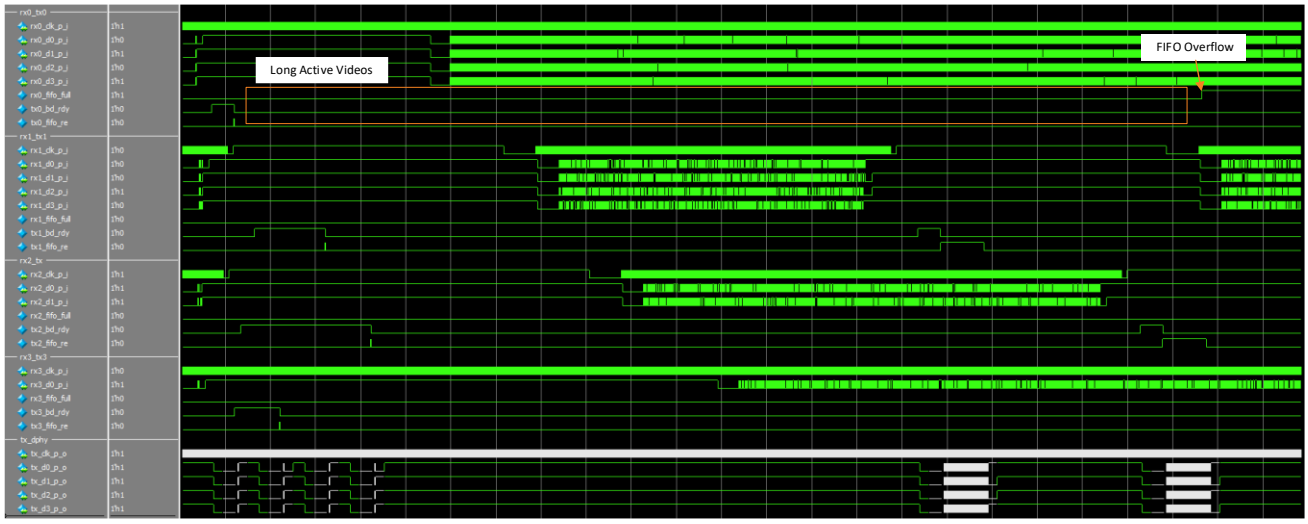

Figure 5.2. FIFO Overflow

6. Known Limitations

The limitations of this reference design are as follows:

- RX Gear 16 is not supported.
- For non-continuous RX clock mode, the continuous byte clock (clk_byte_fr_i) must have the same frequency as the stoppable byte clock (clk_byte_hs_o).

7. Design Package and Project Setup

Figure 7.1. shows the directory structure. The design is targeted for LIFCL-40CABGA400. *synthesis_directives.v* and *simulation_directives.v* are set to configure eight RX channels as an example shown below:

- RX CH #0 : 4 lanes with Hard D-PHY in continuous clock mode
- RX CH #1 : 4 lanes with Soft D-PHY in non-continuous clock mode
- RX CH #2 : 2 lanes with Soft D-PHY in non-continuous clock mode
- RX CH #3 : 1 lane with Soft D-PHY in continuous clock mode
- RX CH #4 : 1 lane with Soft D-PHY in non-continuous clock mode
- RX CH #5 : 1 lane with Soft D-PHY in non-continuous clock mode
- RX CH #6 : 2 lanes with Soft D-PHY in continuous clock mode
- RX CH #7 : 2 lanes with Soft D-PHY in continuous clock mode
- TX : 4 lanes with Gear 16

You can modify the directives for your configuration.

```
├──docs                              # Contains the helper Excel sheet
└──fpga_lifcl
   ├──radiant                        # Contains the Lattice Radiant project files
   │  └──src
   │     ├──constraints              # Contains physical design constraints (.pdc) files
   │     ├──ip                       # Contains generated IPs from Lattice Radiant
   │     │  ├──int_gpll
   │     │  ├──int_osc
   │     │  ├──rx_dphy_00
   │     │  ├──rx_dphy_01
   │     │  ├──rx_dphy_02
   │     │  ├──rx_dphy_03
   │     │  ├──rx_dphy_04
   │     │  ├──rx_dphy_05
   │     │  ├──rx_dphy_06
   │     │  ├──rx_dphy_07
   │     │  └──tx_dphy
   │     ├──rtl                      # Contains the RTLs used in the reference design
   │     └──testbench                # Contains testbench files used in the reference design
   └──sim
      └──questa                      # Contains QuestaSim .do file for RTL simulation
```

Figure 7.1. Directory Structure

Figure 7.2 shows design files used in the Lattice Radiant software project. Including PLL and oscillator modules, the Lattice Radiant software creates 11 *.ipx* files. By specifying csi2_aggr_vc_NX as a top-level design, all unnecessary files are ignored.

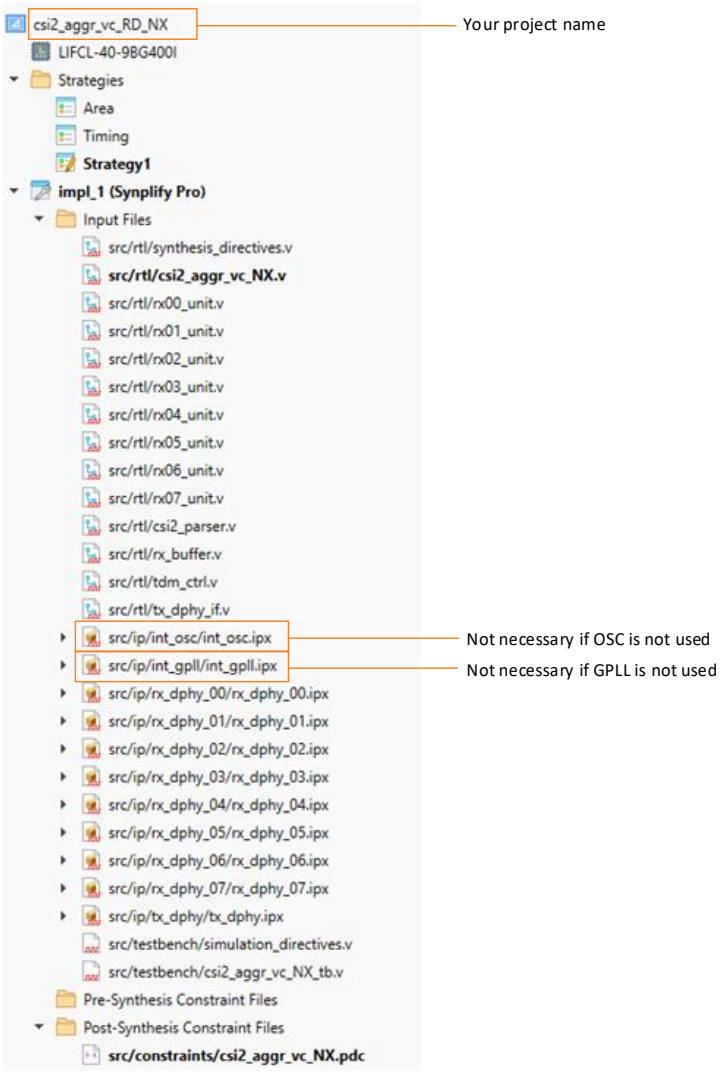

Figure 7.2. Project Files

8. Resource Utilization

Resource utilization depends on the configurations. Table 8.1 shows resource utilization examples under certain configurations targeting LIFCL-40. This is just a reference and actual usage varies. EBR usage depends on the horizontal resolution of each RX channels.

Table 8.1. Resource Utilization Examples

Configuration	LUT	FF	EBR	I/O
8 RX channels with 4/4/2/1/1/1/2/2 lanes, TX 4 lanes with Gear 16	8907	5853	34	41
6 RX channels with 4/4/2/1/1/1 lanes, TX 4 lanes with Gear 16	6780	4471	26	29
4 RX channels with 4/4/2/1 lanes, TX 4 lanes with Gear 16	4948	3351	18	21
2 RX channels with 4/4 lanes, TX 4 lanes with Gear 8	2931	2109	12	11

References

- MIPI Alliance web page for D-PHY Version 1.2, and Camera Serial Interface 2 (CSI-2) Version 1.2 and Version 2.0
- CSI-2/DSI D-PHY Tx IP User Guide (FPGA-IPUG-02080)
- CSI-2/DSI D-PHY Rx IP User Guide (FPGA-IPUG-02081)
- CrossLink-NX web page
- MIPI CSI-2 Virtual Channel Aggregation Reference Design web page
- Lattice Radiant Software web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/en/Support/AnswerDatabase.

Revision History

Revision 1.2, September 2025

Section	Change Summary
All	• Renamed document from *MIPI CSI-2 Virtual Channel Aggregation with CrossLink-NX* to *MIPI CSI-2 Virtual Channel Aggregation with CrossLink-NX Devices*. • Performed minor formatting and editorial edits.
Inclusive Language	Added inclusive language boilerplate.
Supported Device and IP	Updated IP and software versions, and moved to section 1.1 Supported Device and IP.
Introduction	• Added link to the reference design web page in the Introduction section. • Added the Supported Device and IP section. • Updated the non-continuous clock mode in the Features List section. • Updated the description on the clocking scheme example and updated Figure 1.2. Clocking Scheme Example in the Block Diagram section. • Updated the description on the Microsoft Excel calculator and updated Figure 1.3. Microsoft Excel Calculator in the RX and TX Permutations section.
Parameters and Port List	Updated the note on HS_LP mode in Table 2.1. Synthesis Directives.
Design and Module Description	• Updated Figure 3.1. rx_dphy_0* IP Creation in the Lattice Radiant Software and the parameter settings in the rx_dphy_0* section. • Updated the description on the RX FIFO and the clock modes in the RX FIFO section. • Mentioned that the short and long packet captures are for 4 lanes RX DPHY in the csi2_parser section. • Updated the description on the module operation and ports in the rx_buffer section. • Updated Figure 3.13. tx_dphy IP Creation in the Lattice Radiant Software and the parameter settings in the tx_dphy section. • Updated the code and description of the code in the int_gpll section.
Design and File Modifications	• Updated IP versions and added steps to modify the reference design in the Design and File Modifications section. • Updated the Top-Level RTL section. • Added the Post Synthesis Constraint File section.

Design Simulation	• Updated the script file path.
	• Changed Active HDL to QuestaSim.
	• Added the steps to run the simulation.
	• Updated the simulation scripts.
	• Updated the description on the example of FIFO overflow in rx_buffer.
	• Removed the following figures:
	  • *Script File Modification #1*
	  • *Script File Modification #2*
	• Updated the following figures:
	  • Figure 5.1. Functional Simulation Example
	  • Figure 5.2. FIFO Overflow

Known Limitations	Updated the limitations.

Design Package and Project Setup	• Updated the configuration example for RX channels.
	• Updated the following figures:
	  • Figure 7.1. Directory Structure
	  • Figure 7.2. Project Files

Resource Utilization	Updated the description and Table 8.1. Resource Utilization Examples.
References	Updated references.

Revision 1.1, December 2023

Section	Change Summary
Disclaimer	Updated this section.
Supported Device and IP	• Updated D-PHY Receiver IP version to 1.5.0. • Updated D-PHY Transmitter IP version to 1.8.1. • Updated Lattice Radiant Software version to 2022.1.
Introduction	Updated Figure 1.3. Clocking Scheme.
Design and Module Description	• Updated image of Figure 3.1. • Updated image of Figure 3.13.
Design Simulation	• Updated image of Figure 5.1. • Updated image of Figure 5.2.
References	Updated section contents.

Revision 1.0, February 2020

Section	Change Summary
All	Initial release.

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