

# Lattice Radiant Software 2.0 SP1 Release Notes

Welcome to Lattice Radiant® software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs).

## What's New in Radiant Software 2.0 SP1

### ► Device Support:

- CrossLink-NX™ Device Family offers new 17K devices and adds new 40K packages:
  - 17K (-7/-8/-9) HP/LP 1.0V (COM/IND) – Bitstream disabled
    - CABGA256
    - CSFBGA121
    - QFN72
    - WLCSP72
  - 40K (-7/-8/-9) HP/LP 1.0V (COM/IND)
    - CSFBGA121
    - CABGA256

### ► Tool and Other Enhancements:

- **IP Evaluation for CrossLink-NX 40K devices** – If you do not have licenses for the soft intellectual properties (IPs) downloaded from “IP on Server,” you can evaluate these soft IPs for approximately four hours before the device resets itself.
- **New Foundation IPs** - Four new foundation IPs are added:
  - 1D Filter
  - Adder Tree
  - Barrel Shifter
  - DSP\_Mult\_Mult\_Accumulate
- **Programmer** – Programmer has enhanced support for the Security features including Flash protection (128-bit device password) and AS-256 Encryption and Lock.
- **Security Tools (Key Generation)** – A new Radiant Bitstream Security Setting tool has been added that allows you to generate and verify keys that are used for bitstream obfuscation. The GUI provides user entry for Flash protection (128-bit device password) and AES-256 Encryption.
- **sysCONFIG** – A new attribute, CONFIGIO\_VOLTAGE\_BANK0/1, has been added for sysCONFIG.

- **Updated Radiant Tutorial for CrossLink-NX** – An updated [Tutorial](#) has been added using the [CrossLink-NX Evaluation Board](#).

## What's New in Radiant Software 2.0

### ▶ **Device Support:**

- CrossLink-NX Device Family for the following packages:
  - 40K (-7/-8/-9) HP/LP 1.0V (COM/IND) - CABGA400
  - 40K (-7/-8/-9) HP/LP 1.0V (COM/IND) - CSBGA289
  - 40K (-7/-8/-9) HP/LP 1.0V (COM/IND) - QFN72

The [Lattice Radiant 2.0 Software Guide for Lattice Diamond Users](#) has been enhanced to help users to migrate their designs to CrossLink-NX devices using the Radiant software. Users with designs on such Lattice devices as CrossLink and ECP5, designed using Lattice Diamond software, can use this guide to quickly grasp concepts of the new features of CrossLink-NX devices and designing with the Radiant software.

### ▶ **Tool and Other Enhancements:**

- **Device Constraint Editor** – Updates and enhancements have been added to Device Constraint Editor.
- **ECO Editor** – A new Radiant software tool has been added that supports interactive Engineering Change Order (ECO) editing.
- **Floorplan View** – Updates and enhancements have been added to Floorplan View. Updates include a new I/O placement feature that is used for I/O assignment such as DDR interface, DQS and clock assignments.
- **IP Catalog** – Updates and enhancements have been added to modules.
- **Power Calculator** – Updates and enhancements have been added to support CrossLink-NX devices.
- **Propagation of IP Constraints** – Radiant software now supports hierarchical constraints in IP applications and writes a new constraint file to propagate lower level constraints to top level under predefined constraint design rules.
- **Reveal Controller** – A new Radiant software tool has been added for the CrossLink-NX family to create virtual control switches/LEDs; reading/writing to bank of registers/memory; and read/write access to control and status registers of PLL, I2C/FIFO, DPHY, CDR and PCIe hard-IPs.
- **Run Manager** – A new Radiant software tool has been added that is used to run multiple synthesis and place and route passes, compare the results of multiple implementations for further analysis to get best solutions.
- **Source Template** – New CrossLink-NX templates have been added for both Verilog and VHDL in Source Template. In Source Template Editor, see:
  - Verilog > Primitive Templates > lifcl Primitive

- VHDL > Primitive Templates > l1fcl Primitive
- **Simultaneous Switching Outputs (SSO) Calculator** – A new Radiant software tool has been added that estimates Simultaneous Switching Noise (SSN) affecting a victim pin according to the switching characteristics of aggressor pins.
- **Timing Constraint Editor** – Updates and enhancements have been added to Timing Constraint Editor.

## Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Radiant software, start with the following procedures. These procedures adapt the project for the changes in Radiant software.

Find out which version of Diamond your project was created with. Then work through the changes for that and every later version, starting with the earliest and going to the most recent. For example, if your project was created with Radiant software 1.0, you would start with the changes for Radiant software 1.0. After completing those changes, you would work on the changes for Radiant software 2.0, and so on.

Once saved, the project will not be compatible with earlier Radiant software versions.

- ▶ **Migrating IPs** – When an older version IP is migrated to Radiant software 2.0 or 2.0 SP1, observe the following:
  - For PMIs, user must add the Family attribute in all PMI instantiations (Radiant software 2.0 and Radiant software 2.0 SP1).
  - Phase Locked Loop (PLL) IP has been enhanced in Radiant software 2.0 SP1. For designs created in previous versions of Radiant software, it is necessary to re-generate PLL IP in Radiant software 2.0 SP1. Otherwise, Radiant software 2.0 SP1 will issue an error when the previous generated PLL IP is detected in the design.
  - If Foundation IPs generated in Radiant software 1.0 need to be regenerated in Radiant software 2.0 or 2.0 SP1, user must first regenerate the IP in Radiant software 1.1, then Radiant software 2.0, or Radiant software 2.0 SP1.
- ▶ **Update to IO\_Type HDL attribute default value** – The IO\_TYPE HDL attribute default value has been changed in Radiant 2.0 SP1 from LVCMOS18 to LVCMOS33.

## Help Resources

Available information resources for the Radiant software include the following:

- ▶ Online Help updated with CrossLink-NX content.
  - ▶ To view the Online Help, start the Lattice Radiant software and select the  “Getting Started” icon under Information Center.
- ▶ Installation:
  - ▶ [Lattice Radiant Software 2.0 Installation Guide for Windows](#)

This document provides installation instructions for Windows OS.

- ▶ [Lattice Radiant Software 2.0 Installation Guide for Linux/Ubuntu](#)

This document provides installation instructions for Linux/Ubuntu OS.

## System Requirements

The following shows the basic system requirements for Radiant software:

- ▶ Intel Pentium or Pentium-compatible PC
- ▶ 64-bit OS:
  - ▶ Windows 7, Windows 8 and 8.1, or Windows 10
  - ▶ Red Hat Enterprise Linux 6.6 or 7.0
  - ▶ Ubuntu version 16.04 LTS
- ▶ Approximately 3 GB free disk space
- ▶ Computer Memory Requirement: 2 GB Minimum, 3 GB Recommended
- ▶ 1024 X 768 graphics display
- ▶ Network adapter for license and network connectivity
- ▶ A Web browser with JavaScript capability
- ▶ Microsoft Internet Explorer 8 or higher (required for Aldec Active-HDL Lattice Edition simulator)
- ▶ Acrobat Reader 5.0 or later

## Support for Third-Party Synthesis and Simulator Tools

In addition to the Synopsys Synplify Pro® for Lattice and Aldec Active-HDL™ Lattice Edition tools included with Radiant software suite, the following 3<sup>rd</sup>-party synthesis and simulator tools are supported by Radiant software:

- ▶ **Synthesis Tools:**
  - ▶ Synopsys Synplify Pro FPGA synthesis software version P-2019.03LR-SP1-1
- ▶ **Simulator Tools:**
  - ▶ Aldec Active-HDL v10.5 or later
  - ▶ Mentor Questa® Sim v10.4g or later  
v10.6b or later (supports IP encryption)

## Known Issues for Radiant Software 2.0 SP1

The following are known Issues for the Radiant software 2.0 SP1.

### **NVCM Boot time fluctuates when OSC frequency range strategy setting is set to 'Fast'.**

Workaround: Use 'Medium' setting.

Devices affected: iCE40UP

Bug number: DNG-6499

### **DPHY derating for CrossLink-NX does not work.**

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CrossLink-NX

Bug number: DNG-8247

### **MAP incorrectly reports number of DPHY and PCIE/ADC resources for CrossLink-NX QFN72 package.**

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CrossLink-NX

Bug number: DNG-8297

### **For QFN72 package, the SSO data of LVCMOS18 with SLOW SLEWRATE is not correct (too high).**

For assistance with this issue, please contact Lattice Technical Support.

Devices affected: CrossLink-NX

Bug number: DNG-8378

### **When using Aldec Active-HDL the RTL simulation of DLLDEL will output 'x' for VHDL DDR case when the clk < 100Mhz.**

Workaround: Initialize clk signal as 1'b1 in the testbench and toggle the other signal after a delay of 20 ns.

Devices affected: CrossLink-NX

Bug number: DNG-8401

### **After enabling IP Evaluation, an error message stating License Checkout Failed appears when generating bitstream.**

Workaround: Click OK on the error message. Bitstream generation should continue as normal.

Devices affected: All

Bug number: DNG-8932

### **If PLL IP is regenerated, a warning icon still appears.**

After PLL IP is regenerated to the latest version based on a warning icon, the warning icon still appears beside the regenerated IPX file in the File List window > Input Files.

Workaround: Ignore the warning icon after regeneration.

Devices affected: All

Bug number: DNG-8948

## **Radiant software 1.0 Foundation IP can pass Radiant software 2.0 SP1 flow but can't be regenerated with R2.0 SP1 IP Catalog.**

Workaround: Refer to "Migrating IPs" section of "[Updating Projects from an Earlier Version](#)".

Devices affected: iCE40UP

Bug number: DNG-8955

## **PCLKDIV doesn't work without DCS**

Work around: The DCS is required for PCLKDIV. The PCLKDIV output drives the CLK0 port of DCS and SEL port of DCS must be tied to GND.

Devices affected: CrossLink-NX

Bug number: DNG-8991

## **In Programmer, for CrossLink-NX ES devices, power-cycling is required if an error occurs when using SRAM "Fast Configuration" operation.**

Workaround: Cycle power if error occurs.

Devices affected: CrossLink-NX

Bug number: HWII-4279