sysI/O User Guide for Nexus Platform

Technical Note

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Contents

Contents 3
Acronyms in This Document 6
1. Introduction 7
2. sysI/O Overview 7
3. sysI/O Banking Scheme 8
3.1. CrossLink-NX, Certus-NX, and CertusPro-NX Devices 8
3.1.1. V_{CC} (1.0 V) 10
3.1.2. V_{CCIO} Wide Range (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V) 10
3.1.3. V_{CCIO} High Performance (1.0 V/1.2 V/1.35 V/1.5 V/1.8 V) 10
3.1.4. V_{CCAUX} (1.8 V) 10
3.2. MachXO5-NX Devices 10
3.2.1. V_{CC} (1.0 V) 13
3.2.2. V_{CCIO} Wide Range (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V) 13
3.2.3. V_{CCIO} High Performance (1.0 V/1.2 V/1.35 V/1.5 V/1.8 V) 13
3.2.4. V_{CCAUX} (1.8 V) 13
3.3. CrossLink-NX-33 Devices 13
3.3.1. V_{CC} (1.0 V) 14
3.3.2. V_{CCIO} [0, 1, 5] Wide Range (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V) 14
3.3.3. V_{CCIO} [2, 3, 4] High Performance (1.0 V/1.2 V/1.35 V/1.5 V/1.8 V) 14
3.3.4. V_{CCAUX} (1.8 V) 14
3.4. CrossLinkU-NX Devices 14
3.4.1. V_{CC} (1.0 V) 15
3.4.2. V_{CCIO} [0, 1] Wide Range (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V) 15
3.4.3. V_{CCIO} [2, 3, 4] High Performance (1.0 V/1.2 V/1.35 V/1.5 V/1.8 V) 15
3.4.4. V_{CCAUX} (1.8 V) 15
3.5. Standby 15
3.6. High Performance sysI/O Buffer Pairs on Bottom Side 16
3.7. Wide Range sysI/O Buffer Pair on Top, Left, or Right Sides 17
4. V_{CCIO} Requirement for I/O Standards 19
5. sysI/O Buffer Configurations 20
5.1. Programmable Drive Strength 20
5.2. Programmable Slew Rate 20
5.3. Tri-state Control 20
5.4. Open Drain Control 20
5.5. Differential Input Termination 21
5.6. Programmable Clamp 21
5.7. Soft MIPI D-PHY Support 21
6. Software sysI/O Attributes 23
6.1. IO_TYPE 23
6.2. PULLMODE 24
6.3. CLAMP 24
6.4. HYSTERESIS 24
6.5. VREF 24
6.6. OPENDRAIN 24
6.7. SLEWRATE 24
6.8. DIFFRESISTOR 25
6.9. TERMINATION 25
6.10. DRIVE STRENGTH 25
6.11. LOC 26
6.12. DIN/DOUT 26
Appendix A. sysI/O Attribute Examples 27
Appendix B. sysI/O Buffer Design Rules 29

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Appendix C. sysI/O Attributes using the Lattice Radiant Device Constraint Editor User Interface 30
References 31
Technical Support Assistance 32
Revision History 33

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Figures

Figure 3.1. CrossLink-NX, CertusPro-NX, and Certus-NX (LFD2NX-9, LFD2NX-17, LFD2NX-28, and LFD2NX-40) sysI/O Banking 8
Figure 3.2. Certus-NX LFD2NX-15 and LFD2NX-25 sysI/O Banking 9
Figure 3.3. Certus-NX LFD2NX-35 and LFD2NX-65 sysI/O Banking 9
Figure 3.4. LFMXO5-25 and LFMXO5-15D sysI/O Banking 11
Figure 3.5. LFMXO5-100T, LFMXO5-55T, LFMXO5-55TD, LFMXO5-55TDQ, and LFMXO5-65TDQ sysI/O Banking 12
Figure 3.6. LFMXO5-20TD, LFMXO5-20TDQ, LFMXO5-30TD, LFMXO5-30TDQ, LFMXO5-35/T, and LFMXO5-65/T sysI/O Banking 12
Figure 3.7. CrossLink-NX-33 sysI/O Banking 14
Figure 3.8. CrossLinkU-NX sysI/O Banking 15
Figure 3.9. High Performance sysI/O Buffer Pair for Bottom Side 17
Figure 3.10. Wide Range sysI/O Buffer for Top, Left, or Right Side 18
Figure 5.1. Off-Chip and On-Chip Solutions 21
Figure 5.2. MIPI Primitive Symbol 21
Figure C.6.1. Port Tab of Device Constraint Editor 30

Tables

Table 3.1. CrossLink-NX, Certus-NX, and CertusPro-NX Banks 10
Table 3.2. MachXO5-NX Banks 13
Table 4.1. Input Mixed Mode[4] for Wide Range Input Buffers 19
Table 4.2. Input Mixed Mode[3] for High Performance Input Buffers 19
Table 5.1. Programmable Drive Strength Values at Various V_{CCIO} Voltages for Wide Range Output Driver 20
Table 5.2. Programmable Drive Strength Values at Various V_{CCIO} Voltages for High Performance Output Driver 20
Table 5.3. MIPI Port List 22
Table 6.1. IO_TYPE Attribute Values 23
Table 6.2. Drive Strength Values 25

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
DDR	Double Data Rate
DRC	Design Rule Check
GPIO	General Purpose I/O
HDL	Hardware Description Language
HPIO	High Performance I/O
HS	High-Speed
HSTL	High Speed Transceiver Logic
HSUL	High Speed Unterminated Logic
I/O	Input/Output
LP	Low-Power
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVTTL	Low Voltage Transistor-Transistor Logic
MIPI	Mobile Industry Processor Interface
PIO	Programmable Input/Output
Rx	Receiver
SSTL	Stub Series Terminated Logic
SLVS	Scalable Low-Voltage Signaling
Tx	Transmitter
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
WRIO	Wide Range I/O

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1. Introduction

FPGA devices built on the Lattice Nexus™ platform feature sysI/O™ buffers that are designed to support a wide range of interfaces. Two types of I/O are offered, wide range I/O on the top, left, and right banks and high performance I/O on the bottom banks only. It gives you the ability to easily interface with other devices using advanced system I/O standards. For detailed information about supported sysI/O standards, refer to CrossLink™-NX Family Data Sheet (FPGA-DS-02049), Certus™-NX Family Data Sheet (FPGA-DS-02078), CertusPro™-NX Family Data Sheet (FPGA-DS-02086), MachXO5™-NX Family Data Sheet (FPGA-DS-02102), and CrossLink-NX™-33 and CrossLinkU™-NX Data Sheet (FPGA-DS-02104).

2. sysI/O Overview

The key features of the sysI/O block are:

- Wide Range I/O (WRIO) banks support single-ended standards only. High Performance I/O banks support differential standards as well as single-ended standards.
- WRIO banks are located on the Top, Left, and Right sides of the device.
- HPIO banks are located on the Bottom side of the device.
- Internal weak pull-down on all I/O
- Support for on-chip programmable 3.3 kΩ pull-up resistor in WRIO banks, for I2C, I3C, and other general-purpose applications.
- Support for on-chip dynamic differential input 100 Ω termination for I/O in bottom HPIO banks.
- Single-end termination with a programmable 40/50/60/75 Ω resistor is supported in all banks.
- Input Hysteresis on all LVCMOS33/LVTTL33, LVCMOS25, LVCMOS18, and LVCMOS15.
- Programmable Open Drain on all outputs
- Programmable Clamp in WRIO banks
- Hot socket-compliant GPIO is available in WRIO banks

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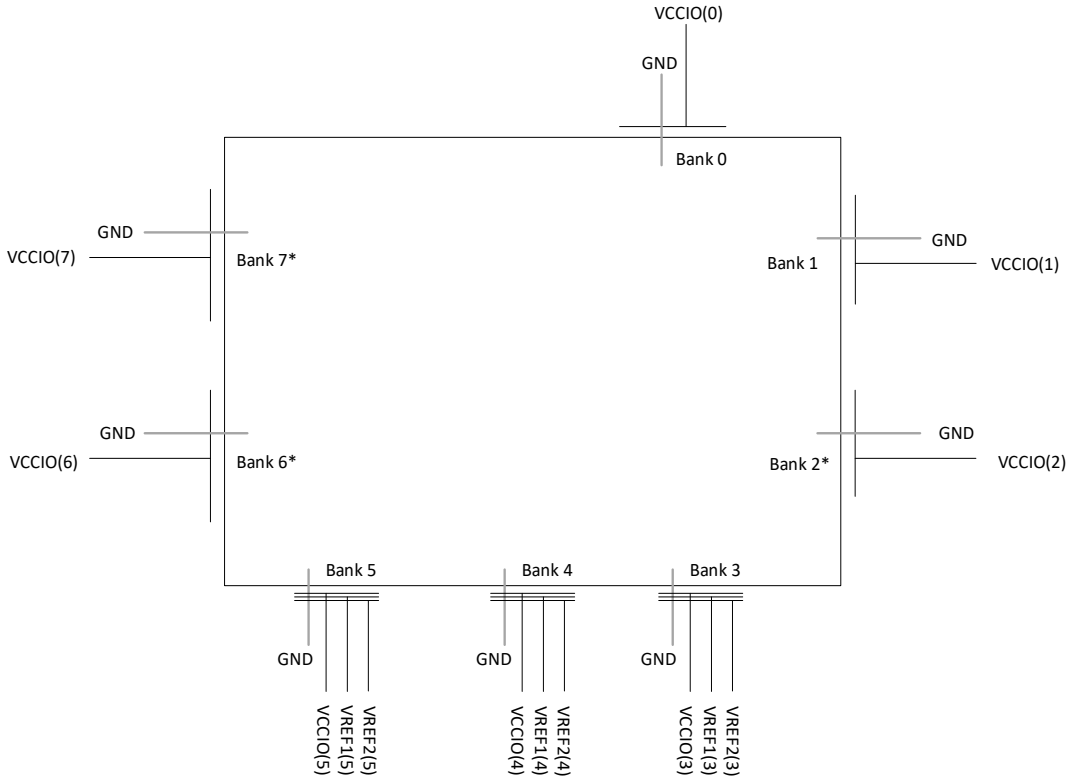
3. sysI/O Banking Scheme

3.1. CrossLink-NX, Certus-NX, and CertusPro-NX Devices

CrossLink-NX, Certus-NX, and CertusPro-NX devices have up to eight banks. For the Certus-NX LFD2NX-28, LFD2NX-40, CrossLink-NX LIFCL-40, CertusPro-NX LFCPNX-50, and LFCPNX-100 devices, there is one bank on top, two banks each on the left and right side of the device, and three on the bottom side of the device. For the Certus-NX LFD2NX-9, LFD2NX-17, and CrossLink-NX LIFCL-17 devices, there is one bank on top, one on the right side, and three on the bottom side of the device. The higher the density of the Nexus platform device, the more pins there are in each bank. I/O in Bank 0, Bank 1, Bank 2, Bank 6, and Bank 7 are wide range I/O support of up to V_{CCIO} 3.3 V. Meanwhile, I/O in Bank 3, Bank 4, and Bank 5 are high performance I/O support of up to V_{CCIO} 1.8 V. In addition, Bank 3, Bank 4, and Bank 5 support two VREF inputs for flexibility to receive two different referenced input levels on the same bank. Figure 3.1 shows the location of each bank.

For Certus-NX LFD2NX-15 and LFD2NX-25 devices, there are ten banks. Two banks are on the top, Bank 0 and Bank 1; three banks are on the left side, Bank 7, Bank 8, and Bank 9; three banks are on the right side, Bank 2, Bank 3, and Bank 4; and two banks are on the bottom, Bank 5 and Bank 6. The bottom HPIO banks, Bank 5 and Bank 6 have two VREF inputs for flexibility to receive two referenced input levels in the same bank. Figure 3.2 shows the location of each bank. Bank 0, Bank 1, Bank 2, Bank 3, Bank 4, Bank 7, Bank 8, and Bank 9 support V_{CCIO} 1.2 V up to V_{CCIO} 3.3 V, while Bank 5 and Bank 6 can support V_{CCIO} 1.0 V up to V_{CCIO} 1.8 V.

For Certus-NX LFD2NX-35 and LFD2NX-65 devices, there are eleven banks. Two banks are on the top, Bank 0 and Bank 1; three banks are on the left side, Bank 7, Bank 8, and Bank 9; three banks are on the right side, Bank 2, Bank 3, and Bank 4; and three banks are on the bottom, Bank 5, Bank 6, and Bank 11. Note that there is no Bank 10. The bottom HPIO banks, Bank 5 and Bank 6 have two VREF inputs for flexibility to receive two referenced input levels in the same bank. Figure 3.3 shows the location of each bank. Bank 0, Bank 1, Bank 2, Bank 3, Bank 4, Bank 7, Bank 8, Bank 9, and Bank 11 support V_{CCIO} 1.2 V up to V_{CCIO} 3.3 V, while Bank 5 and Bank 6 can support V_{CCIO} 1.0 V up to V_{CCIO} 1.8 V.



***Note:** Banks not available in Certus-NX LFD2NX-9, LFD2NX-17, and CrossLink-NX LIFCL-17 devices.

Figure 3.1. CrossLink-NX, CertusPro-NX, and Certus-NX (LFD2NX-9, LFD2NX-17, LFD2NX-28, and LFD2NX-40) sysI/O Banking

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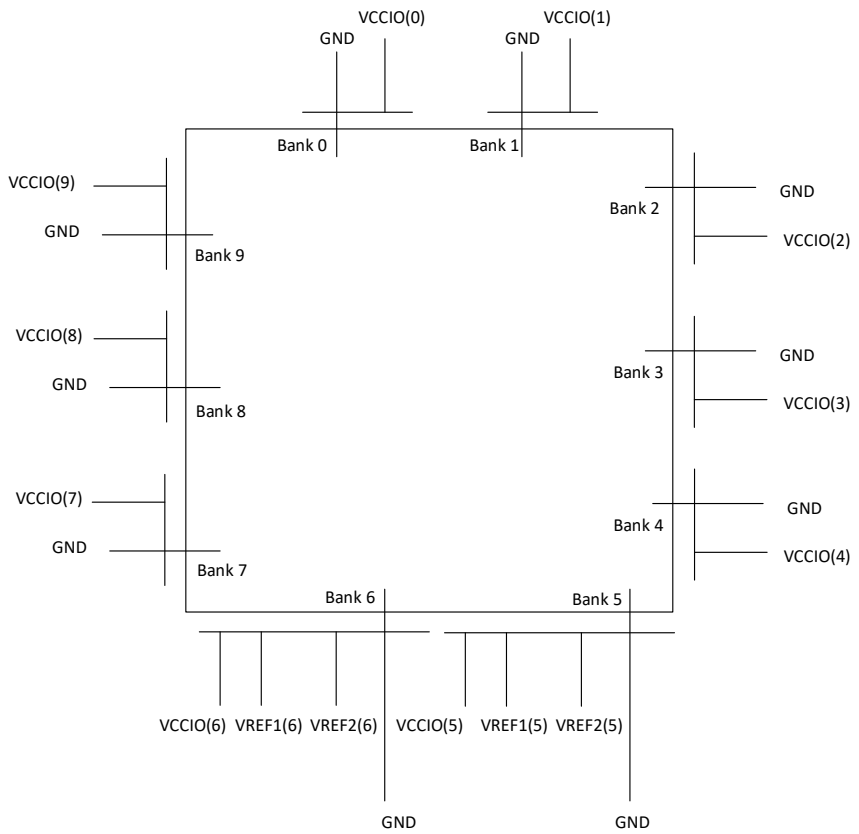

Figure 3.2. Certus-NX LFD2NX-15 and LFD2NX-25 sysI/O Banking

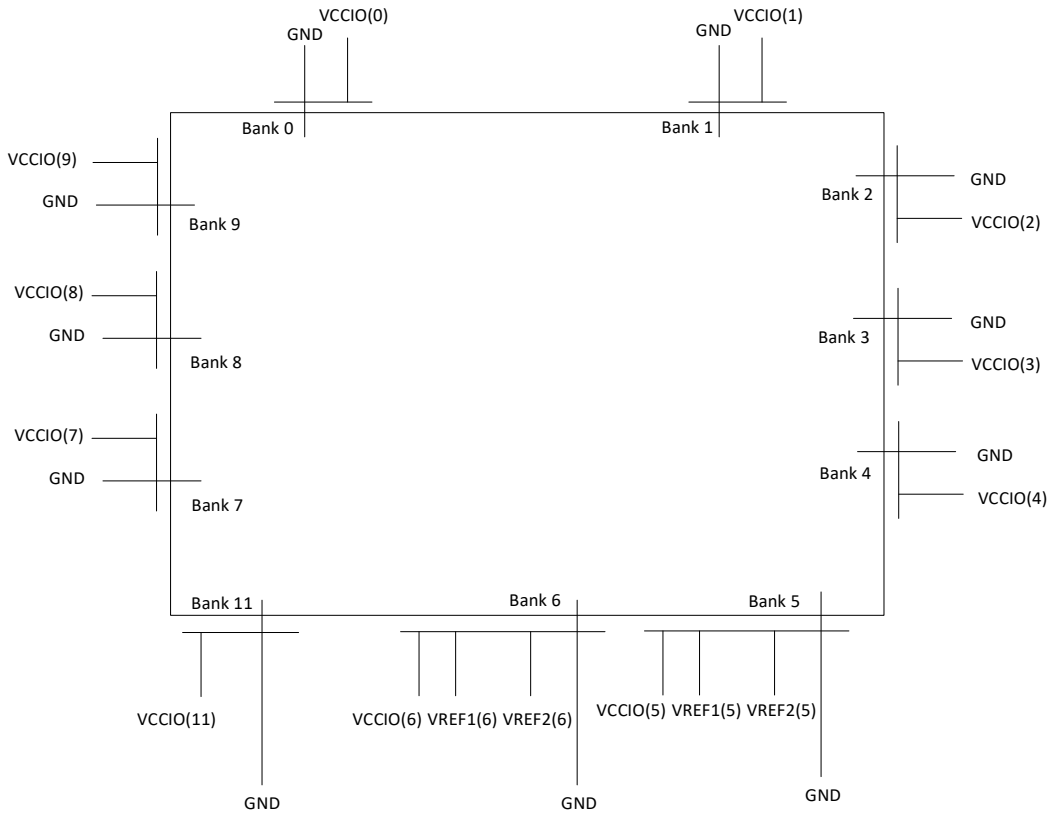

Figure 3.3. Certus-NX LFD2NX-35 and LFD2NX-65 sysI/O Banking

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3.1.1. V_{CC} (1.0 V)

This is the core supply. This V_{CC} supply is used to power the control logic. The control signals and data signals from the I/O logic are then translated to a higher supply of the I/O buffers.

3.1.2. V_{CCIO} Wide Range (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V)

V_{CCIO} is the individual supply voltage for each bank. Some banks are referred to as Wide Range I/O banks as they have a V_{CCIO} supply that operates from 3.3 V down to 1.2 V. These banks have single-ended signals and operate at a lower speed. Refer to the respective data sheet for the exact switching speed.

3.1.3. V_{CCIO} High Performance (1.0 V/1.2 V/1.35 V/1.5 V/1.8 V)

Some banks are referred to as High Performance I/O banks as they have a V_{CCIO} supply that operates from 1.8 V down to 1.2 V. These banks can operate as a differential pair and can operate at a higher speed. Refer to the respective data sheet for the exact switching speed.

Refer to Table 3.1 for WRIO and HPIO banks information in CrossLink-NX, Certus-NX, and CertusPro-NX devices.

Table 3.1. CrossLink-NX, Certus-NX, and CertusPro-NX Banks

Bank ID	I/O Reference		
	CrossLink-NX, CertusPro-NX, Certus-NX (LFD2NX-9, LFD2NX-17, LFD2NX-28, and LFD2NX-40)	Certus-NX LFD2NX-15 LFD2NX-25	Certus-NX LFD2NX-35 LFD2NX-65
Bank 0	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V
Bank 1	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V
Bank 2*	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V
Bank 3	HPIO–1.8 V/1.5 V/1.35 V/1.2 V/1.0 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V
Bank 4	HPIO–1.8 V/1.5 V/1.35 V/1.2 V/1.0 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V
Bank 5	HPIO–1.8 V/1.5 V/1.35 V/1.2 V/1.0 V	HPIO–1.8 V/1.5 V/1.35 V/1.2 V/1.0 V	HPIO–1.8 V/1.5 V/1.35 V/1.2 V/1.0 V
Bank 6*	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	HPIO–1.8 V/1.5 V/1.35 V/1.2 V/1.0 V	HPIO–1.8 V/1.5 V/1.35 V/1.2 V/1.0 V
Bank 7*	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V
Bank 8	—	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V
Bank 9	—	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V
Bank 10	Does not exist.		
Bank 11	—	—	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V

***Note**: Bank 2, Bank 6, and Bank 7 are not available in Certus-NX LFD2NX-9, LFD2NX-17, and CrossLink-NX LIFCL-17 devices.

3.1.4. V_{CCAUX} (1.8 V)

In addition to the bank V_{CCIO} supplies and a V_{CC} core logic supply, Nexus platform devices have a V_{CCAUX} auxiliary supply that powers the differential and referenced input buffers.

3.2. MachXO5-NX Devices

The LFMXO5-25 and LFMXO5-15D devices have ten GPIO banks. There are two banks on top, three banks each on the left and right side of the device, and two on the bottom side of the device.

Bank 1 can support only V_{CCIO} 3.3 V. Bank 0, Bank 2, Bank 3, Bank 4, Bank 7, Bank 8, and Bank 9 support up to V_{CCIO} 3.3 V. Bank 5 and Bank 6 support up to V_{CCIO} 1.8 V. In addition, Bank 5 and Bank 6 support two VREF inputs for flexibility to receive two different referenced input levels on the same bank. Figure 3.4 shows the location of each bank.

The LFMXO5-100T, LFMXO5-55T, LFMXO5-55TD, LFMXO5-55TDQ, and LFMXO5-65TDQ devices have eight GPIO banks. There is one bank on top, two banks each on the left and right side of the device, and three on the bottom side of the device.

Bank 0 can support only V_{CCIO} 3.3 V. Bank 1, Bank 2, Bank 6, and Bank 7 support up to V_{CCIO} 3.3 V. Bank 3, Bank 4, and Bank 5 support up to V_{CCIO} 1.8 V. In addition, Bank 3, Bank 4, and Bank 5 support two VREF inputs for flexibility to receive two different referenced input levels on the same bank. Figure 3.5 shows the location of each bank.

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For LFMXO5-20TD, LFMXO5-20TDQ, LFMXO5-30TD, LFMXO5-30TDQ, LFMXO5-35/T, and LFMXO5-65/T devices, there are eleven banks in total. Two banks are on the top, Bank 0 and Bank 1; three banks are on left side, Bank 7, Bank 8, and Bank 9; three banks are on the right side, Bank 2, Bank 3, and Bank 4; and three banks are on the bottom, Bank 5, Bank 6, and Bank 11. Note that there is no Bank 10. The bottom banks have two VREF inputs for flexibility to receive two referenced input levels in the same bank. Figure 3.6 shows the location of each bank. Bank 1 can only support V_{CCIO} 3.3 V, Bank 0, Bank 2, Bank 3, Bank 4, Bank 7, Bank 8, Bank 9, and Bank 11 support V_{CCIO} 1.2 V up to V_{CCIO} 3.3 V, while Bank 5 and Bank 6 can support V_{CCIO} 1.0 V up to V_{CCIO} 1.8 V.

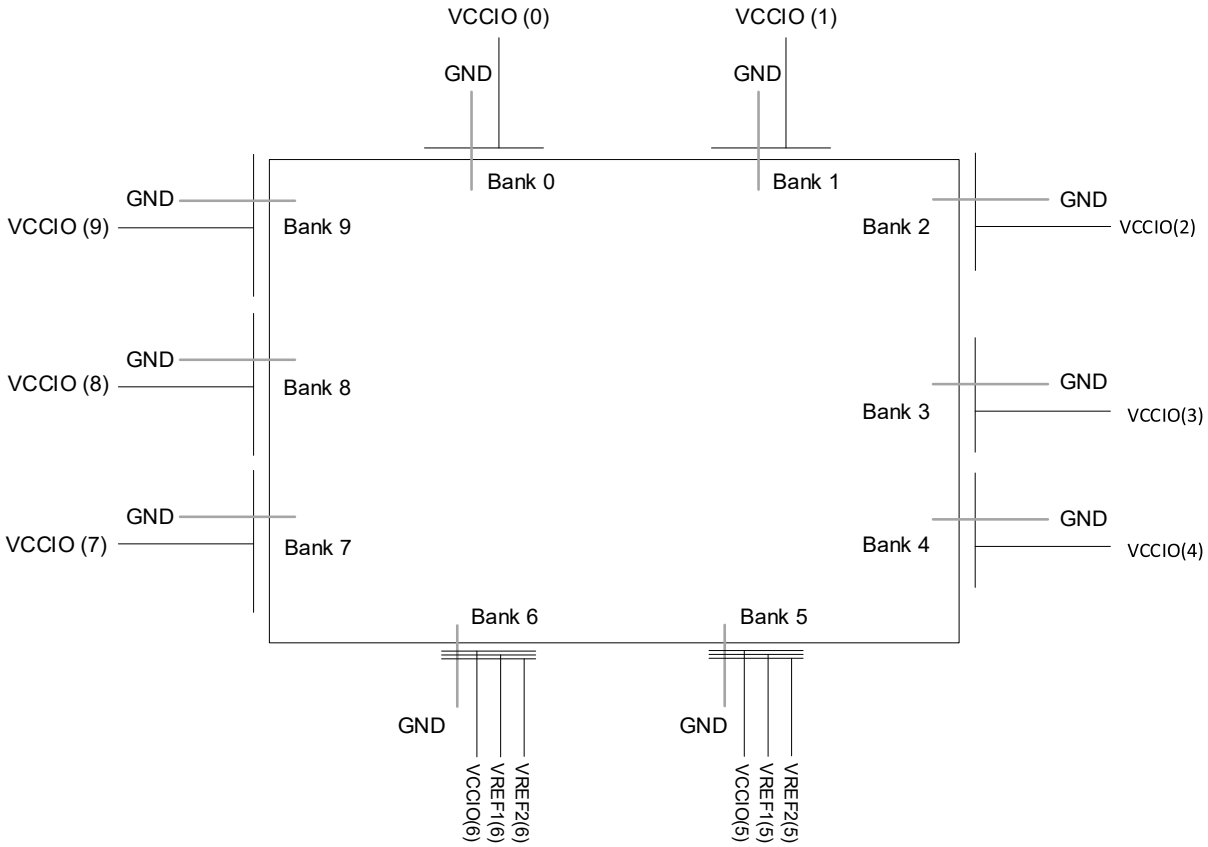

Figure 3.4. LFMXO5-25 and LFMXO5-15D sysI/O Banking

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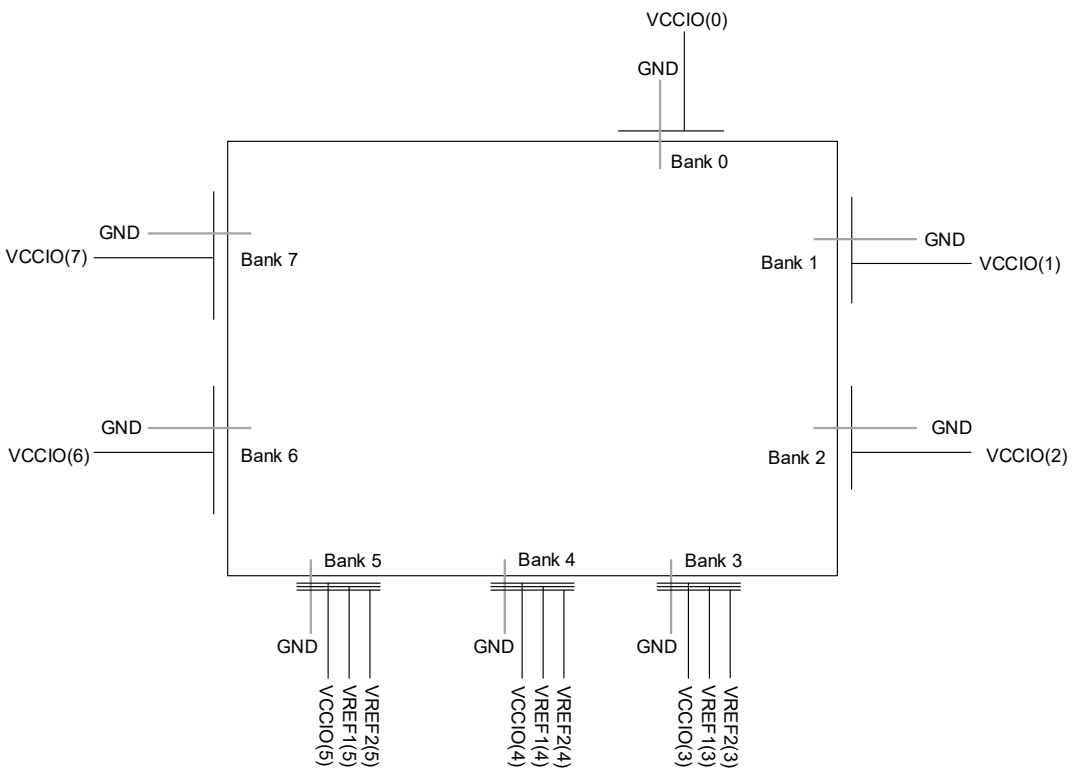

Figure 3.5. LFMXO5-100T, LFMXO5-55T, LFMXO5-55TD, LFMXO5-55TDQ, and LFMXO5-65TDQ sysI/O Banking

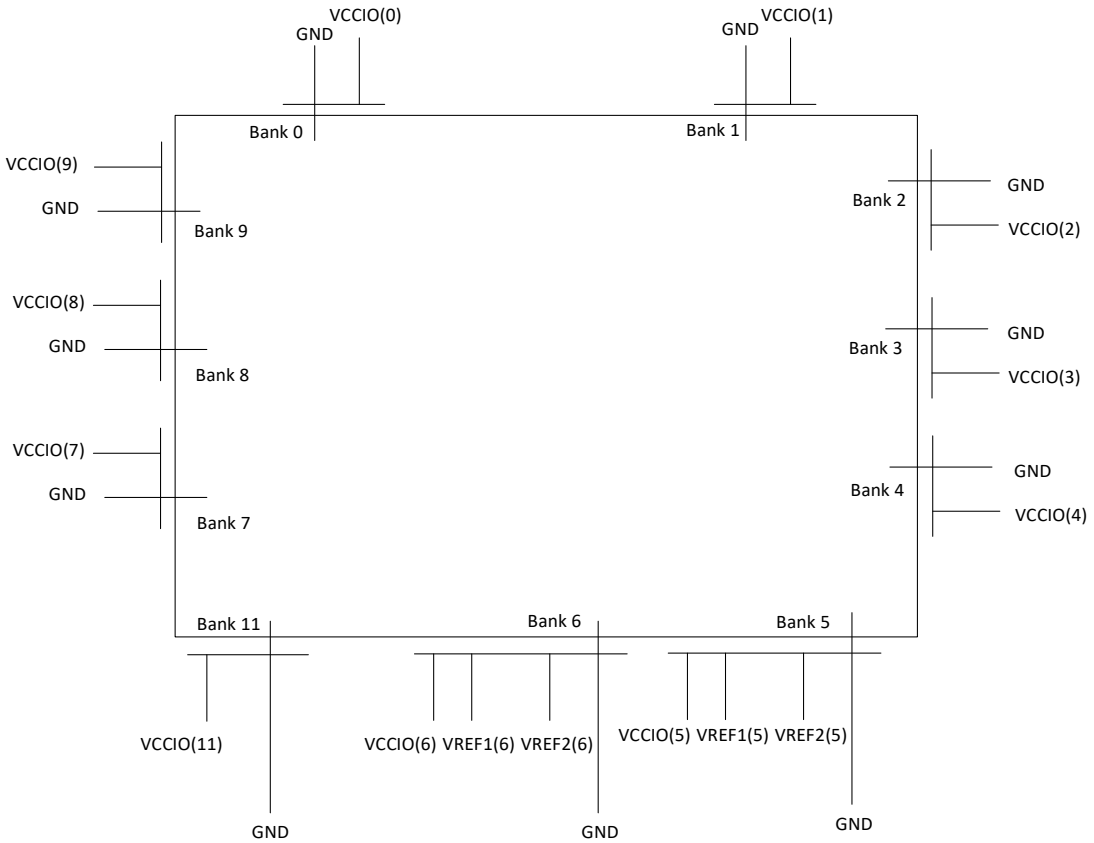

Figure 3.6. LFMXO5-20TD, LFMXO5-20TDQ, LFMXO5-30TD, LFMXO5-30TDQ, LFMXO5-35/T, and LFMXO5-65/T sysI/O Banking

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3.2.1. V_{CC} (1.0 V)

This is the core supply. This V_{CC} supply is used to power the control logic. The control signals and data signals from the I/O logic are then translated to a higher supply of the I/O buffers.

3.2.2. V_{CCIO} Wide Range (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V)

WRIO banks have a V_{CCIO} supply that operates from 3.3 V down to 1.2 V. These banks have single-ended signals and operate at a lower speed. Refer to the respective data sheet for the exact switching speed.

3.2.3. V_{CCIO} High Performance (1.0 V/1.2 V/1.35 V/1.5 V/1.8 V)

HPIO banks have a V_{CCIO} supply that operates from 1.8 V down to 1.2 V. These banks can operate as a differential pair and can operate at a higher speed. Refer to the respective data sheet for the exact switching speed.

Refer to Table 3.2 for WRIO banks and HPIO banks information in MachXO5-NX devices.

Table 3.2. MachXO5-NX Banks

Bank ID	I/O Reference		
	LFMXO5-55T, LFMXO5-100T, LFMXO5-55TD, LFMXO5-55TDQ, LFMXO5-65TDQ	LFMXO5-25,LFMXO5-15D	LFMXO5-20TD, LFMXO5-20TDQ, LFMXO5-30TD, LFMXO5-30TDQ, LFMXO5-35/T, LFMXO5-65/T
Bank 0	Similar to WRIO but fixed as 3.3 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V
Bank 1	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	Similar to WRIO but fixed as 3.3 V	Similar to WRIO but fixed as 3.3 V
Bank 2	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V
Bank 3	HPIO-1.8 V/1.5 V/1.35 V/1.2 V/1.0 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V
Bank 4	HPIO-1.8 V/1.5 V/1.35 V/1.2 V/1.0 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V
Bank 5	HPIO-1.8 V/1.5 V/1.35 V/1.2 V/1.0 V	HPIO-1.8 V/1.5 V/1.35 V/1.2 V/1.0 V	HPIO-1.8 V/1.5 V/1.35 V/1.2 V/1.0 V
Bank 6	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	HPIO-1.8 V/1.5 V/1.35 V/1.2 V/1.0 V	HPIO-1.8 V/1.5 V/1.35 V/1.2 V/1.0 V
Bank 7	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V
Bank 8	—	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V
Bank 9	—	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V
Bank 10	Does not exist.		
Bank 11	—	—	WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V

3.2.4. V_{CCAUX} (1.8 V)

In addition to the bank V_{CCIO} supplies and a V_{CC} core logic supply, Nexus platform devices have a V_{CCAUX} auxiliary supply that powers the differential and referenced input buffers.

3.3. CrossLink-NX-33 Devices

CrossLink-NX-33 devices have six banks in total, three banks on the top side of the device and three banks on the bottom side of the device. I/O in Bank 0, Bank 1, and Bank 5 are wide range I/O support of up to V_{CCIO} 3.3 V. Bank 2, Bank 3, and Bank 4, on the other hand, are high performance I/O support of up to V_{CCIO} 1.8 V. In addition, Bank 2, Bank 3, and Bank 4 support two VREF inputs for flexibility to receive two different referenced input levels on the same bank. Figure 3.7 shows the location of each bank.

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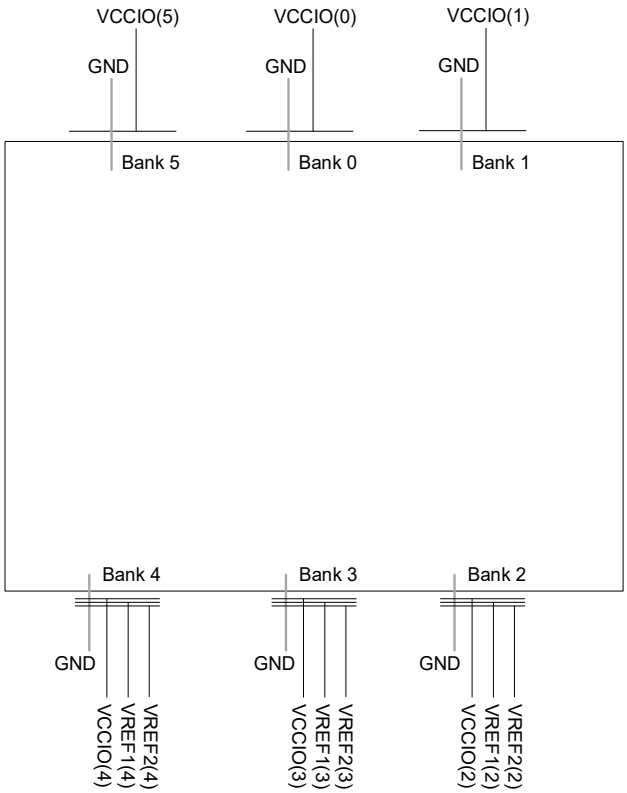

Figure 3.7. CrossLink-NX-33 sysI/O Banking

3.3.1. V_{CC} (1.0 V)

This is the core supply. This V_{CC} supply is used to power the control logic. The control signals and data signals from the I/O logic are then translated to a higher supply of the I/O buffers.

3.3.2. V_{CCIO} [0, 1, 5] Wide Range (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V)

Bank 0, Bank 1, and Bank 5 have a V_{CCIO} supply that operates from 3.3 V down to 1.2 V.

3.3.3. V_{CCIO} [2, 3, 4] High Performance (1.0 V/1.2 V/1.35 V/1.5 V/1.8 V)

Bank 2, Bank 3, and Bank 4 operate with V_{CCIO} of 1.8 V down to 1.0 V. Standards such as LVDS, SSTL, HSTL, and SLVS are only supported on these three banks.

3.3.4. V_{CCAUX} (1.8 V)

In addition to the bank V_{CCIO} supplies and a V_{CC} core logic supply, Nexus platform devices have a V_{CCAUX} auxiliary supply that powers the differential and referenced input buffers.

3.4. CrossLinkU-NX Devices

CrossLinkU-NX devices have five banks in total, two banks on the top side of the device and three banks on the bottom side of device. I/O in Bank 0 and Bank 1 are wide range I/O support of up to V_{CCIO} 3.3 V. Bank 2, Bank 3, and Bank 4, on the other hand, are high performance I/O support of up to V_{CCIO} 1.8 V. In addition, Bank 2, Bank 3, and Bank 4 support two VREF inputs for flexibility to receive two different referenced input levels on the same bank. Figure 3.8 shows the location of each bank.

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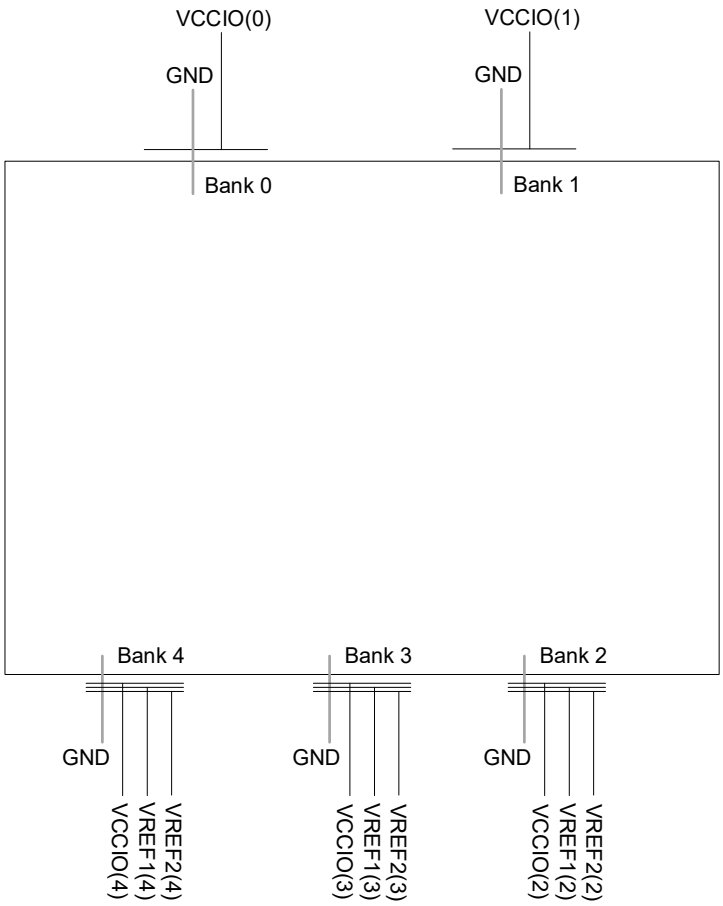

Figure 3.8. CrossLinkU-NX sysI/O Banking

3.4.1. V_{CC} (1.0 V)

This is the core supply. This V_{CC} supply is used to power the control logic. The control signals and data signals from the I/O logic are then translated to a higher supply of the I/O buffers.

3.4.2. V_{CCIO} [0, 1] Wide Range (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V)

Bank 0 and Bank 1 have a V_{CCIO} supply that operates from 3.3 V down to 1.2 V.

3.4.3. V_{CCIO} [2, 3, 4] High Performance (1.0 V/1.2 V/1.35 V/1.5 V/1.8 V)

Bank 2, Bank 3, and Bank 4 operate with V_{CCIO} of 1.8 V down to 1.0 V. Standards such as LVDS, SSTL, HSTL, and SLVS are only supported on these three banks.

3.4.4. V_{CCAUX} (1.8 V)

In addition to the bank V_{CCIO} supplies and a V_{CC} core logic supply, Nexus platform devices have a V_{CCAUX} auxiliary supply that powers the differential and referenced input buffers.

3.5. Standby

Using Standby mode dynamically powers down the bank. It disables the differential/reference receiver, true differential driver, current mirrors, and bias circuits.

In Standby mode, differential drivers and differential input buffers can be powered down to save power. Standby mode is enabled on a bank-by-bank basis. Each bank has user-routed input signals to enable Standby (dynamic power-down) mode.

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Refer to Power Management and Calculation for CrossLink-NX Devices (FPGA-TN-02075) or Power Management and Calculation for Certus-NX, CertusPro-NX, MachXO5-NX (FPGA-TN-02257) for detailed information.

3.6. High Performance sysI/O Buffer Pairs on Bottom Side

The I/O pair consists of two single-ended output drivers and two sets of single-ended input buffers, both ratioed and referenced. The A pad-referenced input buffer can also be configured as a differential input. Each I/O has a weak pull-up, pull-down, or buskeeper feature. These are disabled in the output mode. The two pads in the pair are referred to as True and Comp, where the True pad is associated with the positive side of the differential I/O and the Comp or complement pad is associated with the negative side.

Every pair also has a programmable 100 Ω differential input termination resistor. Every pair also has a true LVDS and SLVS200 Tx driver. They have an independent tri-state capability.

The single-ended driver associated with the complementary pad can be optionally driven by the complement of the data that drives the single-ended driver associated with the true pad. This allows a pair of single-ended drivers to be used to drive complementary outputs with the lowest possible skew between the signals. Pads A and B form a DIFF I/O pair. When this option is selected, the tri-state control for the driver associated with the complementary pad is driven by the same signal as the tri-state control for the driver associated with the true pad.

Refer to the High Performance I/O pair block diagram in Figure 3.9.

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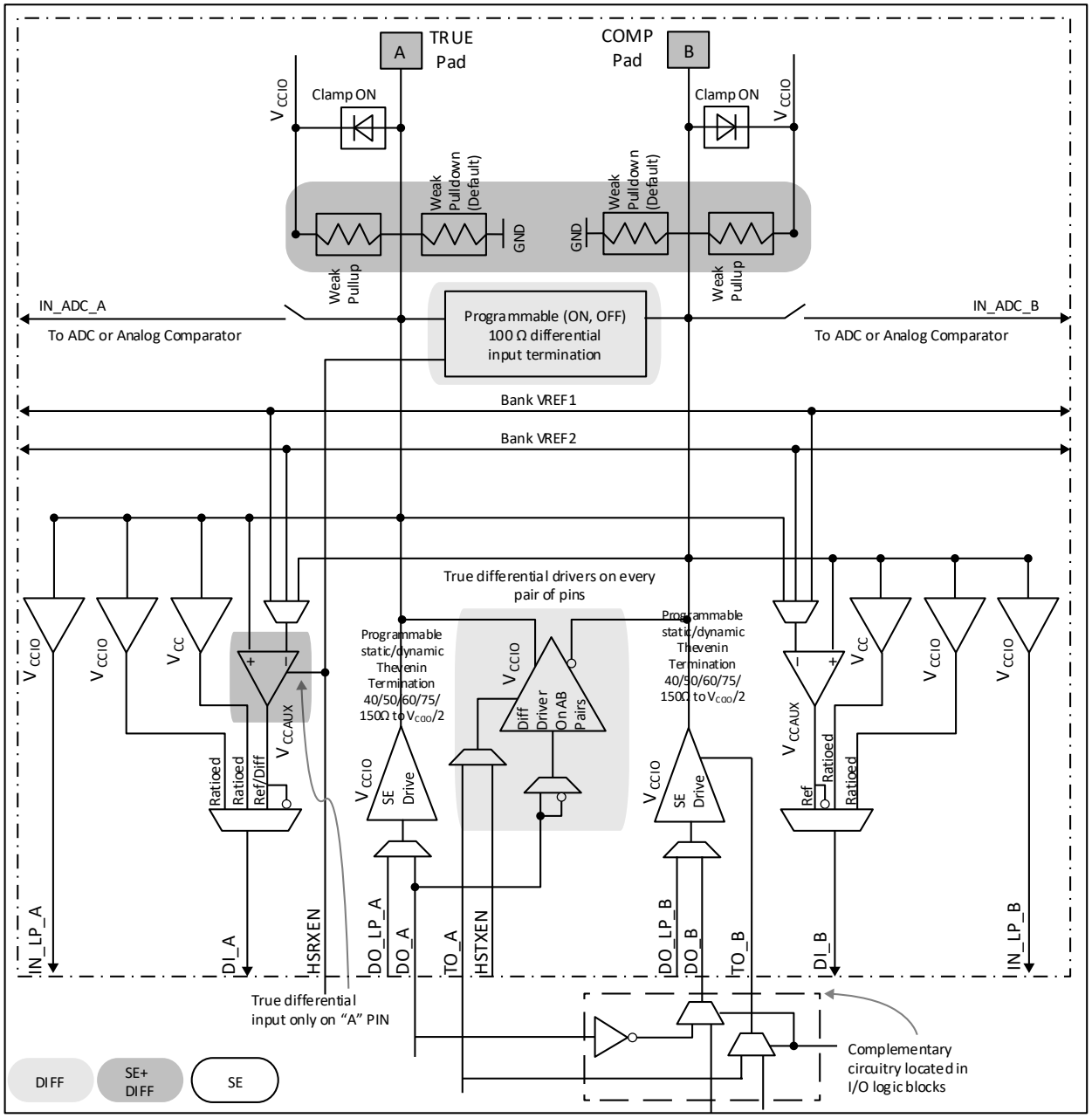

Figure 3.9. High Performance sysI/O Buffer Pair for Bottom Side

3.7. Wide Range sysI/O Buffer Pair on Top, Left, or Right Sides

The I/O pair consists of two single-ended output drivers and two sets of single-ended input buffers that are ratioed-only. Each I/O has a weak pull-up, pull-down, or buskeeper feature. These are disabled in output mode. The two pads in the pair are referred to as True and Comp, where the True pad is associated with the positive side of the Complementary I/O, and the Comp or complement pad is associated with the negative side.

The single-ended driver associated with the complementary pad can be optionally driven by the complement of the data that drives the single-ended driver associated with the True pad. This allows a pair of single-ended drivers to be used to drive complementary outputs with the lowest possible skew between the signals. Pads A and B form a Complementary I/O pair. When this option is selected, the tri-state control for the driver associated with the complement pad is driven by the same signal as the tri-state control for the driver associated with the true pad.

Figure 3.10 shows the Wide Range I/O pair block diagram.

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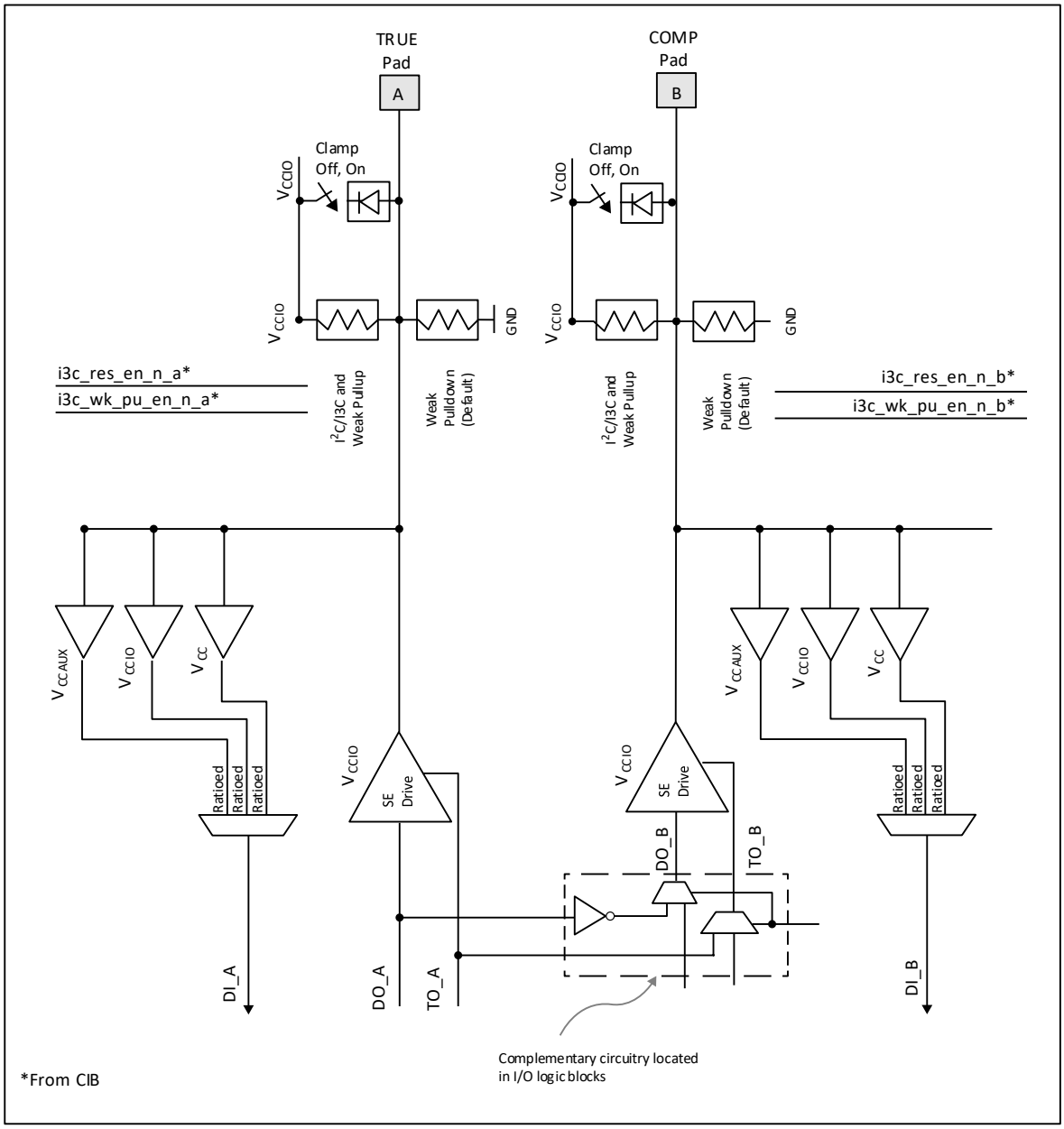

Figure 3.10. Wide Range sysI/O Buffer for Top, Left, or Right Side

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4. V_{CCIO} Requirement for I/O Standards

Each I/O bank of a device built on the Nexus platform has a separate V_{CCIO} supply pin that can be connected to 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V for bottom banks and 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V for the rest of the banks. These voltages are used to power the output I/O standard and source the drive strength for the output. On the input side, each pad is connected to a set of ratioed input buffers that provide support for the following:

- Fixed threshold 1.0 V/1.2 V input standards
- Ratioed V_{CCIO} input standards
- Ratioed V_{CCAUX} based 1.8 V/1.5 V LVCMOS inputs

These three buffers are connected to V_{CC}, V_{CCIO}, and V_{CCAUX} respectively.

Table 4.1. Input Mixed Mode[4] for Wide Range Input Buffers

V_{CCIO} (V)	Input Signaling (V)					
	LVCMOS10	LVCMOS12	LVCMOS15	LVCMOS18	LVCMOS25	LVCMOS33
	V_{CC} Powered Buffer		V_{CCAUX} Powered Buffer		V_{CCIO} Powered Buffer	
1.2	✓[2]	✓[2]	✓[1, 3]	—	—	—
1.5	✓[2]	✓[2]	✓[1, 3]	✓	—	—
1.8	✓[2]	✓[2]	✓[1, 3]	✓	—	—
2.5	✓[2]	✓[2]	✓[1, 3]	✓	✓	—
3.3	✓[2]	✓[2]	✓[1, 3]	✓	✓[3]	✓

Notes:

1. Increased ICC is due to underdrive.
2. No Hysteresis.
3. Reduced Hysteresis.
4. Set CLAMP setting on the I/Os to OFF to support mixed mode.

Table 4.2. Input Mixed Mode[3] for High Performance Input Buffers

V_{CCIO} (V)	Input Signaling (V)			
	LVCMOS1.0	LVCMOS1.2	LVCMOS1.5	LVCMOS1.8
	V_{CC} Powered Buffer		V_{CCIO} Powered Buffer	
1.0	✓	—	—	—
1.2	✓	✓	—	—
1.5	✓	✓	✓	—
1.8	✓	✓	✓[1, 2]	✓

Notes:

1. Increased ICC is due to underdrive.
2. Reduced Hysteresis.
3. Set CLAMP setting on the I/Os to OFF to support mixed mode.

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5. sysI/O Buffer Configurations

This section describes the various sysI/O features available on the Nexus platform device.

5.1. Programmable Drive Strength

All single-ended drivers have programmable drive strength. Table 5.1 and Table 5.2 show the programmable drive strength of all the I/O standards available in devices built on the Nexus platform. The maximum current allowed per bank as well as the package thermal limit current should be taken into consideration when selecting the drive strength.

Table 5.1. Programmable Drive Strength Values at Various V_{CCIO} Voltages for Wide Range Output Driver

I/O TYPE	Drive Strength (mA)
LVCMOS33	2, 4, 8, 12, 16
LVCMOS25	2, 4, 8, 10
LVCMOS18	2, 4, 8
LVCMOS15	2, 4
LVCMOS12	2, 4

Table 5.2. Programmable Drive Strength Values at Various V_{CCIO} Voltages for High Performance Output Driver

I/O TYPE	Drive Strength (mA)
LVCMOS18	2, 4, 8, 12
LVCMOS15	2, 4, 8
LVCMOS12	2, 4, 8
LVCMOS10	2, 4

5.2. Programmable Slew Rate

The single-ended output buffer for each I/O pin has programmable output slew rate control that can be configured for either low noise, SLEWRATE=SLOW; or high speed, SLEWRATE=FAST; or in between, SLEWRATE=MED.

5.3. Tri-state Control

On the output side, each single-ended driver has a separate tri-state control. The differential driver has a tri-state control as well.

5.4. Open Drain Control

In addition to the tri-state control, the single-ended drivers also support open drain operation on each I/O independently. Unlike non-open drain output which consists of a source and sink section, an open drain output is composed of only the sink section of the output driver. You can implement an open drain output by turning on the OPENDRAIN attribute in the software.

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5.5. Differential Input Termination

Nexus platform devices support a programmable 100 Ω input termination between all pairs on the bottom banks. The input termination of 100 Ω can be programmed between on and off. Figure 5.1 shows the discrete off-chip and on-chip solutions for dedicated, differential input termination.

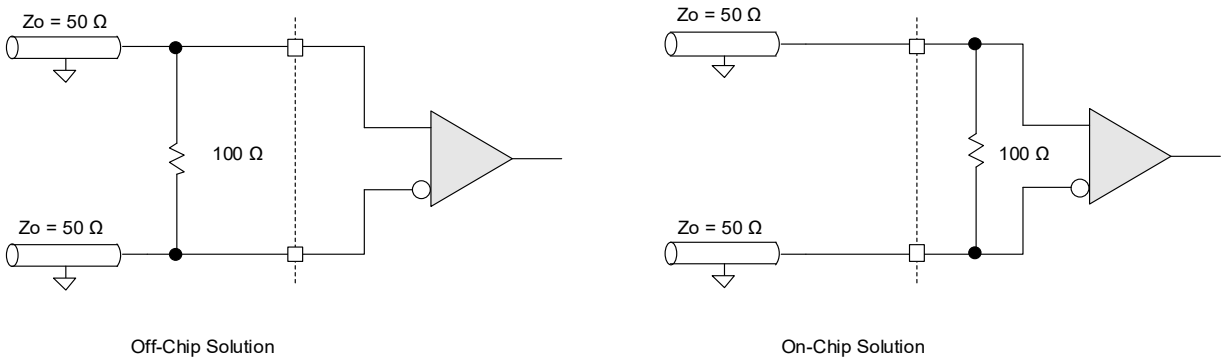

Figure 5.1. Off-Chip and On-Chip Solutions

5.6. Programmable Clamp

Programmable Clamp only applies to I/O on the Top, Left, and Right banks.

5.7. Soft MIPI D-PHY Support

The following primitive should be used when implementing soft MIPI D-PHY I/O in Nexus platform devices for High Speed (HS) as well as Low Power (LP) mode for Rx and Tx. For CrossLink-NX devices, the MIPI primitive is supported in Bank 3, Bank 4, and Bank 5 on the bottom side of the device. For other Nexus devices, refer to their respective data sheets.

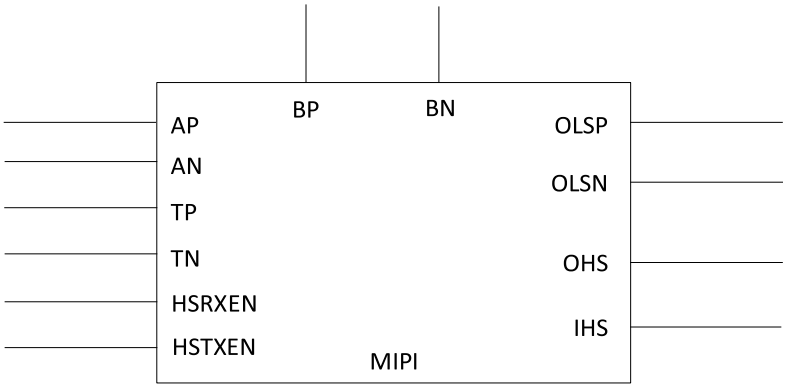

Figure 5.2. MIPI Primitive Symbol

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Table 5.3. MIPI Port List

Port	I/O	Description
BP	I/O	Bidirectional PAD A used for D-PHY Clock/Data in both HS and LP mode
BN	I/O	Bidirectional PAD B used for D-PHY Clock/Data in both HS and LP mode
AP	I	Input from fabric to PAD A – used for LP Tx function only
AN	I	Input from fabric to PAD B – used for LP Tx function only
HSRXEN	I	Enable to receive HS differential signals
HSTXEN	I	Enable to transmit HS differential signals
TP	I	Tri-state for PAD A
TN	I	Tri-state for PAD B
OLSP	O	LP Rx signal from BP
OLSN	O	LP Rx signal from BN
OHS	O	HS Rx signal from BP/BN differential
IHS	I	De-serialized input from DDR output register

When IO_TYPE is MIPI, the MIPI primitive above should be instantiated in the design; otherwise, the software Design Rule Check (DRC) returns an error. The output from the MIPI D-PHY buffer can only be used with the Double Data Rate (DDR) registers. Refer to Certus-NX High-Speed I/O Interface (FPGA-TN-02216), CrossLink-NX High-Speed I/O Interface (FPGA-TN-02097), CertusPro-NX High-Speed I/O Interface (FPGA-TN-02244), MachXO5-NX Family Data Sheet (FPGA-DS-02102), or CrossLink-NX-33 and CrossLinkU-NX Data Sheet (FPGA-DS-02104) for details on building MIPI D-PHY interfaces.

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6. Software sysI/O Attributes

The sysI/O attributes can be specified in the Hardware Description Language (HDL), using Device Constraint Editor, or in Pre/Post Timing Constraint Editor (.ldc/.pdc).

6.1. IO_TYPE

This attribute is used to set the sysI/O standard for an I/O. The V_{CCIO} required to set these I/O standards is embedded in the attribute names. Table 6.1 lists the available I/O types.

Table 6.1. IO_TYPE Attribute Values

sysI/O Signaling Standard	IO_TYPE
Default	LVCMOS18
LVDS 1.8V	LVDS
LVDS 1.8V Emulation	LVDSE
Sub-LVDS	SUBLVDS
Sub-LVDS Emulation	SUBLVDSE
Sub-LVDS Emulation High Speed	SUBLVDSEH
SLVS	SLVS
MIPI_DPHY	MIPI_DPHY
SSTL 1.5V Class I	SSTL15_I
SSTL 1.5V Class II	SSTL15_II
SSTL 1.5V Differential Class I	SSTL15D_I
SSTL 1.5V Differential Class II	SSTL15D_II
SSTL 1.35V Class I	SSTL135_I
SSTL 1.35V Class II	SSTL135_II
SSTL 1.35V Differential Class I	SSTL135D_I
SSTL 1.35V Differential Class II	SSTL135D_II
HSTL 1.5V Class I	HSTL15_I
HSTL 1.5V Differential Class I	HSTL15D_I
HSUL 1.2V	HSUL12
HSUL 1.2V Differential	HSUL12D
LVTTL 3.3V	LVTTL33
LVTTL 3.3V differential	LVTTL33D
LVCMOS 3.3V	LVCMOS33
LVCMOS 3.3V Differential	LVCMOS33D
LVCMOS 2.5V	LVCMOS25
LVCMOS 2.5V Differential	LVCMOS25D
LVCMOS 1.8V High Speed	LVCMOS18H
LVCMOS 1.5V	LVCMOS15
LVCMOS 1.5V High Speed	LVCMOS15H
LVCMOS 1.2V	LVCMOS12
LVCMOS 1.2V High Speed	LVCMOS12H
LVCMOS 1.0V	LVCMOS10
LVCMOS 1.0V High Speed	LVCMOS10H
LVCMOS 1.0V Referenced	LVCMOS10R

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6.2. PULLMODE

The PULLMODE attribute can be enabled for each I/O independently. This attribute is available for all the LVTTL and LVCMOS inputs and bidirectional I/O.

Values: UP, DOWN, NONE, I3C, KEEPER, FAILSAFE[1]

Default: DOWN for standards mentioned above. Others default to NONE.

Note:

1. FAILSAFE is only available for LVDS input. PULLMODE in FAILSAFE mode enables the pull-up for the P input and pull-down for the N input in LVDS.

6.3. CLAMP

The CLAMP option can be enabled for each I/O independently.

Values: ON, OFF

Default: For OUTPUT=OFF.

For INPUT=ON if V_{CCIO} is the same as the I/O standard.

For INPUT=OFF if V_{CCIO} is some other value than the I/O standard.

6.4. HYSTERESIS

The hysteresis option can be used to change the amount of hysteresis for the LVTTL and LVCMOS input and bidirectional I/O standards. LVCMOS12/12H and LVCMOS10/10H do not support hysteresis.

Values: ON, NA

Default: ON for LVTTL and LVCMOS15/18/33 for input and bidirectional standards. Others default to NA.

6.5. VREF

The VREF option is enabled for referenced LVCMOS10 as well as referenced input buffers such as HSTL, SSTL, and HSUL.

Values: OFF, VREF1_LOAD, VREF2_LOAD

Default: VREF1_LOAD for standards mentioned above. Others default to OFF.

6.6. OPENDRAIN

The OPENDRAIN option is available for all LVTTL and LVCMOS.

An I/O can be assigned independently to be an open drain when this attribute is turned on.

Values: OFF, ON

Default: OFF

6.7. SLEWRATE

Each I/O pin has an individual slew rate control. This allows you to specify slew rate control on a pin-by-pin basis. Slew rate control is not a valid attribute for inputs.

Values: SLOW, MED, FAST, NA

Default: SLOW

Hardware default: SLOW

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6.8. DIFFRESISTOR

This attribute is used to provide differential termination. It is available only for differential I/O types.

Values: OFF, 100

Default: 100

6.9. TERMINATION

The I/O supports single-ended input parallel termination to $V_{CCIO}/2$. All input parallel terminations use a Thevenin termination scheme.

Values: OFF, 40, 50, 60, 75

Default: OFF

6.10. DRIVE STRENGTH

The DRIVE STRENGTH attribute is available for the output and bidirectional I/O standards. The default drive value depends on the I/O standard used.

Table 6.2. Drive Strength Values

Output Standard	Drive	DiffDrive	V_{CCIO}
Single-Ended Interfaces			
LVTTL33	2 mA, 4 mA, **8 mA**, 12 mA, 16 mA, 50RS	—	3.3
LVCMOS33	2 mA, 4 mA, **8 mA**, 12 mA, 16 mA, 50RS	—	3.3
LVCMOS25	2 mA, 4 mA, **8 mA**, 12 mA, 50RS	—	2.5
LVCMOS18	2 mA, 4 mA, **8 mA**, 50RS	—	1.8
LVCMOS18H	2 mA, 4 mA, **8 mA**, 12 mA, 50RS	—	1.8
LVCMOS15	2 mA, **4 mA**	—	1.5
LVCMOS15H	2 mA, 4 mA, **8 mA**	—	1.5
LVCMOS12	2 mA, **4 mA**	—	1.2
LVCMOS12H	2 mA, 4 mA, **8 mA**	—	1.2
LVCMOS10H	2 mA, **4 mA**	—	1
LVTTL33 (Open Drain)	2 mA, 4 mA, **8 mA**, 12 mA	—	—
LVCMOS33 (Open Drain)	2 mA, 4 mA, **8 mA**, 12 mA	—	—
LVCMOS25 (Open Drain)	2 mA, 4 mA, **8 mA**, 10 mA	—	—
LVCMOS18 (Open Drain)	2 mA, 4 mA, **8 mA**	—	—
LVCMOS18H (Open Drain)	2 mA, 4 mA, **8 mA**, 12 mA	—	—
LVCMOS15 (Open Drain)	2 mA, **4 mA**	—	—
LVCMOS15H (Open Drain)	2 mA, 4 mA, **8 mA**	—	—
LVCMOS12 (Open Drain)	2 mA, **4 mA**	—	—
LVCMOS12H (Open Drain)	2 mA, 4 mA, **8 mA**	—	—
LVCMOS10H (Open Drain)	2 mA, **4 mA**	—	—
HSUL12	4 mA, 6 mA, **8 mA**	—	1.2
HSTL15_I	8 mA	—	1.5
SSTL15_I	8 mA	—	1.5
SSTL15_II	10 mA	—	1.5
SSTL135_I	8 mA	—	1.35
SSTL135_II	10 mA	—	1.35
Differential Interfaces			
LVDS	—	3.5 mA	1.8
SLVS	—	2.0 mA	—

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Output Standard	Drive	DiffDrive	V_{CCIO}
SUBLVDSE	8 mA	—	1.8
SUBLVDSEH	8 mA	—	1.8
LVDSE	8 mA	—	2.5
HSUL12D	4 mA, 6 mA, **8 mA**	—	1.2
HSTL15D_I	8 mA	—	1.5
SSTL15D_I	8 mA	—	1.5
SSTL15D_II	10 mA	—	1.5
SSTL135D_I	8 mA	—	1.35
SSTL135D_II	10 mA	—	1.35
LVTTL33D	**8 mA**, 2 mA, 4 mA, 12 mA, 50RS	—	3.3
LVCMOS33D	**8 mA**, 2 mA, 4 mA, 12 mA, 50RS	—	3.3
LVCMOS25D	**8 mA**, 2 mA, 4 mA, 12 mA, 50RS	—	2.5

Notes:

1. 50RS is an additional drive strength setting to mitigate reflection issues when driving an unterminated open transmission line trace of 50 Ω. It is only offered for 3.3 V, 2.5 V, and 1.8 V LVCMOS outputs.
2. For Output Standards that have multiple drive values, the default drive values are bolded.

6.11. LOC

This attribute can be used to make pin assignments to the I/O ports in the design. This attribute is used only when the pin assignments are made in HDL source code.

6.12. DIN/DOUT

This attribute can be used when an I/O register needs to be assigned. Using DIN asserts an input register and using DOUT asserts an output register in the design. By default, the software attempts to assign the I/O registers if applicable. You can turn this OFF by using a synthesis attribute. These attributes can only be applied to registers.

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Appendix A. sysI/O Attribute Examples

IO_TYPE

VHDL:

```
ATTRIBUTE IO_TYPE: string;
ATTRIBUTE IO_TYPE OF portA: SIGNAL IS "LVCMOS18";
ATTRIBUTE IO_TYPE OF portB: SIGNAL IS "LVCMOS33";
ATTRIBUTE IO_TYPE OF portC: SIGNAL IS "SSTL15_II";
ATTRIBUTE IO_TYPE OF portD: SIGNAL IS "LVCMOS25";
```

Verilog

```
output [4:0] portA /* synthesis IO_TYPE="LVCMOS33" DRIVE="16" PULLMODE="UP" SLEWRATE="FAST"*/;
```

OPENDRAIN

VHDL:

```
ATTRIBUTE OPENDRAIN: string;
ATTRIBUTE OPENDRAIN OF q_lvttl33_17: SIGNAL IS "ON";
```

Verilog:

```
output [4:0] portA /* synthesis attribute OPENDRAIN of q_lvttl33_17 is ON */;
```

DRIVE

VHDL:

```
ATTRIBUTE DRIVE: string;
ATTRIBUTE DRIVE OF portD: SIGNAL IS "8";
```

Verilog:

```
output [4:0] portA /* synthesis DRIVE = "8" */;
```

DIFFDRIVE

VHDL:

```
ATTRIBUTE DIFFDRIVE: string;
ATTRIBUTE DIFFDRIVE OF portF: SIGNAL IS "3.5";
```

Verilog:

```
output [4:0] portF/* synthesis IO_TYPE="LVDS" DIFFDRIVE="3.5" */;
```

TERMINATION

VHDL:

```
ATTRIBUTE TERMINATION: string;
ATTRIBUTE TERMINATION OF portF: SIGNAL IS "50";
```

Verilog:

```
output [4:0] portA /* synthesis IO_TYPE="SSTL18_I" TERMINATION = "50"*/;
```

DIFFRESISTOR

VHDL:

```
ATTRIBUTE DIFFRESISTOR: string;
ATTRIBUTE DIFFRESISTOR OF portF: SIGNAL IS "100";
```

Verilog:

```
output [4:0] portA /* synthesis IO_TYPE="LVDS"       DIFFRESISTOR = "100"*/;
```

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PULLMODE

VHDL:

```
ATTRIBUTE PULLMODE: string;
ATTRIBUTE PULLMODE OF portF: SIGNAL IS "PULLUP";
```

Verilog:

```
output [4:0] portA /* synthesis IO_TYPE="LVCMOS33"   PULLMODE = "PULLUP"*/;
```

SLEWRATE

VHDL:

```
ATTRIBUTE SLEWRATE: string;
ATTRIBUTE SLEWRATE OF portF: SIGNAL IS "FAST";
```

Verilog:

```
output [4:0] portA /* synthesis IO_TYPE="LVCMOS33"   SLEWRATE = "FAST"*/;
```

CLAMP

VHDL:

```
ATTRIBUTE CLAMP: string;
ATTRIBUTE CLAMP OF portF: SIGNAL IS "ON";
```

Verilog:

```
output [4:0] portA /* synthesis IO_TYPE="LVCMOS33" CLAMP = "ON"*/;
```

HYSTERESIS

VHDL:

```
ATTRIBUTE HYSTERESIS: string;
ATTRIBUTE HYSTERESIS OF portF: SIGNAL IS "ON";
```

Verilog:

```
output [4:0] portA /* synthesis IO_TYPE="LVCMOS25"   HYSTERESIS = "ON"*/;
```

LOC

VHDL:

```
ATTRIBUTE LOC : string;
ATTRIBUTE LOC OF output_vector : SIGNAL IS "H5";
```

Verilog:

```
Input rst  /* synthesis LOC="H5" */ ;
```

VREF

To set User Vref Locate:

1. After opening the design project, choose **Tools > Device Constraint Editor**.
2. Select the **Global** tab at the bottom of the view.
3. Double-click the cell beside **Vref Locate**. A dialog box opens.
4. For each available site, click on the desired row and enter a unique name in the **VREF Name** field.

Syntax

```
ldc_create_vref -name <vref_name> -site <site_value>
where:
<vref_name> = string
<site_value> = already pre-filled by Radiant.
```

For more details regarding I/O type, see the sysI/O User Guide for the target device family.

Example:

This constraint assigns a custom site name TEST_SITE to the selected site.

```
ldc_create_vref –name TESTING_SITE 8
```

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Appendix B. sysI/O Buffer Design Rules

- Only one V_{CCIO} level is allowed in a given bank. As such, all IO_TYPES of that bank should be compatible with the V_{CCIO} level.
- Banks at the top, left, and right sides of the device can only support single-ended I/O.
- Bottom banks support differential inputs and outputs as well as single-ended I/O.
- When an output is configured as an OPENDRAIN, the PULLMODE is set to NONE and the CLAMP setting is set to OFF.
- For bidirectional ports, pull-up and pull-down are allowed. The PULLMODE is set to NONE by default.
- When an output is configured as an OPENDRAIN, it can be placed independent of V_{CCIO}.
- When a ratioed input buffer is placed in a bank with a different V_{CCIO} (mixed mode), the Pull mode options of Up are no longer available.
- The IO_TYPE attribute for a differential buffer can only be assigned to the TRUE pad. The Lattice Radiant™ design tool automatically assigns the other I/O of the differential pair to the complementary pad.
- DIFFRESISTOR termination is available on all sysI/O pairs of bottom banks.
- If none of the pins are used for a given bank, the V_{CCIO} of the bank should be grounded except for the JTAG bank.

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Appendix C. sysI/O Attributes using the Lattice Radiant Device Constraint Editor User Interface

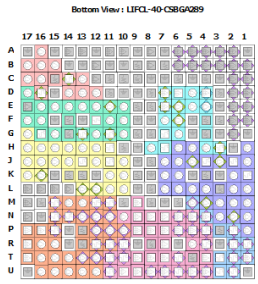
sysI/O buffer attributes can be assigned using the Device Constraint Editor in the Lattice Radiant software. The Port Assignments Sheet lists all the ports in a design and all the available sysI/O attributes in multiple columns. Click on each of these cells for a list of all the valid I/O preferences for that port. Each column takes precedence over the next. Therefore, when you choose a particular IO_TYPE, the columns for the PULLMODE, DRIVE, SLEWRATE, and other attributes list only the valid entries for that IO_TYPE.

Pin locations can be locked by using the Pin column of the Port Tab Sheet or by using the Pin Tab Sheet. You can right-click on a cell and go to Assign Pins to see a list of available pins.

In Device Constraint Editor, go to **Design** > **Constraint DRC** to look for incorrect pin assignments.

All the preferences assigned using the Device Constraint Editor are written into the post synthesis constraint file (.pdc).

Figure C.6.1 shows the Port Sheet of Device Constraint Editor. For further information on how to use Device Constraint Editor, refer to the Lattice Radiant Help documentation, available in the Help menu option of the software.



Name	Group By	Pin	BANK	IO_TYPE	CLAMP	DIFFDRIVE	DIFFRESISTOR	DRIVE	GLITCHFILTER	HYSTERESIS	OPENDRAIN	PULLMODE	SLEWRATE	TERMINATION	VREF
All Port	N/A	N/A	N/A		N/A										
Input	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Clock	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
axis_tvalid_i	N/A	(M4)	(6)	LVCMOS33(LVCMOS33)	ON(ON)	NA(NA)	OFF(OFF)	NA(...	ON(ON)	ON(ON)	OFF(OFF)	DOWN(DOWN)	NA(NA)	OFF(OFF)	
clk_hs_en_i	N/A	(F6)	(7)	LVCMOS33(LVCMOS33)	ON(ON)	NA(NA)	OFF(OFF)	NA(...	ON(ON)	ON(ON)	OFF(OFF)	DOWN(DOWN)	NA(NA)	OFF(OFF)	
d_hs_en_i	N/A	(H3)	(7)	LVCMOS33(LVCMOS33)	ON(ON)	NA(NA)	OFF(OFF)	NA(...	ON(ON)	ON(ON)	OFF(OFF)	DOWN(DOWN)	NA(NA)	OFF(OFF)	
hs_rx_en_i	N/A	(L13)	(2)	LVCMOS33(LVCMOS33)	ON(ON)	NA(NA)	OFF(OFF)	NA(...	ON(ON)	ON(ON)	OFF(OFF)	DOWN(DOWN)	NA(NA)	OFF(OFF)	
lp_en_i	N/A	(J3)	(6)	LVCMOS33(LVCMOS33)	ON(ON)	NA(NA)	OFF(OFF)	NA(...	ON(ON)	ON(ON)	OFF(OFF)	DOWN(DOWN)	NA(NA)	OFF(OFF)	
lp_rx_en_i	N/A	(L12)	(2)	LVCMOS33(LVCMOS33)	ON(ON)	NA(NA)	OFF(OFF)	NA(...	ON(ON)	ON(ON)	OFF(OFF)	DOWN(DOWN)	NA(NA)	OFF(OFF)	
pd_dphy_i[0]	N/A	(E6)	(7)	LVCMOS33(LVCMOS33)	ON(ON)	NA(NA)	OFF(OFF)	NA(...	ON(ON)	ON(ON)	OFF(OFF)	DOWN(DOWN)	NA(NA)	OFF(OFF)	
pll_clkop_i[0]	N/A	(E11)	(1)	LVCMOS33(LVCMOS33)	ON(ON)	NA(NA)	OFF(OFF)	NA(...	ON(ON)	ON(ON)	OFF(OFF)	DOWN(DOWN)	NA(NA)	OFF(OFF)	
pll_clkop_i[1]	N/A	(D7)	(7)	LVCMOS33(LVCMOS33)	ON(ON)	NA(NA)	OFF(OFF)	NA(...	ON(ON)	ON(ON)	OFF(OFF)	DOWN(DOWN)	NA(NA)	OFF(OFF)	
pll_lock_i[0]	N/A	(E7)	(7)	LVCMOS33(LVCMOS33)	ON(ON)	NA(NA)	OFF(OFF)	NA(...	ON(ON)	ON(ON)	OFF(OFF)	DOWN(DOWN)	NA(NA)	OFF(OFF)	
pll_lock_i[1]	N/A	(K16)	(2)	LVCMOS33(LVCMOS33)	ON(ON)	NA(NA)	OFF(OFF)	NA(...	ON(ON)	ON(ON)	OFF(OFF)	DOWN(DOWN)	NA(NA)	OFF(OFF)	
reset_n_i	N/A	(G13)	(1)	LVCMOS33(LVCMOS33)	ON(ON)	NA(NA)	OFF(OFF)	NA(...	ON(ON)	ON(ON)	OFF(OFF)	DOWN(DOWN)	NA(NA)	OFF(OFF)	
sp_en_i	N/A	(J5)	(6)	LVCMOS33(LVCMOS33)	ON(ON)	NA(NA)	OFF(OFF)	NA(...	ON(ON)	ON(ON)	OFF(OFF)	DOWN(DOWN)	NA(NA)	OFF(OFF)	
sync_rst_i	N/A	(N2)	(6)	LVCMOS33(LVCMOS33)	ON(ON)	NA(NA)	OFF(OFF)	NA(...	ON(ON)	ON(ON)	OFF(OFF)	DOWN(DOWN)	NA(NA)	OFF(OFF)	
Output	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Bidi	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Figure C.6.1. Port Tab of Device Constraint Editor

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References

For more information, refer to:

- CrossLink-NX Family Data Sheet (FPGA-DS-02049)
- CrossLink-NX-33 and CrossLinkU-NX Data Sheet (FPGA-DS-02104)
- CertusPro-NX Family Data Sheet (FPGA-DS-02086)
- Certus-NX Family Data Sheet (FPGA-DS-02078)
- MachXO5-NX Family Data Sheet (FPGA-DS-02102)
- Lattice Nexus Platform web page

For more information on Nexus-related IP, reference designs, and board documents, refer to the following web pages:

- IP and Reference Designs for CrossLink-NX
- Development Kits and Boards for CrossLink-NX
- IP and Reference Designs for CertusPro-NX
- Development Kits and Boards for CertusPro-NX
- IP and Reference Designs for Certus-NX
- Development Kits and Boards for Certus-NX
- IP and Reference Designs for MachXO5-NX
- Development Kits and Boards for MachXO5-NX

A variety of technical notes for Lattice Nexus devices are available:

- CrossLink-NX High-Speed I/O Interface (FPGA-TN-02097)
- CrossLink-NX-33 and CrossLinkU-NX High-Speed I/O Interface (FPGA-TN-02280)
- CertusPro-NX High-Speed I/O Interface (FPGA-TN-02244)
- Certus-NX High-Speed I/O Interface (FPGA-TN-02216)
- MachXO5-NX High-Speed I/O Interface (FPGA-TN-02286)
- Power Management and Calculation for CrossLink-NX Devices (FPGA-TN-02075)
- Power Management and Calculation for Certus-NX, CertusPro-NX, and MachXO5-NX (FPGA-TN-02257)

Other references:

- Lattice Insights for Lattice Semiconductor training courses and learning plans
- Lattice Radiant FPGA design software

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Revision History

Revision 3.0, August 2026

Section	Change Summary

sysI/O Banking Scheme	• In the MachXO5-NX Devices section, updated the following to reflect LFMXO5-65TDQ device related information:
	  • changed *The LFMXO5-100T, LFMXO5-55T, LFMXO5-55TD, and LFMXO5-TDQ devices have eight GPIO banks* to *The LFMXO5-100T, LFMXO5-55T, LFMXO5-55TD, LFMXO5-55TDQ, and LFMXO5-65TDQ devices have eight GPIO banks*;
	  • updated the captions of Figure 3.5. LFMXO5-100T, LFMXO5-55T, LFMXO5-55TD, LFMXO5-55TDQ, and LFMXO5-65TDQ sysI/O Banking;
	  • updated Table 3.2. MachXO5-NX Banks to include *LFMXO5-65TDQ* device.

Revision 2.9, June 2026

Section	Change Summary
Software sysI/O Attributes	In Table 6.1. IO_TYPE Attribute Values, removed the row for *LVCMOS 1.8V Differential*.

Revision 2.8, October 2025

Section	Change Summary

sysI/O Banking Scheme	• In the MachXO5-NX Devices section, update the following to reflect LFMXO5-20TD, LFMXO5-20TDQ, LFMXO5-30TD, LFMXO5-30TDQ, and LFMXO5-55TDQ devices related information:
	  • changed *The LFMXO5-100T, LFMXO5-55T, and LFMXO5-55TD devices have eight GPIO banks* to *The LFMXO5-100T, LFMXO5-55T, LFMXO5-55TD, and LFMXO5-55TDQ devices have eight GPIO banks*;
	  • changed *For LFMXO5-35/T and LFMXO5-65/T devices, there are eleven banks in total* to *For LFMXO5-20TD, LFMXO5-20TDQ, LFMXO5-30TD, LFMXO5-30TDQ, LFMXO5-35/T, and LFMXO5-65/T devices, there are eleven banks in total*;
	  • updated the captions of Figure 3.5. LFMXO5-100T, LFMXO5-55T, LFMXO5-55TD, and LFMXO5-55TDQ sysI/O Banking and Figure 3.6. LFMXO5-20TD, LFMXO5-20TDQ, LFMXO5-30TD, LFMXO5-30TDQ, LFMXO5-35/T, and LFMXO5-65/T sysI/O Banking;
	  • updated Table 3.2. MachXO5-NX Banks to include *LFMXO5-55TDQ*, *LFMXO5-20TD*, *LFMXO5-20TDQ*, *LFMXO5-30TD*, and *LFMXO5-30TDQ* devices.

Revision 2.7, August 2025

Section	Change Summary
sysI/O Banking Scheme	Made the following edits to align sysI/O related information in this sysI/O User Guide for Nexus Platform with Certus-NX Family Data Sheet (FPGA-DS-02078 Revision 2.4) and MachXO5-NX Family Data Sheet (FPGA-DS-02102 Revision 2.1): • removed *The top, left, and right banks use the voltage level from the respective* V_{CCIO} from the CrossLink-NX, Certus-NX, and CertusPro-NX Devices and MachXO5-NX Devices sections globally; • added *Bank 0, Bank1, Bank 2, Bank 3, Bank 4, Bank 7, Bank 8, and Bank 9 support* V_{CCIO} *1.2 V up to* V_{CCIO} *3.3 V, while Bank 5 and Bank 6 can support* V_{CCIO} *1.0 V up to* V_{CCIO} *1.8 V* for the description of Certus-NX LFD2NX-15 and LFD2NX-25 devices in CrossLink-NX, Certus-NX, and CertusPro-NX Devices; • added *Bank 0, Bank1, Bank 2, Bank 3, Bank 4, Bank 7, Bank 8, Bank 9, and Bank 11 support* V_{CCIO} *1.2 V up to* V_{CCIO} *3.3 V, while Bank 5 and Bank 6 can support* V_{CCIO} *1.0 V up to* V_{CCIO} *1.8 V* for the description of Certus-NX LFD2NX-35 and LFD2NX-65 devices in CrossLink-NX, Certus-NX, and CertusPro-NX Devices; • added *Bank 1 can only support* V_{CCIO} *3.3 V, Bank 0, Bank 2, Bank 3, Bank 4, Bank 7, Bank 8, Bank 9, and Bank 11 support* V_{CCIO} *1.2 V up to* V_{CCIO} *3.3 V, while Bank 5 and Bank 6 can support* V_{CCIO} *1.0 V up to* V_{CCIO} *1.8 V* for MachXO5-NX LFMXO5-35/T and LFMXO5-65/T devices in MachXO5-NX Devices;

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	• in Table 3.1. CrossLink-NX, Certus-NX, and CertusPro-NX Banks, changed *HPIO–1.8 V/1.5 V/1.35 V/1.2 V/1.0 V* to *WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V* for Bank 11 of Certus-NX LFD2NX-35 and LFD2NX-65 devices; • in Table 3.2. MachXO5-NX Banks, changed *HPIO–1.8 V/1.5 V/1.35 V/1.2 V/1.0 V* to *WRIO–3.3 V/2.5 V/1.8 V/1.5 V/1.2 V* for Bank 11 of MachXO5-NX LFMXO5-35/T and LFMXO5-65/T devices.

Revision 2.6, July 2025

Section	Change Summary
Acronyms in This Document	Updated this section.

sysI/O Banking Scheme	• In the CrossLink-NX, Certus-NX, and CertusPro-NX Devices section:
	  • changed *28k, 40k, 50k, and 100k devices* to *Certus-NX LFD2NX-28, LFD2NX-40, CrossLink-NX LIFCL-40, CertusPro-NX LFCPNX-50, and LFCPNX-100 devices*;
	  • changed *9k and 17k device* to *Certus-NX LFD2NX-9, LFD2NX-17, and CrossLink-NX LIFCL-17 devices;*
	  • added the following description for LFD2NX-15 and LFD2NX-25 sysI/O banking, *For Certus-NX LFD2NX-15 and LFD2NX-25 devices, there are ten banks in total. Two banks are on the top, bank 0 and bank 1; three banks are on left side, bank 7, bank 8, and bank 9; three banks are on the right side, bank 2, bank 3, and bank 4; and two banks are on the bottom, bank 5 and bank 6. The top, left, and right side banks use the voltage level from the respective VCCIO. The bottom HPIO banks bank 5 and bank 6 have two VREF inputs for flexibility to receive two referenced input levels in the same bank. Figure 3.2 shows the location of each bank*;
	  • added the following description for LFD2NX-35 and LFD2NX-65 sysI/O banking, *For Certus-NX LFD2NX-35 and LFD2NX-65 devices, there are eleven banks in total. Two banks are on the top, bank 0 and bank 1; three banks are on left side, bank 7, bank 8, and bank 9; three banks are on the right side, bank 2, bank 3, and bank 4; and three banks are on the bottom, bank 5, bank 6, and bank 11. Note that there is no bank 10. The top, left, and right banks use the voltage level from the respective VCCIO. The bottom HPIO banks bank 5 and bank 6 have two VREF inputs for flexibility to receive two referenced input levels in the same bank. Figure 3.3 shows the location of each bank*;
	  • updated the figure caption of Figure 3.1. CrossLink-NX, CertusPro-NX, and Certus-NX (LFD2NX-9, LFD2NX-17, LFD2NX-28, and LFD2NX-40) sysI/O Banking to its current;
	  • added Figure 3.2. Certus-NX LFD2NX-15 and LFD2NX-25 sysI/O Banking and Figure 3.3. Certus-NX LFD2NX-35 and LFD2NX-65 sysI/O Banking;
	  • general update to the VCCIO Wide Range (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V) and VCCIO High Performance (1.0 V/1.2 V/1.35 V/1.5 V/1.8 V) sections;
	  • added Table 3.1. CrossLink-NX, Certus-NX, and CertusPro-NX Banks.
	• In the MachXO5-NX Devices section:
	  • added the following description for LFMXO5-35 and LFMXO5-65 sysI/O banking, *For LFMXO5-35/T and LFMXO5-65/T devices, there are eleven banks in total. Two banks are on the top, bank 0 and bank 1; three banks are on left side, bank 7, bank 8, and bank 9; three banks are on the right side, bank 2, bank 3, and bank 4; and three banks are on the bottom, bank 5, bank 6, and bank 11. Note that there is no bank 10. The top, left, and right banks use the voltage level from the respective VCCIO. The bottom banks have 2 VREF inputs for flexibility to receive two referenced input levels in the same bank. Figure 3.6 shows the location of each bank*;
	  • added Figure 3.6. LFMXO5-35/T and LFMXO5-65/T sysI/O Banking;
	  • general update to the VCCIO Wide Range (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V) and VCCIO High Performance (1.0 V/1.2 V/1.35 V/1.5V/1.8V) sections;
	  • added Table 3.2. MachXO5-NX Banks.

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Revision 2.5, January 2025

Section	Change Summary
sysI/O Buffer Configurations	In the Soft MIPI D-PHY Support section, changed *MIPI primitive is supported in Bank 3, Bank 4, and Bank 5 on the bottom side of the device* to *For Crosslink-NX devices, the MIPI primitive is supported in Bank 3, Bank 4, and Bank 5 on the bottom side of the device. For other Nexus devices, refer to their respective datasheets.*

Revision 2.4, July 2024

Section	Change Summary

sysI/O Banking Scheme	• In the CrossLink-NX, Certus-NX, and CertusPro-NX Devices section:
	  • changed *For the 40k, 50k, and 100k devices, there is one bank on top, two banks each on the left and right side of the device, and three on the bottom side of the device* to
	  For the 28k, 40k, 50k, and 100k devices, there is one bank on top, two banks each on the left and right side of the device, and three on the bottom side of the device;
	  • changed *For the 17k device, there is one bank on top, one on the right side, and three on the bottom side of the device* to
	  For the 9k and 17k device, there is one bank on top, one on the right side, and three on the bottom side of the device.
	• In Figure 3.1. CrossLink-NX, Certus-NX, CertusPro-NX sysI/O Banking, changed the note from *Banks not available in 17k devices* to *Banks not available in 9k and 17k devices*.

Revision 2.3, June 2024

Section	Change Summary
All	• Changed *MachXO5-NX 25* to *LFMXO5-25* globally. • Changed *MachXO5-NX 100T/55T* to *LFMXO5-100T/LFMXO5-55T* globally.

sysI/O Banking Scheme	• Added *LFMXO5-15D* device to:
	  • the following paragraph in MachXO5-NX Devices:
	  The LFMXO5-25/LFMXO5-15D devices have ten GPIO banks. There are two banks on top, three banks each on the left and right side of the device, and two on the bottom side of the device;
	  • caption of Figure 3.2. LFMXO5-25/LFMXO5-15D sysI/O Banking;
	  • headers of VCCIO [0, 1, 2, 3, 4, 7, 8, 9] Wide Range for LFMXO5-25/LFMXO5-15D (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V) and VCCIO [5, 6] High Performance for LFMXO5-25/LFMXO5-15D (1.0 V/1.2 V/1.35 V/1.5 V/1.8 V) sections.
	• Added *LFMXO5-55TD* device to:
	  • the following paragraph in MachXO5-NX Devices:
	  The LFMXO5-100T/LFMXO5-55T/LFMXO5-55TD devices have eight GPIO banks. There is one bank on top, two banks each on the left and right side of the device, and three on the bottom side of the device;
	  • caption of Figure 3.3. LFMXO5-100T/LFMXO5-55T/LFMXO5-55TD sysI/O Banking;
	  • headers of VCCIO [0, 1, 2, 6, 7] Wide Range for LFMXO5-100T/LFMXO5-55T/ LFMXO5-55TD (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V) and VCCIO [3, 4, 5] High Performance for LFMXO5-100T/LFMXO5-55T/LFMXO5-55TD (1.0 V/1.2 V/1.35 V/1.5 V/1.8 V) sections.

V_{CCIO} Requirement for I/O Standards	Added table notes on *mixed mode* in Table 4.1. Input Mixed Mode[4] for Wide Range Input Buffers and Table 4.2. Input Mixed Mode[3] for High-Performance Input Buffers.

Software sysI/O Attributes	• Added *PULLMODE in FAILSAFE mode enables the pull-up for the P input and pull-down for the N input in LVDS* to the note in the PULLMODE section.
	• Table 6.2. Drive Strength Values:
	  • removed 8 mA from the drive values for LVCMOS15, LVCMOS12, LVCMOS10H, LVCMOS15 (Open Drain), LVCMOS12 (Open Drain), and LVCMOS10H (Open Drain);
	  • added a table note on the default drive value.

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Section	Change Summary
All	• Changed *MachXO5-NX 25* to *LFMXO5-25* globally. • Changed *MachXO5-NX 100T/55T* to *LFMXO5-100T/LFMXO5-55T* globally.
sysI/O Buffer Design Rules	• Added *For bidirectional ports, pull-up and pull-down are allowed. The PULLMODE is set to NONE by default*.

Revision 2.2, October 2023

Section	Change Summary
All	Changed *CrossLink-NX-33U* to *CrossLinkU-NX*.

Revision 2.1, August 2023

Section	Change Summary
Introduction	Updated reference to the combined CrossLink-NX-33 and CrossLinkU-NX Data Sheet.
sysI/O Banking Scheme	• Corrected banks in the VCCIO [0, 1, 5] Wide Range (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V) and VCCIO [2, 3, 4] High Performance (1.0 V/1.2 V/1.35 V/1.5 V/1.8 V) sections. • Added the CrossLinkU-NX section.
sysI/O Buffer Configurations	Added reference to the combined CrossLink-NX-33 and CrossLinkU-NX Data Sheet in the Soft MIPI D-PHY Support section.
References	Updated reference to the combined CrossLink-NX-33 and CrossLinkU-NX Data Sheet. Added references to web pages and other documents.

Revision 2.0, August 2023

Section	Change Summary
sysI/O Banking Scheme	Updated Figure 3.5. High-Performance sysI/O Buffer Pair for Bottom Side to show that the Outputs of the Single Ended Drivers are connected to (+) Referenced Input Comparator and Input Buffers.
Software sysI/O Attributes	In Table 6.2. Drive Strength Values, added I/O Type SSTL135_I and SSTL135_II.
References	Added this section.

Revision 1.9, February 2023

Section	Change Summary
All	Minor adjustments in formatting across the document.
sysI/O Banking Scheme	• Added MachXO5-NX 25 and MachXO5-NX 100T/55T information, including Figure 3.3. MachXO5-NX 100T/55T sysI/O Banking, VCCIO [0, 1, 2, 6, 7] Wide Range for MachXO5-NX 100T/55T (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V), and VCCIO [3, 4, 5] High Performance for MachXO5-NX 100T/55T (1.0 V/1.2 V/1.35 V/1.5 V/1.8 V). • Updated Figure 3.9. High Performance sysI/O Buffer Pair for Bottom Side to add missing connection on the SE drive input.
Software sysI/O Attributes	Updated PULLMODE section to add KEEPER value and note reference for FAILSAFE.

Revision 1.8, December 2022

Section	Change Summary
Software sysI/O Attributes	Changed the default value of the attribute from OFF to 100 in the DIFFRESISTOR section.
Technical Support Assistance	Added reference link to Lattice Answer Database.

Revision 1.7, August 2022

Section	Change Summary
sysI/O Banking Scheme	• Removed reference to the 125k device from the CrossLink-NX, Certus-NX, and CertusPro-NX sections. • Removed reference to MachXO5-NX 55k device from the MachXO5-NX section. Revised banking description and Figure 3.4.

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Section	Change Summary
	• Corrected title of the referenced document to Power Management and Calculation for CrossLink-NX Devices (FPGA-TN-02075).

Revision 1.6, June 2022

Section	Change Summary
All	Added CrossLink-NX-33 support.

Revision 1.5, December 2021

Section	Change Summary
All	Added MachXO5-NX support.

Revision 1.4, October 2021

Section	Change Summary
Software sysI/O Attributes	• In the PULLMODE section, changed Default to DOWN for standards mentioned above. Others defaulted to NONE. • In HYSTERESIS section, changed Default to ON for LVTTL, and LVCMOS15/18/33 for input and bidirectional standards. Others defaulted to NA. • Minor editorial changes.

Revision 1.3, June 2021

Section	Change Summary
All	Added references to the CertusPro-NX data sheet and technical notes.
sysI/O Banking Scheme	• Updated section introduction. • Updated footnote in Figure 3.1. sysI/O Banking. • Updated Figure 3.3. Wide Range sysI/O Buffer for Top, Left/Right Side.

Revision 1.2, November 2020

Section	Change Summary
Introduction	Added references to data sheets and removed some statements.
sysI/O Overview	Added this section.
sysI/O Banking Scheme	• Updated introductory paragraph. • Updated headings of sub-sections 3.2 and 3.3.
sysI/O Buffer Configurations	Updated Programmable Clamp section.
Software sysI/O Attributes	Deleted *Preference Editor* from DIN/DOUT description.
Appendix A. sysI/O Attribute Examples	• Updated default of PULLMODE and CLAMP attributes. • Updated values of TERMINATION attribute. • Updated subheading to DRIVE STRENGTH.
All	Minor adjustments in formatting/style.

Revision 1.1, June 2020

Section	Change Summary
All	• Updated document title to sysI/O Usage Guide for Nexus Platform. • Added Nexus platform (which includes CrossLink-NX and Certus-NX) support.
sysI/O Banking Scheme	• Updated note in Figure 3.1. • Added the High Performance sysI/O Buffer Pairs (On Bottom Side) and Wide Range sysI/O Buffer Pair (On Top, Left/Right Sides) sections. • Added references in Standby section.
sysI/O Buffer Configurations	Added the Soft MIPI D-PHY Support section.
Appendix A. sysI/O Attribute Examples	Added this section.

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Section	Change Summary
Appendix B. sysI/O Buffer Design Rules	Added this section.
Appendix C. sysI/O Attributes using the Lattice Radiant Device Constraint Editor User Interface	Added this section.

Revision 1.0, November 2019

Section	Change Summary
All	Initial release

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