



APB Interconnect Module

IP Version: 1.5.0

User Guide

FPGA-IPUG-02054-1.5

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This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language [FAQ 6878](#) for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
EBR	Embedded Block RAM
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
GPIO	General Purpose Input/Output
HDL	Hardware Description Language
I2C	Inter-Integrated Circuit
IP	Intellectual Property
LUT	Look-Up Table
UART	Universal Asynchronous Receiver/Transmitter

1. Introduction

The Lattice Semiconductor APB Interconnect Module is a fully parameterized soft IP for low latency interconnect fabric for APB system. It can be used to connect one or more APB bus requester to one or more APB bus completer. Requester-side arbitration is implemented within the module to minimize resource use. This means only one requester can access any of the completers at any given time. The APB Interconnect Module supports round-robin based and fixed priority based arbitration when multiple bus requesters access the same completer port. The arbitration completes in one clock cycle, which means that the transaction is delayed by one clock cycle when arbitration occurs.

The design is implemented in Verilog HDL. The IP can be configured and generated based on [Table 1.1](#).

Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation

Supported Devices	IP Configuration and Generation	IP Implementation (Synthesis, Map, Place and Route)
MachXO2™	Lattice Propel™ Builder software	Lattice Diamond™ software
MachXO3™	Lattice Propel Builder software	Lattice Diamond software
MachXO3D™	Lattice Propel Builder software	Lattice Diamond software
Mach™-NX	Lattice Propel Builder software	Lattice Diamond software
MachXO4™	Lattice Propel Builder software	Lattice Radiant™ software
MachXO5™-NX	Lattice Propel Builder software	Lattice Radiant™ software
CrossLink™-NX	Lattice Propel Builder software	Lattice Radiant software
Certus™-NX	Lattice Propel Builder software	Lattice Radiant software
Certus-N2	Lattice Propel Builder software	Lattice Radiant software
CertusPro™-NX	Lattice Propel Builder software	Lattice Radiant software
Lattice Avant™	Lattice Propel Builder software	Lattice Radiant software
iCE40 UltraPlus™	Lattice Propel Builder software	Lattice Radiant software

1.1. Features

The key features of the APB Interconnect Module include:

- Compliance with AMBA 3 APB Protocol v1.0
- Fully parameterized design
- Data Bus width of up to 32 bits [8, 16, 32]
- Address width of up to 32 bits [11,12,...,32]
- Support to up to 32 requesters and 32 completers
- Completer port address decoding
- Requester side arbitration
- Selectable arbitration scheme:
 - Round robin
 - Fixed priority

2. Functional Description

2.1. Overview

The Lattice Semiconductor APB Interconnect Module is a fully parameterized soft IP, low latency interconnect fabric for AMBA 3 APB based systems, enabling one or more bus requesters to be connected to one or more completers. This module is compliant with AMBA 3 APB Protocol v1.0.

AMBA 3 Advanced Peripheral Bus (APB) is a low-cost interface that is optimized for minimal power consumption and reduced interface complexity. APB should be used for any peripherals that are low-bandwidth and do not require the high performance of a pipelined bus interface. Examples include UART, I2C, and GPIO. The APB is an unpipelined protocol, which means that the APB requester can only initiate a new transfer after the previous transfer is completed.

The APB-3 interface protocol does not have any *size* or *byte enable* signals to indicate transfer size. That is, all APB transfers are accessing the full width of the data bus. Thus, in a 32-bit processor system application, the data bus should be 32 bits.

2.2. Interface Description

Figure 2.1 shows the interface diagram for the APB Interconnect Module. The diagram shows all of the available ports for the IP core.

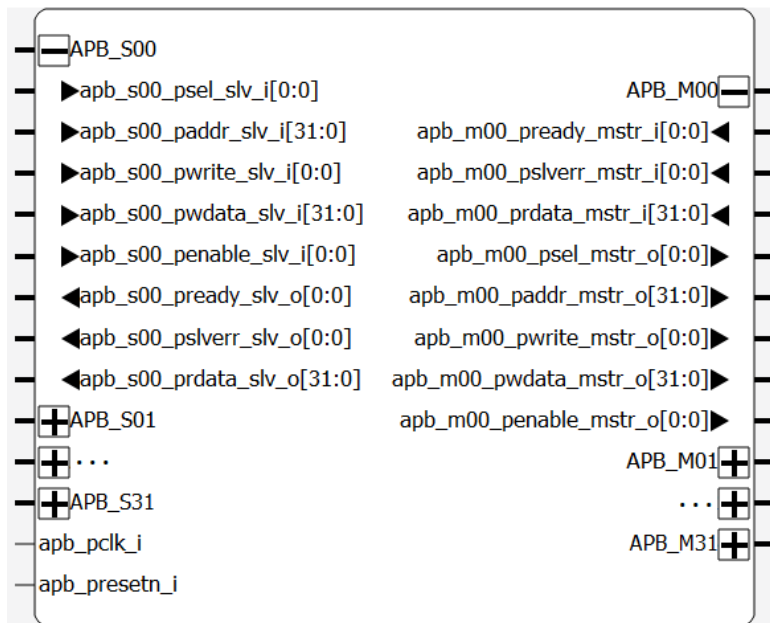


Figure 2.1. APB Interconnect Module Interface Diagram

Table 2.1. APB Interconnect Module Signal Description

Pin Name	Direction	Width (Bits)	Description
Clock and Reset			
apb_pclk_i	In	1	APB clock
apb_presetn_i	In	1	APB active LOW reset
APB Completer Interface 00 (APB_M00)			
apb_m00_psel_mstr_o	Out	1	Select signal Indicates that the completer device is selected and that a data transfer is required.
apb_m00_paddr_mstr_o	Out	<i>M_ADDR_WIDTH</i>	Address signal
apb_m00_pwdata_mstr_o	Out	<i>DATA_WIDTH</i>	Write data signal
apb_m00_pwrite_mstr_o	Out	1	Direction signal Write = 1, Read = 0
apb_m00_penable_mstr_o	Out	1	Enable signal Indicates the second and subsequent cycles of an APB transfer.
apb_m00_pready_mstr_i	In	1	Ready signal Indicates transfer completion. Completer uses this signal to extend an APB transfer.
apb_m00_pslverr_mstr_i	In	1	Error signal Indicates a transfer failure. In case APB Completer does not have this signal, it should be tied to 1'b0.
apb_m00_prdata_mstr_i	In	<i>DATA_WIDTH</i>	Read data signal
APB Completer Interface 01 (APB_M01)			
apb_m01_psel_mstr_o	Out	1	Select signal Indicates that the completer device is selected and that a data transfer is required.
apb_m01_paddr_mstr_o	Out	<i>M_ADDR_WIDTH</i>	Address signal
apb_m01_pwdata_mstr_o	Out	<i>DATA_WIDTH</i>	Write data signal
apb_m01_pwrite_mstr_o	Out	1	Direction signal Write = 1, Read = 0
apb_m01_penable_mstr_o	Out	1	Enable signal Indicates the second and subsequent cycles of an APB transfer.
apb_m01_pready_mstr_i	In	1	Ready signal Indicates transfer completion. Completer uses this signal to extend an APB transfer.
apb_m01_pslverr_mstr_i	In	1	Error signal Indicates a transfer failure. In case APB Completer does not have this signal, it should be tied to 1'b0.
apb_m01_prdata_mstr_i	In	<i>DATA_WIDTH</i>	Read data signal
...			—
APB Completer Interface xx (APB_Mxx)			
apb_mxx_psel_mstr_o	Out	1	Select signal Indicates that the completer device is selected and that a data transfer is required.
apb_mxx_paddr_mstr_o	Out	<i>M_ADDR_WIDTH</i>	Address signal
apb_mxx_pwdata_mstr_o	Out	<i>DATA_WIDTH</i>	Write data signal
apb_mxx_pwrite_mstr_o	Out	1	Direction signal Write = 1, Read = 0
apb_mxx_penable_mstr_o	Out	1	Enable signal Indicates the second and subsequent cycles of an APB transfer.

Pin Name	Direction	Width (Bits)	Description
apb_mxx_pready_mstr_i	In	1	Ready signal Indicates transfer completion. Completer uses this signal to extend an APB transfer.
apb_mxx_pslverr_mstr_i	In	1	Error signal Indicates a transfer failure. In case APB Completer does not have this signal, it should be tied to 1'b0.
apb_mxx_prdata_mstr_i	In	<i>DATA_WIDTH</i>	Read data signal
APB Requester Interface 00 (APB_S00)			
apb_s00_psel_mstr_i	In	1	Select signal Indicates that this APB interface is selected and that a data transfer is required.
apb_s00_paddr_mstr_i	In	<i>M_ADDR_WIDTH</i>	Address signal
apb_s00_pwdata_mstr_i	In	<i>DATA_WIDTH</i>	Write data signal
apb_s00_pwrite_mstr_i	In	1	Direction signal Write = 1, Read = 0
apb_s00_penable_mstr_i	In	1	Enable signal Indicates the second and subsequent cycles of an APB transfer.
apb_s00_pready_mstr_o	Out	1	Ready signal Indicates transfer completion. This signal is used to extend an APB transfer.
apb_s00_pslverr_mstr_o	Out	1	Error signal Indicates a transfer failure.
apb_s00_prdata_mstr_o	Out	<i>DATA_WIDTH</i>	Read data signal
APB Requester Interface 01 (APB_S01)			
apb_s01_psel_mstr_i	In	1	Select signal Indicates that this APB interface is selected and that a data transfer is required.
apb_s01_paddr_mstr_i	In	<i>M_ADDR_WIDTH</i>	Address signal
apb_s01_pwdata_mstr_i	In	<i>DATA_WIDTH</i>	Write data signal
apb_s01_pwrite_mstr_i	In	1	Direction signal Write = 1, Read = 0
apb_s01_penable_mstr_i	In	1	Enable signal Indicates the second and subsequent cycles of an APB transfer.
apb_s01_pready_mstr_o	Out	1	Ready signal Indicates transfer completion. This signal is used to extend an APB transfer.
apb_s01_pslverr_mstr_o	Out	1	Error signal Indicates a transfer failure.
apb_s01_prdata_mstr_o	Out	<i>DATA_WIDTH</i>	Read data signal
...			
APB Requester Interface yy (APB_Syy)			
apb_syy_psel_mstr_i	In	1	Select signal Indicates that this APB interface is selected and that a data transfer is required.
apb_syy_paddr_mstr_i	In	<i>M_ADDR_WIDTH</i>	Address signal
apb_syy_pwdata_mstr_i	In	<i>DATA_WIDTH</i>	Write data signal
apb_syy_pwrite_mstr_i	In	1	Direction signal Write = 1, Read = 0
apb_syy_penable_mstr_i	In	1	Enable signal Indicates the second and subsequent cycles of an APB transfer.

Pin Name	Direction	Width (Bits)	Description
apb_syy_pready_mstr_o	Out	1	Ready signal Indicates transfer completion. This signal is used to extend an APB transfer.
apb_syy_pslverr_mstr_o	Out	1	Error signal Indicates a transfer failure.
apb_syy_prdata_mstr_o	Out	DATA_WIDTH	Read data signal

Notes:

- xx – Possible values are (02, 03,..., Total APB Completers -1).
- yy – Possible values are (02, 03,..., Total APB Requesters -1).

All APB Requester/Completer Interfaces are compliant with APB protocol. Refer to the AMBA 3 APB Protocol Specification in the [Arm](#) web page for the timing diagrams and for more information on the protocol.

2.3. Attributes Summary

Table 2.2 provides a list of the user configurable attributes of the APB Interconnect Module. The attribute values are specified using the IP core configuration user interface in the Propel Builder software as shown in Table 2.2.

Table 2.2. Attributes Table⁴

Attribute	Selectable Values	Default	Dependency on Other Attributes ³
General Tab			
General Group			
Total APB Requesters	1–32	2	Total APB Requesters and Total APB Completers cannot be both 1
Total APB Completers	1–32	2	
Requester Address Width(bits) (M_ADDR_WIDTH)	11–32	32	—
Full Address Decoding up to 1kB ¹	Checked, Unchecked	Checked	—
Data Bus Width(bits) (DATA_WIDTH)	8, 16, 32	32	—
Registered Output ²	Checked, Unchecked	Unchecked	—
Main Settings Tab^{3, 5}			
Completer 0 Settings Group			
S0 Base Address	0–(2 ^{M_ADDR_WIDTH} – 'h400)	32'h00000000	en_s0
S0 Address Range	'h400–2 ^{M_ADDR_WIDTH}	32'h00000400	en_s0
Completer 1 Settings Group			
S1 Base Address	0–(2 ^{M_ADDR_WIDTH} – 'h400)	32'h00000400	en_s1
S1 Address Range	'h400–2 ^{M_ADDR_WIDTH}	32'h00000400	en_s1
...			
Completer 31 Settings Group			
S31 Base Address	0–(2 ^{M_ADDR_WIDTH} – 'h400)	32'h00007c00	en_s31
S31 Address Range	'h400–2 ^{M_ADDR_WIDTH}	32'h00000400	en_s31
Requester Priority Settings Tab			
Completer Settings Group			
Arbiter Scheme	Round Robin, Fixed Priority	Round Robin	en_s0
Requester 0 Priority	0–31	0	en_m1 and (Arbiter Scheme == Fixed Priority)
Requester 1 Priority	0–31	1	en_m1 and (Arbiter Scheme == Fixed Priority)
Requester 2 Priority	0–31	2	en_m2 and (Arbiter Scheme == Fixed Priority)
...			

Attribute	Selectable Values	Default	Dependency on Other Attributes ³
Requester 31 Priority	0–31	31	en_m31 and (Arbiter Scheme == Fixed Priority)

Notes:

- [Full Address Decoding up to 1kB = Unchecked] is currently not supported.
- [Registered Output = Checked] is currently not supported.
- Settings under Main Settings Tab are not configurable when the IP is being configured using System Builder because the tool manages the address map.
- To simplify the condition, en_s0, en_s1 to en_s31 are used for the condition that the corresponding connection to external completer is enabled. Similarly, en_m0, en_m1, en_m2, and en_m31 are used for the condition that the corresponding connection to external requester is enabled.
- The **Main Settings Tab** is not displayed when *Total APB Completers* = 1. Refer to the [Address Validity in Multi-requester Single-completer Configuration](#) section for more details.

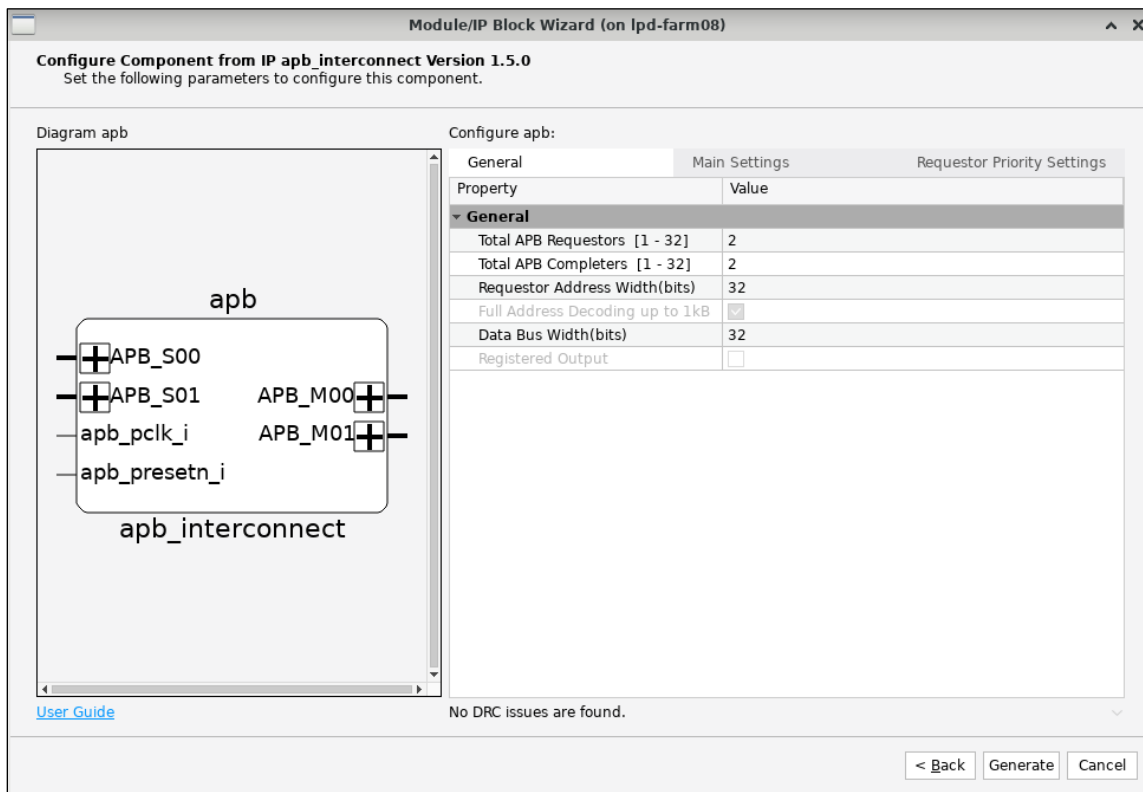


Figure 2.2. APB Interconnect Module/IP Block Wizard

Table 2.3. Attributes Description

Attribute	Description
General Tab	
General Group	
Total APB Requesters	Specifies the number of APB requesters that are connected to this Soft IP.
Total APB Completers	Specifies the number of APB completers that are connected to this Soft IP.
Requester Address Width(bits) (M_ADDR_WIDTH)	Specifies the bit width of all PADDR signals.
Full Address Decoding up to 1kB	Selects the decoder implementation. Refer to the Decoder section for more information.
Data Bus Width(bits) (DATA_WIDTH)	Specifies the bit width of all PWDATA and PRDATA signals.
Registered Output	Unchecked: Output register is disabled (bypassed) Checked: Output register is enabled – this option is currently not supported

Attribute	Description
Main Settings Tab	
Completer <N> Settings Group	
Base Address <N>	Specifies base address for APB completer <N>. If [Full Address Decoding up to 1kB = Checked]: The value must be aligned to 1 kB. If [Full Address Decoding up to 1kB = Unchecked]: The value must be aligned to (or multiple of) the value of Address Range rounded up to power of 2.
Address Range <N>	Specifies address range for APB completer <N>. If [Full Address Decoding up to 1kB = Checked]: The value must be multiple of 1 kB.
Requester Priority Settings Tab	
Completer Settings Group	
Arbiter Scheme	Specifies the arbitration scheme to be implemented for APB completer.
Requester <M> Priority	Specifies priority index of APB requester <M> to access APB completer. [0]: Highest priority ... [31]: Lowest priority

Notes:

- <N> - Completer index [0,1,...,(Total APB Completers)-1].
- <M> - Requester index [0,1,...,(Total APB Requesters)-1].

2.4. Use Models

The APB Interconnect module connects one or more APB requester devices to one or more APB completer devices. Each connected APB requester device could either be:

- A device that originates APB transactions (endpoint requester) or
- A requester interface of an upstream APB Interconnect core being cascaded

Similarly, each connected APB completer device could either be:

- The final target of APB transactions (endpoint completer) or
- A completer interface of a downstream APB Interconnect core being cascaded

In general, APB Interconnect Module can be configured for the following connectivity patterns:

- Single Requester Interconnect – refer to the [Single Requester Interconnect](#) section.
- Multi-Requester Interconnect – refer to the [Multi-Requester Interconnect](#) section.

An example of Single Requester Interconnect application is shown in [Figure 2.3](#). The arrows in the figure are APB interface connections, where *M* stands for an APB requester port, and *S* stands for an APB completer port. In this example, AHB-Lite to APB (AHBL2APB) Bridge is the endpoint APB requester. In an embedded system, this module usually converts the register access AHB-Lite transaction to APB. The APB requester must be registered output for better routing in the FPGA fabric.

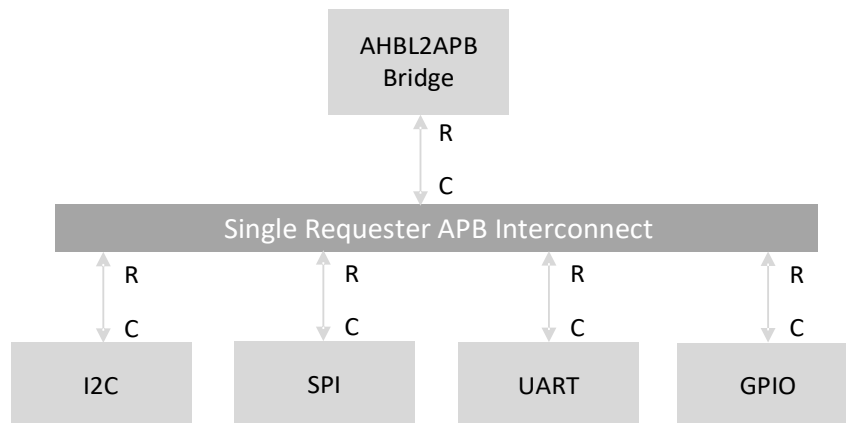


Figure 2.3. Example of Single Requester Interconnect Application

An example of a Multi-Requester Interconnect application is shown in Figure 2.4. This is similar to Figure 2.3 with the addition of the I2CS2APB Bridge. In this example, the I2CS2APB Bridge may be used to perform read and write access to the peripheral registers through the I2C interface that is connected to the external I2C Requester. If the two APB requesters attempt to access the completers (either the same completer or a different completer) at the same time, arbitration occurs and only the granted requester gains access to the target completer. This requester-side arbitration optimizes resource utilization at the expense of reduced performance. This is acceptable for APB interconnect since APB is not intended for high performance application.

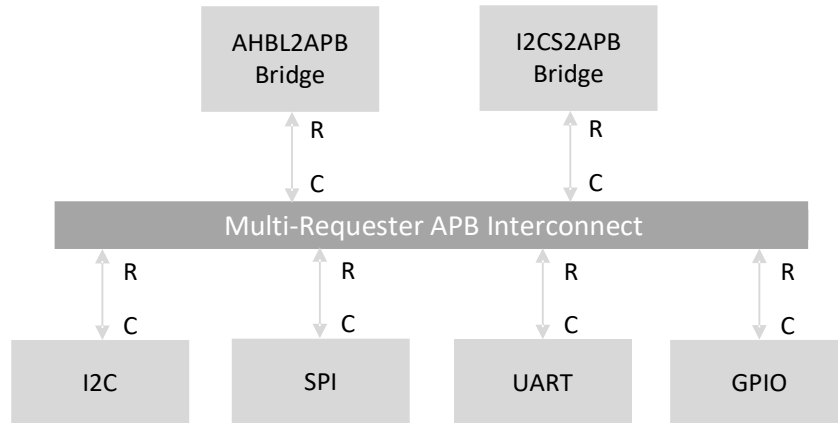


Figure 2.4. Example of Multi-Requester Interconnect Application

2.5. Single Requester Interconnect

The Single Requester Interconnect described in this document is a single requester to multiple completer configuration of the Lattice Semiconductor APB Interconnect Module. The bus interconnect logic is encapsulated inside the soft IP, which consists of an address decoder, a completer-to-requester multiplexor, and a default completer. This is shown in Figure 2.5. The requester-to-completer APB signals (PENABLE, PWRITE, PWDATA, PADDR), not including PSELx, are connected directly from the requester to all the completers. The PADDR also goes to the Decoder component, which generates individual PSELx signals to each completers. The completer treats the transaction as valid when its PSELx input is asserted. When no completer is selected, the PSELx going to the Default Completer asserts. In this case, the Default Completer sends an error response to the multiplexor. The Multiplexor uses the PSELx signals from the Decoder to select the completer to requester signals (PREADY, PRDATA, PSLVERR) from the target completer and route it to the requester.

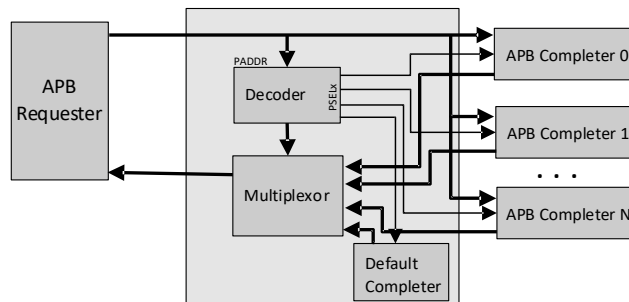


Figure 2.5. Functional Block Diagram of Single Requester Interconnect

2.5.1. Decoder

The Decoder component performs address decoding for each bus transfer and provides a select signal for each completer on the bus. Decoding is done by comparing the appropriate address bits with the user-provided memory-map (*Base Address* and *Address Range*) settings during configuration. This is shown in Figure 2.6. The memory map is static setting; it cannot be changed during operation. During a bus transfer, the select signal goes high for a single completer involved in the transfer. The decoder also sends the PSELx signals to the multiplexor.

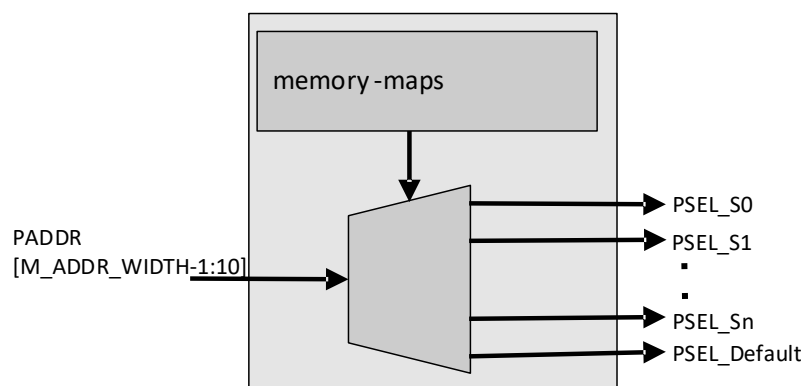


Figure 2.6. Block Diagram of AHB-Lite Decoder

The minimum address space that can be allocated to a single completer is 1 kB. This is done to be consistent with AHB-Lite Interconnect and to reduce the combinatorial delay of address decoding. When configuring the IP, the *Address Range* attribute value for the completer must be a multiple of 1 kB.

The PSELx signal is a combinatorial decode of the high-order address signals. This is done by comparing the higher bits of the address signal with the *Base Address* and *Address Range* settings. The behavior of decoder is controlled by the *Full Address Decoding up to 1 kB* attribute as follows:

- [Full Address Decoding up to 1kB is Checked]: PSEL signal asserts if the following conditions are met:
- $\text{apb_sxx_paddr_slv_i}[M_ADDR_WIDTH - 1:10] \geq \text{Base Address}[M_ADDR_WIDTH - 1:10]$

- $apb_sxx_paddr_slv_i[M_ADDR_WIDTH - 1:10] \leq (\text{Max Address} + \text{Address Range})[M_ADDR_WIDTH - 1:10]$
- [Full Address Decoding up to 1kB is Unchecked]: PSEL signal asserts if the following condition is met:
- $apb_sxx_paddr_slv_i[M_ADDR_WIDTH - 1:XBIT] == \text{Base Address}[M_ADDR_WIDTH - 1:XBIT]$
Wherein $XBIT = \text{Round_up}(\log_2(\text{Address Range}))$

When Full Address Decoding up to 1 kB is Unchecked, the Address Range is not used in comparison because it is in a power of 2 value. Thus, the behavior of the interconnect is undefined if this attribute is not in a power of 2 value.

The user-defined memory maps of the completers are parameters to the decoder IP and are used to select the appropriate completer. If a system design does not contain a completely filled memory map, a default completer is selected when a transfer is attempted to a nonexistent address location.

2.5.2. Default Completer

When a transfer is attempted to an address that does not map to a completer, the Default Completer provides an error response to the multiplexor. An error response is the assertion of the PSLVERR signal when PENABLE and PREADY are both asserted. The PRDATA signal from Default Completer is fixed to 0.

2.5.3. Multiplexor

A Multiplexor component is a completer-to-requester multiplexor. It selects the PRDATA, PREADY, and PSLVERR signals from the completers going to the requester as shown in Figure 2.7. The Multiplexor registers the PSELx signals from the Decoder and uses it to route the appropriate signals from the selected completer to the requester. The registering of the PSELx signal is necessary to break the combinatorial delay. This is important because the PSELx signals are part of the critical path.

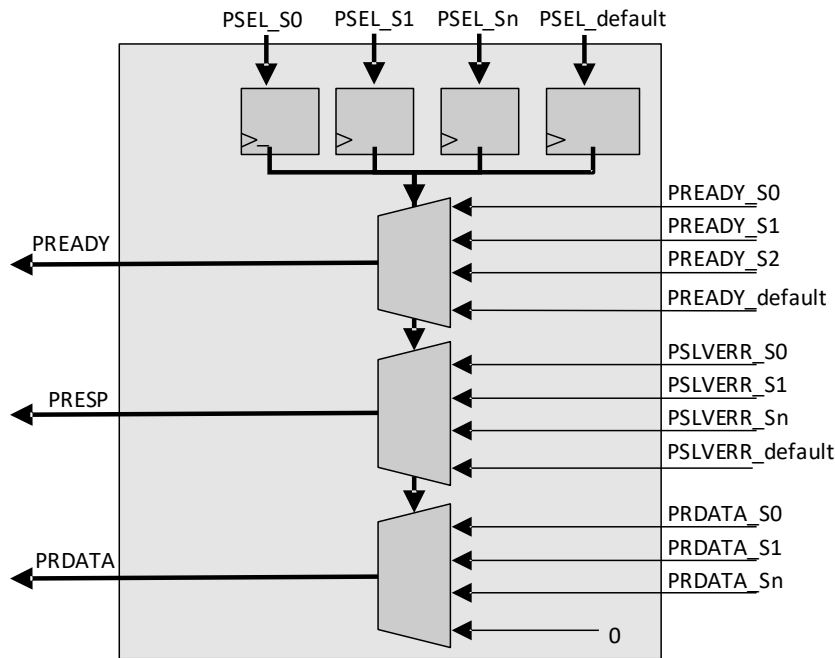


Figure 2.7. Block Diagram of APB Multiplexor

2.6. Multi-Requester Interconnect

The Multi-Requester Interconnect described in this document is a single requester to multiple completer configuration of the Lattice Semiconductor APB Interconnect Module. It implements requester-side arbitration as shown in Figure 2.8. All the APB requesters go to the Arbiter Mux, which selects only one transaction to go through the Single Requester Interconnect. This means that when two or more APB requesters perform transaction to any completers at the same time, arbitration takes place. Only the granted requester can access any of the completers at a given time. You can specify a

different arbitration scheme for each completer, which is used to select a requester during bus contention. Currently, there are two arbitration scheme options:

- Round-robin (default) – Each requester is serviced in round-robin manner, giving each requester equal access to the completer.
- Fixed priority – High priority requesters are always given access to the completer in preference over lower priority requesters.

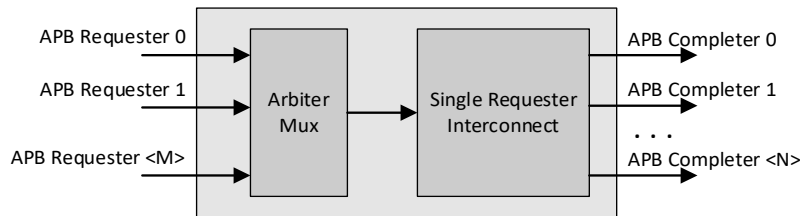


Figure 2.8. Block Diagram of Multi-Requester Interconnect

2.6.1. Arbiter Mux

The Arbiter Mux receives an APB interface from each requester and routes one APB interface to the completer as shown in Figure 2.9. The Arbiter component arbitrates any potential contention between requesters. When PSELx is high from multiple requesters, the Arbiter generates the grant signal to the Multiplexors. The Requester to Completer Multiplexor routes the APB signals from the granted requester to the completer. These signals are PADDR, PSELx, PENABLE, and PWRITE. On the other hand, the Completer to Requester multiplexor routes the PREADY, PRDATA, and PSLVERR signals to the granted requester. The requesters that are not granted have their PREADY input low, thus, the transaction is pended. The pended requester that is recently granted is already in access state. The FSM generates the necessary IDLE and SETUP states of the APB transaction for the newly granted requester.

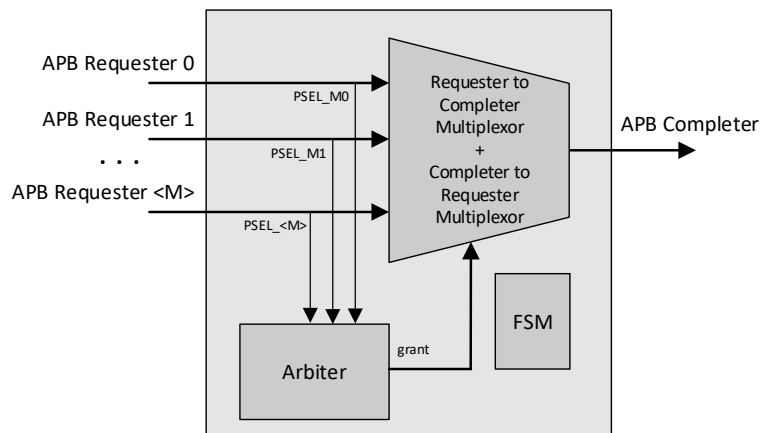


Figure 2.9. Block Diagram of APB Arbiter Mux

3. Design Considerations

3.1. Address Validity in Multi-requester Single-completer Configuration

- For area optimization, the interconnect does not instantiate the bus (decoder, default completer, and multiplexer) when there is more than one requester and exactly one completer. As only one completer can be selected, address decoding is omitted and the interconnect acts as a pass-through.
- In this configuration, the interconnect does not check address ranges, such as `SO_BASE_ADDR` and `SO_ADDR_RANGE`. The interconnect forwards whatever address the granted requester drives to the completer.
- Requesters are responsible for not sending invalid (out-of-range) addresses to the completer. The interconnect does not assert `PSLVERR` or block such transactions.

3.2. APB Interconnect Arbitration Behavior

3.2.1. Non-preemptive Round-Robin Arbitration

The APB Interconnect (APB IC) uses non-preemptive round-robin arbitration evaluated only at ownership-window boundaries instead of at each APB transfer. Arbitration behavior is governed by the following rules:

- Grant lock condition
When a requester is granted access, the grant remains locked while the requester `PSEL` signal remains asserted.
- Release condition
The grant is released only when the current requester de-asserts the `PSEL` signal.
- No preemption
Changes in other requesters request signals do not trigger re-arbitration while the current grant remains active.

Round-robin fairness applies between ownership windows, not between individual APB transfers.

3.2.2. Protocol Requirement

The APB protocol requires stability across `SETUP` and `ACCESS` phases and the implementation follows these requirements:

- `SETUP` to `ACCESS` stability
During the `SETUP` phase, the `PSEL` signal is asserted, and the `PENABLE` signal is asserted in the next clock for the `ACCESS` phase. APB requires address and control to remain stable from the `SETUP` phase into the `ACCESS` phase. The APB IC is a grant-based multiplexer. The APB IC forwards `PADDR`, `PWRITE`, `PWDATA`, and other signals from a requester to the completer. Switching the grant while the current requester still asserts the `PSEL` signal changes the driving source inside an active transfer window, risking a protocol stability violation.
- Back-to-back transfers are represented by keeping the `PSEL` signal asserted
APB explicitly allows the `PSEL` signal to stay high when another transfer follows immediately. The APB IC treats `PSEL=1` as a continuous ownership window (analogous to holding the bus for a burst in other protocols) to ensure the completer sees one coherent initiator across consecutive `SETUP` and `ACCESS` cycles.
- Wait states make mid-window switching unsafe
If `PREADY=0` during the `ACCESS` phase, APB requires address, control, select, and enable signals (and write data where applicable) to remain unchanged for the extended cycles. The APB IC holds the grant while the `PSEL` signal remains asserted enforces single-owner stability through wait states and avoids accidental multiplexer switching during a period where APB mandates stability.

3.2.3. Limitations

The non-preemptive policy introduces the following trade offs:

- Fairness granularity
Arbitration fairness is applied per ownership window instead of per APB transfer.
- Potential latency for other requesters
A requester that keeps the `PSEL` signal continuously asserted can delay service to others. This is an expected behavior under a non-preemptive policy and remains protocol-compliant.

To force arbitration between every transfer, each requester must de-assert the PSEL signal between APB transfers. This creates ownership boundaries, allowing the interconnect to release the bus and re-arbitrate for the next transfer.

Appendix A. Resource Utilization

Note: Resource utilization values in this section are provided for reference only and may change based on the compilation strategy and selected tool options.

The following tables show the resource utilization of the APB Interconnect for different Lattice FPGA devices using the Lattice Radiant software with Synplify Pro® as the synthesis tool.

Table A.1. Resource Utilization Using the LAV-AT-X70ES-1LFG1156I Device

Configuration	Requester Address Width	Data Bus Width	Registers	LUTs	EBRs
Total APB Requesters = 1 Total APB Completers =2	32	8	3	31	0
Total APB Requesters = 1 Total APB Completers =2	32	16	3	47	0
Total APB Requesters = 1 Total APB Completers =2	11	16	2	20	0
Total APB Requesters = 2 Total APB Completers =1	11	32	7	132	0

Table A.2. Resource Utilization Using the LFCPNX-100-8LFG672I Device

Configuration	Requester Address Width	Data Bus Width	Registers	LUTs	EBRs
Total APB Requesters = 1 Total APB Completers =2	32	8	3	25	0
Total APB Requesters = 2 Total APB Completers =1	22	8	7	71	0
Total APB Requesters = 1 Total APB Completers =2	32	16	3	33	0
Total APB Requesters = 1 Total APB Completers =2	11	16	2	20	0
Total APB Requesters = 2 Total APB Completers =4	22	16	12	154	0
Total APB Requesters = 4 Total APB Completers =2	32	32	15	373	0

References

- [Arm](#) web page for the AMBA 3 APB Protocol Specification
- [APB Interconnect Module Release Notes \(FPGA-RN-02077\)](#)
- [Lattice Radiant Timing Constraints Methodology \(FPGA-AN-02059\)](#)
- [CrossLink-NX](#) web page
- [CertusPro-NX](#) web page
- [Certus-NX](#) web page
- [Certus-N2](#) web page
- [Mach-NX](#) web page
- [MachXO2](#) web page
- [MachXO3](#) web page
- [MachXO3D](#) web page
- [MachXO4](#) web page
- [MachXO5-NX](#) web page
- [iCE40 UltraPlus](#) web page
- [Avant-E](#) web page
- [Avant-G](#) web page
- [Avant-X](#) web page
- [Lattice Radiant Software](#) web page
- [Lattice Propel Design Environment](#) web page
- [Lattice Diamond Software](#) web page
- [Lattice Insights](#) for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Note: In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

Revision 1.5, IP v1.5.0, June 2026

Section	Change Summary
All	Performed minor formatting and editorial edits.
Acronyms in This Document	Updated list of acronyms.
Functional Description	<ul style="list-style-type: none"> Updated Table 2.2. Attributes Table4 as follows: <ul style="list-style-type: none"> Added a note for the <i>Main Settings Tab</i>. Updated the default value for the <i>S1 Base Address</i> attribute. Removed the <i>S31_FRAGMENT_CNT</i> attribute. Updated the default value for the <i>S31 Base Address</i> attribute. Updated <i>Completer 0 Settings Group</i> to <i>Completer Settings Group</i> under the <i>Requester Priority Settings Tab</i>. Updated selectable values, default value, and dependency for <i>Requester 0 Priority</i>, <i>Requester 1 Priority</i>, <i>Requester 2 Priority</i>, and <i>Requester 31 Priority</i> attributes. Removed attributes for <i>Completer 1 Settings Group</i> and <i>Completer 31 Settings Group</i>. Updated the notes for <i>Full Address Decoding up to 1kB</i> and <i>Registered Output</i> attributes. Updated Figure 2.2. APB Interconnect Module/IP Block Wizard. Updated Table 2.3. Attributes Description as follows: <ul style="list-style-type: none"> Updated the description for the <i>Full Address Decoding up to 1kB</i> attribute. Updated <i>Completer <N> Settings Group</i> to <i>Completer Settings Group</i> under the <i>Requester Priority Settings Tab</i>. Updated description of <i>Arbiter Scheme</i> and <i>Requester <M> Priority</i> attributes.
Design Considerations	Added this section.
Resource Utilization	<ul style="list-style-type: none"> Added a note on resource utilization values. Updated Table A.1. Resource Utilization Using the LAV-AT-X70ES-1LFG1156I Device and Table A.2. Resource Utilization Using the LFCPNX-100-8LFG672I Device.
References	Updated references.

Revision 1.4, IP v1.4.0, December 2025

Section	Change Summary
Introduction	Added MachXO4™ device in Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation.
Resource Utilization	Updated <i>Lattice Radiant software 2025.1</i> to <i>Lattice Radiant software</i> .
References	Updated references.
Revision History	Added note.

Revision 1.3, IP v1.3.0, June 2025

Section	Change Summary
All	<ul style="list-style-type: none"> Renamed document from <i>APB Interconnect Module - Lattice Propel Builder</i> to <i>APB Interconnect Module</i>. Changed instances of <i>Master</i> to <i>Requester</i> and <i>Slave</i> to <i>Completer</i>.
Disclaimers	Updated disclaimers.
Inclusive Language	Added inclusive language boilerplate.
Introduction	Updated Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation as follows: <ul style="list-style-type: none"> Added MachXO5-NX, Certus-N2, CertusPro-NX, Lattice Avant, and iCE40 UltraPlus

Section	Change Summary
	<p>devices.</p> <ul style="list-style-type: none"> Renamed <i>Supported FPGA Family</i> to <i>Supported Devices</i>.
Functional Description	<ul style="list-style-type: none"> Updated Table 2.2. Attributes Table4 as follows: <ul style="list-style-type: none"> Removed <i>Weighted Round Robin</i> option from the <i>Arbiter Scheme</i> attributes. Removed the note on the <i>Weighted Round Robin Arbiter Scheme</i>. Updated the following figures: <ul style="list-style-type: none"> Figure 2.2. APB Interconnect Module/IP Block Wizard Figure 2.3. Example of Single Requester Interconnect Application Figure 2.4. Example of Multi-Requester Interconnect Application Figure 2.5. Functional Block Diagram of Single Requester Interconnect Figure 2.8. Block Diagram of Multi-Requester Interconnect Figure 2.9. Block Diagram of APB Arbiter Mux
Resource Utilization	Added this section.
References	Updated references.
Technical Support Assistance	Added link to the Lattice Answer Database.

Revision 1.2, May 2021

Section	Change Summary
Introduction	Updated Table 1.1 to add MachXO2 and MachXO3 as supported FPGA family.
References	Updated content to add reference for MachXO2 and MachXO3.

Revision 1.1, December 2020

Section	Change Summary
Introduction	Modified second paragraph and added Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation.
Functional Description	Updated footnote markers in Table 2.2. Attributes Table. Removed footnote markers from Registered Output and Arbiter Scheme in Table 2.3. Attributes Description.
References	Updated this section.

Revision 1.0, May 2020

Section	Change Summary
All	Initial release.



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