# AHB-Lite Interconnect Module

IP Version: 1.6.0

# User Guide

FPGA-IPUG-02051-1.7

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# Acronyms in This Document

A list of acronyms used in this document.

| Acronym | Definition |
|---|---|
| AHB | Advanced High-performance Bus |
| AMBA | Advanced Microcontroller Bus Architecture |
| APB | Advanced Peripheral Bus |
| CPU | Central Processing Unit |
| DRC | Design Rule Check |
| EBR | Embedded Block Random Access Memory (RAM) |
| FPGA | Field Programmable Gate Array |
| HDL | Hardware Description Language |
| IP | Intellectual Property |
| LUT | Look-Up Table |
| Mux | Multiplexer |
| PCIe | Peripheral Component Interconnect Express |
| RTL | Register Transfer Level |

# 1. Introduction

This document provides technical information about the AHB-Lite Interconnect Module and aims to provide information essential for IP/system developers, verification, and software for integration, testing, and validation.

In general, this document covers design specification from RTL to IP packaging and details the procedures for IP generation and integration.

The design is implemented in Verilog HDL. The IP can be configured based on Table 1.1.

**Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation**

| Supported Devices | IP Configuration and Generation | IP Implementation (Synthesis, Map, Place and Route) |
|---|---|---|
| MachXO2™ | Lattice Propel™ Builder software | Lattice Diamond™ software |
| MachXO3™ | Lattice Propel Builder software | Lattice Diamond software |
| MachXO3D™ | Lattice Propel Builder software | Lattice Diamond software |
| Mach™-NX | Lattice Propel Builder software | Lattice Diamond software |
| MachXO4™ | Lattice Propel Builder software | Lattice Radiant™ software |
| MachXO5™-NX | Lattice Propel Builder software | Lattice Radiant software |
| CrossLink™-NX | Lattice Propel Builder software | Lattice Radiant software |
| Certus™-NX | Lattice Propel Builder software | Lattice Radiant software |
| Certus-N2 | Lattice Propel Builder software | Lattice Radiant software |
| CertusPro™-NX | Lattice Propel Builder software | Lattice Radiant software |
| Lattice Avant™ | Lattice Propel Builder software | Lattice Radiant software |
| iCE40 UltraPlus™ | Lattice Propel Builder software | Lattice Radiant software |

## 1.1. Features

The key features of the AHB-Lite Interconnect Module include:

- Compliance with AMBA 3 AHB-Lite protocol
- Fully parameterized design
- Data bus width of up to 1024 bits [8, 16, 32, 64, 128, 256, 512, 1024]
- Address width of up to 32-bits [11,12,...,32]
- Support of up to 32 managers and 32 subordinates
- Full or Sparse connection between managers and subordinates
- Subordinate port address decoding
- Support of fragmented address space of up to eight fragments per subordinate
- Subordinate side arbitration
- Selectable arbitration scheme:
  - Round robin
  - Fixed priority

# 2. Functional Description

## 2.1. Overview

The Lattice Semiconductor AHB-Lite Interconnect Module is a fully parameterized soft IP, high performance, low latency interconnect fabric for AMBA 3 AHB-Lite based systems, enabling one or more managers to be connected to one or more subordinates.

AHB-Lite, defined in the AMBA 3 protocol, is a subset of the full AHB specification for use in designs where only a single bus manager is used. AHB-Lite also does not include signals from the original AHB: request and grant. In addition, there is no support for a split or retry response. The only responses are okay or error.

AHB-Lite implements the features required for high-performance, high clock frequency systems including:

- Burst transfers: one address phase followed by multiple data phases, where each data phase is called a beat. 4/8/16-beat wrapping and incrementing bursts are supported. Incrementing bursts of undefined length are also supported.
- Single-clock edge operation.
- Non-tristate implementation.
- Wide data bus configurations: 64, 128, 256, 512, or 1024 bits wide.
  Note that the following data bus widths are also supported: 8, 16, 32 bits wide.

Refer to the AMBA 3 AHB-Lite Protocol Specification in the Arm web page for more information on the protocol.

Even though AHB-Lite is a single-manager bus protocol, the AHB-Lite Interconnect Module enables the connection of multiple managers to one or more subordinates by implementing multi-layer interconnect. Each manager is considered to be on its own layer and isolated from each other, but can share access to the subordinates. Each manager can access different subordinates in parallel. When more than one manager tries to access the same subordinate, subordinate-side arbitration is performed by the multi-layer interconnect.

## 2.2. Signal Description

Figure 2.1 shows the interface diagram for the AHB-Lite Interconnect Module. The diagram shows all available ports for the IP core.

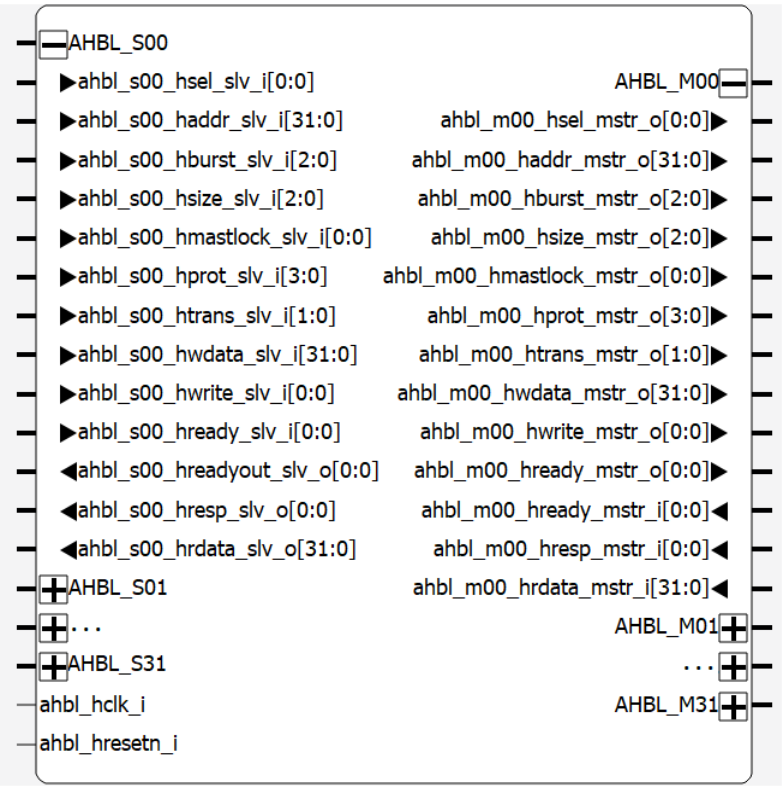


**Figure 2.1. AHB-Lite Interconnect Module Interface Diagram**

**Table 2.1. AHB-Lite Interconnect Module Signal Description**

| Pin Name | Direction | Width (Bits) | Description |
|---|---|---|---|
| **Clock and Reset** | | | |
| ahbl_hclk_i | In | 1 | AHB-Lite clock. |
| ahbl_hresetn_i | In | 1 | AHB-Lite active LOW reset. |
| **AHB-Lite Subordinate Interface 00 (AHBL_M00)** | | | |
| ahbl_m00_hsel_mstr_o | Out | 1 | Subordinate select. |
| ahbl_m00_haddr_mstr_o | Out | M_ADDR_WIDTH | Address. |
| ahbl_m00_hburst_mstr_o | Out | 3 | Burst type (SINGLE, INCR, INCR4/8/16). |
| ahbl_m00_hsize_mstr_o | Out | 3 | Transfer size (8/16/32/64/128/256/512/1024). |
| ahbl_m00_hmastlock_mstr_o | Out | 1 | Current transfer is part of a locked transfer. |
| ahbl_m00_hprot_mstr_o | Out | 4 | Protection control. |
| ahbl_m00_htrans_mstr_o | Out | 2 | Transfer type of the current transfer (IDLE/BUSY/NSEQ/SEQ). |
| ahbl_m00_hwdata_mstr_o | Out | DATA_WIDTH | Write data bus. |
| ahbl_m00_hwrite_mstr_o | Out | 1 | Write = 1, Read = 0. |
| ahbl_m00_hready_mstr_o | Out | 1 | Indicates transfer completion. |
| ahbl_m00_hready_mstr_i | In | 1 | Indicates transfer completion. This signal is driven LOW by the subordinate to extend the transfer. |
| ahbl_m00_hresp_mstr_i | In | 1 | Subordinate response (OKAY/ERROR). |
| ahbl_m00_hrdata_mstr_i | In | DATA_WIDTH | Read data bus. |

| Pin Name | Direction | Width (Bits) | Description |
|---|---|---|---|
| **AHB-Lite Subordinate Interface 01 (AHBL_M01)** | | | |
| ahbl_m01_hsel_mstr_o | Out | 1 | Subordinate select. |
| ahbl_m01_haddr_mstr_o | Out | M_ADDR_WIDTH | Address. |
| ahbl_m01_hburst_mstr_o | Out | 3 | Burst type (SINGLE, INCR, INCR4/8/16). |
| ahbl_m01_hsize_mstr_o | Out | 3 | Transfer size (8/16/32/64/128/256/512/1024). |
| ahbl_m01_hmastlock_mstr_o | Out | 1 | Current transfer is part of a locked transfer. |
| ahbl_m01_hprot_mstr_o | Out | 4 | Protection control. |
| ahbl_m01_htrans_mstr_o | Out | 2 | Transfer type of the current transfer (IDLE/BUSY/NSEQ/SEQ). |
| ahbl_m01_hwdata_mstr_o | Out | DATA_WIDTH | Write data bus. |
| ahbl_m01_hwrite_mstr_o | Out | 1 | Write = 1, Read = 0. |
| ahbl_m01_hready_mstr_o | Out | 1 | Indicates transfer completion. |
| ahbl_m01_hready_mstr_i | In | 1 | Indicates transfer completion. This signal is driven LOW by the subordinate to extend the transfer. |
| ahbl_m01_hresp_mstr_i | In | 1 | Subordinate response (OKAY/ERROR). |
| ahbl_m01_hrdata_mstr_i | In | DATA_WIDTH | Read data bus. |
| … | — | — | — |
| **AHB-Lite Subordinate Interface xx (AHBL_Mxx)** | | | |
| ahbl_mxx_hsel_mstr_o | Out | 1 | Subordinate select. |
| ahbl_mxx_haddr_mstr_o | Out | M_ADDR_WIDTH | Address. |
| ahbl_mxx_hburst_mstr_o | Out | 3 | Burst type (SINGLE, INCR, INCR4/8/16). |
| ahbl_mxx_hsize_mstr_o | Out | 3 | Transfer size (8/16/32/64/128/256/512/1024). |
| ahbl_mxx_hmastlock_mstr_o | Out | 1 | Current transfer is part of a locked transfer. |
| ahbl_mxx_hprot_mstr_o | Out | 4 | Protection control. |
| ahbl_mxx_htrans_mstr_o | Out | 2 | Transfer type of the current transfer (IDLE/BUSY/NSEQ/SEQ). |
| ahbl_mxx_hwdata_mstr_o | Out | DATA_WIDTH | Write data bus. |
| ahbl_mxx_hwrite_mstr_o | Out | 1 | Write = 1, Read = 0. |
| ahbl_mxx_hready_mstr_o | Out | 1 | Indicates transfer completion. |
| ahbl_mxx_hready_mstr_i | In | 1 | Indicates transfer completion. This signal is driven LOW by the subordinate to extend the transfer. |
| ahbl_mxx_hresp_mstr_i | In | 1 | Subordinate response (OKAY/ERROR). |
| ahbl_mxx_hrdata_mstr_i | In | DATA_WIDTH | Read data bus. |
| **AHB-Lite Manager Interface 00 (AHBL_S00)** | | | |
| ahbl_s00_hsel_slv_i | In | 1 | Subordinate select. |
| ahbl_s00_haddr_slv_i | In | M_ADDR_WIDTH | Address. |
| ahbl_s00_hburst_slv_i | In | 3 | Burst type (SINGLE, INCR, INCR4/8/16). |
| ahbl_s00_hsize_slv_i | In | 3 | Transfer size (8/16/32/64/128/256/512/1024). |
| ahbl_s00_hmastlock_slv_i | In | 1 | Current transfer is part of a locked transfer. |
| ahbl_s00_hprot_slv_i | In | 4 | Protection control. |
| ahbl_s00_htrans_slv_i | In | 2 | Transfer type of the current transfer (IDLE/BUSY/NSEQ/SEQ). |
| ahbl_s00_hwdata_slv_i | In | DATA_WIDTH | Write data bus. |
| ahbl_s00_hwrite_slv_i | In | 1 | Write = 1, Read = 0. |
| ahbl_s00_hready_slv_i | In | 1 | Indicates transfer completion. |
| ahbl_s00_hreadyout_slv_o | Out | 1 | Indicates transfer completion. This signal is driven LOW by the subordinate to extend the transfer. |
| ahbl_s00_hresp_slv_o | Out | 1 | Subordinate response (OKAY/ERROR). |
| ahbl_s00_hrdata_slv_o | Out | DATA_WIDTH | Read data bus. |
| **AHB-Lite Manager Interface 01 (AHBL_S01)** | | | |
| ahbl_s01_hsel_slv_i | In | 1 | Subordinate select. |

| Pin Name | Direction | Width (Bits) | Description |
|---|---|---|---|
| ahbl_s01_haddr_slv_i | In | M_ADDR_WIDTH | Address. |
| ahbl_s01_hburst_slv_i | In | 3 | Burst type (SINGLE, INCR, INCR4/8/16). |
| ahbl_s01_hsize_slv_i | In | 3 | Transfer size (8/16/32/64/128/256/512/1024). |
| ahbl_s01_hmastlock_slv_i | In | 1 | Current transfer is part of a locked transfer. |
| ahbl_s01_hprot_slv_i | In | 4 | Protection control. |
| ahbl_s01_htrans_slv_i | In | 2 | Transfer type of the current transfer (IDLE/BUSY/NSEQ/SEQ). |
| ahbl_s01_hwdata_slv_i | In | DATA_WIDTH | Write data bus. |
| ahbl_s01_hwrite_slv_i | In | 1 | Write = 1, Read = 0. |
| ahbl_s01_hready_slv_i | In | 1 | Indicates transfer completion. |
| ahbl_s01_hreadyout_slv_o | Out | 1 | Indicates transfer completion. This signal is driven LOW by the subordinate to extend the transfer. |
| ahbl_s01_hresp_slv_o | Out | 1 | Subordinate response (OKAY/ERROR). |
| ahbl_s01_hrdata_slv_o | Out | DATA_WIDTH | Read data bus. |
| … | — | — | — |
| **AHB-Lite Manager Interface yy (AHBL_Syy)** | | | |
| ahbl_syy_hsel_slv_i | In | 1 | Subordinate select. |
| ahbl_syy_haddr_slv_i | In | M_ADDR_WIDTH | Address. |
| ahbl_syy_hburst_slv_i | In | 3 | Burst type (SINGLE, INCR, INCR4/8/16). |
| ahbl_syy_hsize_slv_i | In | 3 | Transfer size (8/16/32/64/128/256/512/1024). |
| ahbl_syy_hmastlock_slv_i | In | 1 | Current transfer is part of a locked transfer. |
| ahbl_syy_hprot_slv_i | In | 4 | Protection control. |
| ahbl_syy_htrans_slv_i | In | 2 | Transfer type of the current transfer (IDLE/BUSY/NSEQ/SEQ). |
| ahbl_syy_hwdata_slv_i | In | DATA_WIDTH | Write data bus. |
| ahbl_syy_hwrite_slv_i | In | 1 | Write = 1, Read = 0. |
| ahbl_syy_hready_slv_i | In | 1 | Indicates transfer completion. |
| ahbl_syy_hreadyout_slv_o | Out | 1 | Indicates transfer completion. This signal is driven LOW by the subordinate to extend the transfer. |
| ahbl_syy_hresp_slv_o | Out | 1 | Subordinate response (OKAY/ERROR). |
| ahbl_syy_hrdata_slv_o | Out | DATA_WIDTH | Read data bus. |

**Notes:**

1. xx – Possible values are (02, 03,…, *Total AHB-Lite Subordinates* -1).
2. yy – Possible values are (02, 03,…, *Total AHB-Lite Managers* -1).
3. All AHB-Lite Manager/Subordinate Interface are compliant with AHB-Lite protocol. Refer to the AMBA 3 AHB-Lite Protocol Specification in the Arm web page for the timing diagrams and for more information on the protocol.

## 2.3. Attributes Summary

Table 2.2 provides the list of user-configurable attributes for the AHB-Lite Interconnect Module. The attribute values are specified using the IP core Configuration user interface in the Propel Builder software as shown in Table 2.2.

**Table 2.2. Attributes Table**

| Attribute | Selectable Values | Default | Dependency on Other Attributes[3] |
|---|---|---|---|
| **General Tab** | | | |
| **General Group** | | | |
| Total AHB-Lite Managers | 1–32 | 2 | *Total AHB-Lite Managers* and *Total AHB-Lite Subordinates* cannot be both 1 |
| Total AHB-Lite Subordinates | 1–32 | 2 | |
| Manager Address Width(bits) (M_ADDR_WIDTH) | 11–32 | 32 | — |
| Full Address Decoding up to 1kB[1] | Checked, Unchecked | Checked | — |
| Data Bus Width(bits) (DATA_WIDTH) | 8, 16, 32, 64, 128, 256, 512, 1024 | 32 | — |
| Registered Output[2] | Checked, Unchecked | Unchecked | — |
| **Manager 0 Connection Setting Group** | | | |
| Manager 0 Subordinate 0 Connect Enable | Checked, Unchecked | Checked | en_m0 and en_s0 |
| Manager 0 Subordinate 1 Connect Enable | Checked, Unchecked | Checked | en_m0 and en_s1 |
| … | — | — | — |
| Manager 0 Subordinate 31 Connect Enable | Checked, Unchecked | Checked | en_m0 and en_s31 |
| **Manager 1 Connection Setting Group** | | | |
| Manager 1 Subordinate 0 Connect Enable | Checked, Unchecked | Checked | en_m1 and en_s0 |
| Manager 1 Subordinate 1 Connect Enable | Checked, Unchecked | Checked | en_m1 and en_s1 |
| … | — | — | — |
| Manager 1 Subordinate 31 Connect Enable | Checked, Unchecked | Checked | en_m1 and en_s31 |
| … | | | |
| **Manager 31 Connection Setting Group** | | | |
| Manager 31 Subordinate 0 Connect Enable | Checked, Unchecked | Checked | en_m31 and en_s0 |
| Manager 31 Subordinate 1 Connect Enable | Checked, Unchecked | Checked | en_m31 and en_s1 |
| … | — | — | — |
| Manager 31 Subordinate 31 Connect Enable | Checked, Unchecked | Checked | en_m31 and en_s31 |
| **Main Settings Tab** | | | |
| **Subordinate 0 Settings Group** | | | |
| S0_FRAGMENT_CNT | 1–8 | 1 | en_s0 |
| Base Address 0 | 0–($2^{M\_ADDR\_WIDTH}$ – 'h400) | 32'h00000000 | en_s0 and (*S0_FRAGMENT_CNT* > 0) |
| Base Address 1 | 0–($2^{M\_ADDR\_WIDTH}$ – 'h400) | 32'h00000400 | en_s0 and (*S0_FRAGMENT_CNT* > 1) |
| … | — | — | — |
| Base Address 7 | 0–($2^{M\_ADDR\_WIDTH}$ – 'h400) | 32'h00001C00 | en_s0 and (*S0_FRAGMENT_CNT* > 7) |
| Address Range 0 | 'h400–$2^{M\_ADDR\_WIDTH}$ | 32'h00000400 | en_s0 and (*S0_FRAGMENT_CNT* > 0) |
| Address Range 1 | 'h400–$2^{M\_ADDR\_WIDTH}$ | 32'h00000400 | en_s0 and (*S0_FRAGMENT_CNT* > 1) |

| Attribute | Selectable Values | Default | Dependency on Other Attributes[3] |
|---|---|---|---|
| … | — | — | — |
| Address Range 7 | 'h400–$2^{M\_ADDR\_WIDTH}$ | 32'h00000400 | en_s0 and (*S0_FRAGMENT_CNT* > 7) |
| **Subordinate 1 Settings Group** | | | |
| S1_FRAGMENT_CNT | 1–8 | 1 | en_s1 |
| Base Address 0 | 0–($2^{M\_ADDR\_WIDTH}$ – 'h400) | 32'h00002000 | en_s1 and (*S1_FRAGMENT_CNT* > 0) |
| Base Address 1 | 0–($2^{M\_ADDR\_WIDTH}$ – 'h400) | 32'h00002400 | en_s1 and (*S1_FRAGMENT_CNT* > 1) |
| … | — | — | — |
| Base Address 7 | 0–($2^{M\_ADDR\_WIDTH}$ – 'h400) | 32'h00003C00 | en_s1 and (*S1_FRAGMENT_CNT* > 7) |
| Address Range 0 | 'h400–$2^{M\_ADDR\_WIDTH}$ | 32'h00000400 | en_s1 and (*S1_FRAGMENT_CNT* > 0) |
| Address Range 1 | 'h400–$2^{M\_ADDR\_WIDTH}$ | 32'h00000400 | en_s1 and (*S1_FRAGMENT_CNT* > 1) |
| … | — | — | — |
| Address Range 7 | 'h400–$2^{M\_ADDR\_WIDTH}$ | 32'h00000400 | en_s1 and (*S1_FRAGMENT_CNT* > 7) |
| … | | | |
| **Subordinate 31 Settings Group** | | | |
| S31_FRAGMENT_CNT | 1–8 | 1 | en_s31 |
| Base Address 0 | 0–($2^{M\_ADDR\_WIDTH}$ – 'h400) | 32'h0003E000 | en_s31 and (*S31_FRAGMENT_CNT* > 0) |
| Base Address 1 | 0–($2^{M\_ADDR\_WIDTH}$ – 'h400) | 32'h0003E400 | en_s31 and (*S31_FRAGMENT_CNT* > 1) |
| … | — | — | — |
| Base Address 7 | 0–($2^{M\_ADDR\_WIDTH}$ – 'h400) | 32'h0003FC00 | en_s31 and (*S31_FRAGMENT_CNT* > 7) |
| Address Range 0 | 'h400–$2^{M\_ADDR\_WIDTH}$ | 32'h00000400 | en_s31 and (*S31_FRAGMENT_CNT* > 0) |
| Address Range 1 | 'h400–$2^{M\_ADDR\_WIDTH}$ | 32'h00000400 | en_s31 and (*S31_FRAGMENT_CNT* > 1) |
| … | — | — | — |
| Address Range 7 | 'h400–$2^{M\_ADDR\_WIDTH}$ | 32'h00000400 | en_s31 and (*S31_FRAGMENT_CNT* > 7) |
| **Manager Priority Settings Tab** | | | |
| **Subordinate 0 Settings Group** | | | |
| Arbiter Scheme | Round Robin, Fixed Priority | Round Robin | en_s0 |
| Manager 0 Priority | 0–31 | 0 | en_s0 and en_m0 and (*Arbiter Scheme* == Fixed Priority) |
| Manager 1 Priority | 0–31 | 1 | en_s0 and en_m1 and (*Arbiter Scheme* == Fixed Priority) |
| Manager 2 Priority | 0–31 | 2 | en_s0 and en_m2 and (*Arbiter Scheme* == Fixed Priority) |
| … | — | — | — |
| Manager 31 Priority | 0–31 | 31 | en_s0 and en_m31 and (*Arbiter Scheme* == Fixed Priority) |
| **Subordinate 1 Settings Group** | | | |
| Arbiter Scheme | Round Robin, Fixed Priority | Round Robin | en_s1 |
| Manager 0 Priority | 0–31 | 0 | en_s1 and en_m0 and (*Arbiter Scheme* == Fixed Priority) |
| Manager 1 Priority | 0–31 | 1 | en_s1 and en_m1 and (*Arbiter Scheme* == Fixed Priority) |
| Manager 2 Priority | 0–31 | 2 | en_s1 and en_m2 and (*Arbiter Scheme* == Fixed Priority) |
| … | — | — | — |
| Manager 31 Priority | 0–31 | 31 | en_s1 and en_m31 and (*Arbiter Scheme* == Fixed Priority) |
| … | — | — | — |

| Attribute | Selectable Values | Default | Dependency on Other Attributes[3] |
|---|---|---|---|
| **Subordinate 31 Settings Group** | | | |
| Arbiter Scheme | Round Robin, Fixed Priority | Round Robin | en_s31 |
| Manager 0 Priority | 0–31 | 0 | en_s31 and en_m0 and (*Arbiter Scheme* == Fixed Priority) |
| Manager 1 Priority | 0–31 | 1 | en_s31 and en_m1 and (*Arbiter Scheme* == Fixed Priority) |
| Manager 2 Priority | 0–31 | 2 | en_s31 and en_m2 and (*Arbiter Scheme* == Fixed Priority) |
| … | — | — | — |
| Manager 31 Priority | 0–31 | 31 | en_s31 and en_m31 and (*Arbiter Scheme* == Fixed Priority) |
| **Max Burst Size Settings Tab[4]** | | | |
| **Max Burst Size Subordinate Settings** | | | |
| Subordinate 0 Max Burst Size | 0, 32, 64, 128, 256 | 0 | en_s0 |
| Subordinate 1 Max Burst Size | 0, 32, 64, 128, 256 | 0 | en_s1 |
| … | — | — | — |
| Subordinate 31 Max Burst Size | 0, 32, 64, 128, 256 | 0 | en_s31 |

**Notes:**

1. [*Full Address Decoding up to 1kB* = Unchecked] is currently not supported.
2. [*Registered Output* = Checked] is currently not supported.
3. To simplify the condition, en_s0, en_s1 to en_s31 are used for the condition that the corresponding connection to external subordinate is enabled. Similarly, en_m0, en_m1, en_m2 and en_m31 are used for the condition that the corresponding connection to external manager is enabled.
4. The **Max Burst Size Setting Tab** is not displayed and not supported if *Total AHB-Lite Managers* is 1. Refer to the Subordinate Max Burst Size in Single-Manager Multi-Subordinate Configurations section for more details.

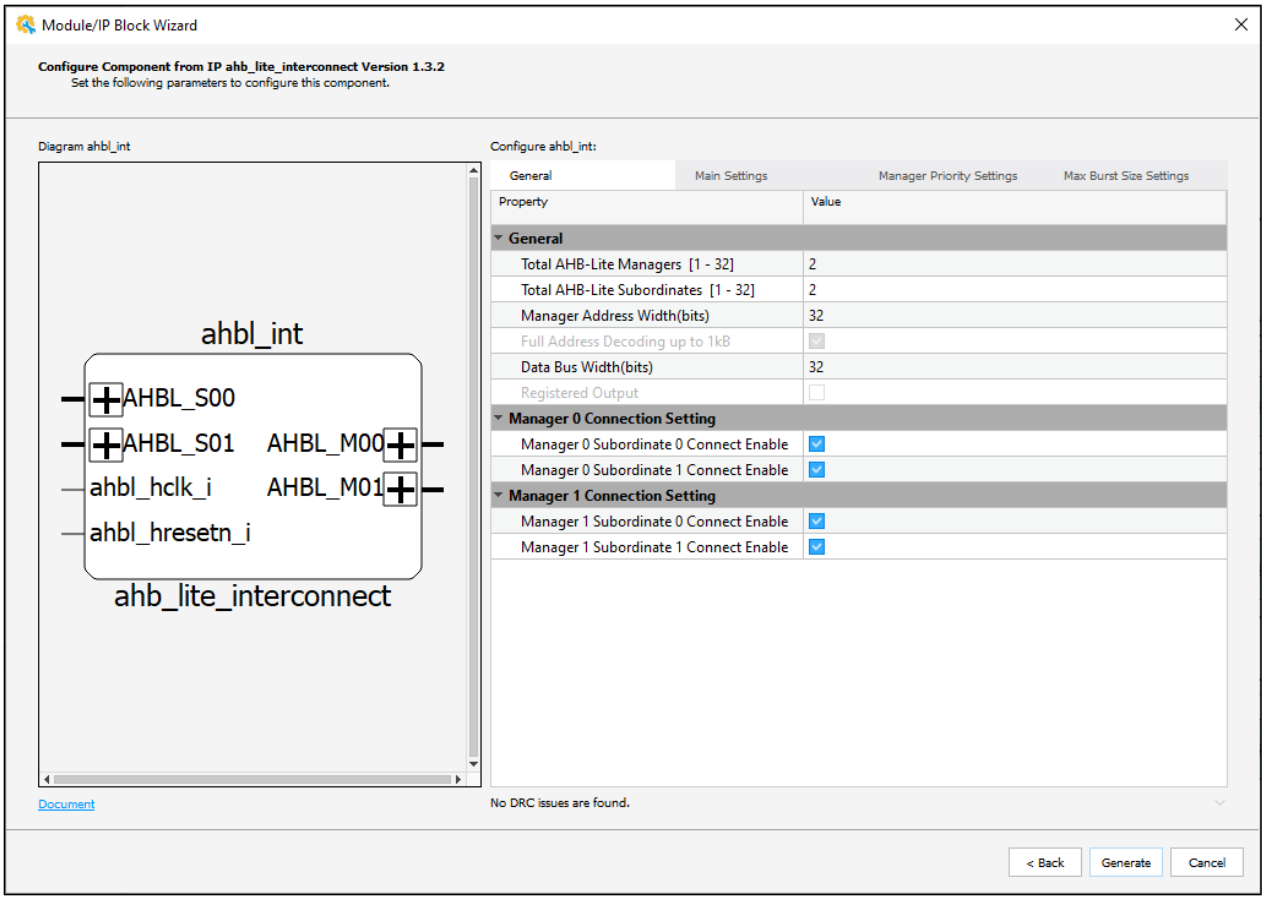


**Figure 2.2. AHB-Lite Interconnect Module Configuration User Interface**

**Table 2.3. Attributes Description**

| Attribute | Description |
|---|---|
| **General Tab** | |
| **General Group** | |
| Total AHB-Lite Managers | Specifies the number of AHB-Lite managers that are connected to this module. |
| Total AHB-Lite Subordinates | Specifies the number of AHB-Lite subordinates that are connected to this module. |
| Manager Address Width(bits) (M_ADDR_WIDTH) | Specifies the bit width of all the HADDR signals. |
| Data Bus Width(bits) (DATA_WIDTH) | Specifies the bit with of all the HWDATA and HRDATA signals. |
| Registered Output | Unchecked – Output register is disabled (bypassed).<br>Checked – Output register is enabled. This option is currently not supported. |
| **Manager <M> Connection Setting Group** | |
| Manager <M> Subordinate <N> Connect Enable | Unchecked – AHB-Lite Manager <M> can access the AHB-Lite Subordinate <N> and corresponding logic is not generated.<br>Checked – AHB-Lite Manager <M> can access the AHB-Lite Subordinate <N>. |
| **Main Settings Tab** | |
| **Subordinate <N> Settings Group** | |
| S<N>_FRAGMENT_CNT | Specifies the number of fragments in AHB-Lite subordinate <N>.<br>Each fragment has its own base address and range boundary, wherein:<br>• Start Address = Base Address<br>• End Address = Base Address + Address Range – 1 |

| Attribute | Description |
|---|---|
| Base Address <F> | Specifies base address for AHB-Lite subordinate <N> – fragment <F>.<br>If [*Full Address Decoding up to 1kB* = Checked]: Must be aligned to 1 kB.<br>If [*Full Address Decoding up to 1kB* = Unchecked]: Must be aligned to (or multiple of) the value of Address Range rounded up to power of 2. |
| Address Range <F> | Specifies number of bytes allocated for AHB-Lite subordinate <N> – fragment <F>.<br>If [*Full Address Decoding up to 1kB* = Checked]: The value must be multiple of 1 kB.<br>If [*Full Address Decoding up to 1kB* = Unchecked]: The value must be power of 2. |
| **Manager Priority Settings Tab** | |
| **Subordinate <N> Settings Group** | |
| Arbiter Scheme | Specifies the arbitration scheme to be implemented for AHB-Lite subordinate <N>. |
| Manager <M> Priority | Specifies priority index of AHB-Lite Manager <M> to access AHB-Lite subordinate <N>.<br>[0]: Highest priority<br>…<br>[31]: Lowest priority |
| **Max Burst Size Settings Tab** | |
| **Max Burst Size Subordinate Settings Group** | |
| Subordinate <N> Max Burst Size | Specifies the maximum burst size for the AHB-Lite subordinate <N> before the Interconnect sends an error response to the manager. This prevents a manager from hogging the bus by generating very long bursts. If this is set to 0, it means the feature is disabled and the corresponding logic is not generated.<br>This feature is hidden and not supported if *Total AHB-Lite Managers* is 1. Refer to the Subordinate Max Burst Size in Single-Manager Multi-Subordinate Configurations section for more details. |

**Notes:**

1. <M> - Manager index [0,1,…,(*Total AHB-Lite Managers*)-1]
2. <N> - Subordinate index [0,1,…,(*Total AHB-Lite Subordinates*)-1]
3. For *Address Range <F>* DRC of the Module/IP Block Wizard flags an error when range is not power of 2. If your target range is not power of 2, you should select the next power of 2 value.

## 2.4. Use Models

The AHB-Lite Interconnect Module connects one or more AHB-Lite manager devices to one or more AHB-Lite subordinate devices. Each connected AHB-Lite manager device could either be:

- A device that originates AHB-lite transactions (endpoint manager) or
- A manager interface of an upstream AHB-Lite Interconnect core being cascaded

Similarly, each connected AHB-Lite subordinate device could either be:

- The final target of AHB-Lite transactions (endpoint subordinate) or
- A subordinate interface of a downstream AHB-Lite Interconnect core being cascaded

In general, AHB-Lite Interconnect Module can be configured for the following connectivity patterns:

- Single Manager Interconnect – refer to the Single Manager Interconnect section.
- Multi-Manager Interconnect – refer to the Multi-Manager Interconnect section.

An example of Single Manager Interconnect application is shown in Figure 2.3. The arrows in the figure are AHB-Lite interface connections, where *M* stands for an AHB-Lite manager port, and *S* stands for an AHB-Lite subordinate port. In this example, the Instruction port of the CPU is directly connected to one port of Dual Port Memory while the Data port of the CPU is connected to the subordinate port of Single Manager Interconnect. This connection allows parallel instruction fetch and data access execution. The manager ports of Single Manager Interconnect are connected to one port of Dual Port Memory, Accelerator, AHB-Lite to APB Bridge, and System Memory. This allows the CPU Data port to access the said subordinates. The APB subordinates connected to AHB-Lite to APB Bridge are not shown in this diagram.

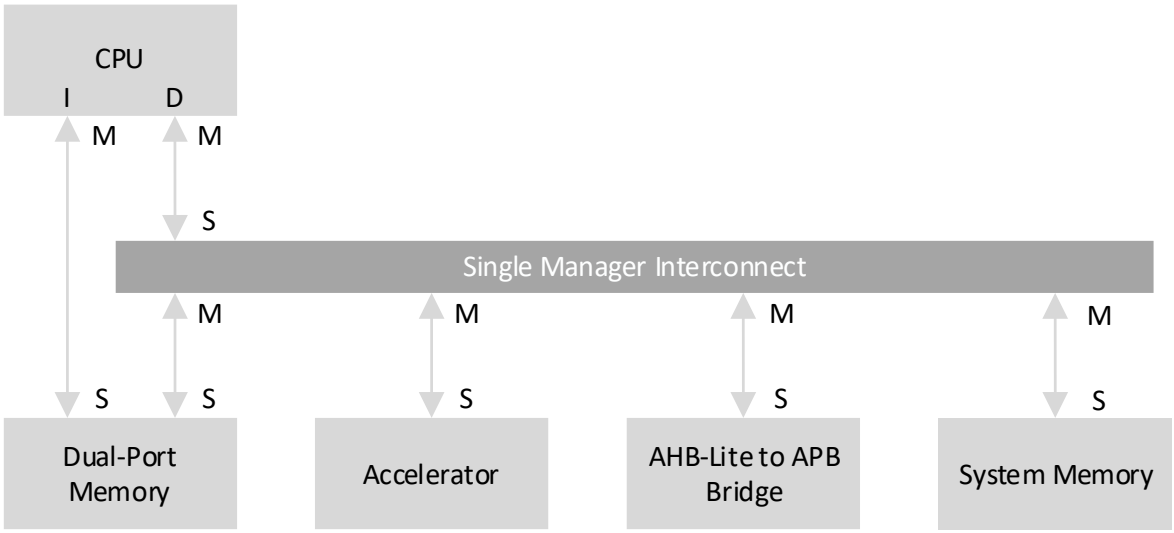


**Figure 2.3. Example of Single Manager Interconnect Application**

An example of Multi-Manager Interconnect application is shown in Figure 2.4. This is similar to Figure 2.3 with the addition of PCIe. In this example, PCIe is configured to have one AHB-Lite manager port for reading and writing data to the System Memory and one AHB-Lite subordinate port for register access by the CPU. The Multi-Manager Interconnect can be configured to remove the connection from PCIe M0 to other subordinates, thus, saving resources and improving Fmax.

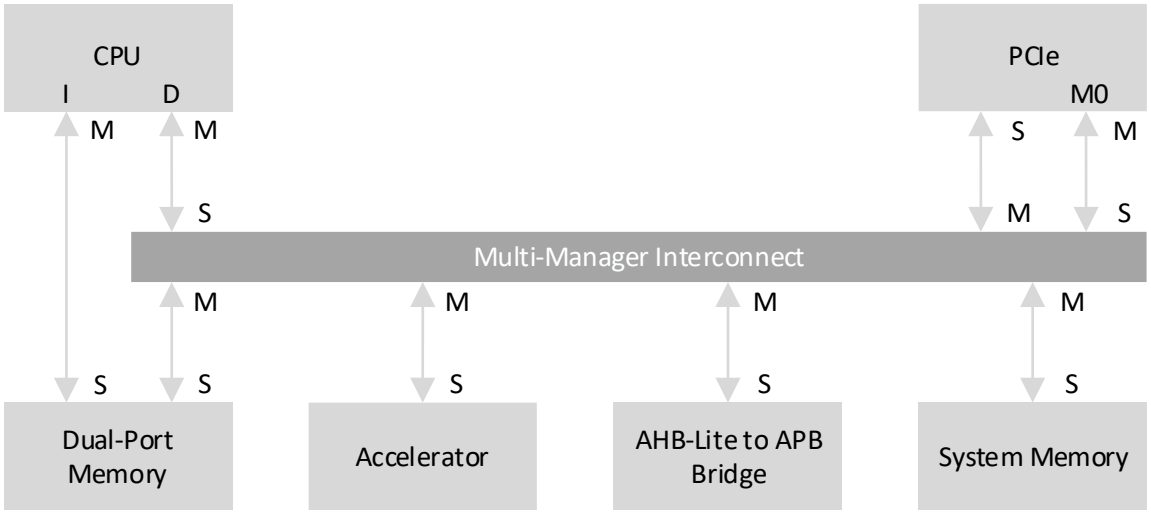


**Figure 2.4. Example of Multi-Manager Interconnect Application**

### 2.4.1. Single Manager Interconnect

For single manager to multiple subordinate configuration, Lattice Semiconductor AHB-Lite Interconnect Module behavior is based on the *Bus Interconnection* section of the AMBA 3 AHB-Lite Protocol Specification in the Arm web page. The bus interconnect logic is encapsulated inside the Soft IP, which consists of an address decoder, a subordinate-to-manager multiplexer and a default subordinate. This is shown in Figure 2.5.

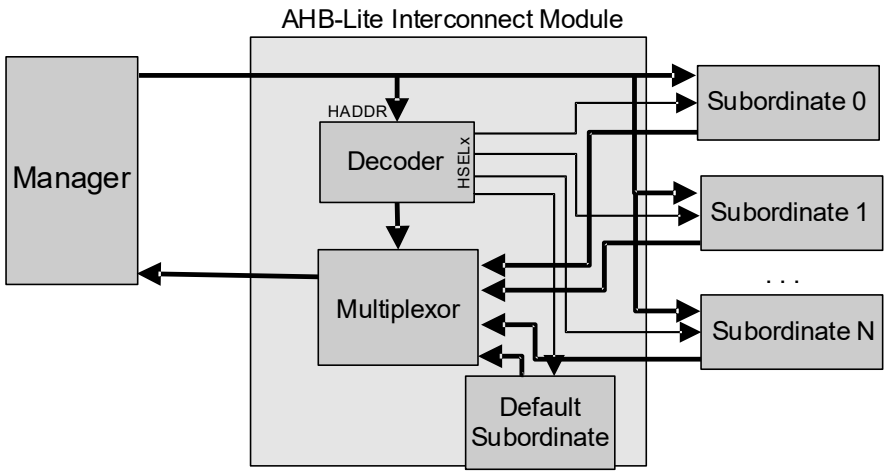


**Figure 2.5. Functional Block Diagram of Single Manager Interconnect**

#### 2.4.1.1. Decoder

The Decoder IP component performs address decoding for each bus transfer and provides a select signal for each subordinate on the bus. Decoding is done by comparing the appropriate address bits with the user-provided memory-map (*Base Address <F>* and *Address Range <F>*) settings and manager connect enable settings during configuration. This is shown in Figure 2.6. The memory map is static setting; it cannot be changed during operation. During a bus transfer, the select signal goes high for a single subordinate involved in the transfer. The decoder also provides control signals to the multiplexor. The manager connect enable settings are mainly used for Multi-Manager Interconnect.

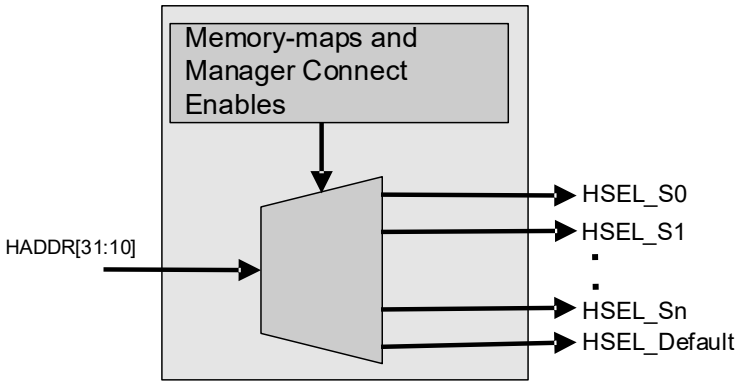


**Figure 2.6. Block Diagram of AHB-Lite Decoder**

According to the AMBA 3 AHB-Lite Specifications, the minimum address space that can be allocated to a single subordinate is 1 kB. When configuring the IP, subordinate Address Range attribute value must be greater than or equal to 1 kB. All managers are designed so that they do not perform incrementing transfers over a 1 kB address boundary. This ensures that a burst never crosses an address decode boundary and that only one subordinate is accessed by the manager during a burst transfer.

The HSEL signal is a combinatorial decode of the high-order address signals. This is done by comparing the higher bits of the address signal with the *Base Address <F>* and *Address Range <F>* settings. The behavior of decoder is controlled by the *Full Address Decoding up to 1 kB* attribute as follows:

- [*Full Address Decoding up to 1kB* is Checked]: HSEL signal asserts if the following conditions are met:
  - ahbl_sxx_haddr_slv_i[*M_ADDR_WIDTH* – 1:10] >= *Base Address <F>*[*M_ADDR_WIDTH* – 1:10]
  - ahbl_sxx_haddr_slv_i[*M_ADDR_WIDTH* – 1:10] <= (Max Address <F>)[*M_ADDR_WIDTH* – 1:10]
    Wherein Max Address <F> = *Base Address <F>* + *Address Range <F>*
- [*Full Address Decoding up to 1kB* is Unchecked]: HSEL signal asserts if the following condition is met:
  - ahbl_sxx_haddr_slv_i[*M_ADDR_WIDTH* – 1:XBIT] == *Base Address <F>*[*M_ADDR_WIDTH* – 1: XBIT]
    Wherein XBIT = Round_up($\log_2$(*Address Range <F>*))

When *Full Address Decoding up to 1kB* is Unchecked, the *Address Range <F>* is not in used in comparison because it is in power of 2 value. Thus, the behavior of the interconnect is undefined if this attribute is not power of 2 value.

The user-defined memory maps of the subordinates are parameters to the decoder IP and are used to select the appropriate subordinate. If a system design does not contain a completely filled memory map, then a default subordinate is selected when a transfer is attempted to a nonexistent address location.

#### 2.4.1.2. Default Subordinate

When a transfer is attempted to an address that does not map to a subordinate, the default subordinate provides a response based on the transfer type (HTRANS) as follows:

- NONSEQUENTIAL or SEQUENTIAL (single or burst transfer) – ERROR response
- IDLE or BUSY (manager is not providing data) – Zero wait state OKAY response

#### 2.4.1.3. Multiplexor

A subordinate-to-manager multiplexor is required to select the HRDATA, HREADY, and HRESP signals from the subordinates to the manager as shown in Figure 2.7. The decoder provides the multiplexor with the HSELx signals to enable the multiplexor to route the appropriate signals from the selected subordinate to the manager. AHB-Lite has an address phase followed by one or more data phases. Therefore, the select signals should be flopped to align with the data phase(s). The registers shown below sample the HSEL signals. They should be updated when HREADY is asserted, indicating that the current transfer is complete.

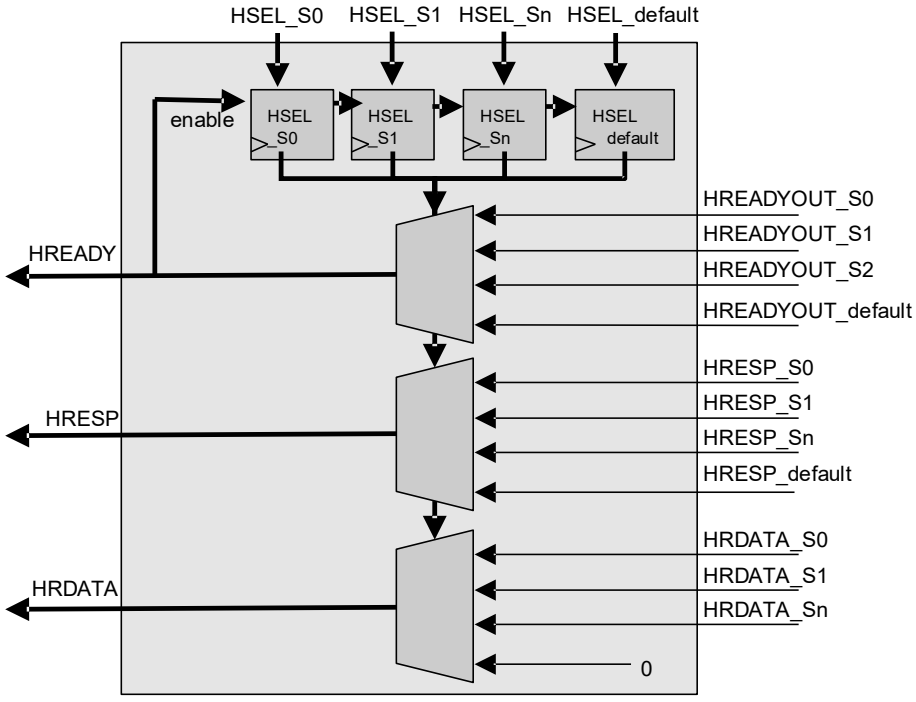


**Figure 2.7. Block Diagram of AHB-Lite Multiplexor**

### 2.4.2. Multi-Manager Interconnect

The Lattice Semiconductor AHB-Lite Interconnect Module implements multi-layer AHB-Lite Interconnect Matrix. Each manager is considered in its own layer and is isolated from other managers. The Multi-Manager Interconnect allows non-contending transactions (between disjoint managers and subordinates) to proceed concurrently. When multiple managers access the same subordinate, arbitration occurs and the interconnect matrix negates the HREADY to the managers that were not given access to the subordinate. Arbitration is the process of changing the grant from one manager to another. The arbitration process has one wait cycle (HREADY is negated) penalty. If only the granted manager access the subordinate for a given time, no arbitration occurs. However, if another not granted manager access the subordinate, arbitration occurs to change the grant to that manager even if no other manager is accessing the same subordinate.

The Multi-Manager Interconnect implements subordinate-side arbitration. Thus, multiple arbitration can occur in parallel if there are contentions in accessing multiple subordinates at the same time. You can specify a different arbitration scheme for each subordinate, which is used to select a manager during bus contention. Currently, there are two arbitration scheme options:

- Round-robin (default) – Each manager is serviced in round-robin manner, giving each manager equal access to the subordinate.
- Fixed priority – High priority managers are always given access to the subordinate in preference over lower priority managers.

By default, all managers are connected to all subordinates. However, this is a waste of resource if at least one manager never accesses at least one subordinate in the target application. An example of this is shown in Figure 2.8. The interconnect optimizes this by implementing configurable manager to subordinate connection which is controlled by the *Manager <M> Connection Setting* attributes. When specific manager to subordinate connection is disabled, corresponding logic is not generated; thus, improving resource utilization and Fmax (fan-out of select signals are reduced).

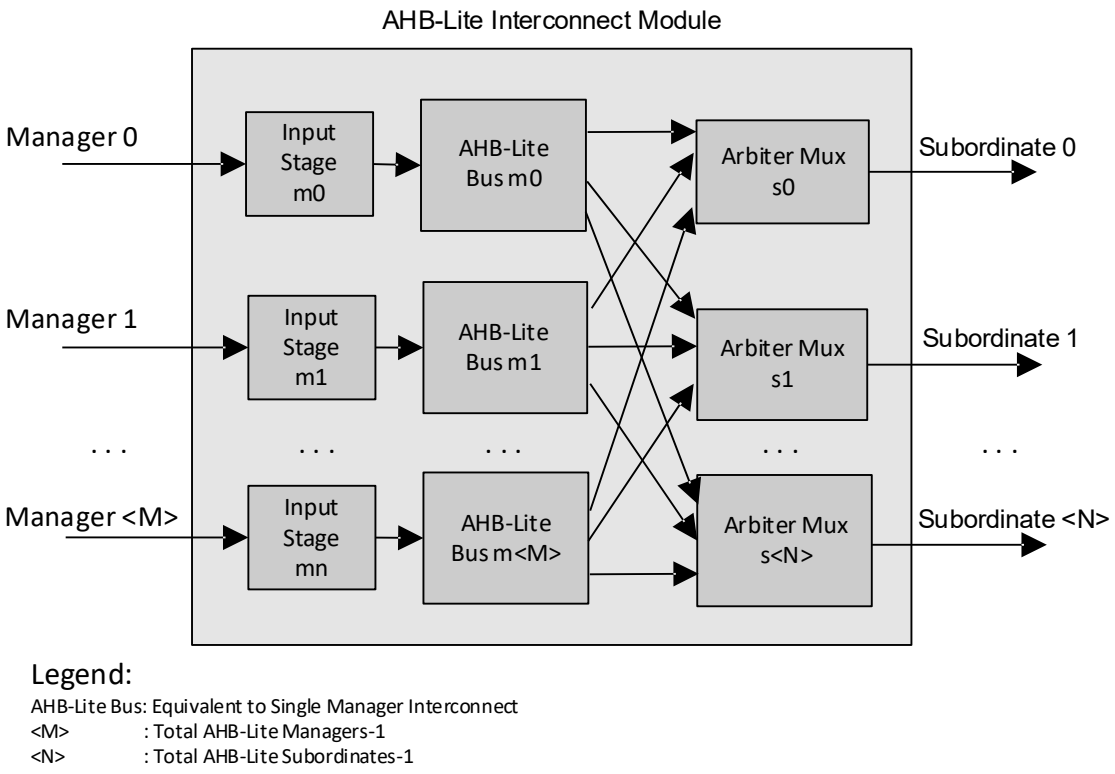


**Figure 2.8. Block Diagram of Multi-Manager Interconnect**

#### 2.4.2.1. Input Stage

The address phase cannot be stalled, hence, the address and control signals need to be registered so that when the manager is not granted access, the registered address/control signals can be used to communicate with the subordinate. The input stage IP block is used to store the address and control until the manager is given access. Control signal consists of all the signals that are sampled at the address phase: HWRITE, HSIZE, HBURST, HPROT, HTRANS, and HMASTLOCK.

Each arbiter mux sends stall signal to corresponding Input Stage if a not granted manager initiates transaction.

#### 2.4.2.2. Arbiter Mux

The arbiter mux uses the subordinate select (HSELx) and HTRANS input signals as requests to the internal arbiter block, which grants only one manager. The grant signal is used in the multiplexer to select the manager signals to the subordinate. In addition, the grant signal is used by the arbiter mux to lower the HREADY signal for all managers that are not selected and to generate the stall signals to the Input Stage.

Each arbiter mux has its own arbiter.

# 3. Design Considerations

## 3.1. Subordinate Max Burst Size in Single-Manager Multi-Subordinate Configurations

When the interconnect is configured with a single manager and multiple subordinates, no arbiter mux is instantiated; therefore, no max burst size handling exists and no error response is sent to the manager.

The max burst size feature performs the following functions:

- Prevent bus hogging: stop one manager from monopolizing the bus with long bursts.
- Ensure fair arbitration: allow other waiting managers to gain access.

The feature is not needed when there is only a single manager for the following reasons:

- No other manager is waiting, and no fairness concerns between competing managers.
- Adding the burst counter wastes area and resources.
- Generating error responses unnecessarily interrupts valid transfers.

The max burst size feature is not supported when *Total AHB-Lite Managers* = 1. The default value is always set to 0.

# Appendix A. Resource Utilization

**Note**: Resource utilization values in this section are provided for reference only and may change based on the compilation strategy and selected tool options.

The following tables show the resource utilization of the AHB-Lite Interconnect for different Lattice FPGA devices using the Lattice Radiant software with Synplify Pro as the synthesis tool.

**Table A.1. Resource Utilization Using the LAV-AT-X70ES-1LFG1156I Device**

| Configuration | Clock Fmax (MHz) | Registers | LUTs | EBRs |
|---|---|---|---|---|
| Total AHB-Lite Managers = 2<br>Total AHB-Lite Subordinates = 2 | 192.271 | 292 | 793 | 0 |
| Total AHB-Lite Managers = 3<br>Total AHB-Lite Subordinates = 4 | 190.621 | 560 | 2006 | 0 |
| Total AHB-Lite Managers = 2<br>Total AHB-Lite Subordinates = 1 | 229.253 | 250 | 430 | 0 |
| Total AHB-Lite Managers = 3<br>Total AHB-Lite Subordinates = 2 | 175.871 | 426 | 1203 | 0 |
| Total AHB-Lite Managers = 3<br>Total AHB-Lite Subordinates = 1 | 194.212 | 348 | 690 | 0 |

**Table A.2. Resource Utilization Using the LFCPNX-100-8LFG672I Device**

| Configuration | Clock Fmax (MHz) | Registers | LUTs | EBRs |
|---|---|---|---|---|
| Total AHB-Lite Managers = 2<br>Total AHB-Lite Subordinates = 4 | 147.189 | 381 | 1153 | 0 |
| Total AHB-Lite Managers = 4<br>Total AHB-Lite Subordinates = 2 | 126.183 | 564 | 1592 | 0 |
| Total AHB-Lite Managers = 2<br>Total AHB-Lite Subordinates = 3 | 136.37 | 325 | 875 | 0 |
| Total AHB-Lite Managers = 4<br>Total AHB-Lite Subordinates = 4 | 116.482 | 758 | 2494 | 0 |

# References

- Arm web page for the AMBA 3 AHB-Lite Protocol Specification
- AHB-Lite Interconnect Module Release Notes (FPGA-RN-02044)
- Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059)
- Mach-NX web page
- MachXO2 web page
- MachXO3 web page
- MachXO3D web page
- MachXO4 web page
- MachXO5-NX web page
- CrossLink-NX web page
- CertusPro-NX web page
- Certus-NX web page
- Certus-N2 web page
- iCE40 UltraPlus web page
- Avant-E web page
- Avant-G web page
- Avant-X web page
- Lattice Radiant Software web page
- Lattice Propel Design Environment web page
- Lattice Diamond Software web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

# Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

# Revision History

**Note:** In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

**Revision 1.7, IP v1.6.0, June 2026**

| Section | Change Summary |
|---|---|
| All | • Performed minor formatting and editorial edits.<br>• Removed the *Known Issues* section. |
| Acronyms in This Document | Updated list of acronyms. |
| Functional Description | • Updated Table 2.2. Attributes Table as follows:<br>  • Updated the default value for the *Base Address 7* attribute.<br>  • Removed a note for the *Arbiter Scheme* attribute.<br>  • Added a note for *Max Burst Size Settings Tab*.<br>• Updated Table 2.3. Attributes Description as follows:<br>  • Removed notes for *Registered Output* and *Arbiter Scheme* attributes.<br>  • Updated description of *Manager <M> Priority* and *Subordinate <N> Max Burst Size* attributes. |
| Design Considerations | Added this section. |
| Resource Utilization | • Added a note on resource utilization values.<br>• Updated Table A.1. Resource Utilization Using the LAV-AT-X70ES-1LFG1156I Device and Table A.2. Resource Utilization Using the LFCPNX-100-8LFG672I Device. |
| References | Updated references. |

**Revision 1.6, IP v1.5.0, December 2025**

| Section | Change Summary |
|---|---|
| Introduction | Added MachXO4™ device in Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation. |
| Resource Utilization | Updated *Lattice Radiant software 2025.1* to *Lattice Radiant software*. |
| References | Updated references. |
| Revision History | Added note. |

**Revision 1.5, IP v1.4.0, June 2025**

| Section | Change Summary |
|---|---|
| Introduction | Updated Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation as follows:<br>• Added iCE40 UltraPlus devices.<br>• Renamed *Supported FPGA Family* to *Supported Devices*. |
| Functional Description | • Updated Table 2.2. Attributes Table as follows:<br>  • Updated the default value of the *Full Address Decoding up to 1kB* attribute.<br>  • Removed the *Early Burst Termination Protection* attribute.<br>  • Updated *Manager Priority Settings* tab.<br>• Removed the *Early Burst Termination Protection* attribute in Table 2.3. Attributes Description. |
| Known Issues | Updated section. |
| Resource Utilization | Added this section. |
| References | Updated references. |

**Revision 1.4, IP v1.3.3, February 2025**

| Section | Change Summary |
|---|---|
| Functional Description | • Added the *Early Burst Termination Protection* attribute under the *General Tab* in Table |

| Section | Change Summary |
|---|---|
| | 2.2. Attributes Table.<br>• Added the *Early Burst Termination Protection* attribute in Table 2.3. Attributes Description.<br>• Updated the Use Models section.<br>• Updated the following figures:<br>  • Figure 2.3. Example of Single Manager Interconnect Application<br>  • Figure 2.4. Example of Multi-Manager Interconnect Application |

**Revision 1.3, IP v1.3.2, December 2024**

| Section | Change Summary |
|---|---|
| All | • Renamed document from AHB-Lite Interconnect Module - Lattice Propel Builder to AHB-Lite Interconnect Module.<br>• Changed instances of *Master* to *Manager*, and *Slave* to *Subordinate*. |
| Disclaimers | Updated disclaimers. |
| Inclusive Language | Added inclusive language boilerplate. |
| Introduction | Added MachXO5-NX, CertusPro-NX, Lattice Avant, and Certus-N2 devices in Table 1.1. FPGA Software for IP Configuration, Generation, and Implementation. |
| Functional Description | • Updated Table 2.2. Attributes Table as follows:<br>  • Removed *Weighted Round Robin* option from the *Arbiter Scheme* attributes.<br>  • Removed the note on the Weighted Round Robin Arbiter Scheme.<br>• Updated Figure 2.2. AHB-Lite Interconnect Module Configuration User Interface. |
| Appendix A. Known Issues | Added this section. |
| References | Updated references. |
| Technical Support Assistance | Added link to the Lattice Answer Database. |

**Revision 1.2, May 2021**

| Section | Change Summary |
|---|---|
| Introduction | Updated document introduction, including Table 1.1 to add MachXO2 and MachXO3 as supported FPGA family. |
| References | Updated content to add reference for MachXO2 and MachXO3. |

**Revision 1.1, November 2020**

| Section | Change Summary |
|---|---|
| Introduction | • Updated information of Features section.<br>• Added Table 1.1. |
| Functional Description | • Updated content of Overview, Use Models, Decoder, and Multi-Master Interconnect section.<br>• Updated Figure 2.2.<br>• Updated Table 2.2. and Table 2.3. |
| References | Updated content to remove reference links for Lattice Propel and Lattice Diamond user guide; and to add reference links for Mach-NX, CrossLink-NX, and Certus-NX web page. |

**Revision 1.0, May 2020**

| Section | Change Summary |
|---|---|
| All | Initial release. |


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