Tri-Speed Ethernet IP

IP Version: v2.2.0

User Guide

FPGA-IPUG-02084-2.5

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Tables

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
AXI	Advanced eXtensible Interface
CRC	Cyclic Redundancy Check
ED	Example Design
FCS	Frame Check Sequence
FIFO	First In First Out
HIP	Hardened IP
IP	Intellectual Property
IPG	Inter-Packet Gap
LMMI	Lattice Memory Mapped Interface
MAC	Media Access Controller
MDIO	Management Data Input/Output
MIIM	Media Independent Interface Management Module
MPCS	Multiple-Protocol Physical Coding Sublayer
PCS	Physical Coding Sublayer
PHY	Physical Layer
PLL	Phase-Locked Loop
RTL	Register Transfer Language
SERDES	Serializer/Deserializer
SFD	Start of Frame Delimiter
SGMII	Serial Gigabit Media Independent Interface
TSE	Tri-Speed Ethernet

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1. Introduction

1.1. Overview of the IP

The Tri-Speed Ethernet (TSE) IP solution consists of the TSE IP Media Access Controller (MAC) core and the SGMII GbE Physical Coding Sublayer (SGMII PCS) IP core. The integration of TSE IP (MAC) core with the SGMII PCS IP core creates a seamless connection between MAC-level operations and physical Ethernet channels.

The TSE IP (MAC) is a complex core containing all the necessary logic, interfacing, and clocking infrastructure to integrate an external industry-standard Ethernet PHY with an internal processor efficiently and with minimal overhead. It supports the ability to transmit and receive data between standard interfaces, such as APB, AHB-Lite or AXI4-Lite, and an Ethernet network.

The SGMII PCS IP core converts GMII frames into 8-bit code groups in both transmit and receive directions and performs auto-negotiation with a link partner as described in the Cisco SGMII and IEEE 802.3z specifications. The SGMII IP is a connection bus for MACs and PHYs and is often used in bridging applications and/or PHY implementations. It is widely used as an interface for a discrete Ethernet PHY chip.

1.2. Quick Facts

Table 1.1. Summary of the TSE IP Core

IP Requirements	Supported Devices[1,2,3,4]	Lattice Avant™, CrossLink™-NX, Certus™-NX, CertusPro™-NX, Certus™-N2, MachXO5™-NX.
	IP Changes[5]	For a list of changes to the IP, refer to the Tri-Speed Ethernet IP Release Notes (FPGA-RN-02036).
Resource Utilization	Supported User Interface	Host: APB, AHB-Lite, and AXI4-Lite. Data: AXI4-Stream.
	Resource Usage	Refer to Appendix A. Resource Utilization section.
Design Tool Support	Lattice Implementation	IP core v2.2.0 —Lattice Radiant™ software 2025.2 or later.
	Synthesis	Synopsys® Synplify Pro® for Lattice.
	Simulation	For a list of supported simulators, see the Lattice Radiant Software User Guide.
Driver Support	API Reference	Refer to the Tri-Speed Ethernet Driver API Reference (FPGA-TN-02341).

Notes:

1. The SGMII interface using LVDS I/O in Certus-NX, CertusPro-NX, MachXO5-NX, and CrossLink-NX FPGAs has limitations when operating across the full specified temperature range. Lattice recommends using alternative interfaces, such as SERDES or RGMII, for designs requiring Gigabit Ethernet. Refer to the Knowledge Base article for details. Contact your local Lattice sales representative for more information.
2. For SGMII (LVDS) only and SGMII (LVDS) + MAC configurations, all Nexus™ (NX) devices require speed grade 9.
3. For SGMII (LVDS) only and SGMII (LVDS) + MAC configurations, this IP is not supported on CrossLink-NX devices with 72 WLCSP and 72 QFN packages.
4. For SGMII (LVDS) only and SGMII (LVDS) + MAC configurations, this IP is not supported on LIFCL-33 and LIFCL-33U devices.
5. In some instances, the IP may be updated without changes to the user guide. This user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

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1.3. IP Support Summary

The following table provides IP support information on the TSE IP core.

Note: The SGMII interface using LVDS I/O in Certus-NX, CertusPro-NX, MachXO5-NX, and CrossLink-NX FPGAs has limitations when operating across the full specified temperature range. Lattice recommends using alternative interfaces, such as SERDES or RGMII, for designs requiring Gigabit Ethernet. Refer to the Knowledge Base article for details. Contact your local Lattice sales representative for more information.

Table 1.2. TSE IP Core Support Readiness

Device Family	Mode	Interface	Data Rate	Radiant Timing Model	Hardware Validated
MachXO5-NX	MAC only	MII/GMII	1G, 100M, 10M	Final	No
		RGMII	1G, 100M, 10M	Final	No
		SGMII Easy Connect	1G, 100M, 10M	Final	No
		Gigabit MAC	1G	Final	No
		RMII	100M, 10M	Final	No
	SGMII (LVDS) only, MAC + SGMII (LVDS)	—	1G, 100M, 10M	Final	Yes
CrossLink-NX, Certus-NX	MAC only	MII/GMII	1G, 100M, 10M	Final	No
		RGMII	1G, 100M, 10M	Final	Yes
		SGMII Easy Connect	1G, 100M, 10M	Final	Yes
		Gigabit MAC	1G	Final	No
		RMII	100M, 10M	Final	No
	SGMII (LVDS) only, MAC + SGMII (LVDS)	—	1G, 100M, 10M	Final	Yes
CertusPro-NX	MAC only	MII/GMII	1G, 100M, 10M	Final	No
		RGMII	1G, 100M, 10M	Final	Yes
		SGMII Easy Connect	1G, 100M, 10M	Final	Yes
		Gigabit MAC	1G	Final	No
		RMII	100M, 10M	Final	Yes
	SGMII (LVDS) only, MAC + SGMII (LVDS), SGMII (SERDES) only, MAC + SGMII (SERDES)	—	1G, 100M, 10M	Final	Yes
Lattice Avant	MAC only	MII/GMII	1G, 100M, 10M	Preliminary	No
		RGMII	1G, 100M, 10M	Preliminary	Yes
		SGMII Easy Connect	1G, 100M, 10M	Preliminary	Yes
		Gigabit MAC	1G	Preliminary	Yes
		RMII	100M, 10M	Preliminary	No
	SGMII (LVDS) only, MAC + SGMII (LVDS), SGMII (SERDES) only, MAC + SGMII (SERDES)	—	1G, 100M, 10M	Preliminary	Yes

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1.4. Features

The TSE IP core offers the following key features:

- Compliant to IEEE 802.3-2005 standard
- 8-bit wide internal datapath
- Full-duplex operation in 1G mode
- Full-duplex and half-duplex operation in 10/100M mode
- Transmit and receive statistics vector and statistic counter
- Programmable Inter-Packet Gap (IPG)
- Multicast address filtering
- Selectable MAC operating options:
    - MII/GMII
    - Gigabit MAC with GMII
    - SGMII Easy Connect MAC with GMII
    - RGMII
    - RMII
- Host control interface configurable to either APB, AHB-Lite, or AXI4-Lite
- Interrupt interface
- Option to select between MAC only, PHY only and MAC + PHY mode
- Flow control using pause frames
- VLAN tagged frames
- Automatic re-transmission on collision
- Automatic padding of short frames
- Multicast and Broadcast frames
- Optional frame check sequence (FCS) transmission and reception
- Optional MII management interface module (MDIO)
- Jumbo frames with maximum frame length of 9,600 bytes

The following lists the key features of the PHY solution:

- Physical Coding Sublayer (PCS) functions of the Cisco SGMII Specification, Revision 1.8
- PCS functions for IEEE 802.3z (1000BASE-X)
- Dynamic selection of SGMII/1000BASE-X PCS operation
- Support for MAC or PHY mode for SGMII auto-negotiation
- Support for (G)MII data rates of 1 Gbps, 10 Mbps, and 100 Mbps
- TSMAC Easy Connect option for seamless integration with the MAC only, SGMII Easy Connect option
- Management Interface Port for control and maintenance

1.5. Licensing and Ordering Information

The Tri-Speed Ethernet IP is available with Lattice Radiant Subscription Software. To purchase the Lattice Radiant Subscription license, contact Lattice Sales or go to the Lattice Online Store.

1.6. Hardware Support

For more information on CertusPro-NX and Avant device support and the boards used with this IP, refer to the Example Design section. The CrossLink-NX Evaluation Board hardware is not supported.

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1.7. Naming Conventions

1.7.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.7.2. Signal Names

- _*n* are active low signals (asserted when value is logic 0)
- _*i* are input signals
- _*o* are output signals

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2. Functional Description

2.1. IP Architecture Overview

The TSE IP core transmits and receives data between a client application and an Ethernet network. The main function of the Ethernet MAC is to ensure that the media access rules specified in the IEEE 802.3 standard are met while transmitting and receiving Ethernet frames.

The MAC core is a fully synchronous machine composed of Transmit and Receive MAC sections that operate independently to support full duplex operation.

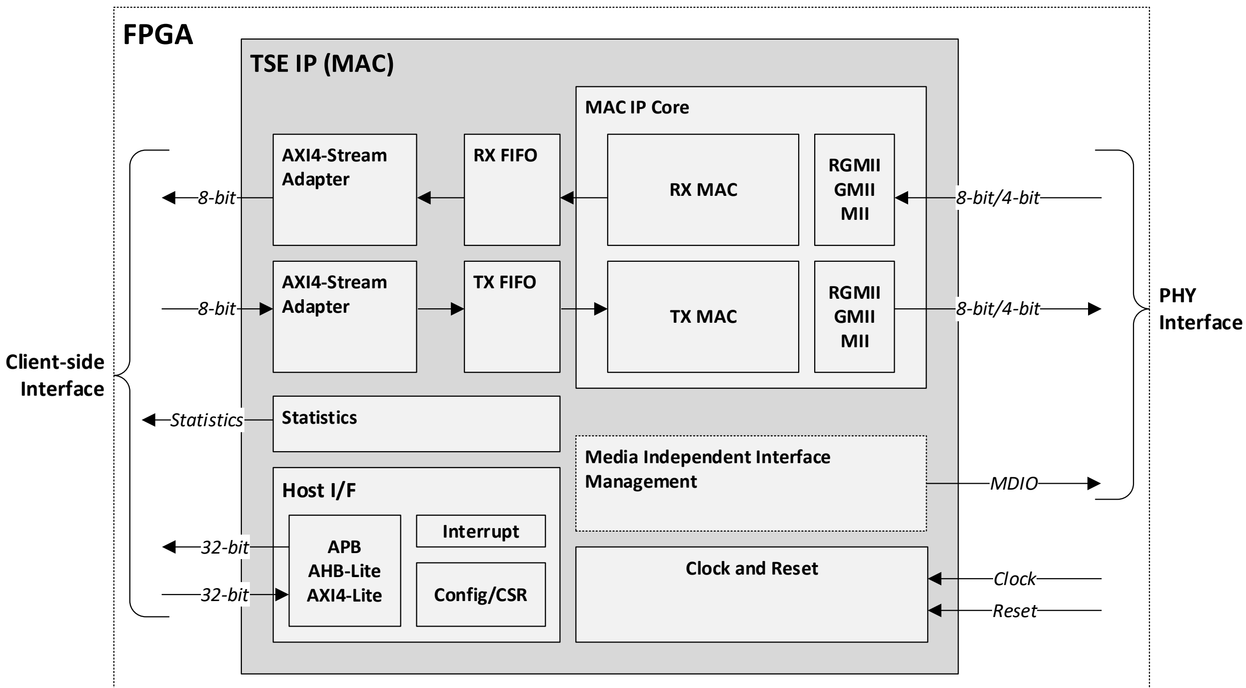

Figure 2.1. MAC Block Diagram

The TSE IP core also provides an option to include the SGMII/Gb Ethernet PCS IP core that converts MII/GMII interfaces of the MAC to serial interfaces in both transmit and receive directions and performs auto-negotiation with a link partner as described in the Cisco SGMII and IEEE 802.3 specifications. The following figure shows the top-level block diagram of the SGMII/Gb Ethernet PCS block.

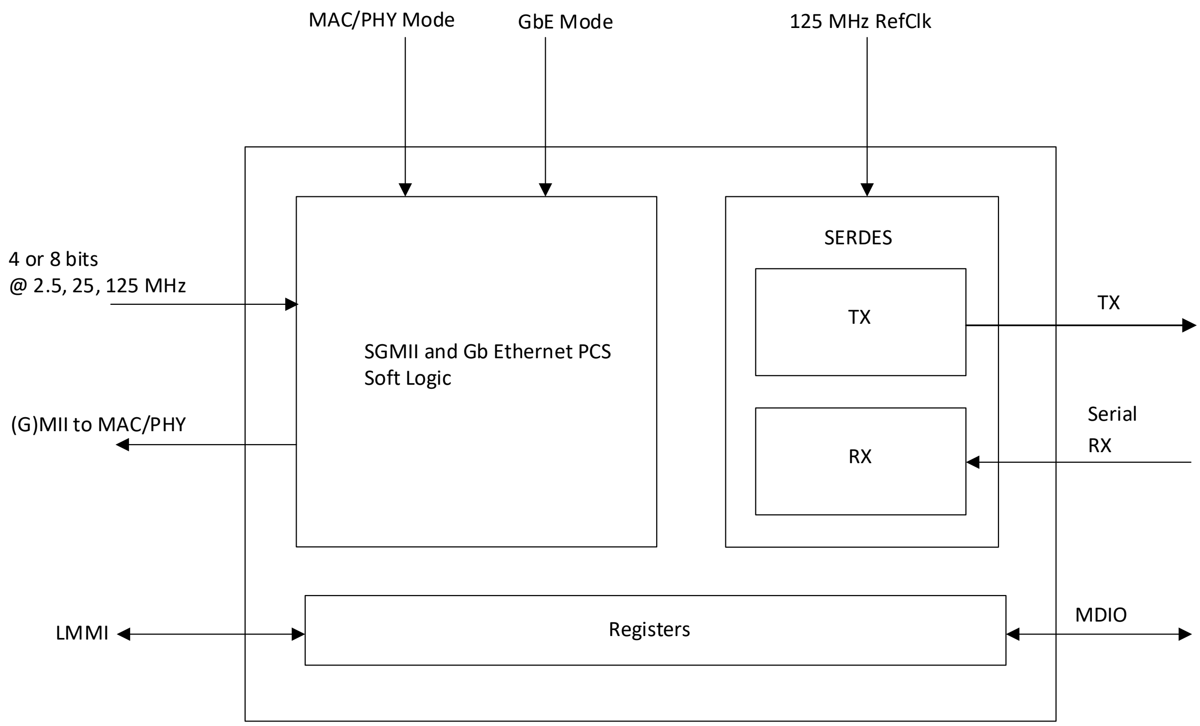

Figure 2.2. SGMII and Gb Ethernet PCS Block Diagram

2.1.1. Implementation Options

The TSE IP core supports multiple Ethernet implementation options shown in Figure 2.3, Figure 2.4, and Figure 2.5. The choice of implementations depends on the required rates, duplex mode, I/O pin count, target device, and capability supported by the external Ethernet PHY. Table 2.2 lists the implementation options.

2.1.1.1. Interface to External PHY with MII/GMII/RGMII/RMII Interface

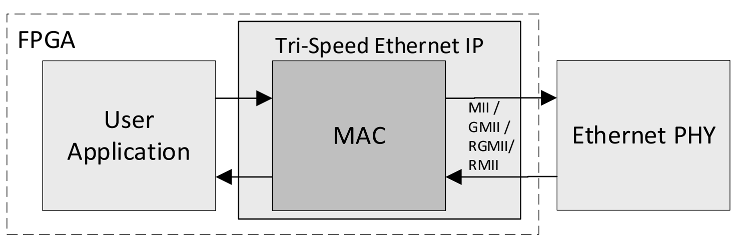

Figure 2.3. TSE IP Connected to External PHY with MII/GMII/RGMII/RMII

This implementation is suitable for FPGAs with limited or high performance I/O, or selected Ethernet PHY that does not support serial interface.

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2.1.1.2. Interface to External PHY with Serial Interface

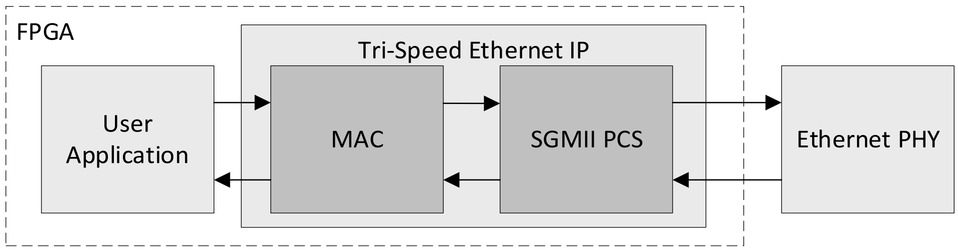

Figure 2.4. TSE IP Connected to External Ethernet PHY with Serial Interface via Embedded SGMII PCS IP

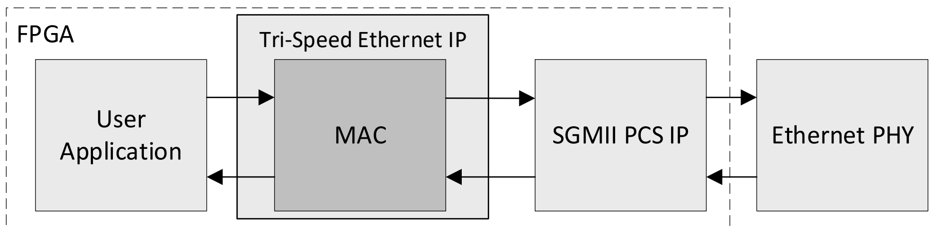

Figure 2.5. TSE IP Connected to External Ethernet PHY with Serial Interface via SGMII PCS IP (Other Devices)

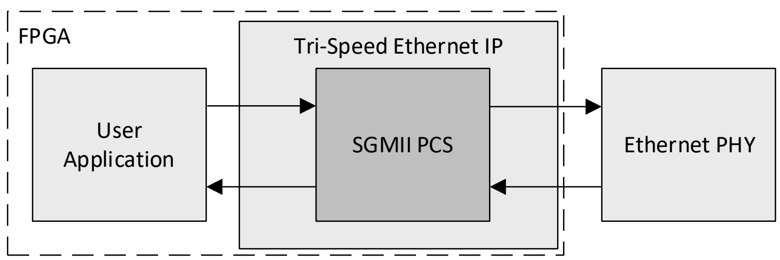

Figure 2.6. TSE IP Connected to External Ethernet PHY with Serial Interface via SGMII Only Mode (All Devices)

This implementation is suitable for FPGAs with high performance I/O. The number of I/O pins and required board traces are smaller.

The TSE IP supports MAC + PHY IP options, which support serial interface (1000BASE-X / SGMII) to external PHY. For TSE IP to external PHY via the SGMII PCS IP, reference designs are available for CertusPro-NX and CrossLink-NX devices on the TSEMAC & SGMII Reference Design web page.

2.1.1.3. Summary of Supported Operation Options

The following table summarizes the description of supported operation options, MAC only, SGMII only, MAC + PHY. The MAC + PHY is a generic option that refers to either the MAC + SGMII (SERDES) or MAC + SGMII (LVDS).

Note: The SGMII interface using LVDS I/O in Certus-NX, CertusPro-NX, MachXO5-NX, and CrossLink-NX FPGAs has limitations when operating across the full specified temperature range. Lattice recommends using alternative interfaces, such as SERDES or RGMII, for designs requiring Gigabit Ethernet. Refer to the Knowledge Base article for details. Contact your local Lattice sales representative for more information.

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Table 2.1. Operation Options

IP Option	Operation	Description
MAC only	MII/GMII	The MAC operates on three speed modes by changing the input clock frequency. This mode is compliant to the IEEE 802.3 Standard, MII/GMII.
	Gigabit MAC	The MAC only operates in 1 speed – 1 Gbps and configured in full-duplex mode only.
	SGMII Easy Connect	The MAC uses clock enables to operate at three different speeds. Use this operation mode to interface with the SGMII PCS IP seamlessly.
	RGMII	The MAC operates in RGMII data rate and configured in full-duplex mode only.
	RMII	The MAC operates in RMII data rate.
SGMII only	Classic	SGMII PCS operates on three speed modes by changing the input clock frequency. This mode is used to convey MII/GMII, IEEE 802.3 Standard interface.
	TSMAC Easy Connect	SGMII PCS operates on three speed modes by This mode is used together with MAC only, SGMII Easy Connect mode.
MAC + SGMII (LVDS)	Multi-rate SGMII Ethernet	The MAC with embedded SGMII PCS operates on three speed modes and interface with external Ethernet PHY using a serial interface.
	Gigabit SGMII Ethernet	The MAC with embedded Gigabit PCS operates in 1,000 Mbps mode and interface with external Ethernet PHY using a serial interface.
MAC + SGMII (SERDES)	Multi-rate SGMII Ethernet	The MAC with embedded Gigabit PCS operates on three speed modes and interface with external Ethernet PHY using a serial interface in the CertusPro-NX MPCS hardened IP (HIP).

2.1.1.4. Summary of Implementation

The following table summarizes implementation options of TSE IP based on External PHY.

Table 2.2. Summary of Implementation Options

External PHY Interface	Rates (Mbps)	Duplex Mode	Datapath I/O Pin Count	IP Configuration	
				IP Option	Operation
MII	10/100	Full-duplex/ Half-duplex	16	MAC only	MII/GMII. Use only lower 4-bit of MII/GMII data signals.
GMII	1000	Full-duplex	22	MAC only	Gigabit MAC.
MII/GMII	10/100/1000	Full-duplex/ Half-duplex (10/100M only)	25	MAC only	MII/GMII.
RGMII	10/100/1000	Full-duplex/ Half-duplex (10/100M only)	12	MAC only	RGMII.
RMII	10/100	Full-duplex/ Half-duplex	8	MAC only	RMII.
1000BASE-X	1000	Full-duplex	4	SGMII only	To use 1000BASE-X auto negotiation—IEEE 802.3 standard, set gbe_mode_i to 1.
				MAC+SGMII	Gigabit 1000BASE-X Ethernet.
SGMII	10/100/1000	Full-duplex/ Half-duplex (10/100M only)	4	SGMII only	To use SGMII auto negotiation, set both gbe_mode_i and sgmii_mode_i to 0.
				MAC+SGMII	Multi-rate SGMII Ethernet.

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2.1.2. MAC Only Mode

2.1.2.1. MII/GMII Configuration Option

When the MII/GMII option is selected, the MAC can be configured to operate in either the 1G mode (1,000 Mbps data rate) or the Fast Ethernet mode (10/100 Mbps data rate) by setting an internal register bit. The following figure shows a block diagram of the MII/GMII configuration option.

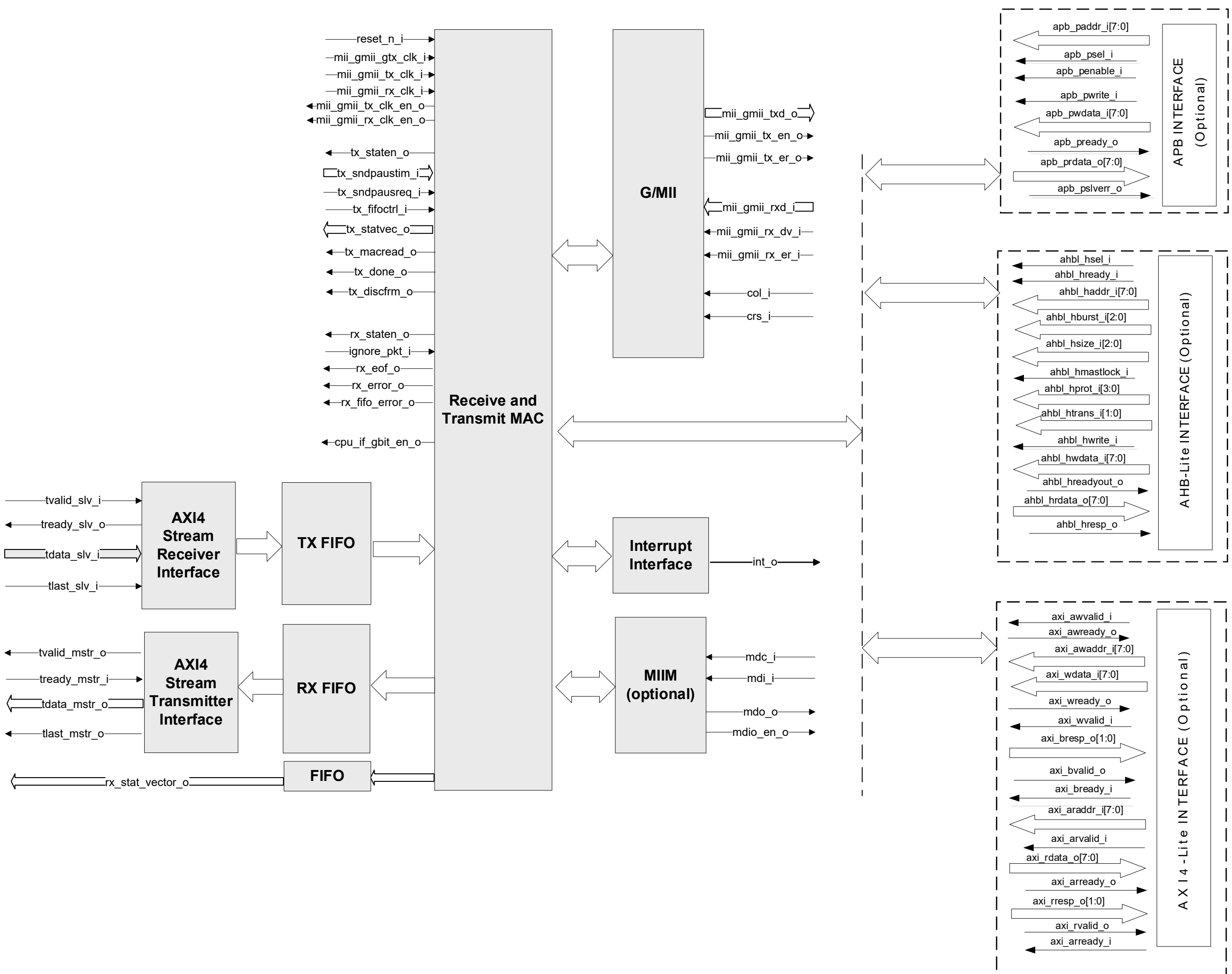

Figure 2.7. Top-Level Block Diagram for the MII/GMII Configuration Option

2.1.2.2. Gigabit MAC Configuration Options

For the Gigabit MAC configuration option, the MAC always operates at the Gigabit data rate and is effectively configured as a full-duplex Gigabit MAC only.

The following figure shows a block diagram of the Gigabit MAC configuration option.

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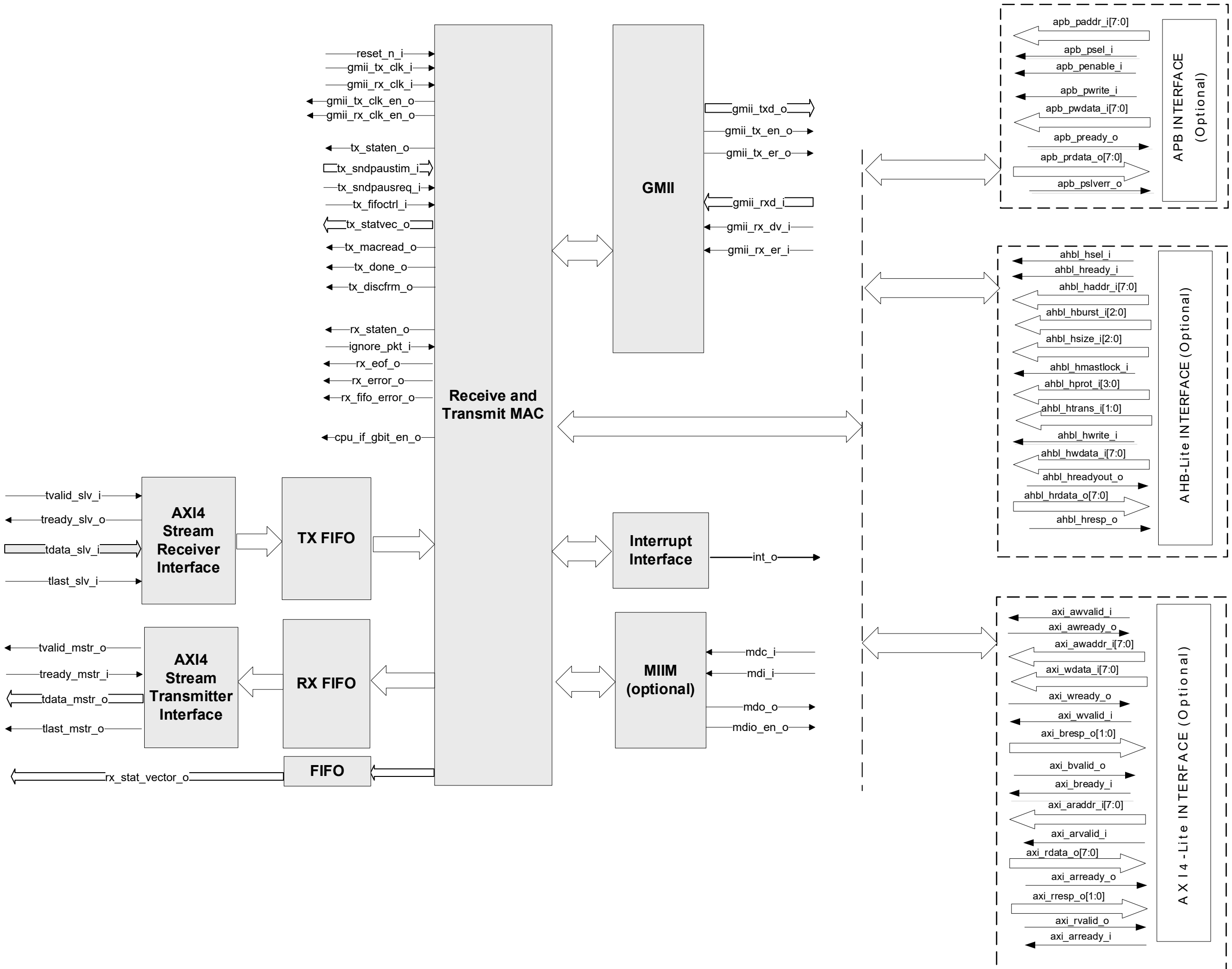

Figure 2.8. Top-Level Block Diagram for Gigabit MAC Configuration Option

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2.1.2.3. SGMII Easy Connect Configuration Options

For the SGMII Easy Connect configuration option, the MAC operates at the Gigabit data rate and uses the clock enables provided by the SGMII PCS IP core to work at three different speeds.

The following figure shows a block diagram of the SGMII Easy Connect configuration option.

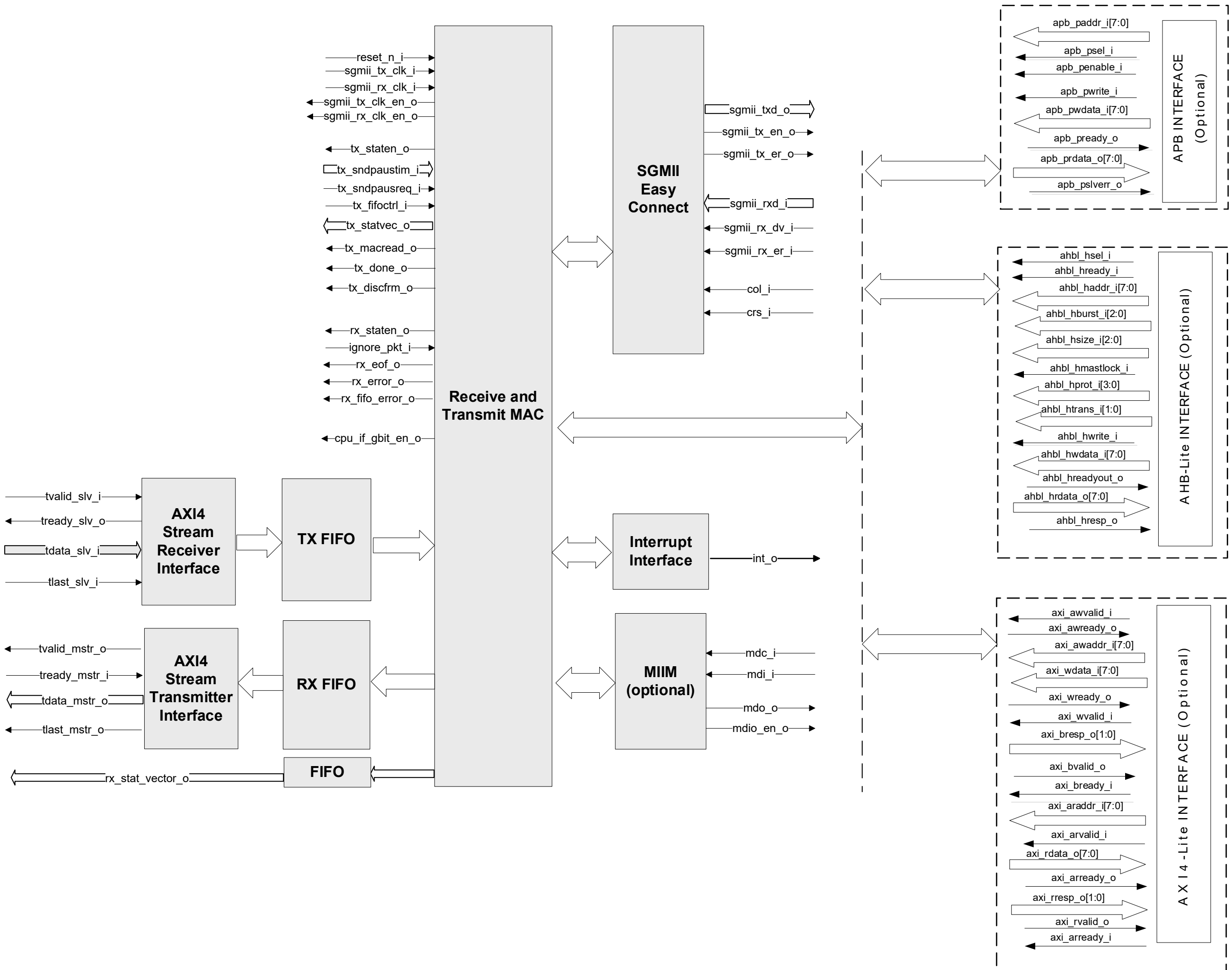

Figure 2.9. Top-Level Block Diagram for the SGMII Easy Connect Configuration Option

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2.1.2.4. RGMII Configuration Option

For the RGMII configuration option, the MAC can be configured to operate in either the 1G mode (1,000 Mbps data rate) or the Fast Ethernet mode (10/100 Mbps data rate).

The following figure shows a block diagram of the RGMII configuration option.

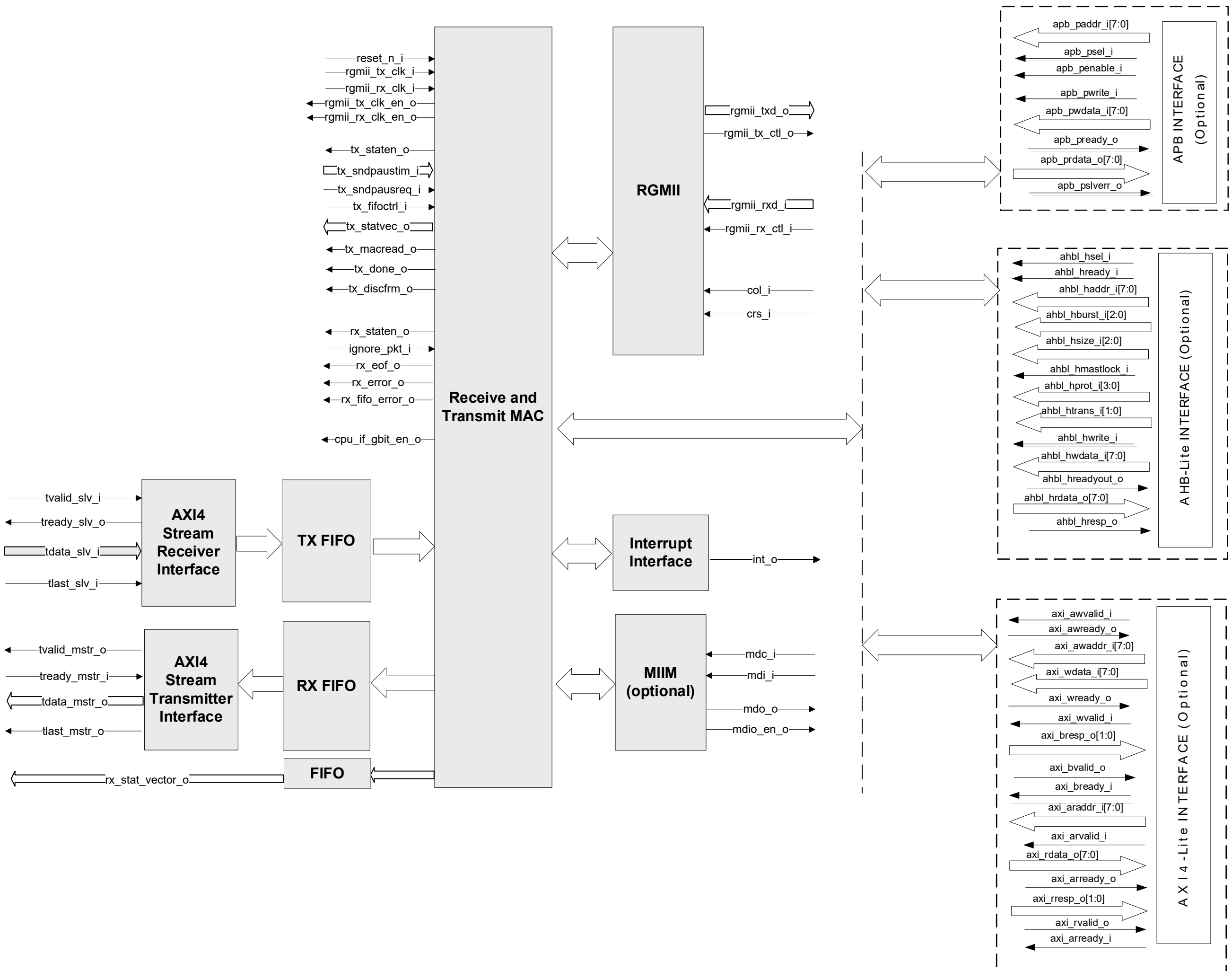

Figure 2.10. Top-Level Block Diagram for the RGMII Configuration Option

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2.1.2.5. RMII Configuration Option

When the RMII option is selected, the MAC operates at the RMII data rate. The following figure shows a block diagram of the RMII configuration option.

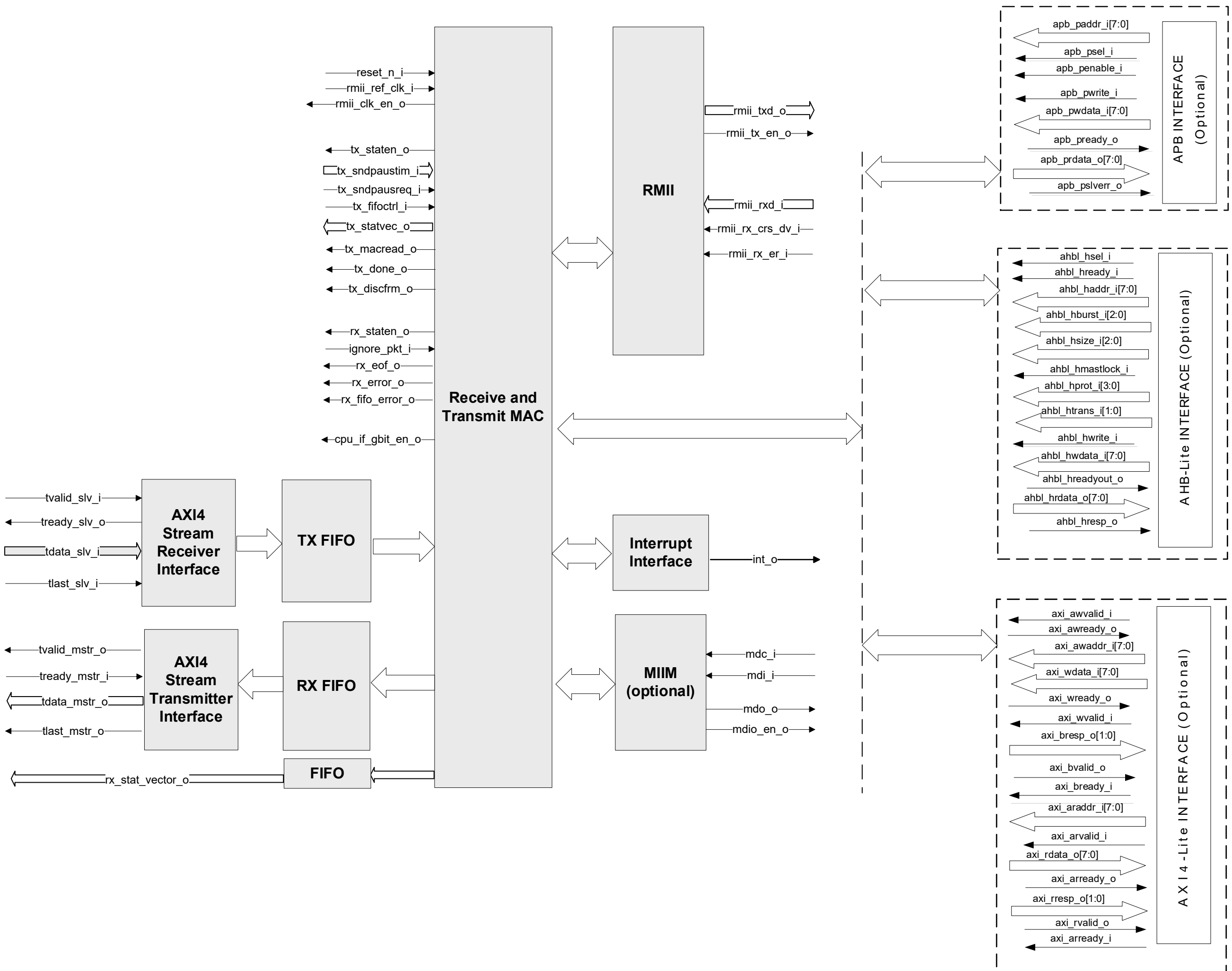

Figure 2.11. Top-Level Block Diagram for the RMII Configuration Option

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2.1.3. SGMII (LVDS) Only Mode

In this mode, TSE IP is offering standalone SGMII PHY solution. This mode converts GMII frames into 8-bit code groups in both transmit and receive directions and performs auto-negotiation with a link partner as described in the Cisco SGMII and IEEE 802.3z specifications. The SGMII is a connection bus for MACs and PHYs and is often used in bridging applications and/or PHY implementations. It is widely used as an interface for a discrete Ethernet PHY chip.

Note: The SGMII interface using LVDS I/O in Certus-NX, CertusPro-NX, MachXO5-NX, and CrossLink-NX FPGAs has limitations when operating across the full specified temperature range. Lattice recommends using alternative interfaces, such as SERDES or RGMII, for designs requiring Gigabit Ethernet. Refer to the Knowledge Base article for details. Contact your local Lattice sales representative for more information.

The following figure shows the detailed block diagram of the SGMII/Gb Ethernet PCS IP core.

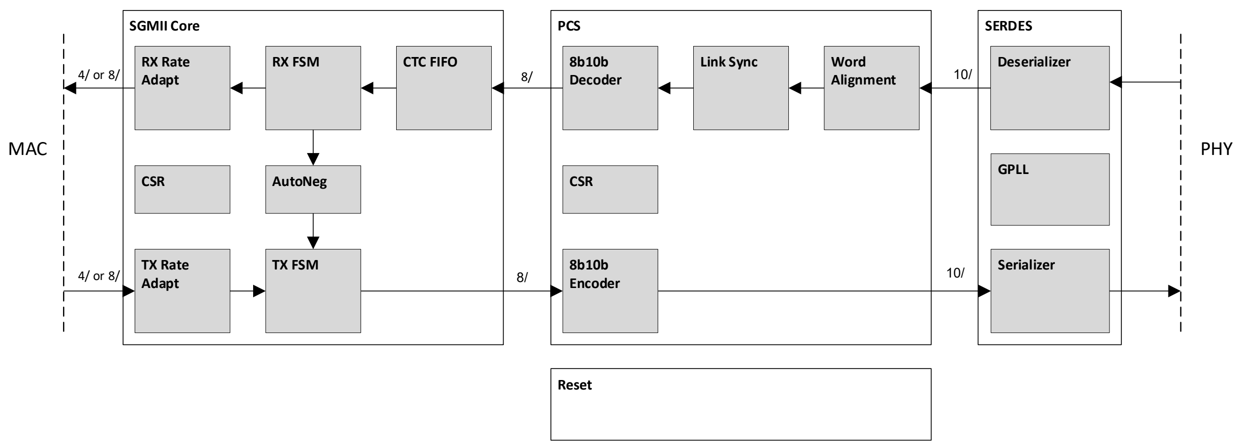

Figure 2.12. Detailed Block Diagram of the SGMII (LVDS) Only Mode

2.1.3.1. SERDES and PCS

This block is composed of Generic DDR blocks that receives and transmits the serial data to and from the PHY. It also instantiates a Generic PLL that generates clock sources for SERDES, PCS, and SGMII core blocks.

See section 36.2 of IEEE 802.3-2018 specifications for PCS modules description.

2.1.3.2. Transmit SGMII Core

Transmit Rate Adaptation

This module adjusts the parallel byte-per-byte data input rate such that the serial output rate is always 1 Gbps. When incoming GMII data operates at 1 Gbps, there is no data rate alteration. The incoming data is 8-bits wide running at 125 MHz and the outgoing data is also 8-bits wide running at 125 MHz. When incoming GMII data operates at 100 Mbps, each incoming data byte is replicated ten times on the outgoing port. The incoming data is 4-bits wide running at 25 MHz and the outgoing data is 8-bits wide running at 125 MHz. The incoming 10 Mbps is similar except that data bytes are replicated 100 times and the incoming clock rate is 2.5 MHz.

When the IP core is generated using the *TSMAC Easy Connect* option, tx_clock_enable_source_o is used to control the flow of incoming GMII data. For 1 Gbps operation, the clock enable is constantly high. For 100 Mbps operation, the clock enable is high for one-out-of-ten 125 MHz clock cycles. For 10 Mbps operation, the clock enable is high for one-out-of-one-hundred 125 MHz clock cycles. When config_source is set to 0, by default, this clock enable behavior is controlled by the setting of the operational rate pins - operational_rate_i. When config_source is set to 1, this clock enable behavior is controlled by the setting of Bit13, Speed Selection[0] and Bit6, Speed Selection[6] in the [0x000] auto-negotiation control register.

For more information on config_source and operational_rate_i registers, refer to the [0x00E] Configuration Source Control Register for Auto-Negotiation section and the SGMII (LVDS) Only Interfaces section.

For more information on auto-negotiation control register, refer to the [0x000] Auto-Negotiation Control Register section.

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The following figure shows the timing diagram of the signals in the Transmit Rate Adaptation block.

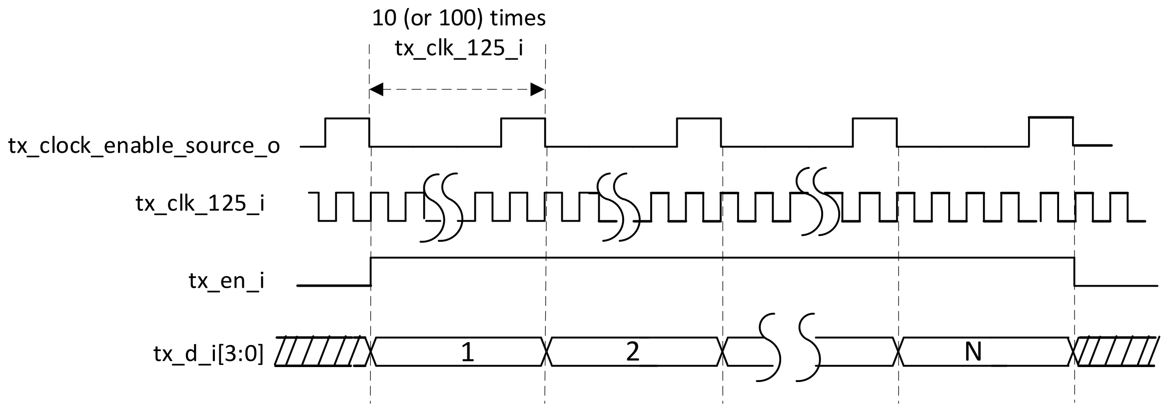

Figure 2.13. SGMII TX-Side Signals Relationship

Transmit State Machine

The transmit state machine implements the transmit function described in clause 36 of the IEEE802.3 specification. The main purpose of the state machine is to convert GMII data frames into code groups. The state machine does not fully implement conversion to 10-bit code groups as specified in IEEE802.3 specification. Instead, partial conversion to 8-bit code groups is performed. A separate encoder in the PCS layer completes the full conversion to 10-bit code groups.

2.1.3.3. Receive SGMII Core

Soft Receive Clock Tolerance Compensation (CTC) Circuit

This block allows the receive path to compensate for slight frequency offsets between two clocks with a nominal frequency of 125 MHz. One timing source is the recovered clock from the SERDES RX physical link. The other timing source is the locally generated RX clock. If the two clock frequencies are within acceptable limits, the compensation circuit can maintain datapath integrity.

You can choose the desired CTC mode when the IP core is generated through the CTC Mode attribute.

Receive State Machine

Receive State Machine implements receive functions described in clause 36 of the IEEE802.3 specification. The main purpose of the state machine is to convert code groups into GMII data frames. The state machine in this IP does not fully implement conversion from 10-bit code groups as specified in the IEEE802.3 specification. Instead, partial conversion from 8-bit code groups is performed. A separate decoder in the PCS performs 10-bit to 8-bit code group conversions.

Receive Rate Adaptation

The function of this block is like the Transmit Rate Adaptation block, except that it operates in reverse. The incoming data rate is always 1 Gbps. The outgoing data rate is reduced by factors of 1X, 10X, or 100X for (G)MII rates of 1 Gbps, 10 Mbps, and 100 Mbps respectively. When the IP core is generated using the TSMAC Easy Connect option, rx_clock_enable_source_o is used to control the flow of incoming GMII data. The idea of the clock enable behavior is similar to the Transmit Rate Adaption module. For more information, refer to the Transmit SGMII Core section.

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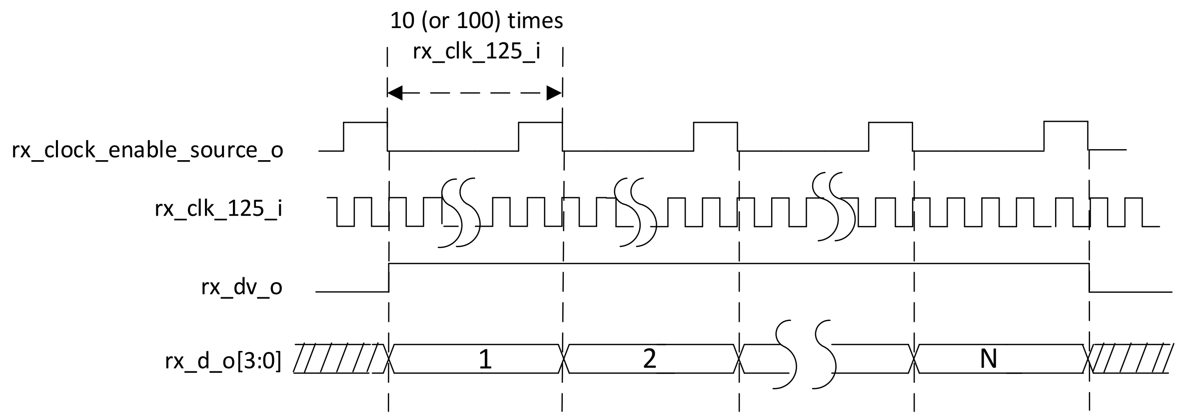

Figure 2.14. SGMII RX-Side Signals Relationship

2.1.3.4. Auto-Negotiation State Machine

Auto-Negotiation State Machine implements link configuration functions described in clause 37 of IEEE802.3 specification. However, the Cisco SGMII specification defines several changes (summarized below). This IP operates in adherence to either specification, based on the setting of the gbe_mode_i pin (1=GBE PCS Mode Active - overrides SGMII PCS Function; 0=GBE PCS Mode Inactive - SGMII PCS Function is now active). Refer to both specifications for detailed description of auto-negotiation operation. Main auto-negotiation functions are to test the physical link for proper operation and to circulate link configuration information between entities sitting on both sides of the link.

Here is a summary of the Cisco SGMII modifications for the auto-negotiation function:

- Decreases link timer interval from 10 msec to 1.6 msec.
- Redefines *link ability* bit assignments.
- Eliminates the need to pass link ability information from MAC to PHY.
- Adds a new condition that forces a restart on the PHY side whenever the PHY link abilities change.

For more information on the Auto-Negotiation configuration, refer to the [0x00E] Configuration Source Control Register for Auto-Negotiation section.

2.1.3.5. MII/GMII Option (Classic Option)

The following figure shows a block diagram of the Classic option. In Classic mode, when the (G)MII data rate is 1 Gbps, all 8 bits of tx_d_i are valid. However, for 10 Mbps and 100 Mbps, only bits 3:0 of tx_d_i are valid.

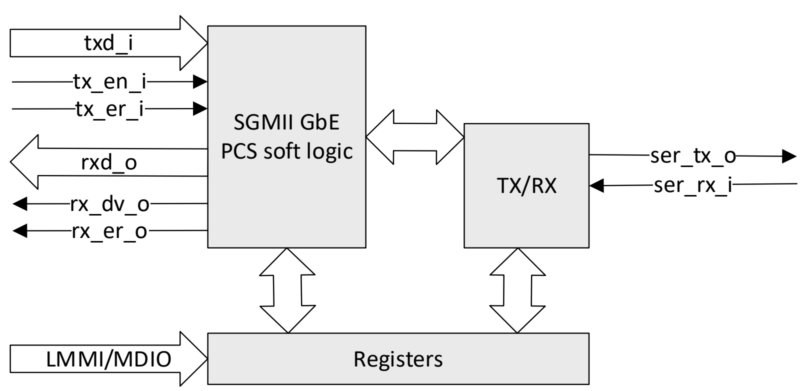

Figure 2.15. Top-Level Block Diagram for MII/GMII Option

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2.1.3.6. TSMAC Easy Connect Option

The block diagram for TSMAC Easy Connect is similar to the block diagram for MII/GMII Option (Classic Option). However, for the *TSMAC Easy Connect* mode all 8 bits of tx_d_i are valid for all (G)MII data rates (1 Gbps, 10 Mbps, 100 Mbps).

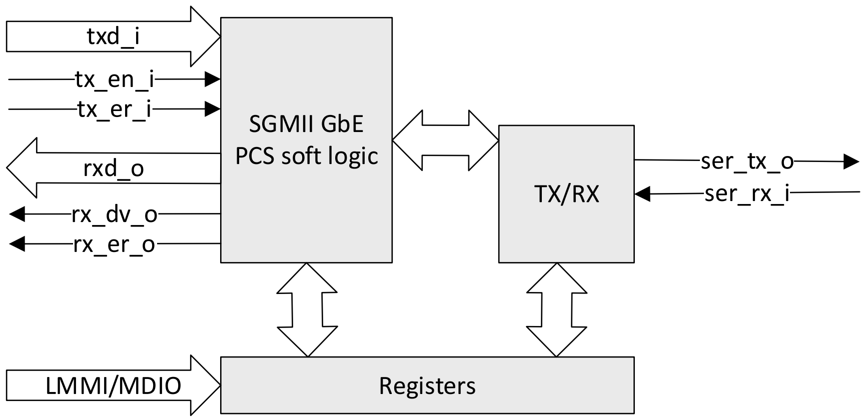

Figure 2.16. Top-Level Block Diagram for TSMAC Easy Connect Option

2.1.4. SGMII (SERDES) Only Mode

SGMII (SERDES) mode is also a PHY solution. The difference in SGMII (LVDS) mode is that the SERDES Primitive (MPCS for Nexus devices or MPPHY for Avant devices) is used as a PHY solution.

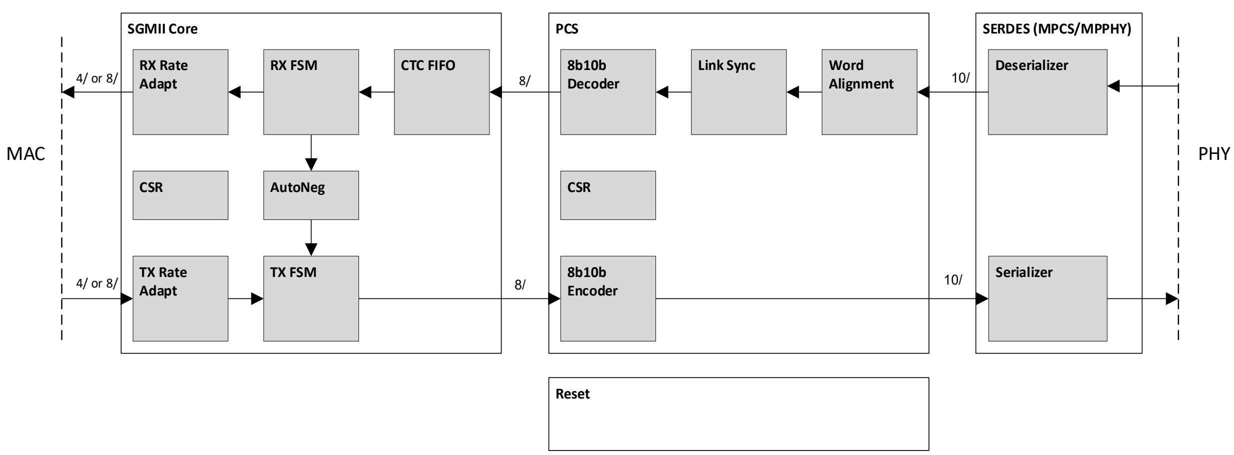

Figure 2.17. Detailed Block Diagram of the SGMII (SERDES) Only Mode

2.1.5. MAC + SGMII (LVDS) Mode

This is a MAC + PHY solution, integrating both MAC only and SGMII only modes. LVDS I/O pins is used as a PHY solution.

Note: The SGMII interface using LVDS I/O in Certus-NX, CertusPro-NX, MachXO5-NX, and CrossLink-NX FPGAs has limitations when operating across the full specified temperature range. Lattice recommends using alternative interfaces, such as SERDES or RGMII, for designs requiring Gigabit Ethernet. Refer to the Knowledge Base article for details. Contact your local Lattice sales representative for more information.

2.1.5.1. Multi-Rate SGMII Ethernet Option (LVDS)

MAC is configured to operate in *SGMII Easy Connect* option and PHY (SGMII (LVDS)) is configured to operate in *TSMAC Easy Connect* option. For the *Multi-Rate SGMII Ethernet* option, it can be configured to operate in either the 1G mode (1,000 Mbps data rate) or the Fast Ethernet mode (10/100 Mbps data rate) by setting the operation rate. Note that col_i and crs_i are for half duplex modes.

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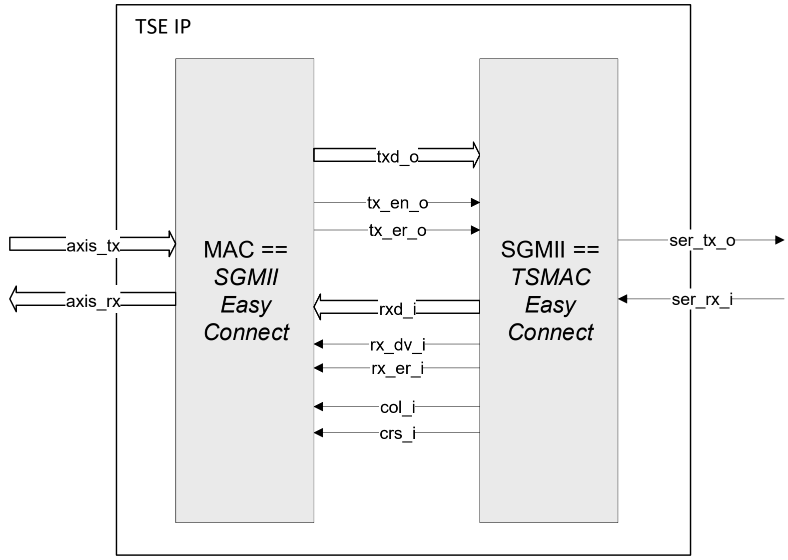

Figure 2.18. Top-Level Block Diagram for Multi-Rate SGMII Ethernet Option

2.1.5.2. Gigabit SGMII Ethernet Option (LVDS)

For the *Gigabit Ethernet* option, MAC is configured to operate in *Gigabit MAC* option and the PHY is configured to operate in *TSMAC Easy Connect* option. It only operates in 1G mode (1,000 Mbps data rate).

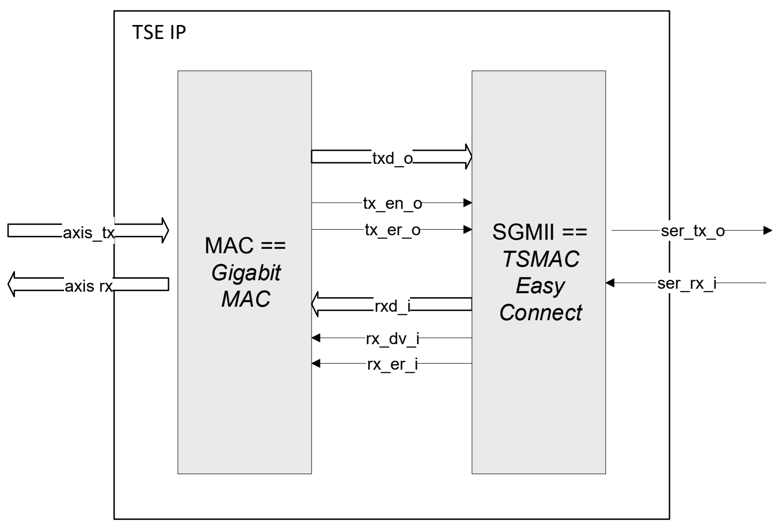

Figure 2.19. Top-Level Block Diagram of Gigabit SGMII Ethernet Option

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2.1.6. MAC + SGMII (SERDES) Mode

The MAC + SGMII (SERDES) mode is also a MAC + PHY solution that combines the MAC only mode and SGMII (SERDES) only mode. The difference in MAC + SGMII (LVDS) mode is that the SERDES Primitive (MPCS for CertusPro-NX devices and MPPHY for Avant devices) is used as a PHY solution.

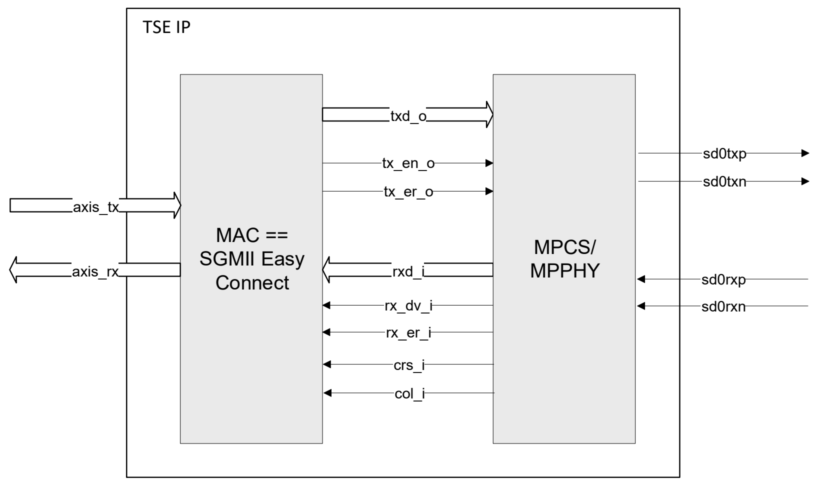

Figure 2.20. Top-Level Block Diagram of MPCS Gigabit Ethernet Option

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2.2. Clocking

2.2.1. Clocking for MAC Only

2.2.1.1. Clocking Overview

The following figure shows the clock network of the TSE IP (MAC). The clock frequency requirements are described in the Clock Interface section. Usage of the clocks are described in the Clocking section. In MAC only configuration, the corresponding clock and clock-enable are used to control the operating speed of MAC, based on the respective mode. Refer to Table 4.2 for the description of clocks and clock-enables. In MAC + PHY configuration, the tx_clk and rx_clk are connected internally to the output clock from the PCS block.

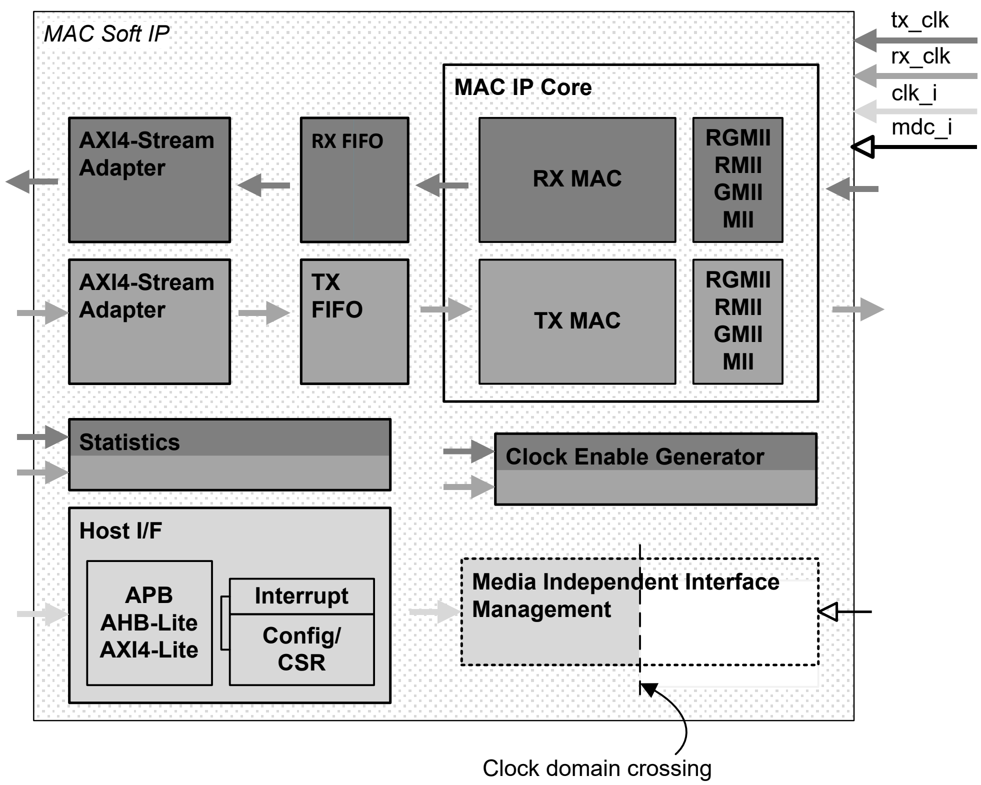

Figure 2.21. Clock Network Diagram—Simplified Clock Scheme Design

In the Simplified Clock Scheme Design—MAC only mode, the cycle of clock enable is generated based on the configuration on the Mode Register, Bit0 gbit_en, and Bit4 hundredbit_en. For the description on clock-enable, refer to Table 4.2. The following table shows the speed selection configuration through the Mode Register [0] and Mode Register [4].

Table 2.3. Speed Selection Configuration of the Simplified Clock Scheme Design

MAC Operating Option	Speed Selection	Mode Register [0], gbit_en	Mode Register [4], hundredbit_en
MII/GMII	1G	1	Don't care.
	100M	0	1
	10M	0	0
GMII	1G	Don't care.	Don't care.
SGMII Easy Connect	1G/100M/10M	Don't care. The operating speed in control by the clock enable signals, txmac_clk_en_i for TX side and rxmac_clk_en_i for RX side. Refer to Table 4.10.	

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MAC Operating Option	Speed Selection	Mode Register [0], gbit_en	Mode Register [4], hundredbit_en
RGMII	1G	1	Don't care.
	100M	0	1
	10M	0	0
RMII	100M	Don't care.	1
	10M	Don't care.	0

2.2.1.2. Clocking of Gigabit MAC

The following figure shows the clocking diagram of Gigabit MAC with GMII interface to external GMII Ethernet PHY. 125 MHz TX clock is provided to the TSE IP (MAC) core and external Ethernet PHY. The external PHY provides 125 MHz RX clocks to the TSE IP (MAC) core.

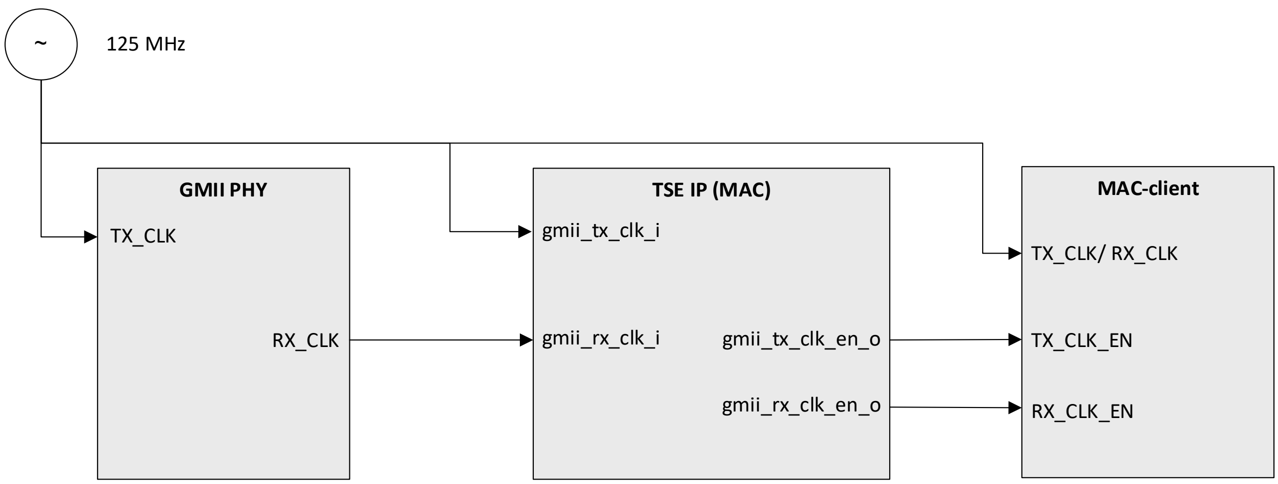

Figure 2.22. Clocking of Gigabit MAC—Simplified Clock Scheme Design

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2.2.1.3. Clocking of MII/GMII

The following figure shows the clocking diagram of MII/GMII operation to external Ethernet PHY. 125 MHz TX clock is provided to the TSE IP (MAC) and external Ethernet PHY. The external PHY provides 2.5/25 MHz clock to mii_gmii_tx_clk_i of the TSE IP (MAC) and 2.5/25/125 MHz clock to gmii_rx_clk_i. The MAC-client uses the 125 MHz clock with clock-enable generated by the TSE IP (MAC). Refer to Table 4.2 for the description of clock-enable.

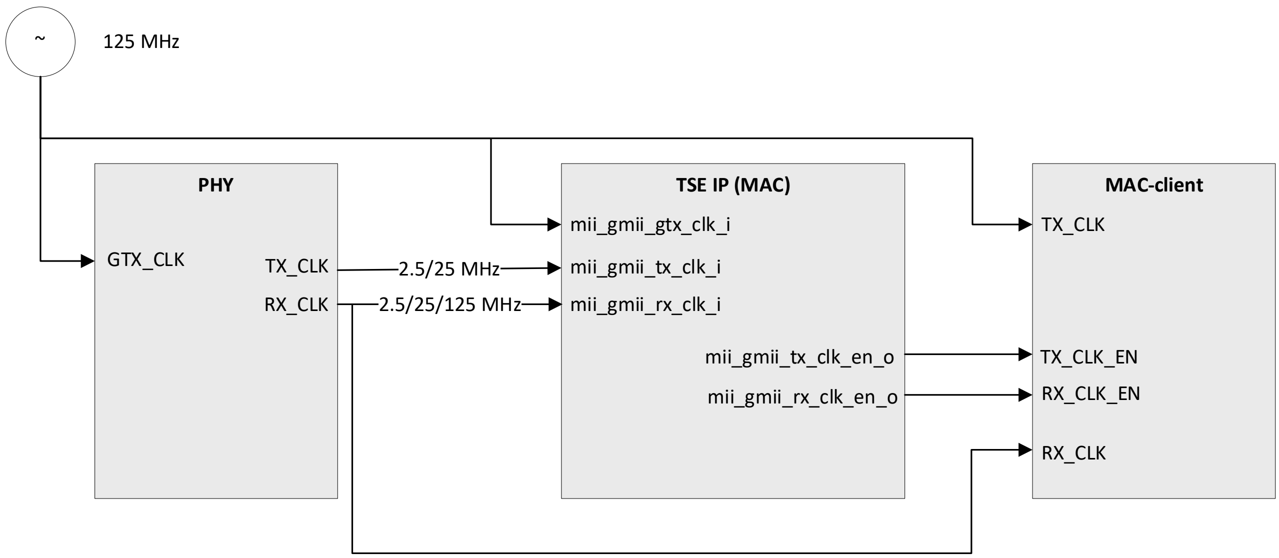

Figure 2.23. Clocking of MII/GMII—Simplified Clock Scheme Design

2.2.1.4. Clocking of RMII

The following figure shows the clocking diagram of the RMII operation to external Ethernet PHY. 50 MHz clock is provided to rmii_ref_clk_i of the TSE IP (MAC) and reference clock input of external Ethernet PHY. The MAC-client uses the 50 MHz clock with clock-enable generated by TSE IP (MAC). Refer to Table 4.2 for the description of clock-enable.

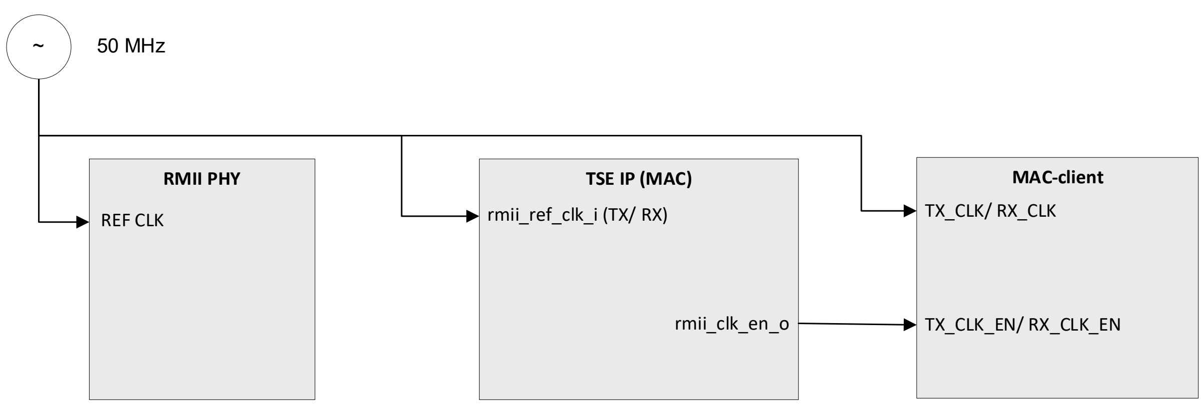

Figure 2.24. Clocking of RMII—Simplified Clock Scheme Design

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2.2.1.5. Clocking of RGMII

The following figure shows the clocking diagram of Gigabit MAC with RGMII interface to external RGMII Ethernet PHY. 2.5/25/125 MHz TX clock is provided to the TSE IP (MAC) and external Ethernet PHY. The external PHY provides 2.5/25/125 MHz RX clocks to the TSE IP (MAC) .

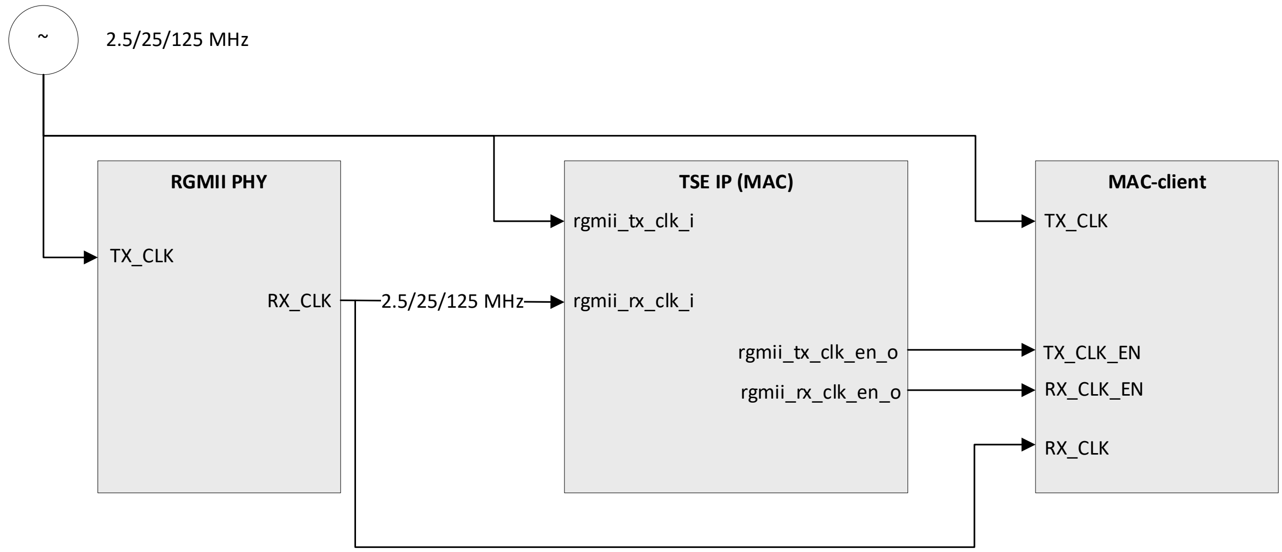

Figure 2.25. Clocking of RGMII—Simplified Clock Scheme Design

2.2.1.6. Clocking of TSE IP MAC Option (SGMII Easy Connect) and SGMII PCS (TSMAC Easy Connect)

The following figure shows the clocking diagram of the TSE IP (MAC) and SGMII PCS IP operating in 10/100/1000M. The 250 MHz reference clock is provided to the SGMII PCS, which produces 125 MHz datapath clocks for the TSE IP MAC option and SGMII PCS datapath. The TX and RX clock enable signals are not clock signals. However, they toggle according to current operating rates. In 10M, the clock enable signals asserted 1 every 100 clock cycles, while in 100M, the signals are asserted 1 every 10 clock cycles. In 1000M, the clock enable signals are always asserted.

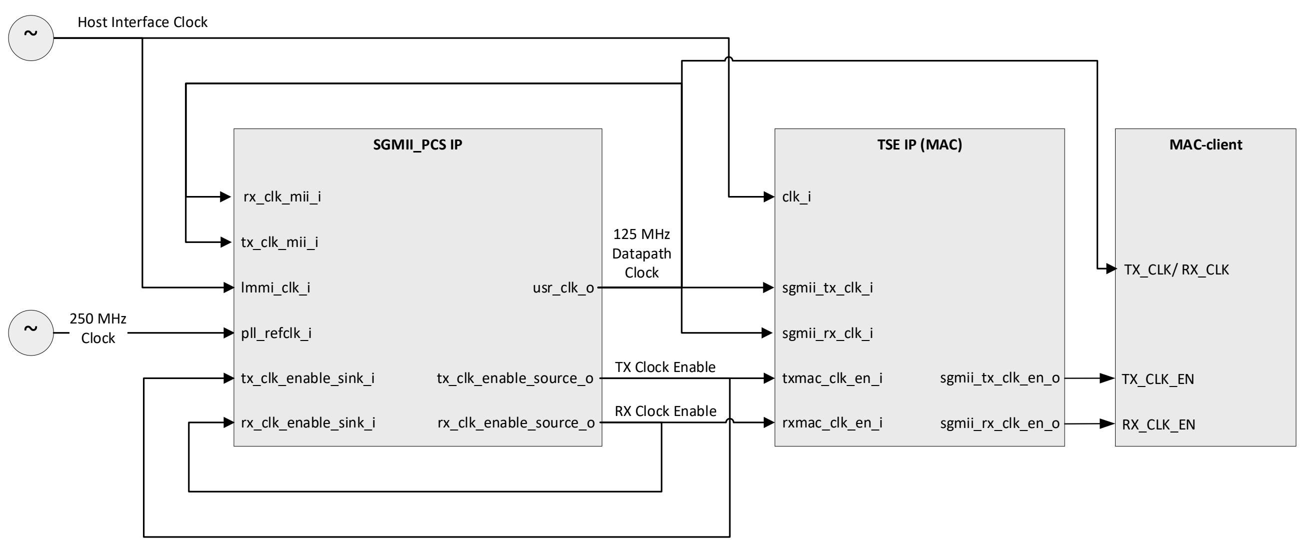

Figure 2.26. Clocking of TSE IP MAC Option (Gigabit MAC) and SGMII PCS (TSMAC Easy Connect)—Simplified Clock Scheme Design

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2.2.2. Clocking for SGMII (LVDS) Only

2.2.2.1. Clocking Overview

The following figure shows the clock network of the SGMII and Gb Ethernet PCS Core of the SGMII Only mode. The pll_ref_clk_i frequency is 250 MHz for Avant devices and 125 MHz for Nexus devices.

Note: The SGMII interface using LVDS I/O in Certus-NX, CertusPro-NX, MachXO5-NX, and CrossLink-NX FPGAs has limitations when operating across the full specified temperature range. Lattice recommends using alternative interfaces, such as SERDES or RGMII, for designs requiring Gigabit Ethernet. Refer to the Knowledge Base article for details. Contact your local Lattice sales representative for more information.

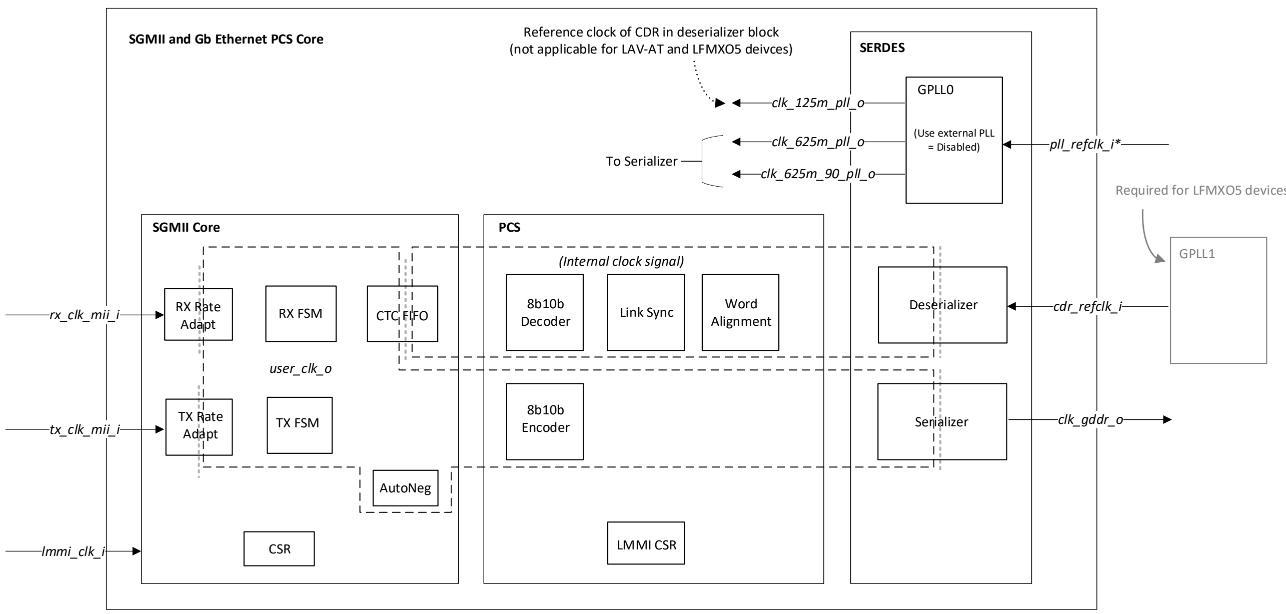

Figure 2.27. Clock Network Diagram of the SGMII (LVDS) Only Mode

2.2.2.2. Clocking of SGMII PCS in MII/GMII Mode (Classic)

When Classic Mode is selected, the following figure shows the clocking diagram with the recommended clock connections. Separate RX and TX MII clocks are recommended but they can be connected to the same source. Refer to the following table for the recommended clock frequencies.

Table 2.4. SGMII Only Clock Frequency for Classic Mode

Device	MII Interface Speed	[rx,tx]_clk_mii_i freq
Avant devices	1 Gbps	125 MHz
	100 Mbps	25 MHz
	10 Mbps	2.5 MHz
Nexus devices	1 Gbps	125 MHz
	100 Mbps	25 MHz
	10 Mbps	2.5 MHz

For robust timing synchronization and to mitigate CTC issues, ensure clk_mii_i and mii_gmii_clk_i must be sourced or derived from usr_clk_o. For clock generation, a 25 MHz clock can be directly synthesized using a PLL. However, a 2.5 MHz clock cannot be generated directly from the PLL, as the minimum output frequency is limited to 15.625 MHz for Avant devices and 6.25 MHz for Nexus devices.

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To achieve 2.5 MHz, you must first generate a higher-frequency clock using the PLL (for example., 25 MHz or 20 MHz), and then apply a CLKDIV or CLKDIVA block to divide it down. Supported division ratios typically include ÷2, ÷4, ÷5, ÷8, allowing flexible generation of lower-speed clocks from a common reference.

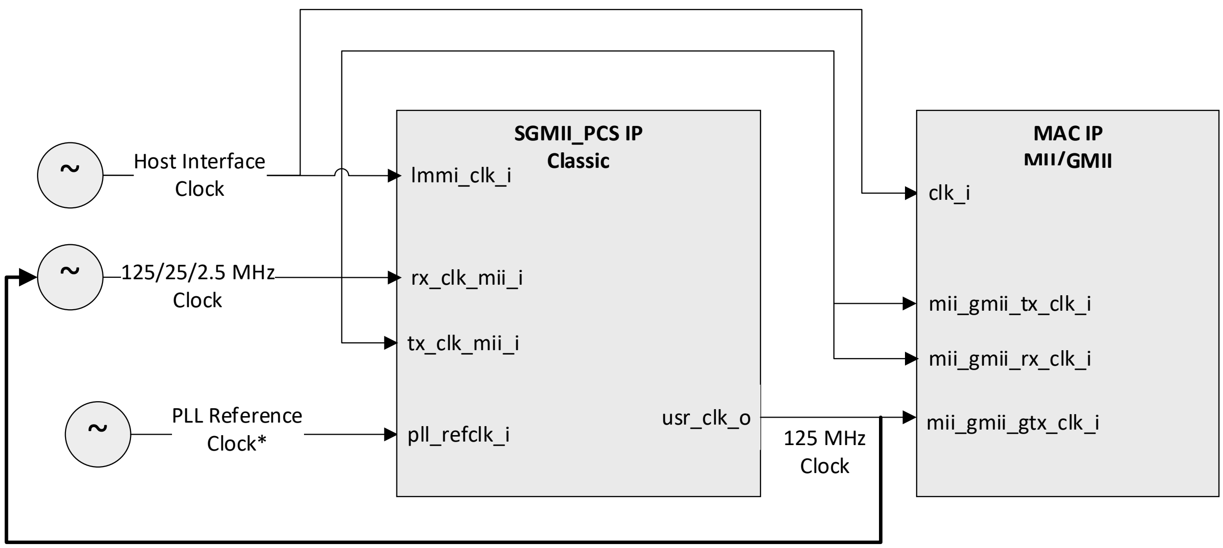

Figure 2.28. Clocking of SGMII (LVDS) PCS in MII/GMII (Classic) Mode

Dynamic switching between these clock frequencies—125 MHz, 25 MHz, and 2.5 MHz—based on the negotiated link speed requires careful handling to prevent glitches and timing hazards. A LUT-based clock multiplexer is used to select one of three input clocks and drive clk_mii_i. The recommended approach is to use the following reset-controlled clock switching:

- Assert Reset—Hold all downstream logic in reset before switching clocks.
- Switch Clock Source—Hold all downstream logic in reset before switching clocks.
- Deassert Reset
  - Release reset only after the clock switch is complete.
  - Logic resumes operation under the new clock domain.

2.2.2.3. Clocking of SGMII PCS in TSMAC Easy Connect Mode

When TSMAC Easy Connect mode is selected, the following figure shows the clocking diagram with the recommended clock connection. Refer to the following table for the recommended clock frequencies.

Table 2.5. SGMII Only Clock Frequency for TSMAC Easy Connect Mode

Device	[rx,tx]_clk_mii_i freq
Avant devices	125 MHz
Nexus devices	125 MHz

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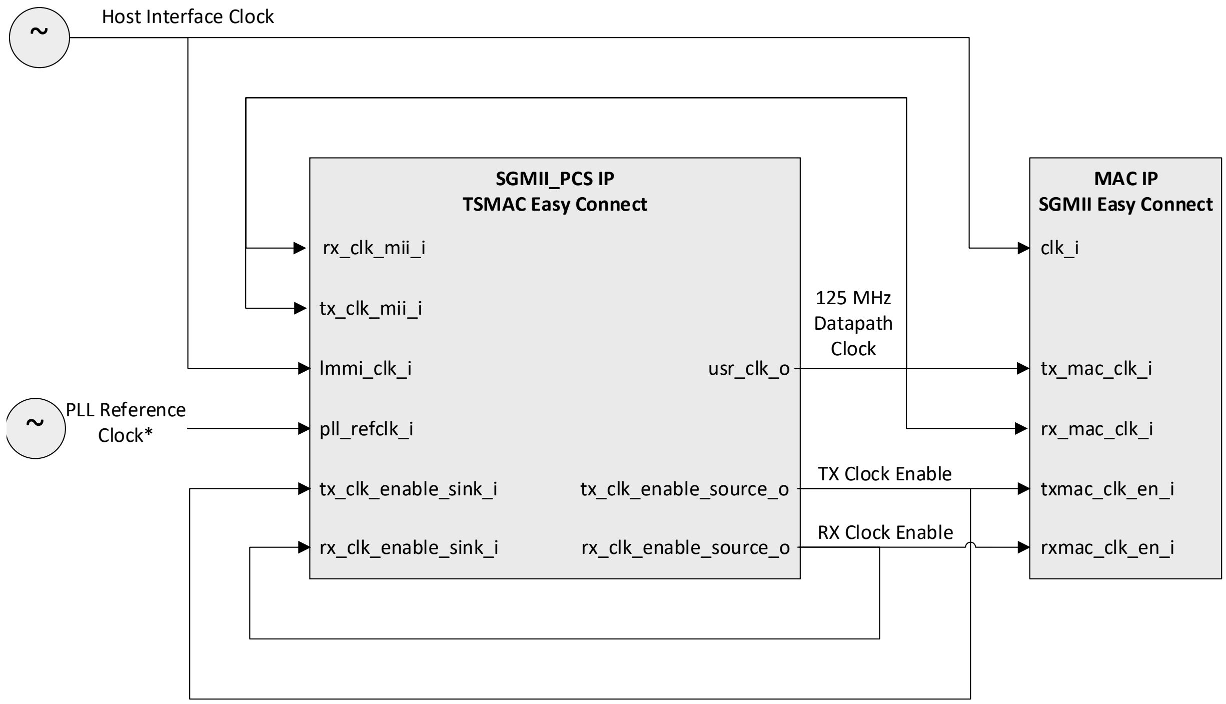

Figure 2.29. Clocking of SGMII (LVDS) PCS in TSMAC Easy Connect Mode

2.2.3. Clocking for SGMII (SERDES) Only

2.2.3.1. Clocking Overview

The following figure shows the clock network of the SGMII and Gb Ethernet PCS Core of SGMII (SERDES) Only Mode.

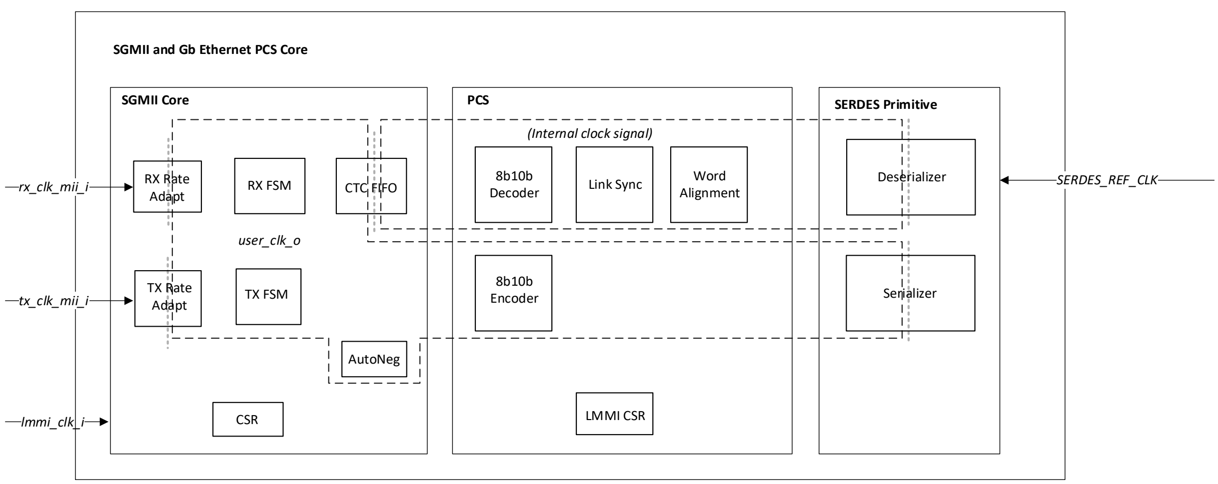

Figure 2.30. Clock Network Diagram, SGMII (SERDES) Only Mode

In this mode, the SERDES Primitive operates in MPCS bypass mode, leveraging the SERDES I/O as the Physical Medium Attachment (PMA). The SERDES Primitive for CertusPro-NX is MPCS, while the SERDES Primitive for Avant is MPPHY.

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2.2.3.2. Clocking of SGMII PCS in MII/GMII Mode (Classic) and TSMAC Easy Connect Mode

For clocking details of the SGMII PCS in MII/GMII Mode (Classic) and TSMAC Easy Connect Mode, refer to the Clocking of SGMII (LVDS) section, as the configurations are similar.

2.2.3.3. Clocking for SERDES Primitive of Nexus Devices

For SERDES primitive, MPCS on Nexus devices provides dynamic selection of reference clocks. The figure below illustrates the internal structure and signal connectivity of the clocks and clock mux in MPCS SERDES primitive.

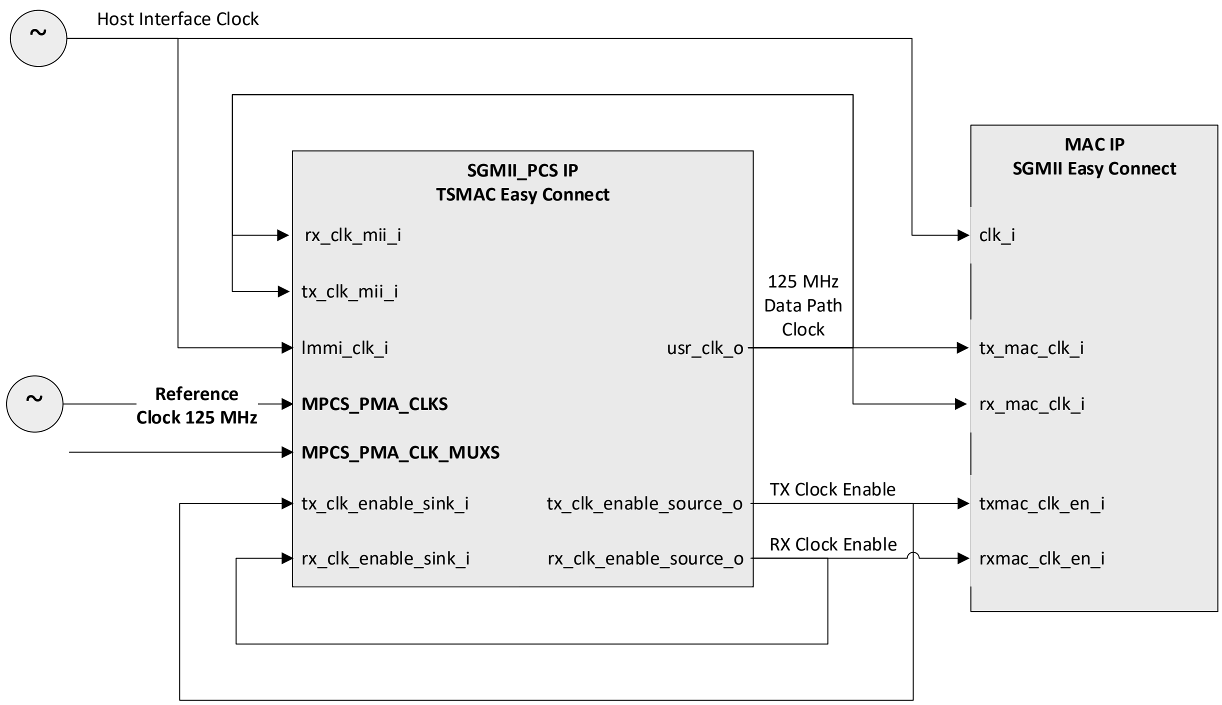

Figure 2.31. Clocking of SGMII (SERDES) PCS in TSMAC Easy Connect Mode (Nexus Devices)

All signals under MPCS_PMA_CLKS operate at a frequency of 125 MHz. This clock group includes the following:

- sd_ext_0_refclk_i
- sd_ext_1_refclk_i
- pll_0_refclk_i
- pll_1_refclk_i
- sd_pll_refclk_i
- sdq_refclkp_q0_i / sdq_refclkn_q0_i
- sdq_refclkp_q1_i / sdq_refclkn_q1_i

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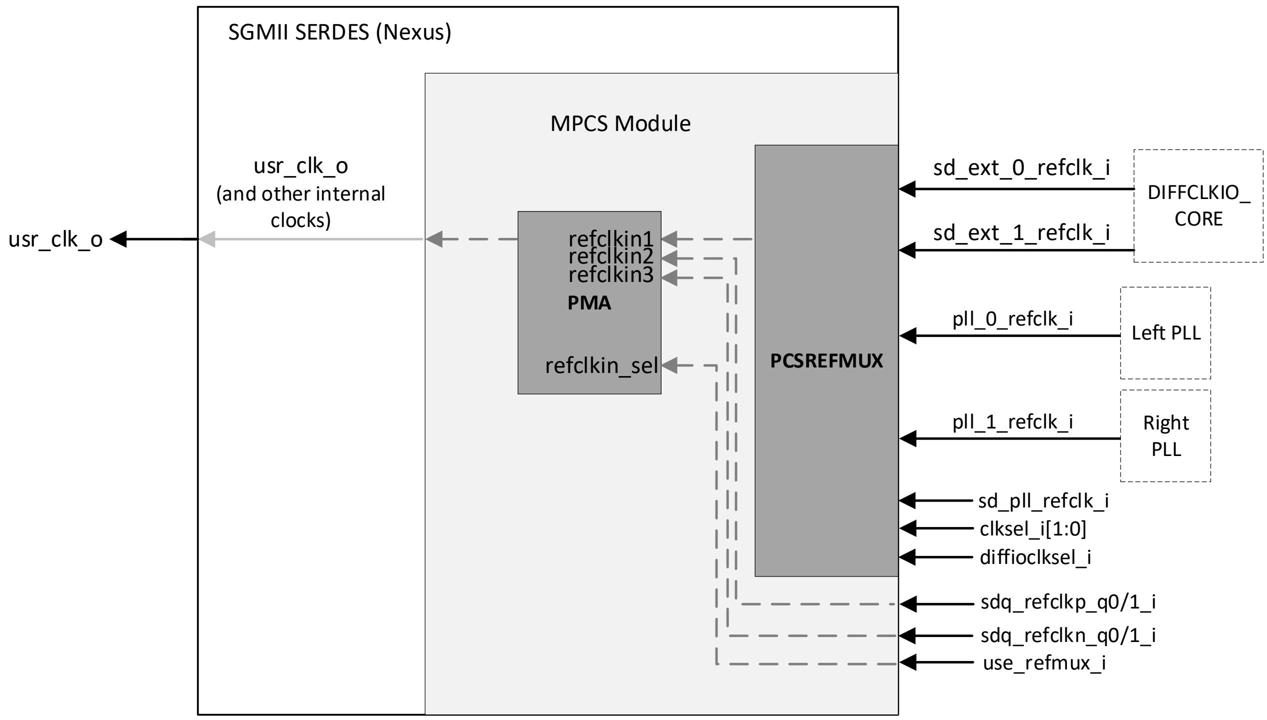

Figure 2.32. Reference Clock Dynamic Selection Block Diagram

The sdq_refclk signals (sdq_refclkp_q0/1_i and sdq_refclkn_q0/1_i) form differential clock pairs, these reference clocks can be sourced externally. Certain clock inputs must be sourced from the following designated components to ensure proper operation:

- sd_ext_0_refclk_i and sd_ext_1_refclk_i must be driven by the DIFFCLKIO_CORE.
- pll_0_refclk_i must be sourced from the LEFT PLL.
- pll_1_refclk_i must be sourced from the RIGHT PLL.

The diffioclksel_i, clksel_i, and use_refmux_i signals are clock multiplexers. The reference clock source control signals are set according to the table below.

Table 2.6. MPCS Reference Clock MUX Tree Control Signals

Reference Clock Control Signal	Usage
use_refmux_i	1’b1 – Use reference clock output from Clock MUX Tree (PCSREFMUX). 1’b0 – Use dedicated reference clocks (sdq_refclkp_q0/1_i and sdq_refclkn_q0/1_i).
diffioclksel_i	1’b1 – Use sd_ext_1_refclk_i as reference clocks. 1’b0 – Use sd_ext_0_refclk_i as reference clocks.
clksel_i[1:0]	2’b00 – Use pll_0_refclk_i as reference clocks. 2’b01 – Use pll_1_refclk_i as reference clocks. 2’b10 – Use reference clock based on diffioclksel_i. 2’b11 – Use sd_pll_refclk_i as reference clock.

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2.2.3.4. Clocking for SERDES Primitive of Avant Devices

For SERDES primitives, MPPHY on Avant devices, the reference clock is 156.25 MHz.

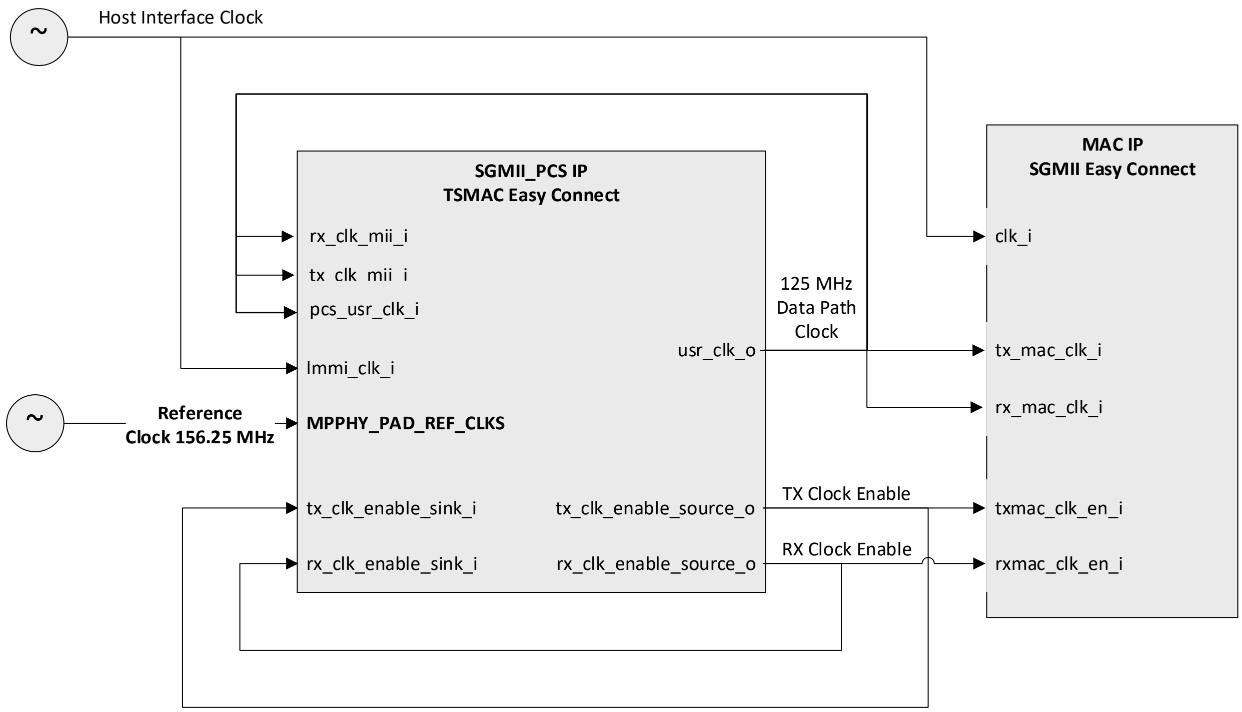

Figure 2.33. Clocking of SGMII (SERDES) PCS in TSMAC Easy Connect Mode (Avant Devices)

2.3. Reset

2.3.1. Reset Overview

The single reset signal of the IP reset_n_i is used to reset all logic in TSE IP when asserted. During power-up, the active-low reset must be asserted, and only de-asserted when all input clocks are valid and stable. The clock stability indicators vary depending on the source of the input clocks:

- PLL output clocks – Indicated by lock_o output port of PLL.
- SGMII PCS output clock, usr_clk_o – Indicated by phy_clk_ready output port of the SGMII PCS.
- Clocks from external PHY – Refer to the external PHY documentation.

To guarantee robust initialization under all operating conditions, the active low reset signal must remain deasserted for a minimum duration of 80 ns.

2.4. User Interfaces

Table 2.7. User Interfaces and Supported Protocols

User Interface	Supported Protocols	Description
Host Interface	• AHB-Lite • APB • AXI4-Lite	The host interface configures the TSE IP and to read out the status and statistics counters of the IP.
User Data Interface	AXI4-Stream	In transmit datapath, receive Ethernet packets from user logic and transmit to PHY. In receive datapath, forward received Ethernet packets from the PHY to user logic.

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User Interface	Supported Protocols	Description
PHY Interface	• MII • GMII • RMII • RGMII • SGMII	Interface with the SGMII & Gb Ethernet PCS IP or with external Ethernet PHY.
Management Interface	MDIO	Access registers of external Ethernet PHY.
Interrupt Interface	—	Send an interrupt signal to the processor for the occurrence of selected events.
Miscellaneous	—	Other MAC signals that are not described above.
MAC + PHY Interface	—	SGMII & Gb Ethernet PCS IP signals are available only in the MAC + PHY configuration.
PHY only (SGMII) MAC facing Interface	• MII/GMII mode (Classic) • TSMAC Easy Connect mode	Interface with the TSE MAC.
PHY only (SGMII) external interface	—	Similar to the external facing MAC + PHY interface.

2.4.1. Host Interface

2.4.1.1. AHB-Lite Interface

Refer to the AMBA 3 AHB-Lite Protocol version 1.0 Specification for the timing details of this protocol.

2.4.1.2. APB Interface

Refer to the AMBA 3 APB Protocol version 1.0 Specification for the timing details of this protocol.

2.4.1.3. AXI4-Lite Interface

The state changes according to the AXI4-Lite Manager, axi_arvalid and axi_awvalid. Assertion of arvalid or awvalid must be held until the completion of the respective request.

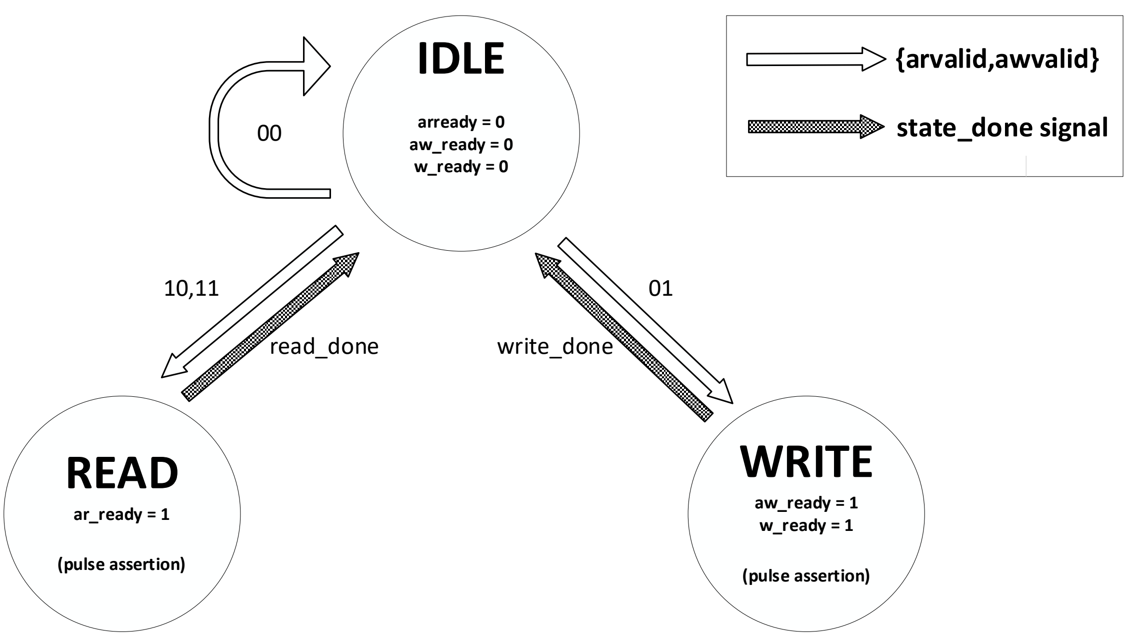

Figure 2.34. State Machine

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- IDLE: Stay idle when both axi_arvalid and axi_awvalid are deasserted.
- READ: Read request when axi_arvalid is asserted, prioritize read if both axi_arvalid and axi_awvalid are asserted.
- WRITE: Write request when only axi-awvalid is asserted.

For the READ state, after a read request is completed, the axi_arready will be pulse-asserted. A handshake happens at the read address channel. For the WRITE state, after a write request is completed, the axi_awready, axi_arready and axi_bready will be pulse-asserted. Handshakes happen at write address channel, write data channel, and write response channel. Whereas axi_rvalid can be asserted at any state, the assertion is held until axi_rready is high. A handshake happens at read data channel. The AXI4-Lite Manager must halt the reading request if axi_rready is low.

Refer to the AMBA 4 AXI4-Lite Protocol version 1.0 Specification for the timing details of this protocol.

2.4.2. Media Independent Interface Management

The Media Independent Interface Management Module (MIIM) accesses management information from the PHY device and writes to or reads from the PHY registers. The MIIM is compliant to the MDIO defined in the IEEE 802.3 Clause 22. A single MIIM can address up to 32 PHY devices. This module runs off its own clock called mdc_i. The standard specifies this clock to be at maximum 2.5 MHz.

The MIIM read or write operations are specified in the GMII Management Register Access Control register. This register also specifies the addressed PHY and the register within the PHY that needs to be accessed. The cmd_fin bit in the GMII Management Register Access Control register is reset as soon as a command to read or write is given. It is set only when the MIIM module completes the operation. While the interface is busy, the GMII Management Register Access Control register cannot be overwritten, and all write operations to the register are ignored.

For a write operation, the data to be written is stored in the GMII Management Access Data register. For a read operation, the data read from the addressed PHY is stored in this register. The ready bit in the GMII Management Access Control is set at the end of the read/write operation.

2.5. Datapath

The following figures show the select frame formats of data transmitted and received on the Ethernet network that the TSE IP core supports.

PREAMBLE 7 bytes	SFD 1 byte	DESTINATION ADDRESS 6 bytes	SOURCE ADDRESS 6 bytes	LENGTH/ TYPE 2 bytes	DATA/PAD 46-1,500 bytes	FRAME CHECK SEQUENCE 4 bytes

Figure 2.35. Un-Tagged Ethernet Frame Format

PREAMBLE 7 bytes	SFD 1 byte	DESTINATION ADDRESS 6 bytes	SOURCE ADDRESS 6 bytes	VLAN TAG HEADER 4 bytes	LENGTH/ TYPE 2 bytes	DATA/PAD 46-1500 bytes	FRAME CHECK SEQUENCE 4 bytes

Figure 2.36. VLAN-Tagged Ethernet Frame Format

PREAMBLE 7 bytes	SFD 1 byte	DESTINATION ADDRESS 01-80-C2-00-00-01 6 bytes	SOURCE ADDRESS 6 bytes	LENGTH/ TYPE 88-08 2 bytes	MAC CTL OP_CODE 00-01 2 bytes	OP_CODE PARAMS/RSV 44bytes	FRAME CHECK SEQUENCE 4 bytes

Figure 2.37. Ethernet Control Frame Format

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On the receiving side, data received from the G/MII interface is first buffered until sufficient data is available to be processed by the Receive MAC (RX MAC). The Preamble and the Start-of-Frame Delimiter (SFD) information are then extracted from the incoming frame to determine the start of a valid frame. The Receive MAC checks the address of the received packet and validates whether the frame can be received before transferring it into the FIFO. Only valid frames are transferred into the FIFO (runts and fragments are discarded). The RX MAC also provides a statistics vector on a 'per packet' basis that can be used by the application. The MAC always calculates cyclic redundancy check (CRC) to check whether the frame was received error-free.

On the transmit side, the TX MAC is responsible for controlling access to the physical medium. The TX MAC reads data from TX FIFO, formats this data into an Ethernet packet and passes it to the G/MII module. The TX MAC reads data from the TX FIFO when a packet is available, and the TX MAC is in its appropriate state. The TX MAC pre-fixes the Preamble and the SFD information to the data and appends the frame check sequence (FCS) at the end of the data. In half-duplex operation, the TX MAC stores the first 64 bytes of data from FIFO in an internal buffer, to be used in re-transmitting data on collisions.

A tagged frame includes a 4-byte VLAN Tag field, which is located between the Source Address field and the Length/Type field. The VLAN Tag field includes the VLAN Identifier and other control information needed when operating with Virtual Bridged LANs as described in IEEE P802.1Q.

2.5.1. Receive MAC

The main function of the RX MAC is to accept formatted data from the G/MII interface and pass it to the AXI-4 Stream interface through FIFO. During this operation, the RX MAC performs the following functions:

- Detect the start of the frame
- Compare MAC address
- Re-calculate CRC
- Process the control frame and pass it to the flow control module

The RX MAC operation is determined by programming the Mode and Transmit and Receive Control Registers. For register definitions and bit descriptions, refer to the Register Description section. Note that you must set the bits for the gbit_en and hundredbit_en mode registers to change or select the MAC operating speed—10M, 100M or 1G. For more information on mode registers, refer to the [0x000] Mode Register section. Events that occur during reception of a frame are logged into the rx_stat_vector_o signal and the Transmit and Receive Status Register. The MAC can report information about miscellaneous events such as:

- FIFO overflow
- CRC error
- Receive error
- Short frame reception
- Long frame reception
- IPG violation

By default, the entire frame (except Preamble and SFD bytes) is sent to FIFO through the RX MAC application interface signals. If you do not want to receive the FCS, the core can be programmed to strip the FCS field as well as any PAD bytes in the frame and send the rest to the FIFO. The RX MAC section operates on the rxmac_clk_i derived from the rx_clk sourced from the PHY. All the signals on the Receive MAC FIFO interface are synchronous to this clock. The RX MAC is disabled while Rx_en is Low (Bit_2 of the Mode Register) and should be enabled only after the associated registers are properly initialized.

2.5.1.1. Receiving Frames

The frames received by the RX MAC are analyzed and the Preamble and SFD bytes are stripped off the frame before it is transferred to the RX FIFO. The AXI-4 Stream interface that is used to read the RX data from the RX FIFO is eight bits wide. The default operation for RX MAC is to transfer the unmodified frame after stripping off the Preamble and SFD bytes. This behavior can be changed by setting bit [1] of the Transmit and Receive Control Register. When bit [1] is set, the RX MAC strips the Preamble, SFD, FCS bytes, and the PAD bytes, if any. Note that the RX MAC assumes that the received frame has PAD bytes if a 64-byte packet is received with its Length/Type field set to the value of less than 46 bytes.

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2.5.1.2. Address Filtering

The RX MAC offers several address filtering methods that you can utilize to effectively block unwanted frames. It also provides a Promiscuous mode in which all supported filtering schemes are abandoned and the RX MAC transfers all the frames irrespective of the address they contain. By default, the RX MAC is configured to filter and discard Broadcast frames (For example, all bits of the received DA == 1) and multicast frames (that is bit[0] of the received DA == 1).

The MAC can be configured to receive broadcast frames by setting bit [7] of the Transmit and Receive Control Register. Multicast frames are received only when bit [4] of the Transmit and Receive Control Register is set. When set, multicast frames are subject to filtering that is dependent on a 64-bit hash table lookup. The 64-bit hash table is organized as eight 8-bit registers. The six middle bits of the most significant byte of the CRC calculated for the destination address field of the frame are used to address one of the 64 bits of the hash table.

The three most significant bits of the calculated CRC select one of the eight tables, and the three least significant bits select a bit. The frame is received only if the retrieved bit is set. The IP registers specifying the hash tables contents are described in the Register Description section. All other regular frames are filtered based on the RX MAC address that is programmed into the MAC address (0, 1, 2) registers.

2.5.1.3. Filtering Based on Frame Length

The default minimum Ethernet frame size is 64 bytes. Any frame smaller than 64 bytes could be a collision fragment. By default, the RX MAC is configured to ignore frames shorter than 64 bytes. You can configure the MAC to receive shorter frames by setting bit [8] of the Transmit and Receive Control Register. Whenever a short frame is received, the appropriate bit is set in the statistics vector, marking it as a Short frame.

The RX MAC has been designed to receive frames larger than the standard specified maximum as easily as any other frame, thus, it may be used in environments that generate jumbo frames. However, for statistical purposes, you can set the maximum length of the frame in the Maximum Packet Size Register. When the received frame is larger than the number in this register, bit [31] of the Receive Statistics Vector bus is set, marking it as a Long frame.

2.5.1.4. Receiving a Pause Frame

When the RX MAC receives a pause frame, the TX MAC continues with the current transmission then pauses for the duration indicated in the pause time. During this time, the TX MAC can transmit Control frames. Although pause frames may contain the Multicast Address, Multicast filtering rules does not apply to pause frames.

If bit [3] of the Transmit and Receive Control Register is set, the RX MAC signals the TX MAC to stop transmitting for the duration specified in the frame. If this bit is reset, the RX MAC assumes the TX MAC does not have the pause capability and/or does not wish to be paused and so the RX MAC does not signal it to stop transmitting. If the drop control, bit[6] in the Transmit and Receive Control Register is set, the pause frame is received but dropped internal to the MAC and is not transferred to the FIFO. Otherwise, the pause frame is received and transferred to FIFO.

2.5.2. Transmit MAC

The Transmit MAC (TX MAC) is responsible for controlling access to the physical medium. The TX MAC reads data from a TX FIFO when the FIFO is not empty and when it detects an active tx_fifoavail. The TX MAC then formats this data into an Ethernet packet and passes it to the G/MII module. The TX MAC is disabled while tx_en is low (bit[3] of the Mode Register) and should only be enabled after the associated registers are properly initialized. Once enabled, the TX MAC continuously monitors FIFO interface for an indication that frame(s) are ready to be transmitted. The TX MAC and TX FIFO interface operations are synchronous to txmac_clk_i.

In 10/100 mode, the TX MAC can be configured to operate in either half-duplex or full-duplex mode. This is done by writing to bit [5] of the Transmit and Receive Control Register. In a full-duplex operation, the receiver’s buffer may be filled up quickly. When this happens, the receiver sends flow control (Pause) frames to the transmitter, requesting it to stop transmitting. The transmitter finishes transmitting the current frame and stops for the duration specified in the pause frame.

2.5.2.1. Transmitting Frames

By default, the TX MAC is configured to generate the FCS pattern for the frame to be transmitted. However, this can be prevented by setting bit [2] of the Transmit and Receive Control Register. This feature is useful if the frames being presented for transmission already contain the FCS field. When the FCS field generation is disabled, you must ensure

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that short frames are properly padded before the FCS is generated. If the MAC receives a frame shorter than 64 bytes when FCS generation is disabled, the frame is sent as is and a Statistic Vector for the condition is generated.

The DA, SA, L/T, and DATA fields are derived from higher applications through the AXI4-Stream interface and then encapsulated into an un-tagged Ethernet frame. This frame is not sent over the network until the network has been idle for a minimum of Inter-Packet Gap (IPG) time.

The frame encapsulation consists of adding the Preamble bits, the SFD bits and the CRC checksum to the end of the frame (FCS). If padding is not disabled, all short frames are padded with hexadecimal 00. The TX MAC requires a continuous stream of data for the entire frame. There cannot be any bubbles of “no data transfer” within a frame. If the MAC was able to transmit a frame without any errors, the tx_done signal is asserted. Once the transmission has ended, data on the tx_statvec_o bus is presented to the client, including all the statistical information collected in the process of transmitting the frame. Data on this bus is qualified by asserting the tx_staten_o signal.

After the TX MAC is done transmitting a frame, it waits for more frames from the FIFO interface. During this time, it goes to an idle state; this can be detected by reading the Transmit and Receive Status Register. Since the Mode Register can be written at any time, the TX MAC can be disabled while it is actively transmitting a frame. In such cases, the MAC completely transmits the current frame and then returns to the idle state. The control registers should be programmed only after the MAC has returned to the idle state.

2.5.2.2. Transmitting a Pause Frame

Two different methods are used for transmitting a pause frame. In the first method, the application layer forms a pause frame and submits it for transmission via the AXI4-Stream interface. In the other method, the application layer signals the TX MAC directly to transmit a pause frame. This is accomplished by asserting tx_sndpausreq_i. In this case, the TX MAC completes transmission of the current packet and then transmits a pause frame with the pause time value supplied through the tx_sndpaustim_i bus.

2.5.2.3. Retries on Collision

When operating in the half-duplex mode, the TX MAC has the capability to perform re-transmission of frames that have experienced in-window collision up to the specified maximum. This is possible because the MAC always buffers the first 64 bytes of the frame.

If the MAC has been disabled while it is backing off (soon after a collision), it only returns to the idle state after it has successfully transmitted the frame or has exceeded the retry limit.

In the 10/100 mode, the TX MAC provides the following information:

- Whether the frame deferred before transmission
- The number of times the frame experiences collision before transmission

This information is sent as part of the statistics vector. For a frame transmitted without any errors, the statistics vector qualified by the enable signal is asserted along with the tx_done_o signal. When the frame experiences excessive collision or late collision, the statistics bit for the appropriate condition is set and the tx_discfrm_o signal is asserted. This indicates an error condition.

2.6. Statistics Vector

By default, the Statistics Vector is generated for all received frames transferred to the FIFO. If you want the RX MAC to ignore all incoming frames, the input signal ignore_pkt_i must be asserted. The frame that should have been received is consequently ignored, and the RX MAC sets the Packet Ignored bit (bit [26]) of the Statistics Vector. The Maximum Packet Size Register is programmed by you as a threshold for setting the Long Frame bit of the Statistics Vector. This value is only used for un-tagged frames. The RX MAC adds “4” to the value specified in this register for all VLAN Tagged frames when checking against the number of bytes received in the frame. This is because all VLAN Tagged frames have an additional four bytes of data. When a tagged frame is received, the entire VLAN Tag field is stored in the *VLAN Tag* Register. Additionally, every time a Statistics Vector is generated, some of the bits are written into the corresponding bit locations [9:1] of the *Transmit and Receive Status* Register. This is done so that you can get this information via the Host interface.

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Table 2.8. Receive Statistics Vector Description

Bit	Description
31	Long Frame. This bit is set when a frame longer than length specified in the *Maximum Packet Size* Register is received.
30	Short Frame. This bit is set when a frame shorter than 64 bytes is received.
29	IPG Violation. This bit is set when a frame is received before the IPG timer runs out (96 bit times).
28	PTP 1588 frame. This bit is set when the MAC receives a PTP 1588 frame.
27	Carrier Event Previously Seen. When asserted, it indicates that a carrier event was detected since the last frame.
26	Packet Ignored. When set, this bit indicates the incoming packet is to be ignored.
25	CRC Error. This bit is set when a frame is received with an error in the CRC field.
24	Length Check Error. This bit is set if the number of data bytes in the incoming frame do not match the value in the length field of the frame.
23	Receive OK. This bit is set if the frame is received without any error.
22	Multicast Address. This bit is set to indicate that the received frame contains a Multicast Address.
21	Broadcast Address. This bit is set to indicate that the received frame contains a Broadcast Address.
20	Dribble Nibble. This bit is set when only four bits of the data presented on the RS interface are valid.
19	Unsupported Opcode. This bit is set if the received control frame has an unsupported opcode. In this version of the IP, only the opcode for pause frame is supported.
18	Control Frame. This bit is set to indicate that a Control frame was received.
17	Pause Frame. This bit is set when the received Control frame contains a valid pause opcode.
16	VLAN Tag Detected. This bit is set when MAC receives a VLAN Tagged frame.
15:0	Frame Byte Count. This bus contains the length of the frame that is received. The frame length includes the DA, SA, L/T, TAG, DATA, PAD and FCS fields.

For every frame transmitted, the statistics vector is generated including all the statistical information collected in the process of transmitting the frame.

Table 2.9. Transmit Statistics Vector Description

Bit	Description
31	PTP 1588 frame. This bit is set when the MAC transmits a PTP 1588 frame.
30	FCS generation is disabled, and short frame was transmitted.
29:26	Number of early collisions.
25	Excessive collision.
24	Late collision.
23	Excessively deferred transmission.
22	Deferred transmission.
21:8	Number of bytes in the transmitted frame.
7	VLAN tagged frame. This bit is set when a VLAN tagged frame is transmitted.
6	Pause frame. This bit is set when a pause frame is transmitted.
5	FIFO under-run.
4	Jumbo frame. This bit is set when the Jumbo frame is transmitted.
3	Bad FCS frame.
2	Broadcast frame. This bit is set when a Broadcast frame is transmitted.
1	Multicast frame. This bit is set when a Multicast frame is transmitted.
0	Unicast frame. This bit is set when a Unicast frame is transmitted.

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2.7. Lane Merging

2.7.1. Lane Merging for SERDES Primitive of Avant Devices

2.7.1.1. Overview

The MPPHY block is a quad made up of four lanes (X4). You can configure the quad to use each lane individually, enabling you to merge multiple MPPHY instances into a single physical quad. This maximizes the usage of silicon resources in your design.
Note: Lane merging is only supported by LAV-AT-G70 and LAV-AT-X70 devices.

2.7.1.2. Usage

Each TSE SGMII IP instantiates an MPPHY foundation IP configured with a 1X1 link width, which occupies a single lane of a quad. By default, the Radiant software attempts to merge MPPHY instances to minimize the device power consumption.

If you want to override this behavior and select specific locations for the MPPHY instances, you can set the LANE ID configuration of the IP according to the number of quads you want to use.

To set the Lane ID, follow these steps:

1. In the **Select IP Option** field, select **SGMII(SERDES) only** or **MAC + SGMII(SERDES)**.
2. In the **PCS Lane ID** field, set the lane ID configuration of the IP as shown in the figure below. By default, the ID is set to **AUTO**. If the **AUTO** Lane ID is selected, the pin location assignment must be included in the sdc or ldc constraint file. If the ID is not set to **AUTO**, in the case of a conflict between the Lane ID configuration and a top-level design port constraint, the top-level design port constraint takes precedence, which means the Lane ID setting is ignored and a warning message is shown.

The LAV-AT-G/X70 silicon supports up to seven usable quads, depending on the package. Each MPPHY block occupies one quad and consists of four lanes (X4 configuration). Therefore, a fully populated device can contain up to 28 lanes across seven quads. The lane-to-quad mapping is as follows:

Table 2.10. Quad-to-Lane ID Mapping for LAV-AT-G/X70

Quad	LANE_IDs
0	0, 1, 2, 3
1	4, 5, 6, 7
2	8, 9, 10, 11
3	12, 13, 14, 15
4	16, 17, 18, 19
5	20, 21, 22, 23
6	24, 25, 26, 27

Lane merging is performed within individual quads only. Each quad consists of four consecutive lane IDs, and merging is restricted to lanes that belong to the same quad. This ensures proper alignment and compatibility within the MPPHY architecture. For example, lanes 0 and 2 can be merged because they reside in Quad 0, but lane 3 cannot be merged with lane 4 because they belong to different quads (Quad 0 and Quad 1, respectively).

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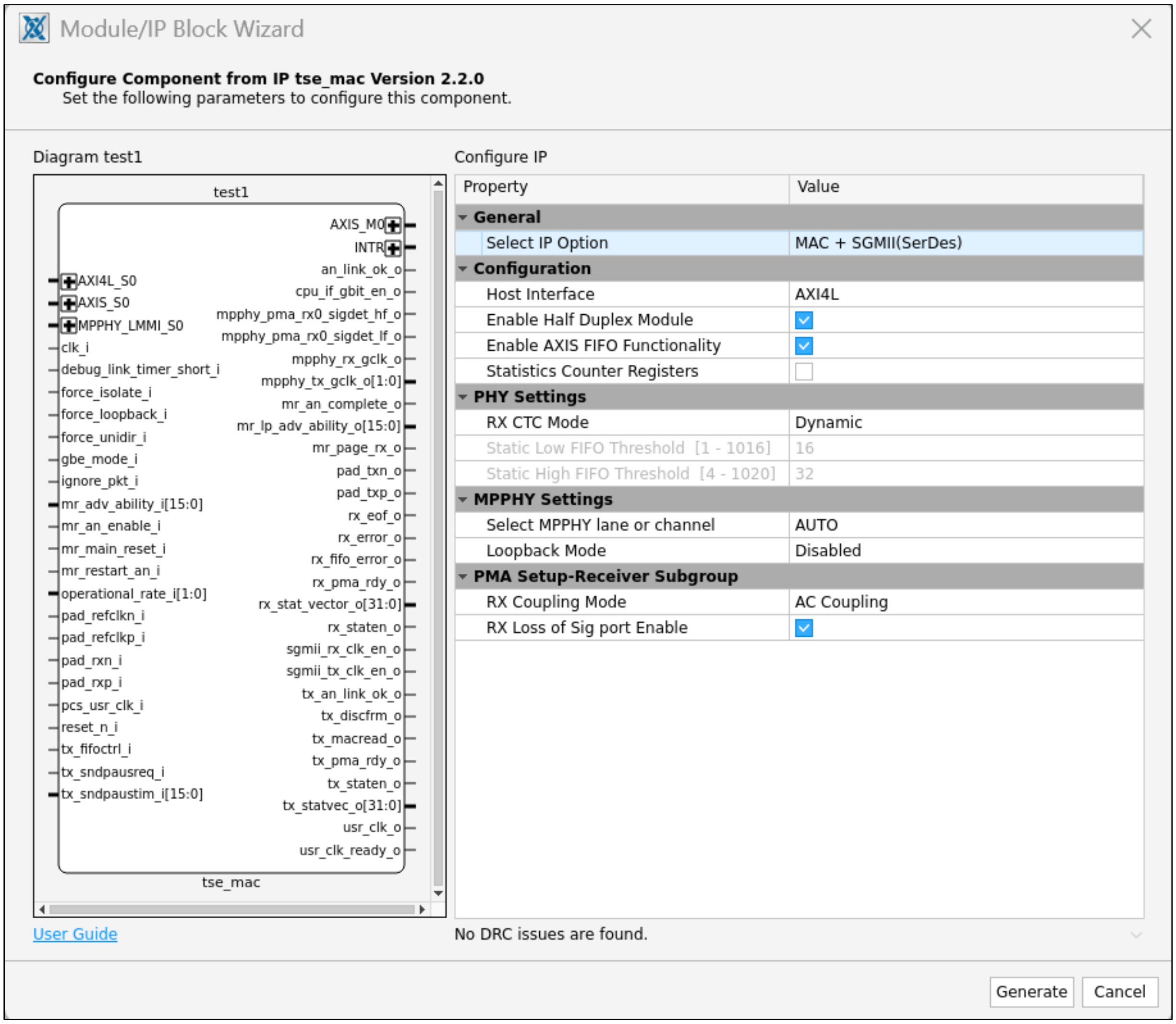

Figure 2.38. Set the Lane ID Configuration of the MAC + SGMII (SERDES)

2.7.1.3. Lane Merging Report

During lane merging, the Post-Synthesis process produces a report file named *mpphy_lane_assignment.mrf* in the project's active implementation folder that shows how the MPPHY design instances were merged into the device MPPHY quads. You can open the report file with any text editor.

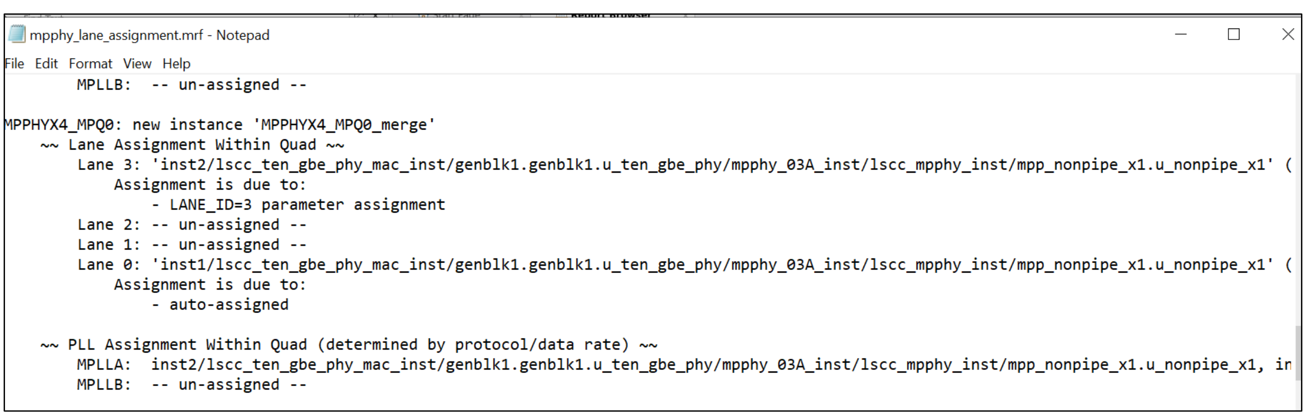

Figure 2.39. Lane Merging Report File

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2.7.1.4. Restrictions and Limitations

To merge instances into the same quad, instances must abide by the following restrictions:

- Shared reference clock connection.
- Shared LMMI clock and reset connections.
- Compatible PLL settings (this is protocol/data rate dependent, and will be configured by the IP Catalog tool)
- Compatible "per-quad" connections – a limited number of ports exposed on the MPPHY IP physically have only a single instance on the silicon. These must be connected to the same net if it is an input, or have a maximum of one connected per-quad if it is an output.
- For output clock, use only output clock from one instance of the quad to drive the logic. Because output clocks from other IP instance intent to be merged to the same quad, do not use the clock to drive any logic.

Table 2.11. Signal Mapping Between MPPHY and TSE IP

MPPHY	TSE IP—SGMII (SERDES) only	TSE IP—MAC + SGMII (SERDES)
lmmiclk_q0_i	clk_i	lmml_clk_i
refclk_p_q0_i refclk_n_q0_i	pad_refclkp_i pad_refclkn_i	pad_refclkp_i pad_refclkn_i
lmmireset_n_q0_i	reset_n_i	rst_n_i
txoutgclk_pll0_q0_o	xg_tx_gclk_o[0] usr_clk_o	xg_tx_gclk_o[0] usr_clk_o
txoutgclk_pll1_q0_o	xg_tx_gclk_o[1]	xg_tx_gclk_o[1]

If any of these restrictions are violated, the Radiant software will not automatically merge the MPPHY instances into a single quad. If user constraints or lane assignment forces incompatible MPPHY instances into the same quad, an error message is issued, and the Radiant software flow will not continue past the Post-Synthesis stage.

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The diagram below shows how to connect the signal that has restriction and limitation for lane merging. To ensure proper quad merging and maintain clock domain integrity, only one lane's output clock—typically from LANE0—must be used to drive downstream logic. Output clocks from other lanes within the same quad (LANE1–LANE3) must not be used for logic purposes. Additionally, all input signals across the lanes must be connected to the same source to guarantee consistent behavior and synchronization. These restrictions prevent ambiguity in clock domain crossings and allow the Radiant software to merge all MPPHY instances into a single quad correctly during synthesis.

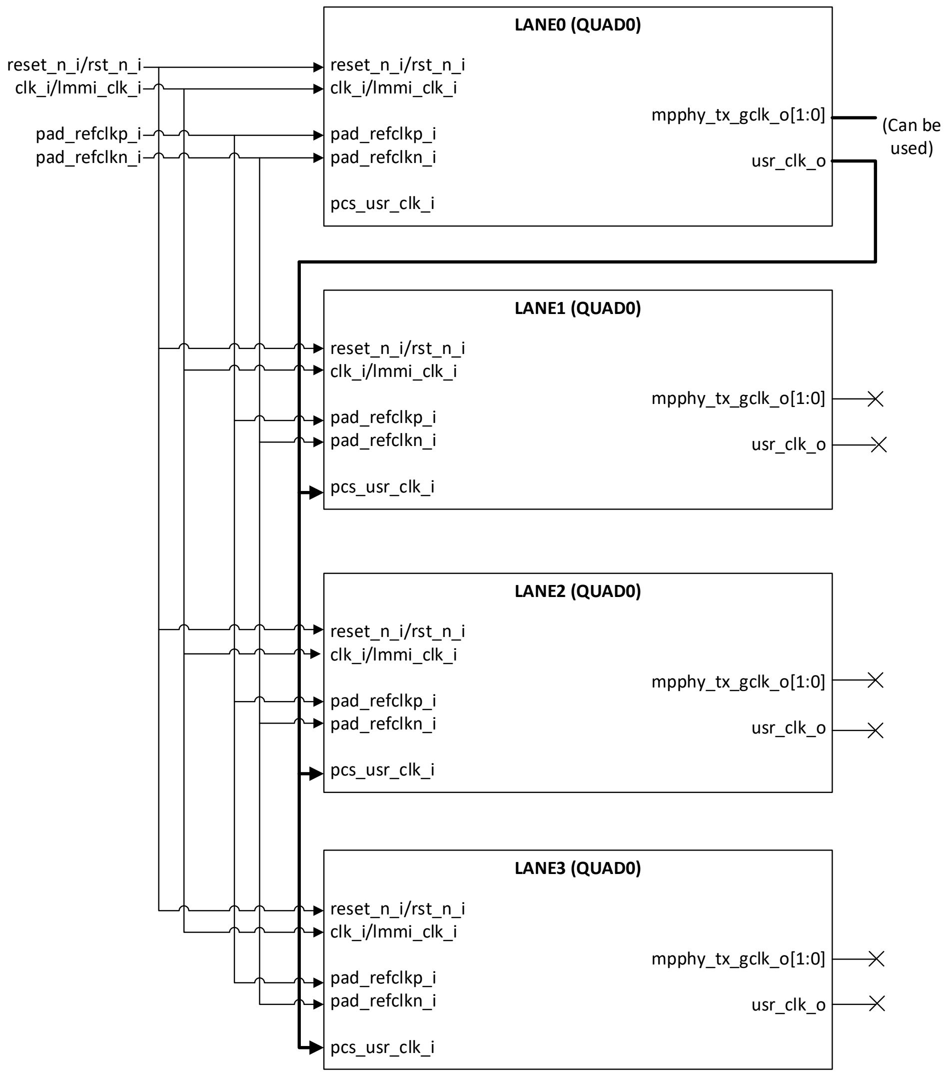

Figure 2.40. Lane Merging Connection—SGMII (SERDES) only and MAC + SGMII (SERDES)

2.8. Hardware Requirements (Avant Devices)

For MAC + SGMII (LVDS) or SGMII (LVDS) only mode, there are PCB requirements. If you want to build your own custom board with an Avant device, ensure that the routing from the pin to the external PHY is kept at a recommended maximum length of 4 inches using 100 ohm differential impedance with a maximum of 1 via per RX or TX signal.

The RX Eye valid window requirement is 0.6UI Eye Opening (480ps for 1.25 Gbps SGMII).

Currently, a maximum of 1 SGMII links per HPIO bank and each bank must have a PLL. Each SGMII x1 link consists of 1 LVDS TX and RX pair. For larger Avant devices, banks 3 to 11 with PLL can be used. For more information, refer to the Lattice Avant Hardware Checklist (FPGA-TN-02317).

For VCCPLL, share the DC supply with VCC and do an AC isolation with an inductor.

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3. IP Parameter Description

The configurable attributes of the TSE IP core are shown in the following tables. You can configure the IP by setting the attributes accordingly in the IP Catalog's Module/IP wizard of the Lattice Radiant software.

Wherever applicable, default values are in bold.

For more information on the parameter settings of common Ethernet implementations, refer to Table 2.2.

3.1. General Attributes

Table 3.1. General Attributes

Attribute	Selectable Values	Description	Dependency on Other Attributes
General			
Select IP Option	Avant devices: • MAC only • MAC + SGMII (SERDES) • **MAC + SGMII (LVDS)** • SGMII (LVDS) only • SGMII (SERDES) only CertusPro-NX devices: • MAC only • **MAC + SGMII (SERDES)** • MAC + SGMII (LVDS) • SGMII (LVDS) only • SGMII (SERDES) only Other devices: • **MAC only**	This attribute configures between MAC only mode, SGMII (LVDS) only mode, SGMII (SERDES) only mode, MAC + SGMII (LVDS) mode, or MAC + SGMII (SERDES) mode. **Note:** The SGMII interface using LVDS I/O in Certus-NX, CertusPro-NX, MachXO5-NX, and CrossLink-NX FPGAs has limitations when operating across the full specified temperature range. Lattice recommends using alternative interfaces, such as SERDES or RGMII, for designs requiring Gigabit Ethernet. Refer to the Knowledge Base article for details. Contact your local Lattice sales representative for more information.	—

3.2. MAC Only Mode Attributes

Table 3.2. MAC Only Mode Attributes

Attribute	Selectable Values	Description	Dependency on Other Attributes
Configuration			
Host Interface	• APB • AHBL • **AXI4L**	This attribute selects the type of Host Interface, either AHB-Lite, APB, or AXI4-Lite.	—
Select MAC Operating Option	• **MII/GMII** • Gigabit MAC • SGMII Easy Connect • RMII	This attribute configures the usage type of the MII interface. For more information, refer to the Implementation Options section.	Enabled when *Select IP Option == MAC only*

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Attribute	Selectable Values	Description	Dependency on Other Attributes
	• RGMII		
Include MIIM Module	• Checked • **Unchecked**	Enables or disables Media Independent Interface Management (MIIM).	Enabled when *Select IP Option == MAC only*
Enable Half Duplex Module	• **Checked** • Unchecked	Enables or disables half-duplex module in TX MAC. When this option is enabled, MAC can operate between half-duplex and full duplex mode. Whereas, when it is disabled, MAC operates in full-duplex mode only.	—
Enable AXIS FIFO Functionality	• **Checked** • Unchecked	Enables or disables AXIS FIFO functionality in both TX and RX. Each FIFO is configured with a depth of 2,048 entries and serves as a temporary buffer to manage data flow.	—
Statistic Counter Registers	• Checked • **Unchecked**	Enables or disables statistics counter registers. For more information, refer to the Statistics Counter Configuration section.	—
RGMII Timing Consideration			
Enable FPGA delay for TX	• Checked • **Unchecked**	TX FPGA delay. Enables you to fine-tune the timing of the TX signal to achieve either center-aligned or edge-aligned configuration. This configuration optimizes the RGMII Ethernet PHY data transfer performance.	Enabled when *Select MAC Operating Option = RGMII*
FPGA delay steps for TX	Nexus devices: 0 – 127 Avant devices: 0 – 511 **(Default: 127)**	Each delay step shifts data by ~10 ps but varies with PVT conditions.	Enabled when *Enable FPGA delay for TX is selected*
Enable FPGA delay for RX	• Checked • **Unchecked**	RX FPGA delay. Enables you to fine-tune the timing of the RX signal to achieve either center-aligned or edge-aligned configuration. This configuration optimizes the RGMII Ethernet PHY data transfer performance.	Enabled when *Select MAC Operating Option = RGMII*
FPGA delay steps for RX	Nexus devices: 0 – 127 Avant devices: 0 – 511 **(Default: 127)**	Each delay step shifts data by ~10 ps but varies with PVT conditions.	Enabled when *Enable FPGA delay for RX is selected*

3.3. SGMII (LVDS) Only Mode Attributes

Note: The SGMII interface using LVDS I/O in Certus-NX, CertusPro-NX, MachXO5-NX, and CrossLink-NX FPGAs has limitations when operating across the full specified temperature range. Lattice recommends using alternative interfaces, such as SERDES or RGMII, for designs requiring Gigabit Ethernet. Refer to the Knowledge Base article for details. Contact your local Lattice sales representative for more information.

Table 3.3. SGMII (LVDS) Only Mode Attributes

Attribute	Selectable Values	Description	Dependency on Other Attributes
PHY Settings			
G(MII) Style	• **Classic** • TSMAC Easy Connect	This attribute affects the behavior and implementation of the (G)MII port. In Classic mode, the (G)MII data port is 8 bits wide. All 8 bits are used for 1 Gbps operation. Only the lower 4 bits are used for 100 Mbps and 10 Mbps operation. A separate MII clock is used to synchronize the (G)MII data. The MII clock frequency varies with the (G)MII data rate: 125 MHz for 1 Gbps, 25 MHz for 100 Mbps, and 2.5 MHz for 10 Mbps. In the TSMAC Easy Connect mode, the (G)MII	—

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Attribute	Selectable Values	Description	Dependency on Other Attributes
		data port is 8 bits wide; and all 8 bits are used, regardless of the (G)MII data rate. A single 125 MHz clock is used to synchronize (G)MII data and a clock enable is used to regulate the (G)MII data rate.	
CTC Mode	• Static • **Dynamic** • None	This attribute controls the behavior of the CTC block. In dynamic mode, the CTC FIFO thresholds are automatically changed based on the current operational rate of the rate adaptation blocks. Optimal thresholds are internally chosen for these three data rates—1 Gbps, 100 Mbps, and 10 Mbps. In static mode, you manually choose the CTC FIFO thresholds, and these thresholds remain fixed. In None mode, the CTC function is replaced by a shallow FIFO that facilitates clock domain crossing between the recovered SERDES clock and the local IP core receive-side 125 MHz clock.	—
Static Low FIFO Threshold	1 – 1,016 **(Default: 16)**	When Static CTC mode is chosen, this attribute specifies the FIFO low (almost empty) threshold. Note: It is essential that the Static High FIFO Threshold, almost full threshold, is always to a value higher than the Static Loew FIFO Threshold, almost empty threshold. This ensures that the FIFO can correctly indicate both low and high occupancy levels without conflict, preventing potential underflow or overflow issues during operation.	Enabled when *CTC Mode == Static*
Static High FIFO Threshold	4 – 1,020 **(Default: 32)**	When Static CTC mode is chosen, this attribute specifies the FIFO high (almost full) threshold.	Enabled when *CTC Mode == Static*
Optional Settings			
Use External PLL (remove internal PLL instance)	• Checked • **Unchecked**	By default, there is a PLL instance inside the IP that provides clock to the CDR and GDDR block. This option allows you to remove the internal PLL instance in the IP. This option is useful if you intend to use some ports of the PLL that are not possible if it is inside the IP. User applications with multiple SGMII instance may prefer to have a common PLL instead of per IP instance. For some devices like LFMXO5, the reference clock of CDR blocks is tied to a common PLL, so this option is needed when implementing multiple SGMII instance.	This option is not available for Avant devices.
CDR Reference clock (Enable Port)	• Checked • **Unchecked**	This is related to the *Use External PLL* option above. When enabled, the internal CDR reference clock input is provided as an IP port. For LFMXO5 devices, this option must always be enabled regardless of the *Use External PLL* setting. CDR and DDR cannot share PLL clocks so you are expected to instantiate a separate PLL in the design. Note that the CDR reference clock can only come from CLKOP of the PLL.	This option is not available for Avant devices.

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3.4. SGMII (SERDES) Only Mode Attributes (Nexus Devices)

Table 3.4. SGMII (SERDES) Only Mode Attributes

Attribute	Selectable Values	Description	Dependency on Other Attributes
PHY Settings			
G(MII) Style	• **Classic** • TSMAC Easy Connect	This attribute affects the behavior and implementation of the (G)MII port. In Classic mode, the (G)MII data port is 8 bits wide. All 8 bits are used for 1 Gbps operation. Only the lower 4 bits are used for 100 Mbps and 10 Mbps operation. A separate MII clock is used to synchronize the (G)MII data. The MII clock frequency varies with the (G)MII data rate: 125 MHz for 1 Gbps, 25 MHz for 100 Mbps, and 2.5 MHz for 10 Mbps. In TSMAC Easy Connect mode, the (G)MII data port is 8 bits wide; and all 8 bits are used, regardless of the (G)MII data rate. A single 125 MHz clock is used to synchronize (G)MII data and a clock enable is used to regulate the (G)MII data rate.	—
CTC Mode	• Static • **Dynamic** • None	This attribute controls the behavior of the CTC block. In dynamic mode, the CTC FIFO thresholds are automatically changed based on the current operational rate of the rate adaptation blocks. Optimal thresholds are internally chosen for these three data rates—1 Gbps, 100 Mbps, and 10 Mbps. In static mode, you manually choose the CTC FIFO thresholds, and these thresholds remain fixed. In None mode, the CTC function is replaced by a shallow FIFO that facilitates clock domain crossing between the recovered SERDES clock and the local IP core receive-side 125 MHz clock.	—
Static Low FIFO Threshold	1 – 1,016 **(Default: 16)**	When Static CTC mode is chosen, this attribute specifies the FIFO low (almost empty) threshold. Note: It is essential that the Static High FIFO Threshold (almost full threshold) is always set to a value higher than the Static Low FIFO Threshold (almost empty threshold). This ensures that the FIFO can correctly indicate both low and high occupancy levels without conflict, preventing potential underflow or overflow issues during operation.	Enabled when *CTC Mode == Static*
Static High FIFO Threshold	4 – 1,020 **(Default: 32)**	When Static CTC mode is chosen, this attribute specifies the FIFO high (almost full) threshold.	Enabled when *CTC Mode == Static*
PCS Settings			
Select MPCS lane or channel	• **AUTO** • 0 • 1 • 2 • 3 • 4 • 5 • 6 • 7	Assign the location of the MPCS lane or channel.	—
MPCS PMA loopback	• Checked • **Unchecked**	Enables the PMA loopback in CertusPro-NX MPCS Primitive.	—
MPCS NAME	• 0 • 1 • 2 • 3	MPCS NAME is an integer parameter used to uniquely identify multiple instances of the MPCS module within a design. For multi-lane SGMII Ethernet support, each instantiated module must be assigned a distinct MPCS	Enabled when *LANE_ID == AUTO*

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Attribute	Selectable Values	Description	Dependency on Other Attributes
	• 4 • 5 • 6 • 7	NAME. The selected value helps differentiate instances at synthesis levels, enabling correct module mapping and functionality in multi-instance configurations.	

3.5. SGMII (SERDES) Only Mode Attributes (Avant Devices)

Table 3.5. SGMII (SERDES) Only Mode Attributes

Attribute	Selectable Values	Description	Dependency on Other Attributes
PHY Settings			
G(MII) Style	• **Classic** • TSMAC Easy Connect	This attribute affects the behavior and implementation of the (G)MII port. In Classic mode, the (G)MII data port is 8 bits wide. All 8 bits are used for 1 Gbps operation. Only the lower 4 bits are used for 100 Mbps and 10 Mbps operation. A separate MII clock is used to synchronize the (G)MII data. The MII clock frequency varies with the (G)MII data rate: 125 MHz for 1 Gbps, 25 MHz for 100 Mbps, and 2.5 MHz for 10 Mbps. In TSMAC Easy Connect mode, the (G)MII data port is 8 bits wide; and all 8 bits are used, regardless of the (G)MII data rate. A single 125 MHz clock is used to synchronize (G)MII data and a clock enable is used to regulate the (G)MII data rate.	—
CTC Mode	• Static • **Dynamic** • None	This attribute controls the behavior of the CTC block. In dynamic mode, the CTC FIFO thresholds are automatically changed based on the current operational rate of the adaptation blocks. Optimal thresholds are internally chosen for these three data rates—1 Gbps, 100 Mbps, and 10 Mbps. In static mode, you manually choose the CTC FIFO thresholds, and these thresholds remain fixed. In None mode, the CTC function is replaced by a shallow FIFO that facilitates clock domain crossing between the recovered SERDES clock and the local IP core receive-side 125 MHz clock.	—
Static Low FIFO Threshold	1 – 1,016 **(Default: 16)**	When Static CTC mode is chosen, this attribute specifies the FIFO low (almost empty) threshold. Note: It is essential that the Static High FIFO Threshold (almost full threshold) is always set to a value higher than the Static Low FIFO Threshold (almost empty threshold). This ensures that the FIFO can correctly indicate both low and high occupancy levels without conflict, preventing potential underflow or overflow issues during operation.	Enabled when *CTC Mode == Static*
Static High FIFO Threshold	4 – 1,020 **(Default: 32)**	When Static CTC mode is chosen, this attribute specifies the FIFO high (almost full) threshold.	Enabled when *CTC Mode == Static*
MPPHY Settings			
Select MPPHY lane or channel	• **AUTO** • 0-27	Assign the location of the MPPHY lane or channel. Specifies the Lane ID.	—
Loopback Mode	• Checked • **Unchecked**	Enables the Fabric loopback or Near PMA loopback or disables the loopback.	—
PMA Setup-Receiver Subgroup (default values are recommended)			
RX Loss of Sig port	• **Enabled**	RX loss of signal capability.	—

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Attribute	Selectable Values	Description	Dependency on Other Attributes
Enable	• Disabled		
RX Coupling Mode	• **AC Coupling** • DC Coupling	PMA coupling mode.	—

3.6. MAC + SGMII (LVDS) Mode Attributes

Table 3.6. MAC + SGMII Mode Attributes

Attribute	Selectable Values	Description	Dependency on Other Attributes
Configuration			
Host Interface	• APB • AHBL • **AXI4L**	This attribute selects the type of Host Interface, either AHB-Lite, APB, or AXI4-Lite.	—
Select MAC + SGMII Operating Option	• **Multi-rate SGMII Ethernet** • Gigabit 1000BaseX Ethernet	This attribute configures the MAC + SGMII option.	—
Host Interface	• APB • AHBL • **AXI4L**	This attribute selects the type of Host Interface, either AHB-Lite, APB, or AXI4-Lite.	—
Enable Half Duplex Module	• **Checked** • Unchecked	Enables or disables half-duplex module in TX MAC. When this option is enabled, MAC can operate between half-duplex and full duplex mode. Whereas, when it is disabled, MAC operates in full-duplex mode only.	—
Enable AXIS FIFO Functionality	• **Checked** • Unchecked	Enables or disables AXIS FIFO functionality in both TX and RX. Each FIFO is configured with a depth of 2,048 entries and serves as a temporary buffer to manage data flow.	—
Statistic Counter Registers	• Checked • **Unchecked**	Enables or disables statistics counter registers. For more information, refer to the Statistics Counter Configuration section.	—
PHY Settings			
Refer to the *PHY Settings* section in Table 3.3.			

3.7. MAC + SGMII (SERDES) Mode Attributes

Table 3.7. MAC + MPCS Mode Attributes

Attribute	Selectable Values	Description	Dependency on Other Attributes
Configuration			
Host Interface	• APB • AHBL • **AXI4L**	This attribute selects the type of Host Interface, either AHB-Lite, APB, or AXI4-Lite.	—
Select MAC + MPCS Operating Option	• **Multi-rate Ethernet** • Gigabit Ethernet	This attribute configures the MAC + SGMII (SERDES) option.	—
Enable Half Duplex Module	• **Checked** • Unchecked	Enables or disables half-duplex module in TX MAC. When this option is enabled, MAC can operate between half-duplex and full duplex mode. Whereas, when it is disabled,	—

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Attribute	Selectable Values	Description	Dependency on Other Attributes
		MAC operates in full-duplex mode only.	
Enable AXIS FIFO Functionality	• **Checked** • Unchecked	Enables or disables AXIS FIFO functionality in both TX and RX. Each FIFO is configured with a depth of 2,048 entries and serves as a temporary buffer to manage data flow.	—
Statistic Counter Registers	• Checked • **Unchecked**	Enables or disables statistics counter registers. For more information, refer to the Statistics Counter Configuration section.	—
PHY Settings			
For the *PHY Settings* refer to Table 3.4 for Nexus devices and Table 3.5 for Avant devices.			

3.8. Statistics Counter Configuration

Table 3.8. Statistics Counter Configuration

Statistics Counter Configuration			
Attribute	**Selectable Values**	**Description**	**Dependency on Other Attributes**
Counter Width	• **32** • 64	Statistics counters register size.	Enabled when *Statistic Counter Registers is selected*
TX Statistics	• **Checked** • Unchecked	TX statistics. Checked to add TX statistics counters.	Enabled when *Statistic Counter Registers is selected*
RX Statistics	• **Checked** • Unchecked	RX statistics. Checked to add RX statistics counters.	Enabled when *Statistic Counter Registers is selected*

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4. Signal Description

This section describes the TSE IP ports.

4.1. Clock Interface

Table 4.1. Common Clock Ports

Port	Type	Description
clk_i	Input	Host Interface (APB, AHB-Lite or AXI4-Lite) Clock. The supported clock frequency is between 20 MHz to 125 MHz.
mdc_i	Input	Management Data Input. Used to transfer information from the PHY to the management module. The clock port is available only if *Include MIIM Module* option is enabled. The clock frequency is 2.5 MHz or below.

Table 4.2. TSE MAC Clock Ports

Port	Type	Description
MII/GMII Clock Interfaces		
mii_gmii_gtx_clk_i	Input	MII/GMII Transmit MAC Application Interface Clock. This clock port is available when the operating mode is in MII/GMII mode. The required clock frequency is 125 MHz. For 1 Gbps operation, this clock is used by the client application, MII interface and MAC. All inputs to the TX MAC on the MII side and all outputs driven by the TX MAC on the client side are synchronous to this clock with clock enable signals—mii_gmii_tx_clock_en_o. For 10 Mbps/100 Mbps operation, this clock is used by the client application and MAC. All outputs driven by the TX MAC on the client side are synchronous to this clock, with clock enable signal—mii_gmii_tx_clk_en_o. Note: This clock is derived from the system clock. Refer to the *Simplified Clock Scheme Design* diagram in the Clocking of MII/GMII section.
mii_gmii_tx_clk_i	Input	MII/GMII Transmit MII Application Interface Clock. This clock port is available when the operating mode is in MII/GMII mode. This clock is used by the MII interface. For 1 Gbps operation, this clock is unused. For 10 Mbps/100 Mbps operation, the required clock frequency is 2.5 MHz or 25 MHz. All outputs driven by the TX MAC on MII side must be synchronous to this clock. Note: This clock is derived from the PCS/PHY TX clock, MII PHY. Refer to the *Simplified Clock Scheme Design* diagram in the Clocking of MII/GMII section.
mii_gmii_rx_clk_i	Input	MII/GMII Receive MAC and MII Application Interface Clock. For 10Mbps/100Mbps/1Gbps operation, this clock is used by the client application, MII interface and MAC. All inputs to the RX MAC on the MII side and all outputs driven by the RX MAC on the client side are synchronous to this clock with clock enable signals, mii_gmii_rx_clk_en_o. Note: This clock is derived from the PCS/PHY RX clock. Refer to the *Simplified Clock Scheme Design* diagram in the Clocking of MII/GMII section.
mii_gmii_tx_clk_en_o	Output	MII/GMII TX Clock Enable. This signal is sync to mii_gmii_gtx_clk_i. The clock enable is always high for 1 Gbps operation. For 100 Mbps operation the clock enable is asserted high once every ten clock (125 MHz) cycles, and for 10 Mbps operation the clock enable is asserted high once every hundred clock (125 MHz) cycles.

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Port	Type	Description
		Note: For 100 Mbps operation and 10 Mbps operation the typical ratio is 1:10 and 1:100 respectively. While the MAC and MII interface are running with two different clock sources, mii_gmii_gtx_clk_i at MAC and mii_gmii_tx_clk_i at MII interface side. Sometimes, the ratio is adjusted to compensate the clock PPM differences between these two clocks. For 10 Mbps operation, the ratio is between 1:5 and 1:20. For 100 Mbps operation, the ration is between 1:50 and 1:200.
mii_gmii_rx_clk_en_o	Output	MII/GMII RX Clock Enable. This signal is sync to mii_gmii_rx_clk_i. The clock enable is always high for 1G operation. For 100 Mbps operation the clock enable is asserted high once every two clock (25 MHz) cycles, and for 10 Mbps operation the clock enable is asserted high once every two clock (2.5 MHz) cycles.
Gigabit MAC Clock Interfaces		
gmii_tx_clk_i	Input	Gigabit MAC Transmit Clock The required clock frequency is 125 MHz. Note: This clock is derived from the system clock. Refer to the *Simplified Clock Scheme Design* diagram in the Clocking of Gigabit MAC section.
gmii_rx_clk_i	Input	Gigabit MAC Receive Clock The required clock frequency is 125 MHz. Note: This clock is derived from the system clock. Refer to the *Simplified Clock Scheme Design* diagram in the Clocking of Gigabit MAC section.
gmii_tx_clk_en_o	Output	Gigabit MAC TX Clock Enable. This signal is always high.
gmii_rx_clk_en_o	Output	Gigabit MAC RX Clock Enable. This signal is always high.
RMII Clock Interfaces		
rmii_ref_clk_i	Input	RMII Reference Clock. This clock interface is only used for RMII option. This required clock frequency is 50 MHz for both 100/10 Mbps operations. All inputs and outputs driven by the MAC must be synchronous to this clock with clock enable signals, rmii_clk_en_o. Note: This clock is derived from the system clock diagram. Refer to the *Simplified Clock Scheme Design* diagram in the Clocking of RMII section.
rmii_clk_en_o	Output	RMII Clock Enable. This signal is syncing to rmii_ref_clk_i. For 100 Mbps operation the clock enable is asserted high once every four clock (50 MHz) cycles, and for 10 Mbps operation the clock enable is asserted high once every forty clock (50 MHz) cycles.
RGMII Clock Interfaces		
rgmii_tx_clk_i	Input	RGMII Transmit Clock. This clock port is available when the operating mode is in RGMII mode. For 10 Mbps/100 Mbps/1 Gbps operation, the required clock frequency is 2.5 MHz/25 MHz or 125 MHz. All outputs driven by the TX MAC on MII side must be synchronous to this clock with clock enable signals, rgmii_tx_clk_en_o. Note: This clock is derived from the system clock. Refer to the *Simplified Clock Scheme Design* diagram in the Clocking of RGMII section.
rgmii_rx_clk_i	Input	RGMII Receive Clock. For 10Mbps/100Mbps/1Gbps operation, this clock is used by the client application, MII interface, and MAC. All inputs to the RX MAC on the MII side

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Port	Type	Description
		and all outputs driven by the RX MAC on the client side are synchronous to this clock with clock enable signals, rgmii_rx_clk_en_o. Note: This clock is derived from the RGMII PHY RX clock. Refer to the *Simplified Clock Scheme Design* diagram in the Clocking of RGMII section.
rgmii_tx_clk_en_o	Output	RGMII TX Clock Enable. This signal is sync to rgmii_tx_clk_i. The clock enable is always high for 1 Gbps operation. For 100 Mbps operation the clock enable is asserted high once every ten clock (125 MHz) cycles, and for 10 Mbps operation the clock enable is asserted high once every hundred clock (125 MHz) cycles.
rgmii_rx_clk_en_o	Output	RGMII RX Clock Enable. This signal is sync to rgmii_rx_clk_i. The clock enable is same as rgmii_tx_clk_en_o.
SGMII Easy Connect Clock Interfaces[1]		
sgmii_tx_clk_i	Input	SGMII Easy Connect Transmit Clock. The required clock frequency is 125 MHz. Note: This clock is derived from the system clock diagram. Refer to the *Simplified Clock Scheme Design* diagram in the Clocking of TSE IP MAC Option (SGMII Easy Connect) and SGMII PCS (TSMAC Easy Connect) section.
sgmii_rx_clk_i	Input	SGMII Easy Connect Receive Clock. The required clock frequency is 125 MHz. Note: This clock is derived from the usr_clk_o, Lattice SGMII PCS IP. Refer to the *Simplified Clock Scheme Design* diagram in the Clocking of TSE IP MAC Option (SGMII Easy Connect) and SGMII PCS (TSMAC Easy Connect) section.
sgmii_tx_clk_en_o	Output	SGMII Easy Connect TX Clock Enable. This signal is sync to sgmii_tx_clk_i. The clock enable is always high for 1 Gbps operation. For 100 Mbps operation the clock enable is asserted high once every ten clock (125 MHz) cycles, and for 10 Mbps operation the clock enable is asserted high once every hundred clock (125 MHz) cycles.
sgmii_rx_clk_en_o	Output	SGMII Easy Connect RX Clock Enable. This signal is sync to sgmii_rx_clk_i. The clock enable is always high for 1 Gbps operation. For 100 Mbps operation the clock enable is asserted high once every ten clock (125 MHz) cycles, and for 10 Mbps operation the clock enable is asserted high once every hundred clock (125 MHz) cycles.

Note:

1. These interfaces are used with the TSMAC Easy Connect interfaces of the Lattice SGMII PCS IP.

4.2. Reset Interface

Table 4.3. Reset Ports

Port	Clock Domain	Direction	Description
reset_n_i	Asynchronous	Input	Reset. This is an active low signal that resets the internal registers and internal logic. When activated, the I/O signals are driven to their inactive levels.

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4.3. AXI4-Stream Transmit Interface

Table 4.4. AXI4-Stream Transmit Interface Ports

Port	Clock Domain[1]	Direction	Description
axis_tx_tvalid_i	gmii_tx_clk_i[2] mii_gmii_gtx_clk_i[3] rmii_ref_clk_i[4] sgmii_tx_clk_i[5] rgmii_tx_clk_i[6]	Input	Transmit Data Validation. This signal indicates that TX source is driving a valid data transfer. The valid signal must remain asserted throughout the entire packet, mid-packet drops are not permitted.
axis_tx_tready_o		Output	Transmit Ready. This signal indicates that the TX destination is ready to accept data. It toggles in sync with the TX clock enable signal.
axis_tx_tlast_i		Input	This signal indicates the boundary or last transfer of a packet.
axis_tx_tdata_i[7:0]		Input	Transmit Data. Carries the actual TX data being transferred.
axis_tx_tkeep_i		Input	This signal indicates valid bytes of the Transmit Data. Always assign 1'b1 to this input port.

Notes:

1. Clock domain varies based on the selected attribute. For more information, refer to the corresponding clock diagram in the Clocking section.
2. Gigabit MAC mode.
3. MII/GMII mode.
4. RMII mode.
5. SGMII Easy Connect mode.
6. RGMII mode.

4.4. AXI4-Stream Receive Interface

Table 4.5. AXI4-Stream Receive Interface Ports

Port	Clock Domain[1]	Direction	Description
axis_rx_tvalid_o	gmii_rx_clk_i[2] mii_gmii_rx_clk_i[3] rmii_ref_clk_i[4] sgmii_rx_clk_i[5] rgmii_rx_clk_i[6]	Output	Receive Data Validation. This signal indicates that RX source is driving a valid data transfer. It toggles in sync with the RX clock enable signal.
axis_rx_tready_i		Input	Receive Ready. This signal indicates that RX destination can accept the data. Note: When the Enable AXIS FIFO Functionality option is disabled, no buffering is provided and tready must always remain asserted. You must ensure continuous data acceptance as any interruption may result in packet loss.
axis_rx_tlast_o		Output	This signal indicates the boundary or last transfer of a packet.
axis_rx_tdata_o[7:0]		Output	Receive Data. Carries the actual RX data being transferred.
axis_rx_tkeep_o		Output	This signal indicates valid bytes of the Receive Data. The value of this output port is always 1'b1.

Notes:

1. Clock domain varies based on the selected attribute. For more information, refer to the corresponding clock diagram in the Clocking section.
2. Gigabit MAC mode.
3. MII/GMII mode.
4. RMII mode.
5. SGMII Easy Connect mode.
6. RGMII mode.

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4.5. Transmit MAC Control and Status Interface

Table 4.6. Transmit MAC Control and Status Interface Ports

Port	Clock Domain[1]	Direction	Description
tx_sndpaustim_i[15:0]	gmii_tx_clk_i[2] mii_gmii_gtx_clk_i[3] rmii_ref_clk_i[4] sgmii_tx_clk_i[5] rgmii_tx_clk_i[6]	Input	Pause Frame Timer. This signal indicates the pause time value that must be sent in the pause frame.
tx_sndpausreq_i		Input	Pause Frame Request. When asserted, the MAC transmits a pause frame. This is also the qualifying signal for the tx_sndpausetim_i bus. You must wait for TX_STAT_PAUSE increment before issuing the next pause req. Otherwise, it may result in indeterminate behavior.
tx_fifoctrl_i		Input	FIFO Control Frame. This signal indicates whether the current frame in the Transmit FIFO is a control frame or a data frame. The following values apply: • 1 = Control frame • 0 = Normal frame
tx_macread_o		Output	Transmit FIFO Read This is the MAC Transmit FIFO read request asserted by the MAC when it reads the FIFO.
tx_done_o		Output	Transmit Done. This signal is asserted for one clock cycle after transmitting a frame if no errors are present in transmission.
tx_discfrm_o		Output	Discard Frame. This signal is asserted at the end of a frame transmit process if the MAC detected an error. The possible conditions are: • A FIFO under-run • Late collision (10/100 mode only) • Excessive collisions (10/100 mode only) The user application normally moves the pointer to the next frame in these conditions.
tx_staten_o		Output	Transmit Statistics Vector Enable. When asserted, the contents of the statistics vector bus tx_statvec_o is valid.
tx_statvec_o[31:0]		Output	Transmit Statistics Vector. This bus includes useful information about the frame that is transmitted.

Notes:
1. Clock domain varies based on the selected attribute. For more information, refer to the corresponding clock diagram in the Clocking section.
2. Gigabit MAC mode.
3. MII/GMII mode.
4. RMII mode.
5. SGMII Easy Connect mode.
6. RGMII mode.

4.6. Receive MAC Control and Status Interface

Table 4.7. Receive MAC Control and Status Interface Ports

Port	Clock Domain[1]	Direction	Description
ignore_pkt_i	gmii_rx_clk_i[2] mii_gmii_rx_clk_i[3] rmii_ref_clk_i[4] sgmii_rx_clk_i[5] rgmii_rx_clk_i[6]	Input	Ignore Next Packet. This signal is asserted by the host to prevent a Receive FIFO Full condition. The Receive MAC continues dropping packets as long as this signal is asserted. This is an asynchronous signal.
rx_eof_o		Output	Receive End of Frame flag.
rx_error_o		Output	Receive Packet Error. When asserted, this signal indicates the packet contains error(s). This signal is qualified with the rx_eof_o signal.

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Port	Clock Domain[1]	Direction	Description
			The rx_error_o signal is asserted for any of the following three conditions: • The rx_er* signal on the GMII is asserted by the PHY during frame reception • There are RX FCS errors on received frames • There is a length check error on the received frame
rx_fifo_error_o		Output	Receive FIFO Error. This signal is asserted when the RX FIFO is full and the RX FIFO is being written to by the RX MAC. When this error signal is asserted, the RX MAC will stop writing to RX FIFO. The rx_fifo_error_o signal is de-asserted when the end of packet exits the receive FIFO.
rx_staten_o		Output	Receive Statistics Vector Enable. When asserted, the contents of the statistics vector bus rx_stat_vector_o is valid.
rx_stat_vector_o[31:0]		Output	Receive Statistics Vector. This bus indicates the events encountered during frame reception.

Notes:

1. Clock domain varies based on the selected attribute. For more information, refer to the corresponding clock diagram in the Clocking section.
2. Gigabit MAC mode.
3. MII/GMII mode.
4. RMII mode.
5. SGMII Easy Connect mode.
6. RGMII mode.

4.7. PHY Interface

The interfaces described in this section is available in the MAC only IP option.

4.7.1. MII/GMII Interface

The MII/GMII interface is only available if the selected MAC Operating Option is MII/GMII.

Table 4.8. MII/GMII Interface Ports

Port	Clock Domain[1]	Direction	Description
mii_gmii_txd_o[7:0]	mii_gmii_tx_clk_i[2] mii_gmii_gtx_clk_i[3]	Output	mii_gmii_txd_o[7:0]—Transmitted data to the PHY Chip in 1G speed. mii_gmii_txd_o[3:0]—Transmitted data to the PHY Chip in 10M/100M speed, only use low nibble.
mii_gmii_tx_en_o		Output	Transmit Data Enable. Asserted by the MAC to indicate the mii_gmii_txd_o bus and mii_gmii_tx_er_o contains valid frame data.
mii_gmii_tx_er_o		Output	Transmit Data Error. Asserted when the MAC core generates a coding error on the byte currently being transferred.
mii_gmii_rxd_i[7:0]	mii_gmii_rx_clk_i[2/3]	Input	mii_gmii_rxd_o[7:0]—Receive data from the PHY Chip in 1G speed mii_gmii_rxd_o[3:0]—Receive data from the PHY Chip in 10M/100M speed, only use low nibble.
mii_gmii_rx_dv_i		Input	Receive Data Valid. Indicates the data on the mii_gmii_rxd_i bus and mii_gmii_rx_er_i signal are valid.
mii_gmii_rx_er_i		Input	Receive Data Error. This signal is asserted by the external PHY device when it detects an error during frame reception.

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Port	Clock Domain[1]	Direction	Description
col_i	Asynchronous	Input	Collision. This active-high signal indicates a collision occurred during transmission. This signal is valid for half-duplex operation in Fast Ethernet (10/100) only.
crs_i	Asynchronous	Input	Carrier Sense. This signal, when logic high, indicates the network has activity. Otherwise, it indicates the network is idle. This signal is valid for half-duplex operation in Fast Ethernet (10/100) only.

Notes:

1. Clock domain varies based on the selected attribute. For more information, refer to the corresponding clock diagram in the Clocking section.
2. MII/GMII mode, 10M/100M operating rate.
3. MII/GMII mode, 1G operating rate.

4.7.2. Gigabit MAC Interface

The Gigabit MAC interface is only available if the selected MAC Operating Option is Gigabit MAC.

Table 4.9. Gigabit MAC Interface Ports

Port	Clock Domain[1]	Direction	Description
gmii_txd_o[7:0]	gmii_tx_clk_i	Output	Transmit Data Sent to the PHY Interface. These GMII TX data outputs go to the SGMII and Gb Ethernet PCS IP or to the external Ethernet PHY.
gmii_tx_en_o		Output	Transmit Enable. Asserted by the MAC to indicate the txd_o bus contains valid frame.
gmii_tx_er_o		Output	Transmit Error. Asserted when the MAC generates a coding error on the byte currently being transferred.
gmii_rxd_i[7:0]	gmii_rx_clk_i	Input	Receive Data from the PHY Interface. These GMII Rx data inputs (valid whenever rx_dv_i is asserted) come from the SGMII and Gb Ethernet PCS IP or from the external Ethernet PHY.
gmii_rx_dv_i		Input	Receive Data Valid. Indicates the data on the rxd_o bus is valid.
gmii_rx_er_i		Input	Receive Data Error. This signal is asserted by the SGMII and Gb Ethernet PCS IP or external PHY device when it detects an error during frame reception.

4.7.3. SGMII Easy Connect Interface

The SGMII Easy Connect interface is only available if the selected MAC Operating Option is SGMII Easy Connect.

Table 4.10. SGMII Easy Connect Interface Ports

Port	Clock Domain[1]	Direction	Description
sgmii_txd_o[7:0]	sgmii_tx_clk_i	Output	Transmit Data Sent to the PHY Interface. These GMII TX data outputs go to the SGMII and Gb Ethernet PCS IP or to the external Ethernet PHY.
sgmii_tx_en_o		Output	Transmit Enable. Asserted by the MAC to indicate the txd_o bus contains valid frame.
sgmii_tx_er_o		Output	Transmit Error. Asserted when the MAC generates a coding error on the byte currently being transferred.
sgmii_rxd_i[7:0]	sgmii_rx_clk_i	Input	Receive Data from the PHY Interface. These GMII RX data inputs (valid whenever rx_dv_i is asserted) come from the SGMII and Gb Ethernet PCS IP or from the external Ethernet PHY.
sgmii_rx_dv_i		Input	Receive Data Valid. Indicates the data on the rxd_o bus is valid.
sgmii_rx_er_i		Input	Receive Data Error. This signal is asserted by the SGMII and Gb Ethernet PCS IP or external PHY device when it detects an error during frame reception.
col_i	Asynchronous	Input	Collision. This active-high signal indicates a collision occurred during transmission. This signal is valid for half-duplex operation on Fast

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Port	Clock Domain[1]	Direction	Description
			Ethernet (10/100) only.
crs_i	Asynchronous	Input	Carrier Sense. This signal, when logic high, indicates the network has activity. Otherwise, it indicates the network is idle. This signal is valid for half-duplex operation on Fast Ethernet (10/100) only.
txmac_clk_en_i	sgmii_tx_clk_i	Input	TX Clock Enable. The SGMII & Gb Ethernet PCS IP core drives this signal. The clock enable is always high for 1G operation. For 100 Mbps operation the clock enable is asserted high once every ten (125 MHz) clocks, and for 10 Mbps operation the clock enable is asserted high once every hundred (125 MHz) clocks.
rxmac_clk_en_i	sgmii_rx_clk_i	Input	RX Clock Enable. The SGMII & Gb Ethernet PCS IP core drives this signal. The clock enable is always high for 1G operation. For 100 Mbps operation the clock enable is asserted high once every ten (125 MHz) clocks, and for 10 Mbps operation the clock enable is asserted high once every hundred (125 MHz) clocks.
sgmii_tx_clk_en_o	sgmii_tx_clk_i	Output	TX Clock Enable Output. An output signal of txmac_clk_en_i
sgmii_rx_clk_en_o	sgmii_rx_clk_i	Output	RX Clock Enable Output. An output signal of rxmac_clk_en_i

4.7.4. RGMII Interface

The RGMII interface is only available if the selected MAC Operating Option is RGMII.

Table 4.11. RGMII Interface Ports

Port	Clock Domain	Direction	Description
rgmii_txd_o[3:0]	rgmii_tx_clk_i	Output	rgmii_txd_o[3:0] – RGMII transmit data sent to the PHY 4-bit at both rising edge and falling edge of the clock.
rgmii_tx_ctl_o	rgmii_tx_clk_i	Output	rgmii_tx_ctl_o – RGMII transmit control signal which is having the enable value in the rising edge of the clock and XOR value of the error and enable signal at the falling edge of the clock.
rgmii_rxd_i[3:0]	rgmii_rx_clk_i	Input	rgmii_rxd_i[3:0] – RGMII receive data from the PHY 4-bit at both rising edge and falling edge of the clock.
rgmii_rx_ctl_i	rgmii_rx_clk_i	Input	rgmii_rx_ctl_i – RGMII receive control signal which is having the enable value in the rising edge of the clock and XOR value of the error and enable signal at the falling edge of the clock.
col_i	Asynchronous	Input	Collision. This active-high signal indicates a collision occurred during transmission. This signal is valid for half-duplex operation in Fast Ethernet (10/100) only.
crs_i	Asynchronous	Input	Carrier Sense. This signal, when logic high, indicates the network has activity. Otherwise, it indicates the network is idle. This signal is valid for half-duplex operation in Fast Ethernet (10/100) only.

4.7.5. RMII Interface

The RMII interface is only available if the selected MAC Operating Option is RMII.

Table 4.12. RMII Interface Ports

Port	Clock Domain	Direction	Description
rmii_txd_o[1:0]	rmii_ref_clk_i	Output	rmii_txd_o[1:0] – synchronous to rmii_ref_clk_i 100 Mbps – sampled on every clock cycle. 10 Mbps – sampled on every 10th clock cycle.
rmii_tx_en_o	rmii_ref_clk_i	Output	Transmit Enable. Asserted by the MAC to indicate the rmii_txd_o bus contains valid frame.
rmii_rxd_i[1:0]	rmii_ref_clk_i	Input	rmii_rxd_o[1:0] – synchronous to rmii_ref_clk_i

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Port	Clock Domain	Direction	Description
			100 Mbps – sampled on every clock cycle. 10 Mbps – sampled on every 10th clock cycle.
rmii_rx_er_i	rmii_ref_clk_i	Input	Transmit Error. Asserted when the MAC generates a coding error on the byte currently being transferred.
rmii_rx_crs_dv_i	Asynchronous / rmii_ref_clk_i	Input	- rmii_rx_crs_dv_i indicates carrier sense at first di-bit of a nibble onto rmii_rxd_i[1:0]. Asserted asynchronously on detection of carrier. Deassertion of rmii_rx_crs_dv_i synchronous to the cycle of rmii_ref_clk_i which presents the first di-bit of a nibble onto rmii_rxd_i[1:0]. - rmii_rx_crs_dv_i indicates data valid at second di-bit of a nibble onto rmii_rxd_i[1:0].

4.8. Host Interface

4.8.1. APB Host Interface

The APB host interface is only available if the selected Host Interface is APB.

Table 4.13. APB Host Interface Ports

Port	Clock Domain	Direction	Description
apb_paddr_i[10:0]	clk_i	Input	APB Address signal. Size: Interface Address Width.
apb_psel_i	clk_i	Input	APB Select signal.
apb_penable_i	clk_i	Input	APB Enable signal.
apb_pwrite_i	clk_i	Input	APB Direction signal.
apb_pwdata_i[31:0]	clk_i	Input	APB Write Data signal. Size: Interface Data Width.
apb_pready_o	clk_i	Output	APB Ready signal.
apb_prdata_o[31:0]	clk_i	Output	APB Read Data signal. Size: Interface Data Width.
apb_pslverr_o	clk_i	Output	APB Completer Error signal.

4.8.2. AHB-Lite Host Interface

The AHB-Lite host interface is only available if the selected Host Interface is AHBL.

Table 4.14. AHB-Lite Host Interface Ports

Port	Clock Domain	Direction	Description
ahbl_hsel_i	clk_i	Input	AHB-Lite Select signal.
ahbl_hready_i	clk_i	Input	AHB-Lite Ready Input signal.
ahbl_haddr_i[10:0]	clk_i	Input	AHB-Lite Address signal.
ahbl_hburst_i[2:0]	clk_i	Input	AHB-Lite Burst Type signal. This feature is not supported. Tie to low.
ahbl_hsize_i[2:0]	clk_i	Input	AHB-Lite Transfer Size signal. This feature is not supported. Tie to low.
ahbl_hmastlock_i	clk_i	Input	AHB-Lite Lock signal. This signal is not supported. Tie to low.
ahbl_hprot_i[3:0]	clk_i	Input	AHB-Lite Protection Control signal. This signal is not supported. Tie to low.
ahbl_htrans_i[1:0]	clk_i	Input	AHB-Lite Transfer Type signal.
ahbl_hwrite_i	clk_i	Input	AHB-Lite Direction signal. Write = High, Read = Low.
ahbl_hwdata_i[31:0]	clk_i	Input	AHB-Lite Write Data signal.

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Port	Clock Domain	Direction	Description
ahbl_hreadyout_o	clk_i	Output	AHB-Lite Ready Output signal.
ahbl_hrdata_o[31:0]	clk_i	Output	AHB-Lite Read Data signal.
ahbl_hresp_o	clk_i	Output	AHB-Lite Transfer Response signal. This is not supported. It always return 0.

4.8.3. AXI4-Lite Host Interface

The AXI4-Lite host interface is only available if the selected Host Interface is AXI4L.

Table 4.15. AXI4-Lite Host Interface Ports

Port	Clock Domain	Direction	Description
axi_awaddr_i[10:0]	clk_i	Input	Write address bus.
axi_awvalid_i	clk_i	Input	Write address valid.
axi_awready_o	clk_i	Output	Write address acknowledge.
axi_awprot_i[1:0]	clk_i	Input	Access permission for write access. This is not supported. Tie to low.
axi_wdata_i[31:0]	clk_i	Input	Write data bus.
axi_wvalid_i	clk_i	Input	Write data valid.
axi_wready_o	clk_i	Output	Write data acknowledge.
axi_wstrb_i[3:0]	clk_i	Input	Write strobe. This feature is not supported. Tie to low.
axi_bresp_o[1:0]	clk_i	Output	Write transaction response. This is not supported. It always returns 2’b00.
axi_bvalid_o	clk_i	Output	Write response valid.
axi_bready_i	clk_i	Input	Write response acknowledge.
axi_araddr_i[10:0]	clk_i	Input	Read address bus.
axi_arvalid_i	clk_i	Input	Read address valid.
axi_arready_o	clk_i	Output	Read address acknowledge.
axi_arprot_i[2:0]	clk_i	Input	Defines the access permission for read accesses. This is not supported. Tie to low.
axi_rdata_o[31:0]	clk_i	Output	Read data output.
axi_rresp_o[1:0]	clk_i	Output	Read data response. This is not supported. It always return 2’b00.
axi_rvalid_o	clk_i	Output	Read data/response valid.
axi_rready_i	clk_i	Input	Read data acknowledge.

4.9. Management Interface

The management interface is only available in MAC only and when MIIM is selected.

Table 4.16. Management Interface Ports

Port	Clock Domain	Direction	Description
mdi_i	mdc_i	Input	Management Data Input. Used to transfer information from the PHY to the management module.
mdo_o	mdc_i	Output	Management Data Output. Used to transmit information from the management module to the PHY.

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Port	Clock Domain	Direction	Description
mdio_en_o	mdc_i	Output	Management Data Out Enable. Asserted whenever mdo_o is valid. This can be used to implement a bi-directional signal for mdi_i and mdo_o.

4.10. Interrupt Interface

Table 4.17. Interrupt Interface Ports

Port	Clock Domain	Direction	Description
int_o	clk_i	Output	Interrupt. Stays high as long as any enabled interrupt is pending.

4.11. Miscellaneous Interface

Table 4.18. Miscellaneous Interface Ports

Port	Clock Domain[1]	Direction	Description
cpu_if_gbit_en_o	gmii_rx_clk_i[2] mii_gmii_rx_clk_i[3] rmii_ref_clk_i[4] sgmii_rx_clk_i[5] rgmii_rx_clk_i[6]	Output	CPU Interface 1G Mode Enabled Indication. This signal, when high, is an indication from the CPU interface that the 1G mode is enabled. This signal reflects the state of bit 0 of the MAC mode register in MII/GMII and RGMII options. It is always high for SGMII Easy Connect and Gigabit options.

Notes:

1. Clock domain varies based on the selected attribute. For more information, refer to the corresponding clock diagram in the Clocking section.
2. Gigabit MAC mode.
3. MII/GMII mode.
4. RMII mode.
5. SGMII Easy Connect mode.
6. RGMII mode.

4.12. SGMII (LVDS) Only Interfaces

Note: The SGMII interface using LVDS I/O in Certus-NX, CertusPro-NX, MachXO5-NX, and CrossLink-NX FPGAs has limitations when operating across the full specified temperature range. Lattice recommends using alternative interfaces, such as SERDES or RGMII, for designs requiring Gigabit Ethernet. Refer to the Knowledge Base article for details. Contact your local Lattice sales representative for more information.

Table 4.19. SGMII (LVDS) Only Clock and Reset Interface Ports

Port	Clock Domain	Direction	Description
tx_clk_mii_i	—	Input	Transmit MII Clock – 125 MHz, 25 MHz, or 2.5 MHz clock for incoming (G)MII transmit data. Data is sampled on the rising edge of this clock. For *TSMAC Easy Connect* option, this clock is always 125 MHz.
tx_clock_enable_source_o[1]	usr_clk_o	Output	Transmit Clock Enable Source – This signal is only present when the IP core is generated using the *TSMAC Easy Connect* (G)MII option. This signal is used in combination with the transmit 125 MHz clock to regulate the flow of transmit (G)MII data. The signal is generated by the transmit rate adaptation block. This clock enable must be tied to the transmit section of the MAC that sends transmit Ethernet frames to the SGMII and Gb Ethernet PCS IP core. This clock enable must also be tied to the Transmit Clock Enable Sink of the SGMII and Gb Ethernet PCS IP core.

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Port	Clock Domain	Direction	Description
tx_clock_enable_sink_i[1]	tx_clk_mii_i	Input	Transmit Clock Enable Sink – This signal is only present when the IP core is generated using the *TSMAC Easy Connect* (G)MII option. This signal is used in combination with the transmit 125 MHz clock to regulate the flow of transmit (G)MII data. When the clock enable is high and the transmit clock edge rises, (G)MII data is sampled.[1]
rx_clk_mii_i	—	Input	Receive MII Clock – 125 MHz, 25 MHz, or 2.5 MHz clock for outgoing (G)MII receive data. Data is launched on the rising edge of this clock. *For TSMAC Easy Connect* option, this clock is always 125 MHz.
rx_clock_enable_source_o[2]	usr_clk_o	Output	Receive Clock Enable Source – This signal is similar to the tx_clock_enable_source_o described above, except that it is used for the receive datapath. This clock enable must also be tied to then Receive Clock Enable Sink of the SGMII and Gb Ethernet PCS IP core. Note that this signal is only present when the IP core is generated using the *TSMAC Easy Connect* (G)MII option.
rx_clock_enable_sink_i[2]	rx_clk_mii_i	Input	Receive Clock Enable Sink – This signal is only present when the IP core is generated using the *TSMAC Easy Connect* (G)MII option. This signal is used in combination with the receive 125 MHz clock to regulate the flow of receive (G)MII data. When the clock enable is high and the receive clock edge rises, (G)MII data is launched.
rst_n_i	Asynchronous	Input	Reset – Active low global reset.
cdr_refclk_i	—	Input	CDR Reference Clock – 125 MHz user-provided CDR reference clock input. Note that this signal is only available for non-Avant devices and *if Enable Port: CDR Reference clock* is enabled. This input clock should be coming from Generic PLL of the device.
clk_125m_pll_i	—	Input	125 MHz PLL Clock – 125 MHz clock input. Note that this signal is only available if *Use External PLL* is enabled in the GUI. The *Use External PLL* option is not available for Avant devices.
clk_625m_pll_i	—	Input	625 MHz PLL Clock – 625 MHz clock input. Note that this signal is only available if *Use External PLL* is enabled in the GUI. The *Use External PLL* option is not available for Avant devices.
clk_625m_90_pll_i	—	Input	90-degree Phase Shift 625 MHz PLL Clock – 625 MHz clock input with 90-degree phase shift. Note that this signal is only available if *Use External PLL* is enabled in the GUI. The *Use External PLL* option is not available for Avant devices.
pll_refclk_i	—	Input	PLL Reference Clock – 250 MHz clock input for Avant devices and 125 MHz clock input for non-Avant devices. Data is sampled on the rising edge of this clock. Note that this signal is only available if *Use External PLL* is disabled in the GUI.
clk_125m_pll_o	—	Output	125 MHz PLL primary output clock – Note that this signal is only available if Enable Port: CDR Reference clock is enabled in GUI or if *Use External PLL* is disabled in the GUI. The *Use External PLL* option is not available for Avant devices.
usr_clk_o	—	Output	User Clock–125 MHz clock from ECLKDIV output. Note that this signal is only present when the IP core is generated using the *TSMAC Easy Connect* (G)MII option.
usr_clk_ready_o	—	Output	User Clock Ready – This signal indicates that the User Clock is ready.
clk_gddr_o	—	Output	DDR Clock – assumes an LVDS buffer.
lmmi_clk_i	—	Input	LMMI clock—The typical recommended frequency is 125 MHz, depending on the fabric clock.
eclk_oddr_o	—	Output	Edge Clock—625 MHz clock from DDR output. It is a CDR clock. This clock signal is for CDR debug purpose. Note: This signal is only available for Avant devices.

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Port	Clock Domain	Direction	Description
sclk_oddr_o	—	Output	Primary System Clock—125 MHz clock from DDR output. It is a divided CDR clock. This clock signal is for CDR debug purpose. Note: This signal is only available for Avant devices.

Notes:

1. Connect tx_clock_enable_sink_i to tx_clock_enable_source_o. Relationships between TX-side signals are shown in Figure 2.13.
2. Connect rx_clock_enable_sink_i to rx_clock_enable_source_o. Relationships between RX-side signals are shown in Figure 2.14.

Table 4.20 SGMII (LVDS) Only GMII Interface Ports

Port	Clock Domain	Direction	Description
tx_d_i[7:0]	rx_clk_mii_i	Input	Transmit Data – Incoming (G)MII data. Note that the behavior of this port varies depending on the (G)MII option used when generating the IP core. For Classic mode, when the (G)MII data rate is 1 Gbps, all 8 bits of tx_d_i are valid. However, for 10 Mbps and 100 Mbps, only bits 3:0 of tx_d_i are valid. For the *TSMAC Easy Connect* mode all 8 bits of tx_d_i are valid for all (G)MII data rates (1 Gbps, 10 Mbps, 100 Mbps).
tx_en_i	rx_clk_mii_i	Input	Transmit Enable – Active high signal; asserts when incoming data is valid.
tx_er_i	rx_clk_mii_i	Input	Transmit Error – Active high signal used to denote transmission errors and carrier extension on incoming (G)MII data port.
rx_d_o[7:0]	rx_clk_mii_i	Output	Receive Data – Outgoing (G)MII data. Note that the behavior of this port varies depending on the (G)MII option used when generating the IP core. For Classic mode, when the (G)MII data rate is 1 Gbps, all 8 bits of rx_d_o are valid. However, for 10 Mbps and 100 Mbps, only bits 3:0 of rx_d_o is valid. For the *TSMAC Easy Connect* mode, all 8 bits of rx_d_o is valid for all (G)MII data rates (1 Gbps, 10 Mbps, 100 Mbps).
rx_dv_o	rx_clk_mii_i	Output	Receive Data Valid – Active high signal, asserts when outgoing data is valid.
rx_er_o	rx_clk_mii_i	Output	Receive Error—Active high signal used to denote transmission errors and carrier extension on outgoing (G)MII data port.
col_o	rx_clk_mii_i	Output	Collision Detect—Active high signal, asserts when tx_en_i and rx_dv_o is active at the same time.
crs_o	rx_clk_mii_i	Output	Carrier Sense Detect – Active high signal, asserts when rx_dv_o is high.

Table 4.21. SGMII (LVDS) Only Management Interface Ports

Port	Clock Domain	Direction	Description
mr_adv_ability_i[15:0][1]	Asynchronous	Input	Advertised Ability—Configuration status transmitted by PCS during auto-negotiation process. This signal must not change during auto-negotiation.
mr_an_enable_i[1]	Asynchronous	Input	Auto-Negotiation Enable—Active high signal that enables auto-negotiation state machine to function. This signal must not change during auto-negotiation.
mr_main_reset_i[1]	Asynchronous	Input	Main Reset—Active high signal that forces all PCS state machines to reset.
mr_restart_an_i[1]	Asynchronous	Input	Auto-Negotiation Restart—Active high signal that forces auto-negotiation process to restart.
mr_an_complete_o	Asynchronous	Output	Auto-Negotiation Complete—Active high signal that indicates that the auto-negotiation process is completed.
mr_lp_adv_ability_o[15:0]	Asynchronous	Output	Link Partner Advertised Ability—Configuration status received from partner PCS entity during the auto-negotiation process. The bit

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Port	Clock Domain	Direction	Description
			definitions are the same as described above for the mr_adv_ability_i port.
mr_page_rx_o	Asynchronous	Output	Auto-Negotiation Page Received—Active high signal that asserts while the auto-negotiation state machine is in the *Complete_Acknowledge* state.
force_isolate_i[1]	Asynchronous	Input	Force PCS Isolate—Active high signal that isolates the PCS. When asserted, the RX direction forces the (G)MII port to all zeros, regardless of the condition of the incoming 1.25 Gbps serial data stream. In the TX direction, the condition of the incoming (G)MII port is ignored. The TX PCS behaves as though the (G)MII TX input port was forced to all zeros. Note, however, that the isolate function does not produce any electrical isolation – such as tri-stating of the (G)MII RX outputs of the IP core. When the signal is de-asserted (low), the PCS isolation functions are deactivated. The use of this signal is optional. If you choose not to use the isolate function, then this signal must be tied low.
force_loopback_i[1]	Asynchronous	Input	Force PCS Loopback—Active high signal that activates the loopback function, before the PCS. When asserted, the 10-bit code-group output of the transmit state machine is looped back to the 10-bit code-group input of the receive state machine. When de-asserted, the loopback function is deactivated. The use of this signal is optional. If you choose not to use the loopback function, then this signal must be tied low.
force_unidir_i[1]	Asynchronous	Input	Force PCS Unidirectional Mode—Active high signal that activates the PCS unidirectional mode. When asserted, the transmit state machine path between the TX (G)MII input and the TX 10-bit code-group output remain operational, regardless of what happens on the RX datapath. (Normally RX loss of sync, invalid code-group reception, auto-negotiation restarts can force the transmit state machine to temporarily ignore inputs from the TX (G)MII port). When de-asserted, the unidirectional mode is deactivated. The use of this signal is optional. If you choose not to use the unidirectional function, then this signal must be tied low.
an_link_ok_o	Asynchronous	Output	Auto-Negotiation Link Status OK—Active high signal that indicates that the link is ok. The signal is driven by the auto-negotiation state machine. When auto-negotiation is enabled, the signal asserts when the state machine is in the LINK_OK state. If auto-negotiation is disabled, the signal asserts when the state machine is in the AN_DISABLE_LINK_OK state (see IEEE 802.3 figure 37-6). This signal is intended to be used to produce the Link Status signal as required by IEEE 802.3, Status Register 1, Bit D2 (see IEEE 802.3 paragraph 22.2.4.2.13).

Note:

1. To control the AN process through these ports, you must set the Configuration Source Control Register (config_source) to 0. For more information, refer to the [0x00E] Configuration Source Control Register for Auto-Negotiation section.

Table 4.22. SGMII (LVDS) Only Serial Interface Ports

Port	Clock Domain	Direction	Description
ser_tx_o	Asynchronous	Output	Serial Transmit Data—DDR data. Assumes an LVDS buffer.
ser_rx_i	Asynchronous	Input	Serial Receive Data—DDR data. Assumes an LVDS buffer.

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Table 4.23. SGMII (LVDS) Only LMMI Interface Ports

Port	Clock Domain	Direction	Description
lmmi_resetn_i	lmmi_clk_i	Input	LMMI active low reset.
lmmi_request_i	lmmi_clk_i	Input	Starts transaction.
lmmi_wr_rdn_i	lmmi_clk_i	Input	Write = 1’b1, Read = 1’b0.
lmmi_offset_i	lmmi_clk_i	Input	Register offset, starting at offset 0.
lmmi_wdata_i	lmmi_clk_i	Input	Output data bus.
lmmi_rdata_o	lmmi_clk_i	Output	Input data bus.
lmmi_rdata_valid_o	lmmi_clk_i	Output	Read transaction is complete and lmmi_rdata_o contains valid data.
lmmi_ready_o	lmmi_clk_i	Output	IP is ready to receive a new transaction. This is always asserted (tied to 1’b1).

Table 4.24. SGMII (LVDS) Only Miscellaneous Interface Ports

Port	Clock Domain	Direction	Description
sgmii_mode_i	Asynchronous	Input	SGMII Mode—Controls the behavior of the auto-negotiation process when the core is operating in SGMII mode. 0 = operates as MAC-side entity, 1 = operates as PHY-side entity.
gbe_mode_i	Asynchronous	Input	Gigabit Ethernet Mode—Controls the PCS function of the core. 0 = operates as SGMII PCS, 1 = operates as Gigabit Ethernet PCS (1000BASE-X).
operational_rate_i[1:0]	Asynchronous	Input	Operational Rate—When the core operates in SGMII PCS mode, this port controls the regulation rate of the rate adaptation circuit blocks as follows: 10 = 1 Gbps Rate 01 = 100 Mbps Rate 00 = 10 Mbps Rate Note: In Gigabit Ethernet PCS mode, the rate adaptation blocks always operate at the 1 Gbps rate, regardless of the settings on the operational_rate_i control pins.
debug_link_timer_short_i	Asynchronous	Input	Debug Link Timer Mode—Active high signal that forces the auto-negotiation link timer to run much faster than normal. This mode is provided for debug purposes (for example, allowing simulations to run through the auto-negotiation process much faster than normal). This signal must not change during auto-negotiation.
pll_lock_i	—	Input	PLL Lock—External PLL lock signal. Note that this signal is only available if *Use External PLL* is enabled in GUI.

4.13. SGMII (SERDES) Only Interfaces

Avant and Nexus devices implement different SERDES primitives, resulting in distinct interface characteristics between the two platforms.

4.13.1.SGMII (SERDES) Only Interfaces, Nexus SERDES Primitive, MPCS

For more information on MPCS interfaces and register, refer to the NX MPCS Module User Guide (FPGA-IPUG-02118).

Table 4.25. SGMII (SERDES) Only Serial Interface Ports on Nexus Devices

Port	Clock Domain	Direction	Description
sd0txp_o	Asynchronous	Output	Serial Transmit Data (positive).
sd0txn_o	Asynchronous	Output	Serial Transmit Data (negative).

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Port	Clock Domain	Direction	Description
sd0rxp_i	Asynchronous	Input	Serial Receive Data (positive).
sd0rxn_i	Asynchronous	Input	Serial Receive Data (negative).

Table 4.26. SGMII (SERDES) Only Clock and Reset Interface Ports on Nexus Devices

Port	Clock Domain	Direction	Description
clksel_i[1:0]	Asynchronous	Input	PMA-related clock multiplexer in MPCS Primitive. It is used to select from I/O pad, PLL, and fabric for PCS quad0 [1:0].
diffioclksel_i	Asynchronous	Input	PMA-related clock multiplexer in MPCS Primitive. Selection between I/O pad0 and I/O pad1.
use_refmux_i	Asynchronous	Input	PMA related clock multiplexer in MPCS Primitive. It is used to enable PCSREFMUX, which is a RefClk Mux Tree. This is used for dynamic switching of reference clock.
sdq_refclkp_q0_i	—	Input	MPCS PLL Reference Clock (positive) for Quad 0 – 125 MHz clock input.
sdq_refclkn_q0_i	—	Input	MPCS PLL Reference Clock (negative) for Quad 0 – 125 MHz clock input.
sdq_refclkp_q1_i	—	Input	MPCS PLL Reference Clock (positive) for Quad 1 – 125 MHz clock input.
sdq_refclkn_q1_i	—	Input	MPCS PLL Reference Clock (negative) for Quad 1 – 125 MHz clock input.
pll_0_refclk_i	—	Input	MPCS PLL Reference Clock from Left GPLL – 125 MHz clock input.
pll_1_refclk_i	—	Input	MPCS PLL Reference Clock from Right GPLL – 125 MHz clock input.
sd_ext_0_refclk_i	—	Input	MPCS PLL Reference Clock from external I/O pad0 - 125 MHz clock input.
sd_ext_1_refclk_i	—	Input	MPCS PLL Reference Clock from external I/O pad1 - 125 MHz clock input.
sd_pll_refclk_i	—	Input	MPCS PLL Reference Clock from fabric - 125 MHz clock input.
usr_clk_o	—	Output	User clock. 125 MHz clock from the MPCS IP output.
usr_clk_ready_o	—	Output	User Clock Ready. This signal indicates that the User Clock is ready.
epcs_clkin_i	—	Input	An additional clock required by the MPCS IP. It can be clocked by a PLL output at 125 MHz.
tx_clk_mii_i	—	Input	Transmit MII Clock – 125 MHz, 25 MHz, or 2.5 MHz clock for incoming (G)MII transmit data. Data is sampled on the rising edge of this clock. For *TSMAC Easy Connect* option, this clock is always 125 MHz.
tx_clock_enable_source_o[1]	usr_clk_o	Output	Transmit Clock Enable Source – This signal is only present when the IP core is generated using the *TSMAC Easy Connect* (G)MII option. This signal is used in combination with the transmit 125 MHz clock to regulate the flow of transmit (G)MII data. The signal is generated by the transmit rate adaptation block. This clock enable must be tied to the transmit section of the MAC that sends transmit Ethernet frames to the SGMII and Gb Ethernet PCS IP core. This clock enable must also be tied to the Transmit Clock Enable Sink of the SGMII and Gb Ethernet PCS IP core.
tx_clock_enable_sink_i[1]	tx_clk_mii_i	Input	Transmit Clock Enable Sink – This signal is only present when the IP core is generated using the *TSMAC Easy Connect* (G)MII option. This signal is used in combination with the transmit 125 MHz clock to regulate the flow of transmit (G)MII data. When the clock enable is high and the transmit clock edge rises, (G)MII data is sampled.[1]
rx_clk_mii_i	—	Input	Receive MII Clock – 125 MHz, 25 MHz, or 2.5 MHz clock for outgoing (G)MII receive data. Data is launched on the rising edge of this clock. *For TSMAC Easy Connect* option, this clock is always

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Port	Clock Domain	Direction	Description
			125 MHz.
rx_clock_enable_source_o[2]	usr_clk_o	Output	Receive Clock Enable Source – This signal is similar to the tx_clock_enable_source_o described above, except that it is used for the receive datapath. This clock enable must also be tied to the Receive Clock Enable Sink of the SGMII and Gb Ethernet PCS IP core. Note that this signal is only present when the IP core is generated using the *TSMAC Easy Connect* (G)MII option.
rx_clock_enable_sink_i[2]	rx_clk_mii_i	Input	Receive Clock Enable Sink – This signal is only present when the IP core is generated using the *TSMAC Easy Connect* (G)MII option. This signal is used in combination with the receive 125 MHz clock to regulate the flow of receive (G)MII data. When the clock enable is high and the receive clock edge rises, (G)MII data is launched.
rst_n_i	Asynchronous	Input	Reset – Active low global reset.
lmmi_clk_i	—	Input	LMMI clock—The typical recommended frequency is 125 MHz, depending on the fabric clock.
lmmi_resetn_i	Asynchronous	Input	LMMI active low reset.

Notes:

1. Connect tx_clock_enable_sink_i to tx_clock_enable_source_o. Relationships between TX-side signals are shown in Figure 2.13.
2. Connect rx_clock_enable_sink_i to rx_clock_enable_source_o. Relationships between RX-side signals are shown in Figure 2.14.

Table 4.27. SGMII (SERDES) Only GMII Interface Ports on Nexus Devices

Port	Clock Domain	Direction	Description
tx_d_i[7:0]	rx_clk_mii_i	Input	Transmit Data – Incoming (G)MII data. Note that the behavior of this port varies depending on the (G)MII option used when generating the IP core. For Classic mode, when the (G)MII data rate is 1 Gbps, all 8 bits of tx_d_i are valid. However, for 10 Mbps and 100 Mbps, only bits 3:0 of tx_d_i are valid. For the *TSMAC Easy Connect* mode all 8 bits of tx_d_i are valid for all (G)MII data rates (1 Gbps, 10 Mbps, and 100 Mbps).
tx_en_i	rx_clk_mii_i	Input	Transmit Enable – This active high signal asserts when incoming data is valid.
tx_er_i	rx_clk_mii_i	Input	Transmit Error – Active high signal used to denote transmission errors and carrier extension on incoming (G)MII data port.
rx_d_o[7:0]	rx_clk_mii_i	Output	Receive Data – Outgoing (G)MII data. Note that the behavior of this port varies depending on the (G)MII option used when generating the IP core. For Classic mode, when the (G)MII data rate is 1 Gbps, all 8 bits of rx_d_o are valid. However, for 10 Mbps and 100 Mbps, only bits 3:0 of rx_d_o are valid. For the *TSMAC Easy Connect* mode, all 8 bits of rx_d_o are valid for all (G)MII data rates (1 Gbps, 10 Mbps, and 100 Mbps).
rx_dv_o	rx_clk_mii_i	Output	Receive Data Valid – This active high signal asserts when outgoing data is valid.
rx_er_o	rx_clk_mii_i	Output	Receive Error—This active high signal denotes transmission errors and carrier extension on outgoing (G)MII data port.
col_o	rx_clk_mii_i	Output	Collision Detect— This active high signal asserts when tx_en_i and rx_dv_o are active at the same time.
crs_o	rx_clk_mii_i	Output	Carrier Sense Detect – This active high signal asserts when rx_dv_o is high.

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Table 4.28. SGMII (SERDES) Only Management Interface Ports on Nexus Devices

Port	Clock Domain	Direction	Description
mr_adv_ability_i[15:0][1]	Asynchronous	Input	Advertised Ability—Configuration status transmitted by PCS during auto-negotiation process. This signal must not change during auto-negotiation.
mr_an_enable_i[1]	Asynchronous	Input	Auto-Negotiation Enable—Active high signal that enables auto-negotiation state machine to function. This signal must not change during auto-negotiation.
mr_main_reset_i[1]	Asynchronous	Input	Main Reset—Active high signal that forces all PCS state machines to reset.
mr_restart_an_i[1]	Asynchronous	Input	Auto-Negotiation Restart—Active high signal that forces auto-negotiation process to restart.
mr_an_complete_o	Asynchronous	Output	Auto-Negotiation Complete—This active high signal indicates that the auto-negotiation process is completed.
mr_lp_adv_ability_o[15:0]	Asynchronous	Output	Link Partner Advertised Ability—Configuration status received from partner PCS entity during the auto-negotiation process. The bit definitions are the same as described above for the mr_adv_ability_i port.
mr_page_rx_o	Asynchronous	Output	Auto-Negotiation Page Received—Active high signal that asserts while the auto-negotiation state machine is in the *Complete_Acknowledge* state.
force_isolate_i[1]	Asynchronous	Input	Force PCS Isolate—Active high signal that isolates the PCS. When asserted, the RX direction forces the (G)MII port to all zeros, regardless of the condition of the incoming 1.25 Gbps serial data stream. In the TX direction, the condition of the incoming (G)MII port is ignored. The TX PCS behaves as though the (G)MII TX input port was forced to all zeros. Note that the isolate function does not produce any electrical isolation – such as tri-stating of the (G)MII RX outputs of the IP core. When the signal is deasserted (low), the PCS isolation functions are deactivated. The use of this signal is optional. If you choose not to use the isolate function, then this signal must be tied low.
force_loopback_i[1]	Asynchronous	Input	Force PCS Loopback—Active high signal that activates the loopback function, before the PCS. When asserted, the 10-bit code-group output of the transmit state machine is looped back to the 10-bit code-group input of the receive state machine. When deasserted, the loopback function is deactivated. The use of this signal is optional. If you choose not to use the loopback function, then this signal must be tied low.
force_unidir_i[1]	Asynchronous	Input	Force PCS Unidirectional Mode—Active high signal that activates the PCS unidirectional mode. When asserted, the transmit state machine path between the TX (G)MII input and the TX 10-bit code-group output remain operational, regardless of what happens on the RX datapath. Normally RX loss of sync, invalid code-group reception, auto-negotiation restarts can force the transmit state machine to temporarily ignore inputs from the TX (G)MII port. When deasserted, the unidirectional mode is deactivated. The use of this signal is optional. If you choose not to use the unidirectional function then this signal must be tied low.

Note:

1. To control the AN process through these ports, you must set the Configuration Source Control Register (config_source) to 0. For more information, refer to the [0x00E] Configuration Source Control Register for Auto-Negotiation section.

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Table 4.29. SGMII (SERDES) Only LMMI Interface Ports on Nexus Devices

Port	Clock Domain	Direction	Description
lmmi_request_i	lmmi_clk_i	Input	Starts transaction.
lmmi_wr_rdn_i	lmmi_clk_i	Input	Write = 1'b1, Read = 1'b0.
lmmi_offset_i	lmmi_clk_i	Input	Register offset, starting at offset 0.
lmmi_wdata_i	lmmi_clk_i	Input	Output data bus.
lmmi_rdata_o	lmmi_clk_i	Output	Input data bus.
lmmi_rdata_valid_o	lmmi_clk_i	Output	Read transaction is complete and lmmi_rdata_o contains valid data.
lmmi_ready_o	lmmi_clk_i	Output	IP is ready to receive a new transaction. This is always asserted (tied to 1'b1).

The signals below are directly connected to the MPCS foundation IP, which must only be used for debug purposes. Note that this LMMI interface shares the same clock and reset as the LMMI interface in the table above.

Table 4.30. SGMII (SERDES) Only SERDES LMMI Interface Ports on Nexus Devices

Port	Clock Domain	Direction	Description
mpcs_lmmi_request_i	lmmi_clk_i	Input	Starts transaction.
mpcs_lmmi_wr_rdn_i	lmmi_clk_i	Input	Write = 1'b1, Read = 1'b0.
mpcs_lmmi_offset_i	lmmi_clk_i	Input	Register offset, starting at offset 0.
mpcs_lmmi_wdata_i	lmmi_clk_i	Input	Input write data bus.
mpcs_lmmi_rdata_o	lmmi_clk_i	Output	Output read data bus.
mpcs_lmmi_rdata_valid_o	lmmi_clk_i	Output	Read transaction is complete and lmmi_rdata_o contains valid data.
mpcs_lmmi_ready_o	lmmi_clk_i	Output	IP is ready to receive a new transaction.

Table 4.31. SGMII (SERDES) Only Miscellaneous Interface Ports on Nexus Devices

Port	Clock Domain	Direction	Description
sgmii_mode_i	Asynchronous	Input	SGMII Mode—Controls the behavior of the auto-negotiation process when the core is operating in SGMII mode. 0 = operates as MAC-side entity, 1 = operates as PHY-side entity.
gbe_mode_i	Asynchronous	Input	Gigabit Ethernet Mode—Controls the PCS function of the core. 0 = operates as SGMII PCS, 1 = operates as Gigabit Ethernet PCS (1000BASE-X).
operational_rate_i[1:0]	Asynchronous	Input	Operational Rate—When the core operates in SGMII PCS mode, this port controls the regulation rate of the rate adaptation circuit blocks as follows: 10 = 1 Gbps rate. 01 = 100 Mbps rate. 00 = 10 Mbps rate. Note: In Gigabit Ethernet PCS mode, the rate adaptation blocks always operate at the 1 Gbps rate, regardless of the settings on the operational_rate_i control pins.
debug_link_timer_short_i	Asynchronous	Input	Debug Link Timer Mode—Active high signal that forces the auto-negotiation link timer to run much faster than normal. This mode is provided for debug purposes. For example, allowing simulations to run through the auto-negotiation process much faster than normal. This signal must not change during the auto-negotiation process.
an_link_ok_o	Asynchronous	Output	Auto-Negotiation Link Status OK— This active high signal indicates that the link is ok. The signal is driven by the auto-negotiation state machine. When auto-negotiation is enabled, the signal asserts when the state machine is in the LINK_OK state. If auto-negotiation is disabled, the signal asserts when the state machine is in the

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Port	Clock Domain	Direction	Description
			AN_DISABLE_LINK_OK state (see IEEE 802.3 figure 37-6). This signal produces the Link Status signal as required by IEEE 802.3, Status Register 1, Bit D2 (see IEEE 802.3 paragraph 22.2.4.2.13).

4.13.2.SGMII (SERDES) Only Interfaces, Avant SERDES Primitive, MPPHY

For more information on MPPHY interfaces and register, refer to the Lattice Avant-G/X MPPHY Module User Guide (FPGA-IPUG-02233) .

Table 4.32. SGMII (SERDES) Only Serial Interface Ports on Avant Devices

Port	Clock Domain	Direction	Description
pad_txp_o	Asynchronous	Output	Serial Transmit Data (positive).
pad_txn_o	Asynchronous	Output	Serial Transmit Data (negative).
pad_rxp_i	Asynchronous	Input	Serial Receive Data (positive).
pad_rxn_i	Asynchronous	Input	Serial Receive Data (negative).

Table 4.33. SGMII (SERDES) Only Clock and Reset Interface Ports on Avant Devices

Port	Clock Domain	Direction	Description
pad_refclkp_i	—	Input	MPPHY Quad Reference Clock of positive polarity. 156.25 MHz clock input.
pad_refclkn_i	—	Input	MPPHY Quad Reference Clock of negative polarity. 156.25 MHz clock input.
mpphy_rx_gclk_o	—	Output	Output receive clock forwarded to global clock distribution from the MPPHY IP output.
mpphy_tx_gclk_o	—	Output	Output transmit clock forwarded to global clock distribution from the MPPHY IP output.
pcs_usr_clk_i	—	Input	PCS User Clock. This 125 MHz clock input must connect to usr_clk_o.
usr_clk_o	—	Output	User Clock. 125 MHz clock from the MPPHY IP output.
usr_clk_ready_o	—	Output	User Clock Ready. This signal indicates that the User Clock is ready.
epcs_clkin_i	—	Input	An additional clock required by the MPCS IP. It can be clocked by a PLL output at 125 MHz.
tx_clk_mii_i	—	Input	Transmit MII Clock – 125 MHz, 25 MHz, or 2.5 MHz clock for incoming (G)MII transmit data. Data is sampled on the rising edge of this clock. For *TSMAC Easy Connect* option, this clock is always 125 MHz.
tx_clock_enable_source_o[1]	usr_clk_o	Output	Transmit Clock Enable Source – This signal is only present when the IP core is generated using the *TSMAC Easy Connect* (G)MII option. This signal is used in combination with the transmit 125 MHz clock to regulate the flow of transmit (G)MII data. The signal is generated by the transmit rate adaptation block. This clock enable must be tied to the transmit section of the MAC that sends transmit Ethernet frames to the SGMII and Gb Ethernet PCS IP core. This clock enable must also be tied to the Transmit Clock Enable Sink of the SGMII and Gb Ethernet PCS IP core.
tx_clock_enable_sink_i[1]	tx_clk_mii_i	Input	Transmit Clock Enable Sink – This signal is only present when the IP core is generated using the *TSMAC Easy Connect* (G)MII option. This signal is used in combination with the transmit 125 MHz clock to regulate the flow of transmit (G)MII data. When the clock enable is high and the transmit clock edge rises, (G)MII data is sampled.[1]
rx_clk_mii_i	—	Input	Receive MII Clock – 125 MHz, 25 MHz, or 2.5 MHz clock for

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Port	Clock Domain	Direction	Description
			outgoing (G)MII receive data. Data is launched on the rising edge of this clock. *For TSMAC Easy Connect* option, this clock is always 125 MHz.
rx_clock_enable_source_o[2]	usr_clk_o	Output	Receive Clock Enable Source – This signal is similar to the tx_clock_enable_source_o described above, except that it is used for the receive datapath. This clock enable must also be tied to the Receive Clock Enable Sink of the SGMII and Gb Ethernet PCS IP core. Note that this signal is only present when the IP core is generated using the *TSMAC Easy Connect* (G)MII option.
rx_clock_enable_sink_i[2]	rx_clk_mii_i	Input	Receive Clock Enable Sink – This signal is only present when the IP core is generated using the *TSMAC Easy Connect* (G)MII option. This signal is used in combination with the receive 125 MHz clock to regulate the flow of receive (G)MII data. When the clock enable is high and the receive clock edge rises, (G)MII data is launched.
rst_n_i	Asynchronous	Input	Reset – Active low global reset.
lmmi_clk_i	—	Input	LMMI clock—The typical recommended frequency is 125 MHz, depending on the fabric clock.
lmmi_resetn_i	Asynchronous	Input	LMMI active low reset.
mdc_i	—	Input	Management Data Clock – Clock source for the serial management interface. The IEEE 802.3 specification (clause 22) dictates that the maximum frequency for this clock is 2.5 MHz. Note that this signal is only present when the IP core Register Access is in *MDIO* option.

Notes:

1. Connect tx_clock_enable_sink_i to tx_clock_enable_source_o. Relationships between TX-side signals are shown in Figure 2.13.
2. Connect rx_clock_enable_sink_i to rx_clock_enable_source_o. Relationships between RX-side signals are shown in Figure 2.14.

Table 4.34. SGMII (SERDES) Only GMII Interface Ports on Avant Devices

Port	Clock Domain	Direction	Description
tx_d_i[7:0]	rx_clk_mii_i	Input	Transmit Data – Incoming (G)MII data. Note that the behavior of this port varies depending on the (G)MII option used when generating the IP core. For Classic mode, when the (G)MII data rate is 1 Gbps, all 8 bits of tx_d_i are valid. However, for 10 Mbps and 100 Mbps, only bits 3:0 of tx_d_i are valid. For the *TSMAC Easy Connect* mode all 8 bits of tx_d_i are valid for all (G)MII data rates (1 Gbps, 10 Mbps, and 100 Mbps).
tx_en_i	rx_clk_mii_i	Input	Transmit Enable – This active high signal asserts when incoming data is valid.
tx_er_i	rx_clk_mii_i	Input	Transmit Error – Active high signal used to denote transmission errors and carrier extension on incoming (G)MII data port.
rx_d_o[7:0]	rx_clk_mii_i	Output	Receive Data – Outgoing (G)MII data. Note that the behavior of this port varies depending on the (G)MII option used when generating the IP core. For Classic mode, when the (G)MII data rate is 1 Gbps, all 8 bits of rx_d_o are valid. However, for 10 Mbps and 100 Mbps, only bits 3:0 of rx_d_o are valid. For the *TSMAC Easy Connect* mode, all 8 bits of rx_d_o are valid for all (G)MII data rates (1 Gbps, 10 Mbps, and 100 Mbps).
rx_dv_o	rx_clk_mii_i	Output	Receive Data Valid – This active high signal asserts when outgoing data is valid.
rx_er_o	rx_clk_mii_i	Output	Receive Error—This active high signal denotes transmission errors and carrier extension on outgoing (G)MII data port.
col_o	rx_clk_mii_i	Output	Collision Detect— This active high signal asserts when tx_en_i and rx_dv_o are active at the same time.

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Port	Clock Domain	Direction	Description
crs_o	rx_clk_mii_i	Output	Carrier Sense Detect – This active high signal asserts when rx_dv_o is high.

Table 4.35. SGMII (SERDES) Only Management Interface Ports on Avant Devices

Port	Clock Domain	Direction	Description
mr_adv_ability_i[15:0][1]	Asynchronous	Input	Advertised Ability—Configuration status transmitted by PCS during auto-negotiation process. This signal must not change during auto-negotiation.
mr_an_enable_i[1]	Asynchronous	Input	Auto-Negotiation Enable—Active high signal that enables auto-negotiation state machine to function. This signal must not change during auto-negotiation.
mr_main_reset_i[1]	Asynchronous	Input	Main Reset—Active high signal that forces all PCS state machines to reset.
mr_restart_an_i[1]	Asynchronous	Input	Auto-Negotiation Restart—Active high signal that forces auto-negotiation process to restart.
mr_an_complete_o	Asynchronous	Output	Auto-Negotiation Complete—This active high signal indicates that the auto-negotiation process is completed.
mr_lp_adv_ability_o[15:0]	Asynchronous	Output	Link Partner Advertised Ability—Configuration status received from partner PCS entity during the auto-negotiation process. The bit definitions are the same as described above for the mr_adv_ability_i port.
mr_page_rx_o	Asynchronous	Output	Auto-Negotiation Page Received—Active high signal that asserts while the auto-negotiation state machine is in the *Complete_Acknowledge* state.
force_isolate_i[1]	Asynchronous	Input	Force PCS Isolate—Active high signal that isolates the PCS. When asserted, the RX direction forces the (G)MII port to all zeros, regardless of the condition of the incoming 1.25 Gbps serial data stream. In the TX direction, the condition of the incoming (G)MII port is ignored. The TX PCS behaves as though the (G)MII TX input port was forced to all zeros. Note that the isolate function does not produce any electrical isolation – such as tri-stating of the (G)MII RX outputs of the IP core. When the signal is deasserted (low), the PCS isolation functions are deactivated. The use of this signal is optional. If you choose not to use the isolate function, then this signal must be tied low.
force_loopback_i[1]	Asynchronous	Input	Force PCS Loopback—Active high signal that activates the loopback function, before the PCS. When asserted, the 10-bit code-group output of the transmit state machine is looped back to the 10-bit code-group input of the receive state machine. When deasserted, the loopback function is deactivated. The use of this signal is optional. If you choose not to use the loopback function then this signal must be tied low.
force_unidir_i[1]	Asynchronous	Input	Force PCS Unidirectional Mode—Active high signal that activates the PCS unidirectional mode. When asserted, the transmit state machine path between the TX (G)MII input and the TX 10-bit code-group output remain operational, regardless of what happens on the RX datapath. Normally RX loss of sync, invalid code-group reception, auto-negotiation restarts can force the transmit state machine to temporarily ignore inputs from the TX (G)MII port. When deasserted, the unidirectional mode is deactivated. The use of this signal is optional. If you choose not to use the unidirectional function then this signal must be tied low.

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Note:

1. To control the AN process through these ports, you must set the Configuration Source Control Register (config_source) to 0. For more information, refer to the [0x00E] Configuration Source Control Register for Auto-Negotiation section.

Table 4.36. SGMII (SERDES) Only LMMI Interface Ports on Avant Devices

Port	Clock Domain	Direction	Description
lmmi_request_i	lmmi_clk_i	Input	Starts transaction.
lmmi_wr_rdn_i	lmmi_clk_i	Input	Write = 1’b1, Read = 1’b0.
lmmi_offset_i	lmmi_clk_i	Input	Register offset, starting at offset 0.
lmmi_wdata_i	lmmi_clk_i	Input	Output data bus.
lmmi_rdata_o	lmmi_clk_i	Output	Input data bus.
lmmi_rdata_valid_o	lmmi_clk_i	Output	Read transaction is complete and lmmi_rdata_o contains valid data.
lmmi_ready_o	lmmi_clk_i	Output	IP is ready to receive a new transaction. This is always asserted (tied to 1’b1).

The signals below are directly connected to the MPCS foundation IP, which must only be used for debug purposes. Note that this LMMI interface shares the same clock and reset as the LMMI interface in the table above.

Table 4.37. SGMII (SERDES) Only SERDES LMMI Interface Ports on Avant Devices

Port	Clock Domain	Direction	Description
mpphy_lmmi_request_i	lmmi_clk_i	Input	Starts transaction.
mpphy_lmmi_wr_rdn_i	lmmi_clk_i	Input	Write = 1’b1, Read = 1’b0.
mpphy_lmmi_offset_i	lmmi_clk_i	Input	Register offset, starting at offset 0.
mpphy_lmmi_wdata_i	lmmi_clk_i	Input	Input write data bus.
mpphy_lmmi_rdata_o	lmmi_clk_i	Output	Output read data bus.
mpphy_lmmi_rdata_valid_o	lmmi_clk_i	Output	Read transaction is complete and lmmi_rdata_o contains valid data.
mpphy_lmmi_ready_o	lmmi_clk_i	Output	IP is ready to receive a new transaction.

Table 4.38. SGMII (SERDES) Only Miscellaneous Interface Ports on Avant Devices

Port	Clock Domain	Direction	Description
sgmii_mode_i	Asynchronous	Input	SGMII Mode—Controls the behavior of the auto-negotiation process when the core is operating in SGMII mode. 0 = operates as MAC-side entity, 1 = operates as PHY-side entity.
gbe_mode_i	Asynchronous	Input	Gigabit Ethernet Mode—Controls the PCS function of the core. 0 = operates as SGMII PCS, 1 = operates as Gigabit Ethernet PCS (1000BASE-X).
operational_rate_i[1:0]	Asynchronous	Input	Operational Rate—When the core operates in SGMII PCS mode, this port controls the regulation rate of the rate adaptation circuit blocks as follows: 10 = 1 Gbps rate. 01 = 100 Mbps rate. 00 = 10 Mbps rate. Note: In Gigabit Ethernet PCS mode, the rate adaptation blocks always operate at the 1 Gbps rate, regardless of the settings on the operational_rate_i control pins.
debug_link_timer_short_i	Asynchronous	Input	Debug Link Timer Mode—Active high signal that forces the auto-negotiation link timer to run much faster than normal. This mode is provided for debug purposes. For example, allowing simulations to run through the auto-negotiation process much faster than normal. This signal must not change during the auto-negotiation process.
an_link_ok_o	Asynchronous	Output	Auto-Negotiation Link Status OK— This active high signal indicates

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Port	Clock Domain	Direction	Description
			that the link is ok. The signal is driven by the auto-negotiation state machine. When auto-negotiation is enabled, the signal asserts when the state machine is in the LINK_OK state. If auto-negotiation is disabled, the signal asserts when the state machine is in the AN_DISABLE_LINK_OK state (see IEEE 802.3 figure 37-6). This signal produces the Link Status signal as required by IEEE 802.3, Status Register 1, Bit D2 (see IEEE 802.3 paragraph 22.2.4.2.13).
mpphy_pma_rx0_sigdet_hf_o	Asynchronous	Output	PMA Receive high-frequency signal detection output. When asserted, it indicates that the receiver is receiving high-frequency signals.
mpphy_pma_rx0_sigdet_lf_o	Asynchronous	Output	PMA Receive low-frequency signal detection output. When asserted, it indicates that the receiver is receiving low-frequency signals.

4.14. MAC + SGMII (LVDS) Interfaces

The MAC + SGMII (LVDS) interface is only available in the MAC + SGMII (LVDS) configuration.

Note: The SGMII interface using LVDS I/O in Certus-NX, CertusPro-NX, MachXO5-NX, and CrossLink-NX FPGAs has limitations when operating across the full specified temperature range. Lattice recommends using alternative interfaces, such as SERDES or RGMII, for designs requiring Gigabit Ethernet. Refer to the Knowledge Base article for details. Contact your local Lattice sales representative for more information.

Table 4.39. MAC + SGMII (LVDS) Clock Interface Ports

Port	Clock Domain	Direction	Description
pll_refclk_i	—	Input	PLL Reference Clock – 250 MHz clock input for Avant devices and 125 MHz clock input for non-Avant devices.
clk_gddr_o	—	Output	DDR Clock – Assumes an LVDS buffer.
sgmii_tx_clk_en_o	usr_clk_o	Output	TX Clock Enable. The SGMII & Gb Ethernet PCS IP core drives this signal. The clock enable is always high for 1G operation. For 100 Mbps operation the clock enable is asserted high once every ten (125 MHz) clocks, and for 10 Mbps operation the clock enable is asserted high once every hundred (125 MHz) clocks.
sgmii_rx_clk_en_o	usr_clk_o	Output	RX Clock Enable. The SGMII & Gb Ethernet PCS IP core drives this signal. The clock enable is always high for 1G operation. For 100 Mbps operation the clock enable is asserted high once every ten (125 MHz) clocks, and for 10 Mbps operation the clock enable is asserted high once every hundred (125 MHz) clocks.
usr_clk_o	—	Output	User Clock. 125 MHz clock from the ECLKDIV output.
usr_clk_ready_o	—	Output	User Clock Ready. This signal indicates that the User Clock is ready.

Table 4.40. MAC + SGMII (LVDS) Serial Interface Ports

Port	Clock Domain	Direction	Description
ser_tx_o	Asynchronous	Output	Serial Transmit Data – DDR data. Assumes an LVDS buffer.
ser_rx_i	Asynchronous	Input	Serial Receive Data – DDR data. Assumes an LVDS buffer.

Table 4.41. MAC + SGMII (LVDS) Configuration Interface Ports

Port	Clock Domain	Direction	Description
operational_rate_i[1:0]	Asynchronous	Input	Operational Rate – When the core operates in SGMII PCS mode, this port controls the regulation rate of the rate adaptation circuit blocks as follows:

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Port	Clock Domain	Direction	Description
			10—1 Gbps rate 01—100 Mbps rate 00—10 Mbps rate Note in *Gigabit Ethernet* mode, the rate adaptation blocks always operate at the 1 Gbps rate, regardless of the settings on the operational_rate_i control pins.
debug_link_timer_short_i	Asynchronous	Input	Debug Link Timer Mode. Active high signal that forces the auto-negotiation link timer to run much faster than normal. This mode is provided for debug purposes. For example, allowing simulations to run through the auto-negotiation process much faster than normal. This signal must not change during the auto-negotiation process.

Table 4.42. MAC + SGMII (LVDS) Miscellaneous Interface Ports

Port	Clock Domain	Direction	Description
mr_main_reset_i	Asynchronous	Input	Main Reset.
mr_an_enable_i	Asynchronous	Input	Auto-Negotiation Enable.
mr_adv_ability_i[15:0]	Asynchronous	Input	Advertised Ability.
mr_restart_an_i	Asynchronous	Input	Auto-Negotiation Restart.
mr_an_complete_o	Asynchronous	Output	Auto-Negotiation Complete.
mr_lp_adv_ability_o[15:0]	Asynchronous	Output	Link Partner Advertised Ability.
mr_page_rx_o	Asynchronous	Output	Auto-Negotiation Page Received.
force_isolate_i	Asynchronous	Input	Force PCS Isolate.
force_loopback_i	Asynchronous	Input	Force PCS Loopback.
force_unidir_i	Asynchronous	Input	Force PCS Unidirectional Mode. Active high signal that activates the PCS unidirectional mode. When asserted, the transmit state machine path between the TX (G)MII input and the TX 10-bit code-group output remain operational, regardless of what happens on the RX datapath. (Normally RX loss of sync, invalid code-group reception, and auto-negotiation restarts can force the transmit state machine to temporarily ignore inputs from the TX (G)MII port). When de-asserted, the unidirectional mode is deactivated. The use of this signal is optional. If you choose not to use the unidirectional function, then this signal must be tied low.
an_link_ok_o	Asynchronous	Output	Auto-Negotiation Link Status OK.

4.15. MAC + SGMII (SERDES) Interfaces

The MAC + SGMII (SERDES) interface is only available in the MAC + SGMII (SERDES) configuration. Avant and Nexus devices implement different SERDES primitives, resulting in distinct interface characteristics between the two platforms.

4.15.1.MAC + SGMII (SERDES) Interfaces, Nexus SERDES Primitive, MPCS

For more information on MPCS interfaces and register, refer to the NX MPCS Module User Guide (FPGA-IPUG-02118).

Table 4.43. MAC + SGMII (SERDES) Clock and Reset Interface Ports on Nexus Devices

Port	Clock Domain	Direction	Description
clksel_i[1:0]	Asynchronous	Input	PMA-related clock multiplexer in MPCS Primitive. It is used to select from I/O pad, PLL, and fabric for PCS quad0 [1:0].

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Port	Clock Domain	Direction	Description
diffioclksel_i	Asynchronous	Input	PMA-related clock multiplexer in MPCS Primitive. Selection between I/O pad0 and I/O pad1.
use_refmux_i	Asynchronous	Input	PMA related clock multiplexer in MPCS Primitive. It is used to enable PCSREFMUX, which is a RefClk Mux Tree. This is used for dynamic switching of reference clock.
sdq_refclkp_q0_i	—	Input	MPCS PLL Reference Clock (positive) for Quad 0 – 125 MHz clock input.
sdq_refclkn_q0_i	—	Input	MPCS PLL Reference Clock (negative) for Quad 0 – 125 MHz clock input.
sdq_refclkp_q1_i	—	Input	MPCS PLL Reference Clock (positive) for Quad 1 – 125 MHz clock input.
sdq_refclkn_q1_i	—	Input	MPCS PLL Reference Clock (negative) for Quad 1 – 125 MHz clock input.
pll_0_refclk_i	—	Input	MPCS PLL Reference Clock from Left GPLL – 125 MHz clock input.
pll_1_refclk_i	—	Input	MPCS PLL Reference Clock from Right GPLL – 125 MHz clock input.
sd_ext_0_refclk_i	—	Input	MPCS PLL Reference Clock from external I/O pad0 - 125 MHz clock input.
sd_ext_1_refclk_i	—	Input	MPCS PLL Reference Clock from external I/O pad1 - 125 MHz clock input.
sd_pll_refclk_i	—	Input	MPCS PLL Reference Clock from fabric - 125 MHz clock input.
usr_clk_o	—	Output	User Clock. 125 MHz clock from the MPCS IP output.
usr_clk_ready_o	—	Output	User Clock Ready. This signal indicates that the User Clock is ready.
epcs_clkin_i	—	Input	Additional clock required by the MPCS IP, which is clocked by 125 MHz clock.
sgmii_tx_clk_en_o	usr_clk_o	Output	TX Clock Enable. The SGMII & Gb Ethernet PCS IP core drives this signal. The clock enable is always high for 1G operation. For 100 Mbps operation the clock enable is asserted high once every ten (125 MHz) clocks, and for 10 Mbps operation the clock enable is asserted high once every hundred (125 MHz) clocks.
sgmii_rx_clk_en_o	usr_clk_o	Output	RX Clock Enable. The SGMII & Gb Ethernet PCS IP core drives this signal. The clock enable is always high for 1G operation. For 100 Mbps operation the clock enable is asserted high once every ten (125 MHz) clocks, and for 10 Mbps operation the clock enable is asserted high once every hundred (125 MHz) clocks.
lmmi_clk_i	—	Input	LMMI clock—The typical recommended frequency is 125 MHz, depending on the fabric clock.
lmmi_resetn_i	Asynchronous	Input	LMMI active low reset.

Table 4.44. MAC + SGMII (SERDES) Serial Interface Ports on Nexus Devices

Port	Clock Domain	Direction	Description
sd0txp_o	Asynchronous	Output	Serial Transmit Data (positive).
sd0txn_o	Asynchronous	Output	Serial Transmit Data (negative).
sd0rxp_i	Asynchronous	Input	Serial Receive Data (positive).
sd0rxn_i	Asynchronous	Input	Serial Receive Data (negative).

Table 4.45. MAC + SGMII (SERDES) Configuration Interface Ports on Nexus Devices

Port	Clock Domain	Direction	Description
operational_rate_i[1:0]	Asynchronous	Input	Operational Rate – When the core operates in SGMII PCS mode, this port controls the regulation rate of the rate adaptation circuit blocks as follows: 10 — 1 Gbps rate

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Port	Clock Domain	Direction	Description
			01—100 Mbps rate 00—10 Mbps rate Note in Gigabit Ethernet mode, the rate adaptation blocks always operate at the 1 Gbps rate, regardless of the settings on the operational_rate_i control pins.
debug_link_timer_short_i	Asynchronous	Input	Debug Link Timer Mode. Active high signal that forces the auto-negotiation link timer to run much faster than normal. This mode is provided for debug purposes. For example, allowing simulations to run through the auto-negotiation process much faster than normal. This signal must not change during the auto-negotiation process.

Table 4.46. MAC + SGMII (SERDES) Miscellaneous Interface Ports on Nexus Devices

Port	Clock Domain	Direction	Description
gbe_mode_i	Asynchronous	Input	Set to 1 for 1000BASE-X Auto Negotiation, set to 0 for SGMII Auto Negotiation.
mr_main_reset_i	Asynchronous	Input	Main Reset.
mr_an_enable_i	Asynchronous	Input	Auto-Negotiation Enable.
mr_adv_ability_i[15:0]	Asynchronous	Input	Advertised Ability.
mr_restart_an_i	Asynchronous	Input	Auto-Negotiation Restart.
mr_an_complete_o	Asynchronous	Output	Auto-Negotiation Complete.
mr_lp_adv_ability_o[15:0]	Asynchronous	Output	Link Partner Advertised Ability.
mr_page_rx_o	Asynchronous	Output	Auto-Negotiation Page Received.
force_isolate_i	Asynchronous	Input	Force PCS Isolate.
force_loopback_i	Asynchronous	Input	Force PCS Loopback.
force_unidir_i	Asynchronous	Input	Force PCS Unidirectional Mode.
an_link_ok_o	Asynchronous	Output	Auto-Negotiation Link Status OK.

The signals below are direct connection to the MPCS foundation IP, which must only be used for debug purposes.

Table 4.47. MAC + SGMII (SERDES) LMMI Interface Ports on Nexus Devices

Port	Clock Domain	Direction	Description
mpcs_lmmi_request_i	clk_i	Input	Starts transaction.
mpcs_lmmi_wr_rdn_i	clk_i	Input	Write = 1'b1, Read = 1'b0.
mpcs_lmmi_offset_i	clk_i	Input	Register offset, starting at offset 0.
mpcs_lmmi_wdata_i	clk_i	Input	Input write data bus.
mpcs_lmmi_rdata_o	clk_i	Output	Output read data bus.
mpcs_lmmi_rdata_valid_o	clk_i	Output	Read transaction is complete and lmmi_rdata_o contains valid data.
mpcs_lmmi_ready_o	clk_i	Output	IP is ready to receive a new transaction.

4.15.2.MAC + SGMII (SERDES) Interfaces, Avant SERDES Primitive, MPPHY

For more information on MPPHY interfaces and register, refer to the Lattice Avant-G/X MPPHY Module User Guide (FPGA-IPUG-02233) .

Table 4.48. MAC + SGMII (SERDES) Clock and Reset Interface Ports on Avant Devices

Port	Clock Domain	Direction	Description
pad_refclkp_i	—	Input	MPPHY Quad Reference Clock of positive polarity. 156.25 MHz clock input.

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Port	Clock Domain	Direction	Description
pad_refclkn_i	—	Input	MPPHY Quad Reference Clock of negative polarity. 156.25 MHz clock input.
mpphy_rx_gclk_o	—	Output	Output receive clock forwarded to global clock distribution from the MPPHY IP output.
mpphy_tx_gclk_o	—	Output	Output transmit clock forwarded to global clock distribution from the MPPHY IP output.
pcs_usr_clk_i	—	Input	PCS User Clock. This 125 MHz clock input must connect to usr_clk_o.
usr_clk_o	—	Output	User Clock. 125 MHz clock from the MPPHY IP output.
usr_clk_ready_o	—	Output	User Clock Ready. This signal indicates that the User Clock is ready.
sgmii_tx_clk_en_o	usr_clk_o	Output	TX Clock Enable. The SGMII & Gb Ethernet PCS IP core drives this signal. The clock enable is always high for 1G operation. For 100 Mbps operation the clock enable is asserted high once every ten (125 MHz) clocks, and for 10 Mbps operation the clock enable is asserted high once every hundred (125 MHz) clocks.
sgmii_rx_clk_en_o	usr_clk_o	Output	RX Clock Enable. The SGMII & Gb Ethernet PCS IP core drives this signal. The clock enable is always high for 1G operation. For 100 Mbps operation the clock enable is asserted high once every ten (125 MHz) clocks, and for 10 Mbps operation the clock enable is asserted high once every hundred (125 MHz) clocks.
lmmi_clk_i	—	Input	LMMI clock—The typical recommended frequency is 125 MHz, depending on the fabric clock.
lmmi_resetn_i	Asynchronous	Input	LMMI active low reset.

Table 4.49. MAC + SGMII (SERDES) Serial Interface Ports on Avant Devices

Port	Clock Domain	Direction	Description
pad_txp_o	Asynchronous	Output	Serial Transmit Data (positive).
pad_txn_o	Asynchronous	Output	Serial Transmit Data (negative).
pad_rxp_i	Asynchronous	Input	Serial Receive Data (positive).
pad_rxn_i	Asynchronous	Input	Serial Receive Data (negative).

Table 4.50. MAC + SGMII (SERDES) Configuration Interface Ports on Avant Devices

Port	Clock Domain	Direction	Description
operational_rate_i[1:0]	Asynchronous	Input	Operational Rate – When the core operates in SGMII PCS mode, this port controls the regulation rate of the rate adaptation circuit blocks as follows: 10 — 1 Gbps rate 01—100 Mbps rate 00—10 Mbps rate Note that in Gigabit Ethernet mode, the rate adaptation blocks always operate at 1 Gbps rate, regardless of the settings on the operational_rate_i control pins.
debug_link_timer_short_i	Asynchronous	Input	Debug Link Timer Mode. Active high signal that forces the auto-negotiation link timer to run much faster than normal. This mode is provided for debug purposes. For example, allowing simulations to run through the auto-negotiation process much faster than normal. This signal must not change during the auto-negotiation process.

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Table 4.51. MAC + SGMII (SERDES) Miscellaneous Interface Ports on Avant Devices

Port	Clock Domain	Direction	Description
gbe_mode_i	Asynchronous	Input	Set to 1 for 1000BASE-X Auto Negotiation, set to 0 for SGMII Auto Negotiation.
mr_main_reset_i	Asynchronous	Input	Main Reset.
mr_an_enable_i	Asynchronous	Input	Auto-Negotiation Enable.
mr_adv_ability_i[15:0]	Asynchronous	Input	Advertised Ability.
mr_restart_an_i	Asynchronous	Input	Auto-Negotiation Restart.
mr_an_complete_o	Asynchronous	Output	Auto-Negotiation Complete.
mr_lp_adv_ability_o[15:0]	Asynchronous	Output	Link Partner Advertised Ability.
mr_page_rx_o	Asynchronous	Output	Auto-Negotiation Page Received.
force_isolate_i	Asynchronous	Input	Force PCS Isolate.
force_loopback_i	Asynchronous	Input	Force PCS Loopback.
force_unidir_i	Asynchronous	Input	Force PCS Unidirectional Mode.
an_link_ok_o	usr_clk_o	Output	Auto-Negotiation Link Status OK.
tx_pma_rdy_o	Asynchronous	Output	TX PMA ready.
rx_pma_rdy_o	Asynchronous	Output	RX PMA ready.
mpphy_pma_rx0_sigdet_hf_o	Asynchronous	Out	PMA Receive high-frequency signal detection output. When asserted, indicates that the receiver is receiving high-frequency signals.
mpphy_pma_rx0_sigdet_lf_o	Asynchronous	Out	PMA Receive low-frequency signal detection output. When asserted, indicates that the receiver is receiving low-frequency signals.

The signals below are direct connection to the MPCS foundation IP, which must only be used for debug purposes.

Table 4.52. MAC + SGMII (SERDES) LMMI Interface Ports on Avant Devices

Port	Clock Domain	Direction	Description
mpphy_lmmi_request_i	clk_i	Input	Starts transaction.
mpphy_lmmi_wr_rdn_i	clk_i	Input	Write = 1’b1, Read = 1’b0.
mpphy_lmmi_offset_i	clk_i	Input	Register offset, starting at offset 0.
mpphy_lmmi_wdata_i	clk_i	Input	Input write data bus.
mpphy_lmmi_rdata_o	clk_i	Output	Output read data bus.
mpphy_lmmi_rdata_valid_o	clk_i	Output	Read transaction is complete and lmmi_rdata_o contains valid data.
mpphy_lmmi_ready_o	clk_i	Output	IP is ready to receive a new transaction.

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5. Register Description

This section provides detailed descriptions of the TSE IP registers. Note that registers that are not available are highlighted in gray. When MAC Transmit or MAC Receive is enabled, the following registers are not configurable, 0x000 (except bit 2, Receive Enable and bit 3, Transmit Enable), 0x004, 0x008, 0x00C, 0x010, 0x014, 0x028, 0x02C.

The following table list the register address map that specifies the available IP core registers. The registers from offset 0x000 to 0x048 are MAC core registers.

Table 5.1. Register Address Map

Offset	Register Name	Access	Description
0x000	Mode	RW	Enables or disables IP core functions. This register can be written at any time.
0x004	Transmit and Receive Control	RW	This register can be overwritten only when the RX MAC and TX MAC are disabled. This register controls various features of the MAC.
0x008	Maximum Packet Size	RW	This register can be overwritten only when the MAC is disabled. All frames longer than the value (number of bytes) in this register is tagged as long frames.
0x00C	IPG (Inter-Packet Gap)	RW	Time between packet transmission.
0x010	MAC Address Word 0	RW	Contains the Ethernet address Word 0.
0x014	MAC Address Word 1	RW	Contains the Ethernet address Word 1.
0x018	Transmit and Receive Status	RO	This register reports events that have occurred while receiving or transmitting a packet.
0x01C	VLAN Tag	RO	This register has the VLAN tag field of the most recent tagged frame that was received.
0x020	GMII Management Interface Control	RW	The GMII Management Access register controls the Management Interface Module (MIIM). This register can be overwritten only when the interface is not busy. A write operation is ignored when the interface is busy.
0x024	GMII Management Data	RW	The contents of this register are transmitted when a Write operation is to be performed. When a Read operation is performed, this register contains the value that was read from a PHY register.
0x028	Multicast Table Word 0	RW	Multicast Table Word 0. First 4-bytes of the 64-bit hash.
0x02C	Multicast Table Word 1	RW	Multicast Table Word 1. The last 4-bytes of the 64-bit hash.
0x030	Pause Opcode	RO	PAUSE Opcode.
0x034	TX FIFO Almost Full Threshold	RW	This register can be overwritten only when the MAC is disabled.
0x038	TX FIFO Almost Empty Threshold	RW	This register can be overwritten only when the MAC is disabled.
0x03C	RX FIFO Almost Full Threshold	RW	This register can be overwritten only when the MAC is disabled.
0x040	RX FIFO Almost Empty Threshold	RW	This register can be overwritten only when the MAC is disabled.
0x044	Interrupt Status	RW1C	For more information on these registers, refer to the Lattice Memory Mapped Interface (LMMI) and Lattice Interrupt Interface (LINTR) User Guide (FPGA-UG-02039).
0x048	Interrupt Enable	RW	
0x04C-0x220	Statistic Counter registers	RO	For more information, refer to the [0x04C – 0x220] Statistics Counters section.
0x400-0x50C	SGMII PHY	—	For more information on this register, refer to the SGMII and Gb Ethernet PCS Soft IP Register section. For address mapping details, refer to the [0x400 – 0x50C] SGMII and Gb Ethernet PCS Soft IP Register section.
—	MPCS PHY	—	For more information on this register, refer to the NX MPCS Module User Guide (FPGA-IPUG-02118). This register is only accessible through MPCS LMMI interface ports.
—	MPPHY PHY	—	For more information on this register, refer to the Lattice Avant-G/X MPPHY Module User Guide (FPGA-IPUG-02233) . This

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Offset	Register Name	Access	Description
			register is only accessible through MPPHY LMMI interface ports.

The table below shows that the behavior of registers to write and read access is defined by its access type.

Table 5.2. Access Type Definition

Access Type	Behavior on Read Access	Behavior on Write Access
RO	Returns register value.	Ignores write access.
RW	Returns register value.	Updates register value.
RW1C	Returns register value.	Clears the register on write of 1, write value 0 is ignored.
RSVD	Returns 0.	Ignores write access.

5.1. [0x000] Mode Register

Table 5.3. Mode Register

Field	Name	Description	Access	Default
[31:5]	—	—	RSVD	27’h000_0000
[4]	hundredbit_en	100 Mbps Enable. This bit is only used for MII/GMII, RGMII, and RMII option. For RMII to operate in 100 Mbps, this bit must be set to 1. For RMII to operate in 10 Mbps, this bit must be set to 0. When bit [0] of mode register is set to 1, this bit doesn’t control anything. This bit echoes back what is written to it.	RW	1’b1
[3]	tx_en	Transmit Enable. When set to 1, the TX MAC is enabled to transmit frames. When reset, the TX MAC completes transmission of the packet currently being processed, then stops. Note: After enablement of TX MAC, wait 100us for the MAC to be stable.	RW	1’b0
[2]	rx_en	Receive Enable. When set to 1, the RX MAC is enabled to receive frames. When reset, the RX MAC completes reception of the packet currently being processed, then stops. Note: After enablement of TX MAC, wait 100us for the MAC to be stable.	RW	1’b0
[1]	fc_en	Flow-control Enable. When set to 1, it enables the flow control functionality of the TX MAC. This bit should be set to enable the TX MAC to transmit a PAUSE frame via the tx_sndpausreq_i and tx_sndpaustim_i[15:0] MAC input ports.	RW	1’b0
[0]	gbit_en	Gigabit Enable. For the MII/GMII and RGMII options, to operate in GbE mode, this bit must be set to 1. For 10/100 mode, this bit must be set to 0. For the RMII, SGMII Easy Connect MAC, and Gigabit MAC option, this bit does not control anything (Note: The MAC operation speed is determined by the clock enables provided by the SGMII IP core). This bit echoes back what is written to it. Note: The state of this bit is useful for system use	RW	1’b0

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Field	Name	Description	Access	Default
[31:5]	—	—	RSVD	27’h000_0000
		because the cpu_if_gbit_en_o output signal from the core always reflects the state of this register bit.		

5.2. [0x004] Transmit and Receive Control Register

Table 5.4. Transmit and Receive Control Register

Field	Name	Description	Access	Default
[31:9]	—	—	RSVD	23’h000_0000
[8]	receive_short	Receive Short Frames. When set to 1, it enables the RX MAC to receive frames shorter than 64 bytes.	RW	1’b0
[7]	receive_brdcst	Receive Broadcast. When set to 1, it enables the RX MAC to receive broadcast frames.	RW	1’b0
[6]	drop_control	Drop control. When set to 1, received control frames are dropped internal to the MAC and not transferred to the external RX client FIFO.	RW	1’b0
[5]	hden	Half-duplex Enable (10/100 mode only). When set to 1, configures the TX MAC to operate in half-duplex mode. When Enable Half Duplex Module Option is unchecked, this bit does not control anything. This bit echoes back what is written to it.	RW	1’b0
[4]	receive_mltcst	Receive Multicast. When set to 1, the multicast frames are received per the filtering rules for such frames. When set to 0, no Multicast (except PAUSE) frames is received.	RW	1’b0
[3]	receive_pause	Receive PAUSE frame. When set to 1, the RX MAC indicates the RX PAUSE frame reception to the TX MAC and thereby causes the TX MAC to pause the transmission of data frames for the period specified within the RX PAUSE frame.	RW	1’b0
[2]	tx_dis_fcs	Transmit Disable FCS. When set to 1, the FCS field generation is disabled in the TX MAC and the client is responsible for generating the appropriate FCS field.	RW	1’b0
[1]	discard_fcs	RX Discard FCS and Pad. When set to 1, the FCS and any of the padding bytes of an IEEE 802.3 frame are stripped off the frame before it is transferred to the RX FIFO. When set to 0, the entire frame is transferred into the RX FIFO. Note: Discarding padding bytes is only applicable to pure IEEE 802.3 frames (such as in backplane applications) and does not function on Ethernet frames (IP, UDP, ICMP, and so on) where the length field is now interpreted as a protocol type field.	RW	1’b0
[0]	prms	Promiscuous Mode. When set to 1, all filtering schemes are abandoned, and the RX MAC receives frames with any address.	RW	1’b0

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5.3. [0x008] Maximum Packet Size Register

Table 5.5. Maximum Packet Size Register

Field	Name	Description	Access	Default
[31:14]	—	—	RSVD	18’h00000
[13:0]	max_frame	The maximum packet size that can be handled by the core. Used only for statistical purposes. All frames longer than the value given here are marked as long. The value of this register does not affect the frame’s reception. Valid values: 14’0000 thru 14’h3FFB Maximum value is 14’h3FFB: any larger values are unsupported.	RW	14’h05EE

5.4. [0x00C] IPG (Inter-Packet Gap) Register

Table 5.6. Inter-Packet Gap Register

Field	Name	Description	Access	Default
[31:5]	—	—	RSVD	27’h000_0000
[4:0]	ipg	Inter-packet gap value in units of byte time. This register value is used by the TX MAC. The minimum Inter-packet gap value is 8.	RW	5'b01100

5.5. [0x010 – 0x014] MAC Address Register (0,1)

The MAC address is stored in the registers in hexadecimal form. For example, to set the MAC address to: AC-DE-48-00-00-80 would require writing 0xAC_DE_48_00 to address 0x010 (MAC_ADDR_0). 0x00_08 to address 0x014 (MAC_ADDR_1).

Table 5.7. MAC Address Word 0 Register

Field	Name	Description	Access	Default
[31:0]	mac_addr0	First four bytes of the MAC address. Ethernet address assigned to the port supported by the MAC.	RW	32’h0000_0000

Table 5.8. MAC Address Word 1 Register

Field	Name	Description	Access	Default
[31:16]	—	—	RSVD	16’h0000
[15:0]	mac_addr1	Last two bytes of the MAC address. Ethernet address assigned to the port supported by the MAC.	RW	16’h0000

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5.6. [0x018] Transmit and Receive Status Register

Table 5.9. Transmit and Receive Status Register

Field	Name	Description	Access	Default
[31:11]	—	—	RSVD	21’h000_0000
[10]	rx_idle	Receive MAC idle. Receive MAC in idle condition is used to reset configurations by the CPU interface.	RO	1’b1
[9]	tagged_frame	Tagged frame received.	RO	1’b0
[8]	brdcst_frame	Indicates that a Broadcast packet was received.	RO	1’b0
[7]	multcst_frame	Indicates that a Multicast packet was received.	RO	1’b0
[6]	ipg_shrink	IPG Shrink. Received frame with shrunk IPG (IPG < 96 bit time).	RO	1’b0
[5]	short_frame	Indicates that a packet shorter than 64 bytes has been received.	RO	1’b0
[4]	long_frame	Indicates receipt of a packet longer than the maximum allowable packet size specified in the MAX_PKT_SIZE Register.	RO	1’b0
[3]	error_frame	GMII rx_er_i asserted. Indicates the frame was received with the rx_er_isignal asserted.	RO	1’b0
[2]	crc	CRC error. Indicates a packet was received with a CRC error.	RO	1’b0
[1]	pause_frame	PAUSE frame. Indicates a PAUSE frame was received.	RO	1’b0
[0]	tx_idle	Transmit MAC idle. Transmit MAC in idle condition is used to reset configurations by the CPU interface.	RO	1’b1

5.7. [0x01C] VLAN Tag Register

Table 5.10. VLAN Tag Register

Field	Name	Description	Access	Default
[31:16]	—	—	RSVD	16’h0000
[15:0]	vlan	This field defines the length/type of field of the VLAN tag of the most recent tagged frame that was received.	RO	16’h0000

5.8. [0x020] GMII Management Register Access Control Register

Table 5.11. GMII Management Register Access Control Register

Field	Name	Description	Access	Default
[31:15]	—	—	RSVD	17’h000_0000
[14]	cmd_fin	Command Finished. When high, it means the interface has completed the intended operation. This bit is set to 0 when the interface is busy.	RO	1’b1
[13]	rw_phyreg	Read/Write PHY Registers When ‘1’—write operation When ‘0’—read operation	RW	1’b0
[12:8]	phy_add	GMII PHY Address. The address of the accessed PHY Bit 12 is the most significant bit, and it is the first PHY address bit to be transmitted and received.	RW	5’h00
[7:5]	—	—	RSVD	3’b000
[4:0]	reg_add	GMII Register Address. The address of the register is	RW	5’h00

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Field	Name	Description	Access	Default
		accessed. Bit 4 is the most significant bit and is the first register address bit to be transmitted or received.		

5.9. [0x024] GMII Management Access Data Register

Table 5.12. GMII Management Access Data Register

Field	Name	Description	Access	Default
[31:16]	—	—	RSVD	16'h0000
[15:0]	gmii_dat	GMII Data. Bit 15 is the most significant bit corresponding to bit 15 of the accessed register.	RW	16'h0000

5.10. [0x028 – 0x02C] Multicast Table Registers (0,1)

When the core is programmed to receive multicast frames, a filtering scheme is used to decide whether the frame should be received or not. The six middle bits of the most significant byte of the CRC value, calculated for the destination address, are used as a key to the 64-bit hash table. The three most significant bits select one of the eight tables, and the three least significant bits select a bit. The frame is received only if this bit is set.

Table 5.13. Multicast Table Word 0 Register

Field	Name	Description	Access	Default
[31:0]	multicast_table0	Multicast Table Word 0. Lower 32-bit of the 64-bit hash.	RW	32'h0000_0000

Table 5.14. Multicast Table Word 1 Register

Field	Name	Description	Access	Default
[31:0]	multicast_table1	Multicast Table Word 1. Upper 32-bit of the 64-bit hash.	RW	32'h0000_0000

5.11. [0x030] Pause Opcode Register

Table 5.15. Pause Opcode Register

Field	Name	Description	Access	Default
[31:16]	—	—	RSVD	16'h0000
[15:0]	pause_opcode	This register contains the pause opcode, which is compared against the opcode in the received pause frame. This value is also included in any pause frame transmitted by the MAC. Bit [15] is transmitted first and bit [0] is transmitted last.	RO	16'h0001

5.12. [0x034] TX FIFO Almost Full Threshold Register

Table 5.16. TX FIFO Almost Full Threshold Register

Field	Name	Description	Access	Default
[31:11]	—	—	RSVD	21'h00_0000
[10:0]	tx_fifo_afull_th	Almost Full Threshold.	RW	11'h1FF

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5.13. [0x038] TX FIFO Almost Empty Threshold Register

Table 5.17. TX FIFO Almost Empty Threshold Register

Field	Name	Description	Access	Default
[31:11]	—	—	RSVD	21’h00_0000
[10:0]	tx_fifo_aempty_th	Almost Empty Threshold	RW	11’h004

5.14. [0x03C] RX FIFO Almost Full Threshold Register

Table 5.18. RX FIFO Almost Full Threshold Register

Field	Name	Description	Access	Default
[31:11]	—	—	RSVD	21’h00_0000
[10:0]	rx_fifo_afull_th	Almost Full Threshold.	RW	11’h1FF

5.15. [0x040] RX FIFO Almost Empty Threshold Register

Table 5.19. RX FIFO Almost Empty Threshold Register

Field	Name	Description	Access	Default
[31:11]	—	—	RSVD	21’h00_0000
[10:0]	rx_fifo_aempty_th	Almost Empty Threshold.	RW	11’h004

5.16. [0x044] Interrupt Status Register

Table 5.20. Interrupt Status Register

Field	Name	Description	Access	Default
[31:8]	—	—	RSVD	24’h00_0000
[7]	tx_overflow_int	Indicates that a write request during the prior clock cycle was rejected because the FIFO is full. Overflowing the FIFO is not destructive to the contents of the FIFO. 0 – No interrupt. 1 – Interrupt pending. Write 1 to clear.	RW1C	1’b0
[6]	tx_full_int	Indicates that the TX FIFO is full. 0 – No interrupt. 1 – Interrupt pending. Write 1 to clear.	RW1C	1’b0
[5]	tx_afull_int	Indicates that the number of words in the TX FIFO is greater than or equal to the threshold. 0 – No interrupt. 1 – Interrupt pending. Write 1 to clear.	RW1C	1’b0
[4]	tx_aempty_int	Indicates that the number of words in the FIFO is less than or equal to the threshold. 0 – No interrupt. 1 – Interrupt pending. Write 1 to clear.	RW1C	1’b0
[3]	rx_underflow_int	Indicates that a read request during the previous	RW1C	1’b0

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Field	Name	Description	Access	Default
		clock cycle was rejected because the FIFO is empty. Underflowing the FIFO is not destructive to the FIFO. 0 – No interrupt. 1 – Interrupt pending. Write 1 to clear.		
[2]	rx_empty_int	Indicates that the FIFO is empty. 0 – No interrupt. 1 – Interrupt pending. Write 1 to clear.	RW1C	1’b0
[1]	rx_aempty_int	Indicates that the number of words in the FIFO is less than or equal to the threshold. 0 – No interrupt. 1 – Interrupt pending. Write 1 to clear.	RW1C	1’b0
[0]	rx_afull_int	Indicates that the number of words in the RX FIFO is greater than or equal to the threshold. 0 – No interrupt. 1 – Interrupt pending. Write 1 to clear.	RW1C	1’b0

5.17. [0x048] Interrupt Enable Register

Table 5.21. Interrupt Enable Register

Field	Name	Description	Access	Default
[31:8]	—	—	RSVD	24’h00_0000
[7]	tx_overflow_en	Defines the interrupt enabled bit corresponding to Transmit Buffer Overflow Interrupt source. 0 – Interrupt disabled. 1 – Interrupt enabled.	RW	1’b0
[6]	tx_full_en	Defines the interrupt enabled bit corresponding to Transmit Buffer Full Interrupt source. 0 – Interrupt disabled. 1 – Interrupt enabled.	RW	1’b0
[5]	tx_afull_en	Defines the interrupt enabled bit corresponding to Transmit Buffer Almost Full Interrupt source. 0 – Interrupt disabled. 1 – Interrupt enabled.	RW	1’b0
[4]	tx_aempty_en	Defines the Interrupt enabled of bit corresponding to Transmit Buffer Almost Empty Interrupt source. 0 – Interrupt disabled. 1 – Interrupt enabled.	RW	1’b0
[3]	rx_underflow_en	Defines the interrupt enabled bit corresponding to Receive Buffer Underflow Interrupt source. 0 – Interrupt disabled. 1 – Interrupt enabled.	RW	1’b0
[2]	rx_empty_en	Defines the interrupt enabled bit corresponding to Receive Buffer Empty Interrupt source. 0 – Interrupt disabled.	RW	1’b0

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Field	Name	Description	Access	Default
		1 – Interrupt enabled.		
[1]	rx_aempty_en	Defines the interrupt enabled bit corresponding to Receive Buffer Almost Empty Interrupt source. 0 – Interrupt disabled. 1 – Interrupt enabled.	RW	1'b0
[0]	rx_afull_en	Defines the Interrupt enabled of bit corresponding to Receive Buffer Almost Full Interrupt source. 0 – Interrupt disabled. 1 – Interrupt enabled.	RW	1'b0

5.18. [0x04C – 0x220] Statistics Counters

These statistic counters are wraparound counters and can only be reset when the system reset is asserted. Default value of these counters are 0.

Register name with "_0" means the least significant word of the counter and "_1" is the most significant word.

Table 5.22. Summary of Statistics Counters

Offset	Register Name	Description	Access
0x04C	TX_STAT_UNICST_0	Transmit Unicast Frame Statistic Counter. Counts the total number of unicast frames transmitted. tx_statvec_o[0] is used to implement this counter.	RO
0x050	TX_STAT_UNICST_1		RO
0x054	TX_STAT_MULTCST_0	Transmit Multicast Frame Statistic Counter. Counts the total number of multicast frames transmitted. tx_statvec_o[1] is used to implement this counter.	RO
0x058	TX_STAT_MULTCST_1		RO
0x05C	TX_STAT_BRDCST_0	Transmit Broadcast Frame Statistic Counter. Counts the total number of broadcast frames transmitted. tx_statvec_o[2] is used to implement this counter.	RO
0x060	TX_STAT_BRDCST_1		RO
0x064	TX_STAT_BADFCS_0	Transmit Bad FCS Frame Statistic Counter. Counts the total number of frames transmitted with BAD FCS. tx_statvec_o[3] is used to implement this counter.	RO
0x068	TX_STAT_BADFCS_1		RO
0x06C	TX_STAT_JMBO_0	Transmit Jumbo Frame Statistic Counter. Counts the total number of Jumbo frames transmitted. tx_statvec_o[4] is used to implement this counter.	RO
0x070	TX_STAT_JMBO_1		RO
0x074	TX_STAT_UNDER_RUN_0	FIFO Under-Run Statistic Counter. tx_statvec_o[5] is used to implement this counter.	RO
0x078	TX_STAT_UNDER_RUN_1		RO
0x07C	TX_STAT_PAUSE_0	Transmit Pause Frame Statistics Counter. Counts the total number of PAUSE frames transmitted. tx_statvec_o[6] is used to implement this counter.	RO
0x080	TX_STAT_PAUSE_1		RO
0x084	TX_STAT_VLN_TG_0	Transmit VLAN Tagged Frame Statistics Counter. Counts the total number of VLAN tagged frames transmitted. tx_statvec_o[7] is used to implement this counter.	RO
0x088	TX_STAT_VLN_TG_1		RO
0x08C	TX_STAT_FRM_LNGTH_0	Transmit Frame Length. Indicates the total number of octets transmitted in a particular frame. tx_statvec_o[21:8] is used to implement this counter.	RO
0x090	TX_STAT_FRM_LNGTH_1		RO

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Offset	Register Name	Description	Access
0x094	TX_STAT_DEFERRED_TRANS_0	Deferred Transmission Statistics Counter. tx_statvec_o[22] is used to implement this counter.	RO
0x098	TX_STAT_DEFERRED_TRANS_1		RO
0x09C	TX_STAT_EXCESSIVE_DEFERRED_TRANS_0	Excessive Deferred Transmission Statistics Counter. tx_statvec_o[23] is used to implement this counter.	RO
0x0A0	TX_STAT_EXCESSIVE_DEFERRED_TRANS_1		RO
0x0A4	TX_STAT_LATE_COL_0	Transmit Late Collision Statistics Counter. tx_statvec_o[24] is used to implement this counter.	RO
0x0A8	TX_STAT_LATE_COL_1		RO
0x0AC	TX_STAT_EXCESSIVE_COL_0	Transmit Excessive Collision Statistics Counter. tx_statvec_o[25] is used to implement this counter.	RO
0x0B0	TX_STAT_EXCESSIVE_COL_1		RO
0x0B4	TX_STAT_NUM_EARLY_COL_0	Transmit Number of Early Collisions. tx_statvec_o[29:26] is used to implement this counter.	RO
0x0B8	TX_STAT_NUM_EARLY_COL_1		RO
0x0BC	TX_STAT_SHRT_FRM_DIS_FCS_0	Transmit Short Frame (FCS Disabled) Statistics Counter. Counts the total number of short frames transmitted while the FCS generation is disabled. tx_statvec_o[30] is used to implement this counter.	RO
0x0C0	TX_STAT_SHRT_FRM_DIS_FCS_1		RO
0x0C4	TX_STAT_PTP1588_FRM_0	Transmit PTP1588 Frame Statistic Counter. Counts the total number of PTP1588 frames transmitted. tx_statvec_o[31] is used to implement this counter.	RO
0x0C8	TX_STAT_PTP1588_FRM_1		RO
0x0CC	TX_STAT_FRM_64_0	Transmit Frame 64 Statistics Counter. Counts the total number of frames transmitted with length equal to 64.	RO
0x0D0	TX_STAT_FRM_64_1		RO
0x0D4	TX_STAT_FRM_65_127_0	Transmit Frame 65 - 127 Statistics Counter. Counts the total number of frames transmitted with length between 65 and 127.	RO
0x0D8	TX_STAT_FRM_65_127_1		RO
0x0DC	TX_STAT_FRM_128_255_0	Transmit Frame 128-255 Statistics Counter. Counts the total number of frames transmitted with length between 128 and 255.	RO
0x0E0	TX_STAT_FRM_128_255_1		RO
0x0E4	TX_STAT_FRM_256_511_0	Transmit Frame 256-511 Statistics Counter. Counts the total number of frames transmitted with length between 256 and 511.	RO
0x0E8	TX_STAT_FRM_256_511_1		RO
0x0EC	TX_STAT_FRM_512_1023_0	Transmit Frame 512-1023 Statistics Counter. Counts the total number of frames transmitted with length between 512 and 1023.	RO
0x0F0	TX_STAT_FRM_512_1023_1		RO
0x0F4	TX_STAT_FRM_1024_1518_0	Transmit Frame 1024-1518 Statistics Counter. Counts the total number of frames transmitted with length between 1024 and 1518.	RO
0x0F8	TX_STAT_FRM_1024_1518_1		RO
0x0FC	TX_STAT_FRM_1519_2047_0	Transmit Frame 1519-2047 Statistics Counter. Counts the total number of frames transmitted with length between 1024 and 2047.	RO
0x100	TX_STAT_FRM_1519_2047_1		RO
0x104	TX_STAT_FRM_2048_4095_0	Transmit Frame 2048-4095 Statistics Counter. Counts the total number of frames transmitted with length between 2048 and 4095.	RO
0x108	TX_STAT_FRM_2048_4095_1		RO
0x10C	TX_STAT_FRM_4096_9216_0	Transmit Frame 4096-9216 Statistics Counter. Counts the total number of frames transmitted with length between 4096 and 9216.	RO
0x110	TX_STAT_FRM_4096_9216_1		RO
0x114	TX_STAT_FRM_9217_16383_0	Transmit Frame 9217-16383 Statistics Counter. Counts the total number of frames transmitted with length between 9217 and 16383.	RO
0x118	TX_STAT_FRM_9217_16383_1		RO

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Offset	Register Name	Description	Access
0x11C	RX_STAT_FRM_LNGTH_0	Receive Frame Length. Indicates the total number of octets received in a particular frame. rx_stat_vector_o [15:0] is used to implement this counter.	RO
0x120	RX_STAT_FRM_LNGTH_1		RO
0x124	RX_STAT_VLN_TG_0	Receive VLAN Tagged Frame Statistics Counter. Counts the total number of VLAN tagged frames received. rx_stat_vector_o [16] is used to implement this counter.	RO
0x128	RX_STAT_VLN_TG_1		RO
0x12C	RX_STAT_PAUSE_0	Receive Pause Frame Statistics Counter. Counts the total number of PAUSE frames received. rx_stat_vector_o [17] is used to implement this counter.	RO
0x130	RX_STAT_PAUSE_1		RO
0x134	RX_STAT_CTRL_0	Receive Control Frame Statistics Counter. Counts the total number of control frames received. rx_stat_vector_o [18] is used to implement this counter.	RO
0x138	RX_STAT_CTRL_1		RO
0x13C	RX_STAT_UNSP_OPCODE_0	Receive Unsupported Opcode Statistics Counter. Counts the total number of unsupported opcodes of the received control frames. rx_stat_vector_o [19] is used to implement this counter.	RO
0x140	RX_STAT_UNSP_OPCODE_1		RO
0x144	RX_STAT_DRIBB_NIBB_0	Receive Dribble Nibble Statistics Counter. rx_stat_vector_o [20] is used to implement this counter.	RO
0x148	RX_STAT_DRIBB_NIBB_1		RO
0x14C	RX_STAT_BRDCST_0	Receive Broadcast Frame Statistics Counter. Counts the total number of broadcast frames received. rx_stat_vector_o [21] is used to implement this counter.	RO
0x150	RX_STAT_BRDCST_1		RO
0x154	RX_STAT_MULTCST_0	Receive Multicast Frame Statistics Counter. Counts the total number of multicast frames received. rx_stat_vector_o [22] is used to implement this counter.	RO
0x158	RX_STAT_MULTCST_1		RO
0x15C	RX_STAT_UNICST_0	Receive Unicast Frame Statistics Counter. Counts the total number of unicast frames received.	RO
0x160	RX_STAT_UNICST_1		RO
0x164	RX_STAT_RCVD_OK_0	Receive OK Statistics Counter. Counts the total number of frames received without any error. rx_stat_vector_o [23] is used to implement this counter.	RO
0x168	RX_STAT_RCVD_OK_1		RO
0x16C	RX_STAT_LNGTH_ERR_0	Receive Length Check Error Frame Statistics Counter. Counts the total number of frames received with length check error. rx_stat_vector_o [24] is used to implement this counter.	RO
0x170	RX_STAT_LNGTH_ERR_1		RO
0x174	RX_STAT_CRC_ERR_0	Receive CRC Error Frame Statistics Counter. Counts the total number of frames received with CRC error. rx_stat_vector_o [25] is used to implement this counter.	RO
0x178	RX_STAT_CRC_ERR_1		RO
0x17C	RX_STAT_PKT_IGNORE_0	Receive Packet Ignored Statistics Counter. Counts the total number of packets ignored. rx_stat_vector_o [26] is used to implement this counter.	RO
0x180	RX_STAT_PKT_IGNORE_1		RO
0x184	RX_STAT_PREVIOUS_CARRIER_EVENT_0	Receive Carrier Event Previously Seen Statistics Counter. Counts the total number of previous frames	RO
0x188	RX_STAT_PREVIOUS_CARRIER_EVENT_1		RO

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Offset	Register Name	Description	Access
		received with a carrier event detected. rx_stat_vector_o [27] is used to implement this counter.	
0x18C	RX_STAT_PTP1588_FRM_0	Receive PTP1588 Frame Statistics Counter. Counts the total number of control frames received. rx_stat_vector_o [28] is used to implement this counter.	RO
0x190	RX_STAT_PTP1588_FRM_1		RO
0x194	RX_STAT_IPG_VIOL_0	Receive IPG Violation Frame Statistics Counter. Counts the total number of frames received with IPG violation. rx_stat_vector_o [29] is used to implement this counter.	RO
0x198	RX_STAT_IPG_VIOL_1		RO
0x19C	RX_STAT_SHRT_FRM_0	Receive Short Frame Statistics Counter. Counts the total number of short frames received. rx_stat_vector_o [30] is used to implement this counter.	RO
0x1A0	RX_STAT_SHRT_FRM_1		RO
0x1A4	RX_STAT_LNG_FRM_0	Receive Long Frame Statistics Counter. Counts the total number of long frames received. rx_stat_vector_o [31] is used to implement this counter.	RO
0x1A8	RX_STAT_LNG_FRM_1		RO
0x1AC	RX_STAT_FRM_UNDERSIZE_0	Receive Undersize Frame Statistics Counter. Counts the number of frames received that were less than 64 octets long and were otherwise well formed.	RO
0x1B0	RX_STAT_FRM_UNDERSIZE_1		RO
0x1B4	RX_STAT_FRM_FRAGMENTS_0	Receive Frame Fragments Statistics Counter. Counts the number of frames received with less than 64 octets in length and has either an FCS error or an Alignment error. rx_stat_vector_o [15:0] and rx_stat_vector_o [25] is used to implement this counter.	RO
0x1B8	RX_STAT_FRM_FRAGMENTS_1		RO
0x1BC	RX_STAT_FRM_JABBER_0	Receive Frame Jabbers Statistics Counter. Counts the number of frames received with length longer than 1518 octets and has either an FCS error or an Alignment error. rx_stat_vector_o [15:0] and rx_stat_vector_o [25] is used to implement this counter.	RO
0x1C0	RX_STAT_FRM_JABBER_1		RO
0x1C4	RX_STAT_FRM_64_GOOD_CRC_0	Receive Packet 64 With Good CRC Statistics Counter. Counts the number of packets received with a length less than 64 and with a good CRC. rx_stat_vector_o [15:0] and rx_stat_vector_o [25] is used to implement this counter.	RO
0x1C8	RX_STAT_FRM_64_GOOD_CRC_1		RO
0x1CC	RX_STAT_FRM_1518_GOOD_CRC_0	Receive Frame 1518 with Good CRC Statistics Counter. Counts the number of frames received with length more than 1518 and with a good CRC. rx_stat_vector_o [15:0] and rx_stat_vector_o [25] is used to implement this counter.	RO
0x1D0	RX_STAT_FRM_1518_GOOD_CRC_1		RO
0x1D4	RX_STAT_FRM_64_0	Receive Frame 64 Statistics Counter. Counts the total number of frames received with length equal to 64.	RO
0x1D8	RX_STAT_FRM_64_1		RO
0x1DC	RX_STAT_FRM_65_127_0	Receive Frame 65 - 127 Statistics Counter. Counts the total number of frames received with length between 65 and 127.	RO
0x1E0	RX_STAT_FRM_65_127_1		RO
0x1E4	RX_STAT_FRM_128_255_0	Receive Frame 128-255 Statistics Counter. Counts the total number of frames received with length	RO
0x1E8	RX_STAT_FRM_128_255_1		RO

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Offset	Register Name	Description	Access
		between 128 and 255.	
0x1EC	RX_STAT_FRM_256_511_0	Receive Frame 256-511 Statistics Counter. Counts the total number of frames received with length between 256 and 511.	RO
0x1F0	RX_STAT_FRM_256_511_1		RO
0x1F4	RX_STAT_FRM_512_1023_0	Receive Frame 512-1023 Statistics Counter. Counts the total number of frames received with length between 512 and 1023.	RO
0x1F8	RX_STAT_FRM_512_1023_1		RO
0x1FC	RX_STAT_FRM_1024_1518_0	Receive Frame 1024-1518 Statistics Counter. Counts the total number of frames received with length between 1024 and 1518.	RO
0x200	RX_STAT_FRM_1024_1518_1		RO
0x204	RX_STAT_FRM_1519_2047_0	Receive Frame 1519-2047 Statistics Counter. Counts the total number of frames received with length between 1024 and 2047.	RO
0x208	RX_STAT_FRM_1519_2047_1		RO
0x20C	RX_STAT_FRM_2048_4095_0	Receive Frame 2048-4095 Statistics Counter. Counts the total number of frames received with length between 2048 and 4095.	RO
0x210	RX_STAT_FRM_2048_4095_1		RO
0x214	RX_STAT_FRM_4096_9216_0	Receive Frame 4096-9216 Statistics Counter. Counts the total number of frames received with length between 4096 and 9216.	RO
0x218	RX_STAT_FRM_4096_9216_1		RO
0x21C	RX_STAT_FRM_9217_16383_0	Receive Frame 9217-16383 Statistics Counter. Counts the total number of frames received with length between 9217 and 16383.	RO
0x220	RX_STAT_FRM_9217_16383_1		RO
0x224	TX_STAT_PKT_LNGTH_ACC_0	Transmit Accumulation Byte Statistic Counter. Count and accumulate the total packet length that will receive from AXIS interface and transmit to the corresponding MII interface. The counter will roll over to 0 if full.	RO
0x228	TX_STAT_PKT_LNGTH_ACC_1		RO
0x22C	RX_STAT_PKT_LNGTH_ACC_0	Receive Accumulation Byte Statistic Counter. Count and accumulate the total packet length that will receive from corresponding MII interface and transmit to AXIS interface. The counter will not increase if the received packet is discarded by MAC. The counter will roll over to 0 if full.	RO
0x230	RX_STAT_PKT_LNGTH_ACC_1		RO

5.19. [0x400 – 0x50C] SGMII and Gb Ethernet PCS Soft IP Register

For MAC + PHY configuration, the SGMII and Gb Ethernet PCS soft IP is embedded as part of the TSE IP, the register access of the PCS performed via host interface of the TSE IP. Each address offset in the TSE MAC host interface is mapped to two addresses in the SGMII and Gb Ethernet PCS space. Single read/write access with the TSE IP (MAC) host interface will access two addresses in the PCS registers according to address mapping shown in Table 5.23.

For example, if you perform a register read access from address 0x0408 of TSE IP (MAC) host interface, the 32-bit host interface read data signal will contain values from the Advertised Ability register (offset: 0x004) as lower 16-bit of read data signal and Link Partner Ability register (offset: 0x005) as upper 16-bit of read data signal from the PCS.

If you perform a register write access to address 0x0440 of TSE IP (MAC) host interface, the 32-bit host interface write data signal must contain values for PCS Control Register 0 (offset: 0x020) as the lower 16-bit of write data signal and PCS Control Register 1 (offset: 0x021) as upper 16-bit of write data signal to the PCS.

For more information on PCS registers, refer to the SGMII and Gb Ethernet PCS Soft IP Register section.

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Table 5.23. Register Address Mapping of SGMII and Gb Ethernet PCS

MAC Address	PCS Address	MAC Host Interface 32-bit Data
0x0400	0x000	[15:0]
	0x001	[31:16]
0x0408	0x004	[15:0]
	0x005	[31:16]
0x040C	0x006	[15:0]
0x041C	0x00E	[15:0]
	0x00F	[31:16]
0x0440	0x020	[15:0]
	0x021	[31:16]
0x0450	0x029	[31:16]
0x0454	0x02A	[15:0]
	0x02B	[31:16]

5.20. SGMII and Gb Ethernet PCS Soft IP Register

List of registers for the SGMII only mode selection. Same registers will persist for the MAC + SGMII option, and can be accessed via the offsets as described in the [0x400 – 0x50C] SGMII and Gb Ethernet PCS Soft IP Register section.

This section provides detailed descriptions of SGMII data registers. Note that registers that are not available are highlighted in gray.

The table below lists the register address map that specifies the available IP core registers.

Table 5.24. Register Address Map

Offset	Register Name	Description
0x000	Control Register	These are five management registers specified in IEEE 802.3, Clause 37 – Control, Status, Auto Negotiation Advertisement, Link Partner Ability, Auto Negotiation Expansion, and Extended Status. The register set is accessible through the LMMI or MDIO interface.
0x001	Status Register	
0x004	Advertised Ability	
0x005	Link Partner Ability	
0x006	Auto Negotiation Expansion Register	
0x00F	Extended Status Register	
0x00E	Configuration Source Control Register	Switches between SGMII Core management ports and internal configuration registers. This register is accessible through the LMMI or MDIO interface.
0x010 – 0x01C	Reserved	Do not use.
0x020	PCS Control Register 0	PCS Debugging Control Register 0. This register is only accessible through the LMMI interface.
0x021	PCS Control Register 1	PCS Debugging Control Register 1. This register is only accessible through the LMMI interface.
0x029	PCS Status Register 9	RX, TX, and CTC FIFO Status. This register is only accessible through the LMMI interface.
0x02A	PCS Control Register 10	PCS Debugging Control Register 10. This register is only accessible through the LMMI interface.
0x02B	PCS Control Register 11	PCS Debugging Control Register 11. This register is only accessible through the LMMI interface.

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5.20.1. [0x000] Auto-Negotiation Control Register

Table 5.25. Control Register

Field	Name	Access	Width	Description	Default
15	Reset	RW	1	1 – Reset (self-clearing) 0 – Normal operation This register is equivalent to mr_main_reset_i.	1’b0
14	Loopback	RW	1	1 – Loopback 0 – Normal operation This register is equivalent to force_loopback_i.	1’b0
13	Speed Selection[0]	RW	1	Combined with bit[6] to form 2-bit vector Speed Selection [1:0] = 11 = reserved Speed Selection [1:0] = 10 = 1 Gbps Speed Selection [1:0] = 01 = 100 Mbps Speed Selection [1:0] = 00 = 10 Mbps In GbE Mode, Speed Selection [1:0] is stuck at *10* = 1 Gbps. In SGMII Mode, the Speed Selection [1:0] bits can be written to any value.	1’b0
12	Auto Neg Enable	RW	1	1 – Enable 0 – Disable	1’b1
11	Power Down	RW	1	1 – Enable 0 – Disable This feature is not supported.	1’b0
10	Isolate	RW	1	1 – Isolate 0 – Normal operation This register is equivalent to force_isolate_i.	1’b0
9	Restart Auto Neg	RW	1	1 – Restart auto-negotiation 0 – Normal operation This register is equivalent to mr_an_restart_i.	1’b0
8	Duplex Mode	RO	1	1 – Full Duplex 0 – Half Duplex Note that the setting of this bit has no effect on the operation of the PCS channel. The PCS channel is always a 4-wire interface with separate TX and RX datapaths.	1’b1
7	Collision Test	RO	1	1 – Enable test 0 – Normal operation This register is dependent on bit[14] or force_loopback_i. Setting this bit only takes effect when bit[14] or force_loopback_i is asserted.	1’b0
6	Speed Selection[1]	RW	1	Combined with bit [13] to form the 2-bit vector Speed Selection [1:0]	1’b1
5	Unidirectional	RW	1	1 – Loopback 0 – Normal operation This register is equivalent to force_unidir_i.	1’b0
4:0	—	RSVD	5	—	5’h00

5.20.2. [0x001] Auto-Negotiation Status Register

Table 5.26. Status Register

Bit Field	Name	Access	Width	Description	Default
15	100BASE-T4	RO	1	0 – Not supported	1’b0
14	100BASE-X Full Duplex	RO	1	0 – Not supported	1’b0
13	100BASE-X Half Duplex	RO	1	0 – Not supported	1’b0
12	10 Mbps Full Duplex	RO	1	0 – Not supported	1’b0
11	10 Mbps Half Duplex	RO	1	0 – Not supported	1’b0
10	100BASE-T2 Full Duplex	RO	1	0 – Not supported	1’b0

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Bit Field	Name	Access	Width	Description	Default
9	100BASE-T2 Half Duplex	RO	1	0 – Not supported	1’b0
8	Extended Status	RO	1	1 – Supported	1’b1
7	Unidirectional Capability	RO	1	1 – Supported 0 – Not supported	1’b0
6	MF Preamble Suppress	RO	1	0 – Not supported	1’b0
5	Auto Neg Complete	RO	1	1 – Complete 0 – Not complete Ignore this bit, if AN is disabled.	1’b0
4	Remote Fault	RO	1	0 – Not supported	1’b0
3	Auto Neg Ability	RO	1	1 – Supported	1’b1
2	Link Status	RO	1	1 – Link Up 0 – Link Down (or has been down) Latches on 0 if Link Status goes down. A subsequent read operation clears the latch.	1’b0
1	Jabber Detect	RO	1	0 – Not supported	1’b0
0	Extended Capability	RO	1	0 – Not supported	1’b0

5.20.3. [0x004] Auto-Negotiation Advertised Ability Register

Table 5.27. For PCS=GbE

Bit Field	Name	Access	Width	Description	Default
15	Next Page	RW	1	The Base Page and subsequent Next Pages may set the NP bit to a logic one to request Next Page transmission. Subsequent Next Pages may set the NP bit to a logic zero to communicate that there is no more Next Page information to be sent (see Clause 37.2.4.3 of IEEE 802.3). A device may implement Next Page ability and choose not to engage in a Next Page exchange by setting the NP bit to a logic zero. This feature is not supported. This bit should always be 0.	1’b0
14	Acknowledge	RW	1	The Ack bit is used by the Auto-Negotiation function to indicate that a device has successfully received its link partner’s base or Next Page.	1’b1
13:12	Remote Fault	RW	2	The Remote Fault function may indicate to the link partner that a fault or error condition has occurred. 0 – No error, link OK (default) 1 – Offline 2 – Link Failure 3 – Auto-Negotiation Error	2’b00
11:9	—	RSVD	3	—	3’b000
8:7	Pause	RW	2	Pause provides a pause capability exchange mechanism. 0 – No PAUSE 1 – Asymmetric PAUSE toward link partner 2 – Symmetric PAUSE 3 – Both Symmetric PAUSE and Asymmetric PAUSE toward local device	2’b00
6	Half Duplex	RW	1	Half Duplex Capability	1’b0
5	Full Duplex	RW	1	Full Duplex Capability	1’b0
4:0	—	RSVD	5	—	5’b00000

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Table 5.28. For PCS=SGMII-PHY-Side

Bit Field	Name	Access	Width	Description	Default
15	Link Status	RW	1	1 – Link Up 0 – Link Down	1’b0
14	Acknowledge	RW	1	The Ack bit is used by the Auto-Negotiation function to indicate that a device has successfully received its link partner’s base or Next Page.	1’b1
13	—	RSVD	1	—	1’b0
12	Duplex Mode	RW	1	1 – Full Duplex 0 – Half Duplex	1’b0
11:10	Speed	RW	2	11 – Reserved 10 – 1 Gbps 01 – 100 Mbps 00 – 10 Mbps	2’b00
9:0	—	RO	10	Value=10’h001	10’h001

Table 5.29. For PCS=SGMII-MAC-Side

Bit Field	Name	Access	Width	Description	Default
15:0	—	RO	16	Value=16’h4001	16’h40 01

5.20.4.[0x005] Auto-Negotiation Link Partner Ability

Table 5.30. For PCS=GbE

Bit Field	Name	Access	Width	Description	Default
15	Next Page	RO	1	The Base Page and subsequent Next Pages may set the NP bit to a logic one to request Next Page transmission. Subsequent Next Pages may set the NP bit to a logic zero to communicate that there is no more Next Page information to be sent (see Clause 37.2.4.3 of IEEE 802.3). A device may implement Next Page ability and choose not to engage in a Next Page exchange by setting the NP bit to a logic zero.	1’b0
14	Acknowledge	RO	1	The Ack bit is used by the Auto-Negotiation function to indicate that a device has successfully received its link partner’s base or Next Page.	1’b0
13:12	Remote Fault	RO	2	The Remote Fault function may indicate to the link partner that a fault or error condition has occurred. 0 – No error, link OK (default) 1 – Offline 2 – Link Failure 3 – Auto-Negotiation Error	2’b00
11:9	—	RSVD	3	—	3’b000
8:7	Pause	RO	2	Pause provides a pause capability exchange mechanism. 0 – No PAUSE 1 – Asymmetric PAUSE toward link partner 2 – Symmetric PAUSE 3 – Both Symmetric PAUSE and Asymmetric PAUSE toward local device	2’b00
6	Half Duplex	RO	1	Half duplex capability.	1’b0
5	Full Duplex	RO	1	Full duplex capability.	1’b0
4:0	—	RSVD	5	—	5’b00000

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Table 5.31. For PCS=SGMII-PHY-Side

Bit Field	Name	Access	Width	Description	Default
15	Link Status	RO	1	1 – Link Up 0 – Link Down	1'b0
14	Acknowledge	RO	1	The Ack bit is used by the Auto-Negotiation function to indicate that a device has successfully received its link partner's base or Next Page.	1'b0
13	—	RSVD	1	—	1'b0
12	Duplex Mode	RO	1	1 – Full Duplex 0 – Half Duplex	1'b0
11:10	Speed	RO	2	11 – Reserved 10 – 1 Gbps 01 – 100 Mbps 00 – 10 Mbps	2'b00
9:0	—	RO	10	Value=10'h001	10'h001

5.20.5. [0x006] Auto Negotiation Expansion Register

Table 5.32. Auto-Negotiation Expansion Register

Bit Field	Name	Access	Width	Description	Default
15:3	—	RSVD	13	—	13'h0000
2	Next Page Able	RO	1	0 – Not supported	1'b0
1	Page Received	RO	1	1 – Received 0 – Not received latch on 1, clear on read	1'b0
0	—	RSVD	1	—	1'b0

5.20.6. [0x00F] Auto-Negotiation Extended Status Register

Table 5.33. Auto-Negotiation Extended Status Register

Bit Field	Name	Access	Width	Description	Default
15	1000BASE-X Full Duplex	RO	1	1 – Supported	1'b1
14	1000BASE-X Half Duplex	RO	1	0 – Not supported	1'b0
13	1000BASE-T Full Duplex	RO	1	0 – Not supported	1'b0
12	1000BASE-T Half Duplex	RO	1	0 – Not supported	1'b0
11:0	—	RSVD	12	—	12'h000

5.20.7. [0x00E] Configuration Source Control Register for Auto-Negotiation

Table 5.34. Configuration Source Control Register

Bit Field	Name	Access	Width	Description	Default
15:1	—	RSVD	15	—	15'h0000
0	config_source	RW	1	Select the Configuration Source for Auto-Negotiation. 0 – From Management Ports, mr_* ports 1 – From Auto-Negotiation Programmable Registers [0x000] – [0x00F] *Note: This method of using management ports is not validated in Avant devices.	1'b0

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5.20.8. [0x020] PCS Control Register 0

Table 5.35. PCS Control Register 0

Bit Field	Name	Access	Width	Description	Default
15	enable_cgalign	RW	1	1 – Enable/restart code group alignment 0 – Disable code group alignment This bit is only valid when lsm_disable = 1. **Note**: The IP core ignores any value of this bit because lsm_eca of PCS Control Register 10 is always enabled.	1’b1
14:13	—	RSVD	2	—	2’b00
12	ge_an_enable	RW	1	Auto-negotiation enable. 1 – Enables the feature 0 – Disables the feature	1’b0
11:0	—	RSVD	12	—	12’h000

5.20.9. [0x021] PCS Control Register 1

Table 5.36. PCS Control Register 1

Bit Field	Name	Access	Width	Description	Default
15	—	RSVD	1	—	1’b0
14	sb_bypass	RW	1	This bit must always be active (1). Deactivation breaks the link. For debugging purpose only.	1’b1
13:12	—	RSVD	2	—	2’b00
11	enc_bypass	RW	1	This bit must always be inactive (0). Activation excludes the encoder from the TX path. For debugging purpose only.	1’b0
10	—	RSVD	1	—	1’b0
9	tx_gear_bypass	RW	1	1 – Bypass PCS TX gear box 0 – Enable PCS TX gear box This bit must always be active (1). Deactivation breaks the link.	1’b1
8	fb_loopback	RW	1	Activates RX-TX loopback. Loopback activation must be done at least 500 ns before tx_en activation and removed later than at least 500 ns after tx_en drop (or core tx-rx latency delay). This makes the transition from loopback to normal mode seamless. When this bit is enabled, You must ignore data coming out from the RX MAC.	1’b0
7	lsm_disable	RW	1	1 – Disable RX link synchronizer. When RX link synchronizer is disabled, user must manually control the word alignment through enable_cgalign bit of PCS Control Register 0. 0 – Enable RX link synchronizer. When this bit is set, ls_sync_status of PCS Control Register 9 is always 1’b1. This bit is only valid when lsm_eca of PCS Control Register 10 is disabled. **Note**: The IP core ignores any value of this bit because lsm_eca of PCS Control Register 10 is always enabled.	1’b0

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Bit Field	Name	Access	Width	Description	Default
6	signal_detect	RW	1	1 – Force to enable/restart RX link synchronization 0 – Start of link synchronization is dependent on the Link Status (bit[2] of Status Register).	1’b0
5	rx_gear_bypass	RW	1	This bit must always be active (1). Deactivation breaks the RX link.	1’b1
4	ctc_bypass	RW	1	This bit must always be active (1). Otherwise, additional CTC is added into the RX path, which is necessary when SGMII is in the Gigabit Ethernet Mode.	1’b1
3	dec_bypass	RW	1	This bit must always be inactive (0). Otherwise, it breaks the link. For debugging purposes.	1’b0
2	wa_bypass	RW	1	This bit must always be inactive (0). Otherwise, it breaks the link. For debugging purposes.	1’b0
1:0	—	RSVD	2	—	2’b00

5.20.10. [0x029] PCS Control Register 9

Table 5.37. PCS Control Register 9

Bit Field	Name	Access	Width	Description	Default
15:11	—	RSVD	6	—	7’h00
10:7	align_status	RO	4	Word alignment status – number of bits that the input has been shifted.	4’h0
6	ls_sync_status	RO	1	Link synchronization status 1 – Link synchronization achieved. 0 – Link synchronization not yet achieved.	1’b0
5	rstb_rxf	RO	1	Receiver reset pulse.	1’b0
4	rstb_txf	RO	1	Transmitter reset pulse.	1’b0
3:0	—	RSVD	4	—	4’h0

5.20.11. [0x02A] PCS Control Register 10

Table 5.38. PCS Control Register 10

Bit Field	Name	Access	Width	Description	Default
15	lsm_eca	RW	1	Enables code group alignment regardless of *lsm_disable* and *fc_mode*. This bit must always be 1 for this IP core.	1’b1
14:13	—	RSVD	2	—	2’b00
12	wa_mode	RW	1	1 – Bitslip word alignment mode. 0 – Barrel shift word alignment mode. This bit must always be 0 for this IP core.	1’b0
11:10	—	RSVD	2	—	2’b00
9	fc_mode	RW	1	1 – Fiber channel link synchronization. 0 – 1000BASE-X link synchronization. This bit must always be 0 for this IP core.	1’b0
8:0	—	RSVD	9	—	9’h000

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6. Example Design

The Tri-Speed Ethernet IP example design allows you to compile, simulate, and test the Tri-Speed Ethernet IP on the following Lattice evaluation boards:

- Avant-E Evaluation Board
- Avant-G/X Versa Board
- CertusPro-NX Versa Board
- CertusPro-NX Evaluation Board

6.1. Design Boards and Ethernet FMC Overview

The Lattice Semiconductor evaluation board allows you to investigate and experiment with the features of the FPGA device. The features of the evaluation board can assist you with rapid prototyping and testing of your specific design.

6.1.1. Avant-E Evaluation Board

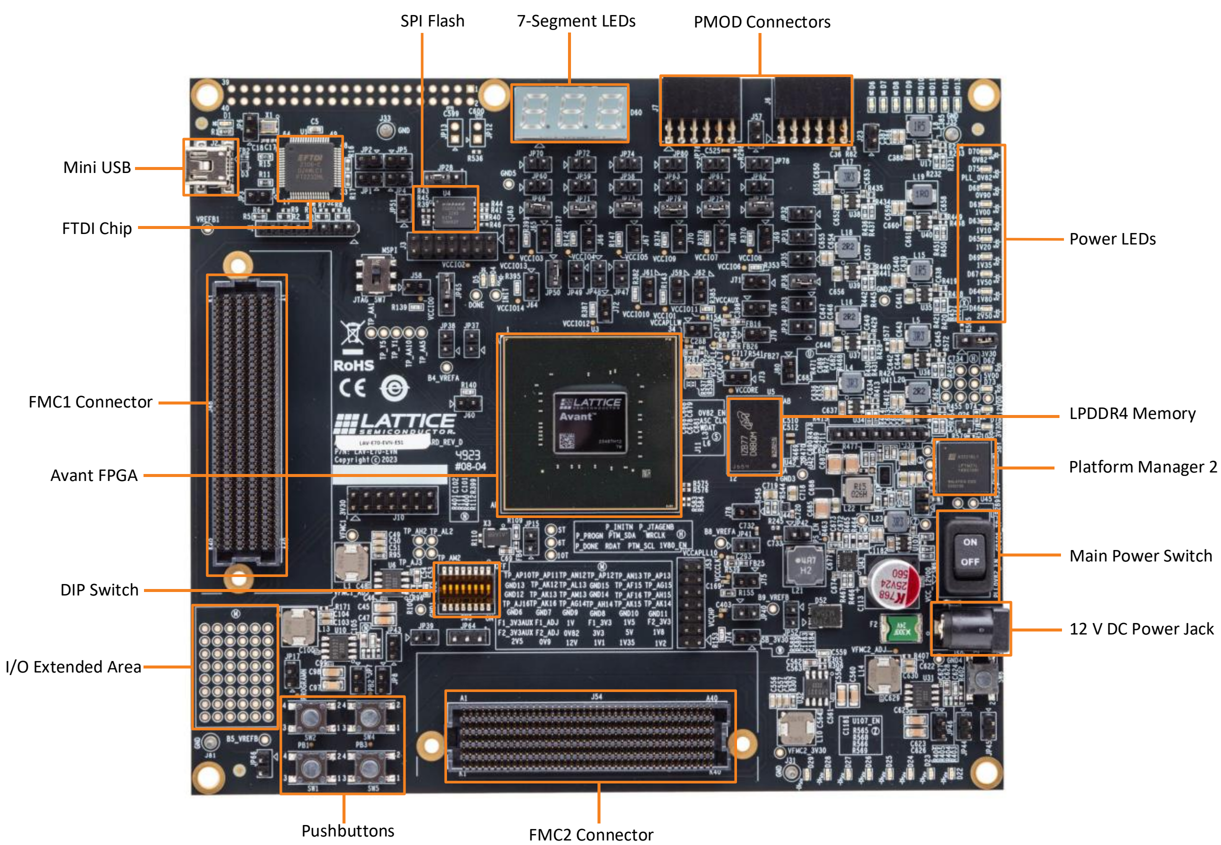

Figure 6.1. Top View of Avant-E Evaluation Board

For more information on Avant Evaluation Board, refer to the Avant Evaluation Board User Guide (FPGA-EB-02057).

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6.1.2. Avant G/X Versa Board

The Avant-G/X Versa Board features the Avant-AT-G/X FPGA in the LFG1156 package. The board can expand the usability of the Avant-G/X FPGA with FMC+, SFP28. QSFP28, and Raspberry Pi connectors. Easy-to-use board resources of the jumpers, LED indicators, pushbuttons, and switches are available for various user-defined applications.

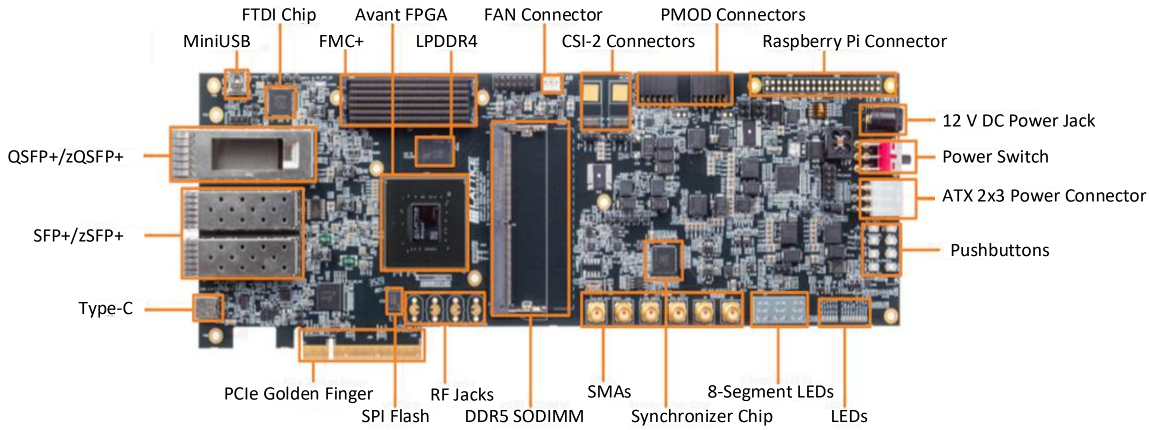

Figure 6.2. Top View of the Avant-G/X Versa Board

For more information on the Avant-G/X Versa Board, refer to the Avant-G/X Versa Board User Guide (FPGA-EB-02063).

6.1.3. CertusPro-NX Versa Board

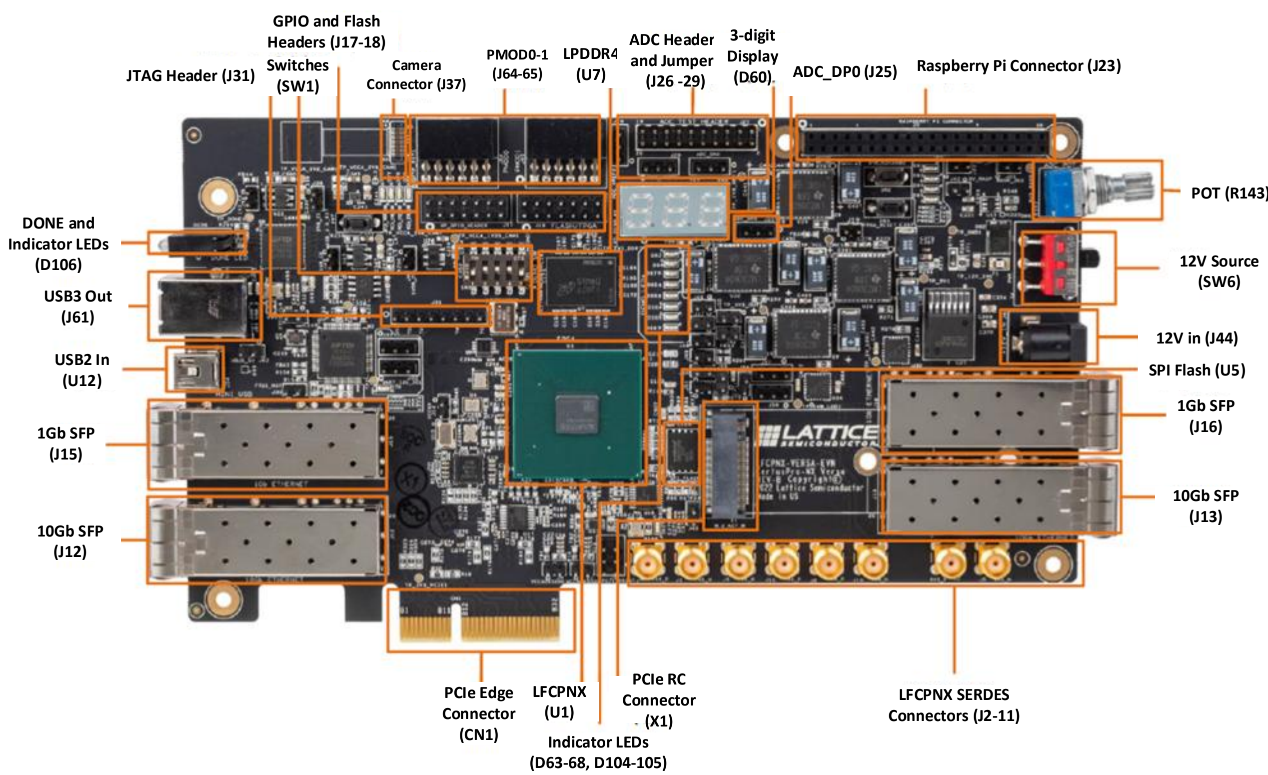

Figure 6.3. Top View of CertusPro-NX Versa Board

For details on the CertusPro-NX Versa Board, refer to the CertusPro-NX Versa Board User Guide (FPGA-EB-02053).

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6.1.4. CertusPro-NX Evaluation Board

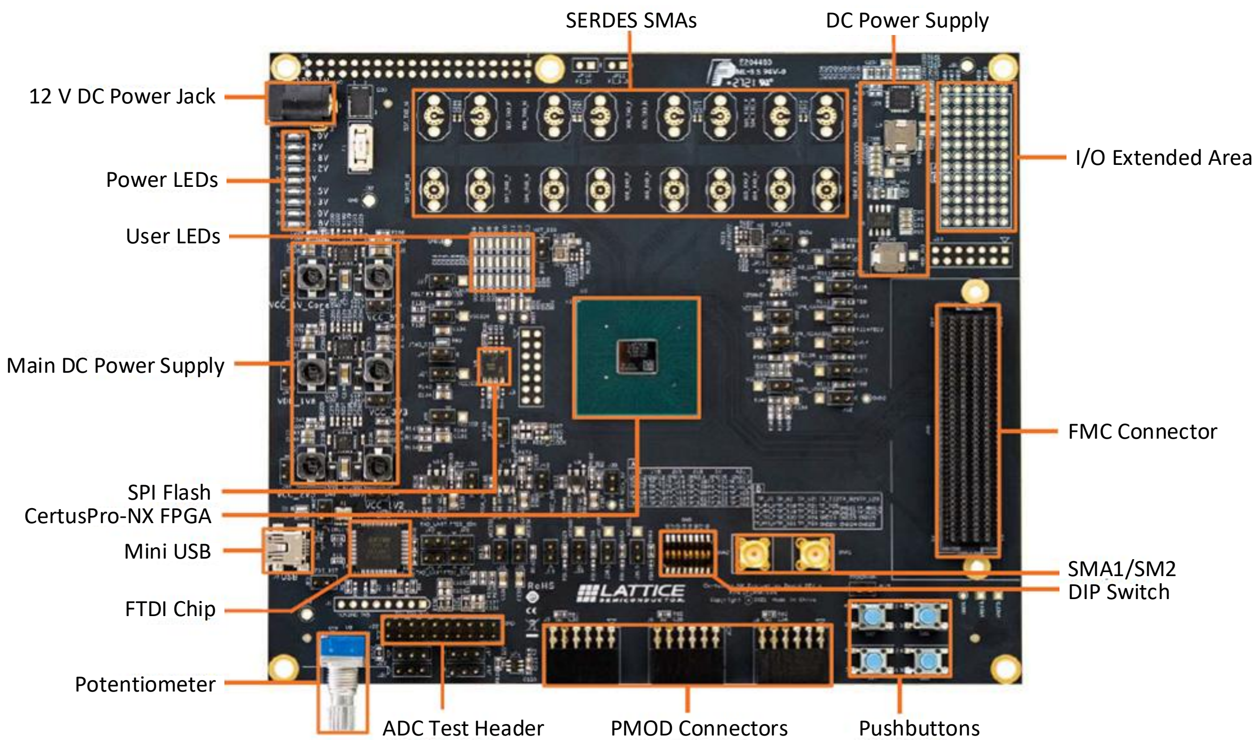

Figure 6.4. Top View of CertusPro-NX Evaluation Board

For more information on CertusPro-NX Evaluation Board, refer to the CertusPro-NX Evaluation Board User Guide (FPGA-EB-02046).

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6.1.5. Ethernet FMC Module

The Ethernet FPGA Mezzanine Card (FMC) is an add-on or expansion board for FPGA and SoC-based development boards. The mezzanine card has 4X Marvell 88E151x Gigabit Ethernet PHYs to provide four ports of gigabit Ethernet connectivity to the carrier development board.

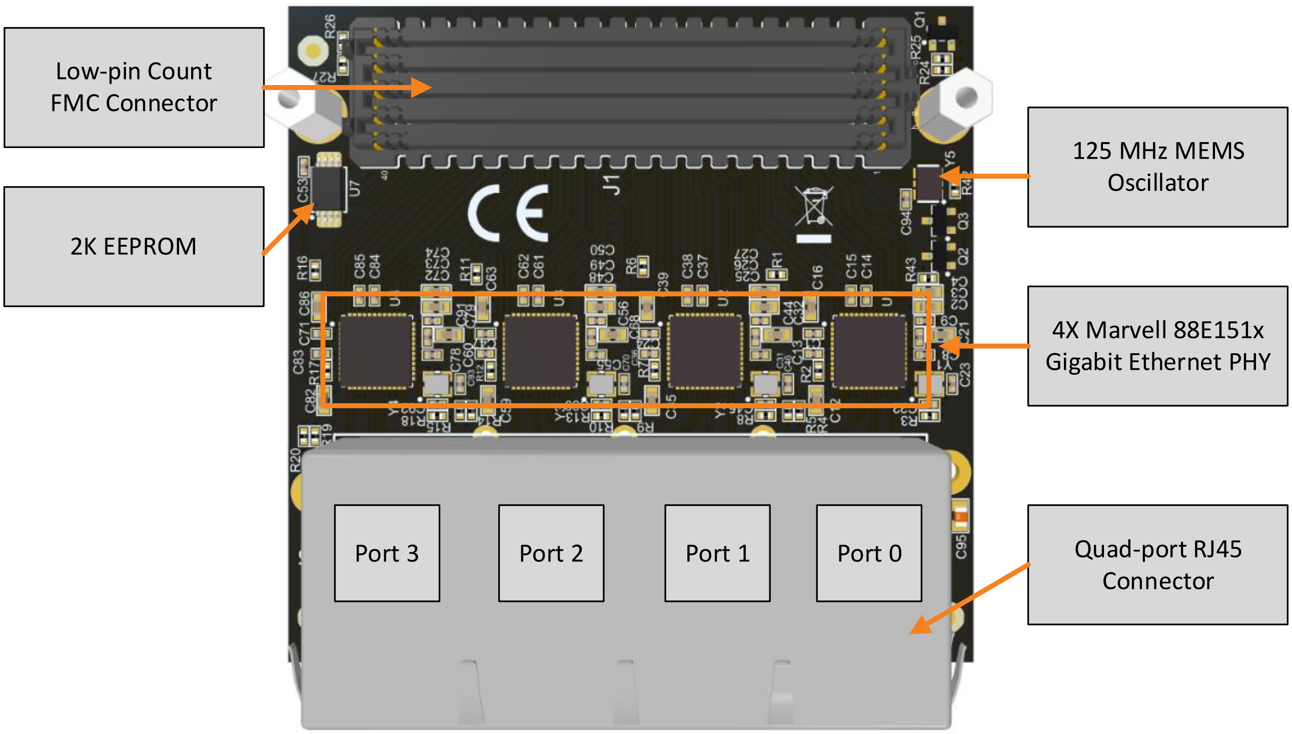

Figure 6.5. Top View of Ethernet FMC

For more information on Ethernet FMC, refer to the Ethernet FMC website.

6.2. Example Design Supported Configuration

This section provides information on how to use the Tri-Speed Ethernet IP with the following example designs:

- RGMII example design on Avant-E Evaluation Board, CertusPro-NX Evaluation Board with external PHY using FMC card cable loopback.
- RMII example design on CertusPro-NX Versa Board.
- SGMII (LVDS) example design on Avant-G/X Versa Board with PCS loopback.
- SGMII (SERDES) example design on CertusPro-NX Versa Board and Avant-X Versa Board with SFP loopback

Table 6.1. TSE IP Configuration Supported by Example Designs

TSE IP GUI Parameter	Example Design			
	RGMII Design	**RMII Design**	**SGMII (LVDS) Design**	**SGMII (SERDES) Design**
Device	Avant-E, CertusPro-NX	CertusPro-NX	Avant-G/X	Avant-X, CertusPro-NX
PHY	External PHY with FMC card	—	—	SFP+ Transceiver module
IP Option	MAC only	MAC only	MAC + SGMII (LVDS)	MAC + SGMII (SERDES)
Operating Option	RGMII	RMII	Multi-rate SGMII Ethernet	Multi-rate SGMII Ethernet
Simplified Clock Scheme	Checked	Checked	Checked	Checked

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TSE IP GUI Parameter	Example Design			
	RGMII Design	**RMII Design**	**SGMII (LVDS) Design**	**SGMII (SERDES) Design**
Host Interface	APB	APB	APB	APB
Include MIIM Module	Checked	—	—	—
Enable Half Duplex Module	Checked	Checked	Checked	Checked
Enable AXIS FIFO Functionality	Checked	Checked	Checked	Checked
Statistics Counter Registers	Unchecked	Unchecked	Unchecked	Unchecked
RX CTC Mode	—	—	Dynamic	Dynamic

6.3. RGMII Example Design

This section describes how to use the Tri-Speed Ethernet IP RGMII example design on the Avant-E Evaluation Board and CertusPro-NX Evaluation Board.

6.3.1. Overview of the RGMII Example Design and Features

Key features of the example design include:

- Tri-speed selection including 1G, 100M, and 10M speed in the *top level* file. Refer to the Importing Versa Files into a Project section.
- Traffic generator and checker to generate data for transmission and perform checking in loopback.

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6.3.2. RGMII Example Design Components

The following figure shows the block diagram of the example design. The example design features the 1G, 100M, and 10M with different PLL clock speeds. The RGMII PHY on FMC module is configured via the MDIO of TSE, through APB, mainly for operating speed configuration. TX RGMII CLK is generated from a PLL, while RX RGMII CLK is provided by PHY (FMC Module). Clock divider is used for dividing PLL output clock to achieve low-speed clock for 10M. The required clock frequency of RGMII CLKs are provided in the figure below.

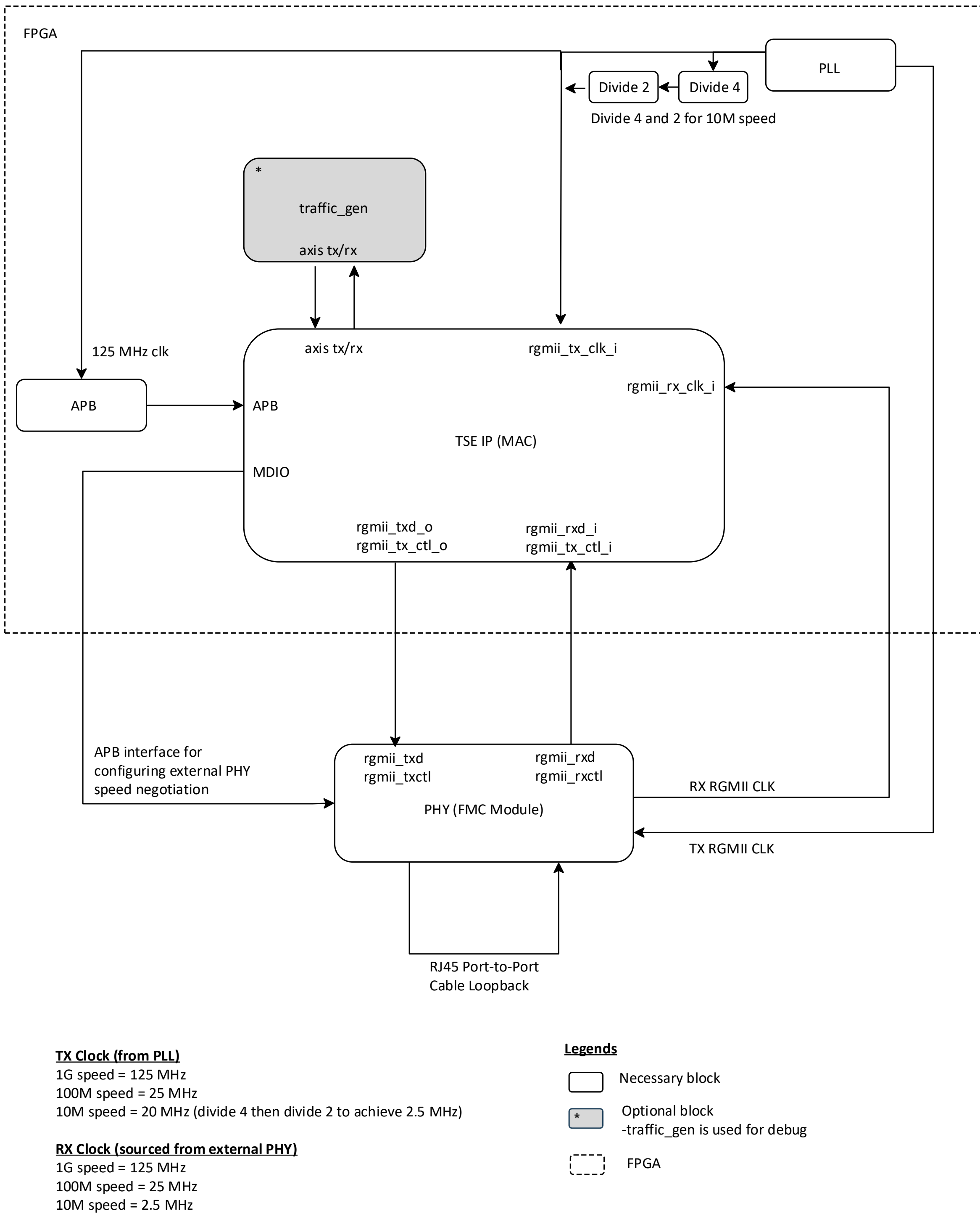

Figure 6.6. RGMII_eval_top Block Diagram for Avant-E and CertusPro-NX Devices

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The RGMII example design includes the following blocks:

- Tri-Speed Ethernet IP
- PHY (FMC Module)
- PLL
- Clock Divider
- APB
- Traffic_gen

6.3.2.1. Tri-Speed Ethernet IP

The Tri-Speed Ethernet IP core contains all the necessary logic, interfacing, and clocking infrastructure to integrate an external industry-standard Ethernet PHY with internal processor efficiently. It supports the ability to transmit and receive data between standard interfaces, such as APB, AHB-Lite or AXI4-Lite, and an Ethernet network.

6.3.2.2. PHY FMC Module

The Ethernet FPGA Mezzanine Card (FMC) is an add-on or expansion board for Avant-E Evaluation Board. The mezzanine card has 4X Marvel 88E151x Gigabit Ethernet PHYs to provide four ports of gigabit Ethernet connectivity to the carrier development board.

6.3.2.3. PLL

The phase-locked loop module is capable of frequency synthesis and clock phase management including clock injection delay cancellation. It has flexibility of input and feedback source selections, multiple output selections, and independent phase-shifting features.

6.3.2.4. Clock Divider

Clock dividers are provided to create the divided-down locks used with the gearing logic and to drive the primary clock routing to the fabric.

6.3.2.5. APB

The Advanced Peripheral Bus is the standard interface that the TSE IP core uses to interface with the host. The example design includes APB wrapper to configure MAC and external PHY registers.

6.3.2.6. Traffic Gen

The Traffic Generator block module is used to generate traffic for transmission using AXI4-Stream Transmit and Receive Interface. This module has data checker included, which performs checking on the data received against the data transmitted.

6.4. RMII Example Design

This section describes how to use the TSE IP RMII example design on the CertusPro-NX Versa Board.

6.4.1. Overview of RMII Example Design and Features

Key features of the example design include:

- Tri-speed selection including 100M, and 10M speed in the *top level* file.
- Traffic generator and checker to generate data for transmission and perform checking in loopback.

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6.4.2. RMII Example Design Components

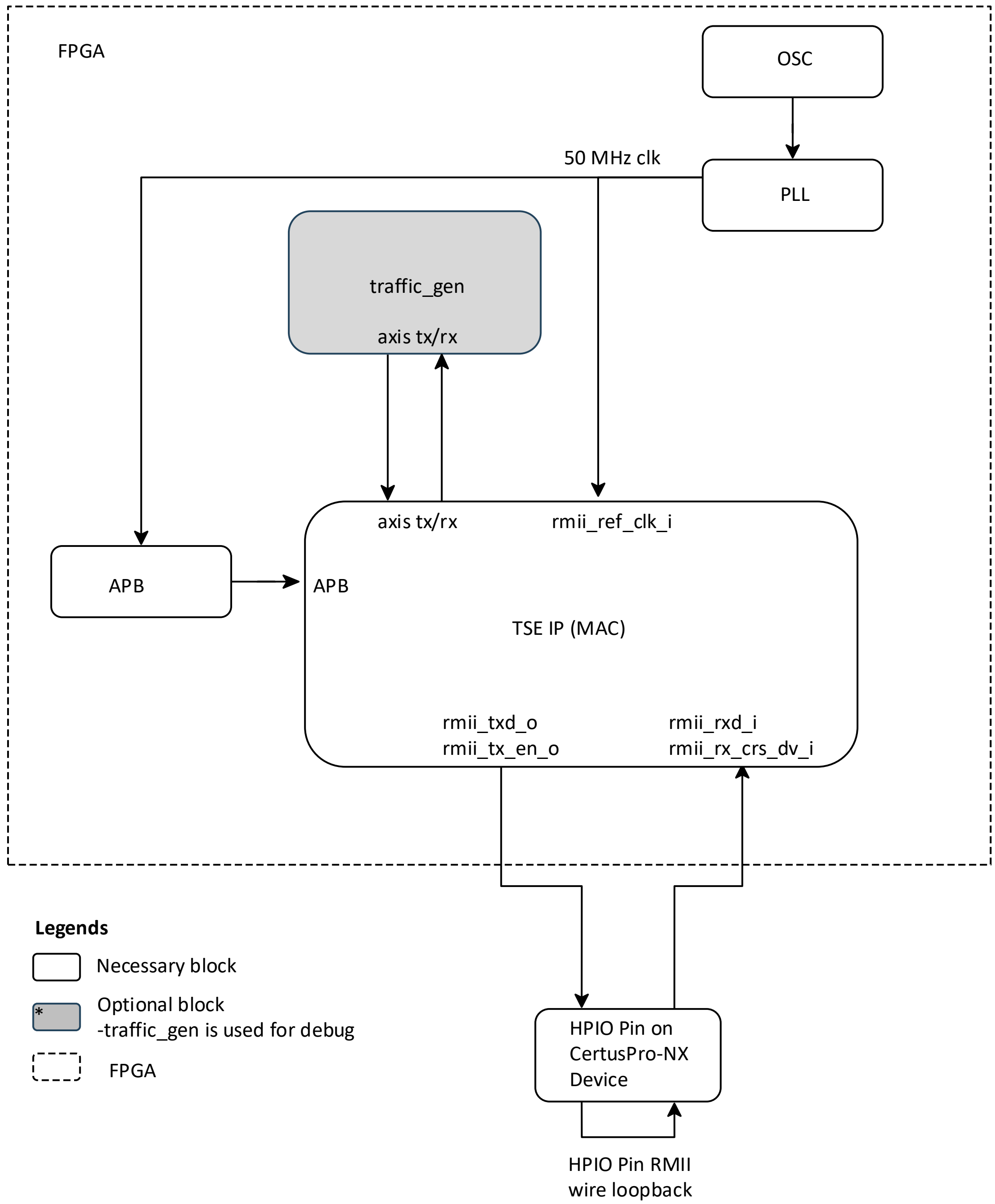

Figure 6.7. RMII Block Diagram for CertusPro-NX Devices

The RMII example design includes the following blocks:

- Tri-Speed Ethernet IP
- OSC
- PLL
- APB
- Traffic gen

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6.4.2.1. Tri-Speed Ethernet IP

The TSE IP core contains all the necessary logic, interfacing, and clocking infrastructure to integrate an external industry-standard Ethernet PHY with internal processor efficiently. It supports the ability to transmit and receive data between standard interfaces, such as APB, AHB-Lite, or AXI4-Lite, and an Ethernet network.

6.4.2.2. OSC

The oscillator module is designed to produce two clock signals that drive the FPGA clock tree.

6.4.2.3. PLL

The phase-locked loop module is capable of frequency synthesis and clock phase management including clock injection delay cancellation. It has flexibility of input and feedback source selections, multiple output selections, and independent phase-shifting features.

6.4.2.4. APB

The Advanced Peripheral Bus is the standard interface that the TSE IP core uses to interface with the host. The example design includes APB wrapper to configure MAC registers.

6.4.2.5. Traffic gen

The Traffic Generator block module is used to generate traffic for transmission using AXI4-Stream Transmit and Receive interface. This module includes a data checker that checks the data received against the data transmitted.

6.5. SGMII Example Design

This section describes how to use the TSE IP SGMII example design on the following boards:

- SGMII (LVDS) for Avant-X Versa Board
- SGMII (SERDES) for CertusPro-NX Versa Board

6.5.1. Overview of SGMII Example Design and Features

Key features of the example design include:

- Tri-speed selection including 1G, 100M, and 10M speed using a DIP switch.
- Traffic generator and checker to generate data for transmission and perform checking in loopback.

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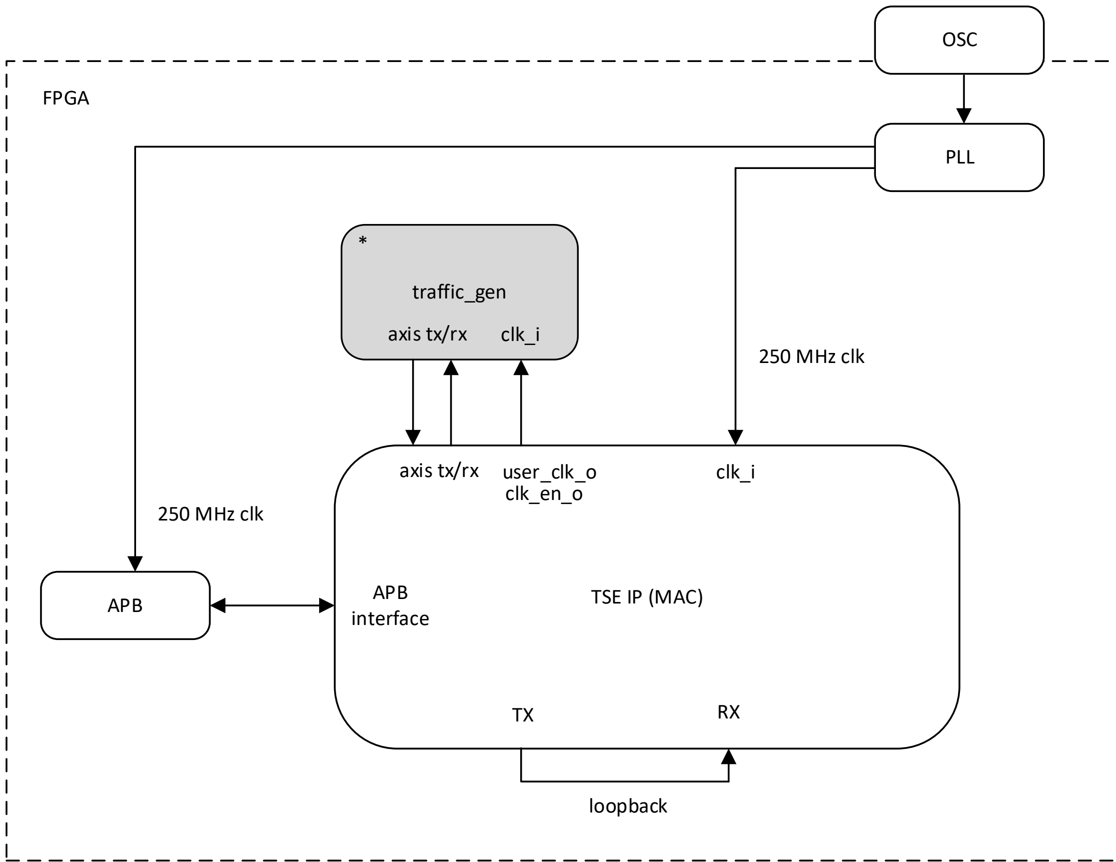
6.5.2. SGMII LVDS and SERDES Example Design Components



PLL
250 MHz clock to TSE MAC clk_i
To configure low-speed TSE, leverage clk_en_o and user_clk_o from TSE MAC to application to scale the clock

Legends

Necessary block

Optional block
-traffic_gen is used for debug

FPGA

Figure 6.8. SGMII LVDS Example Design Block Diagram for Avant-X Devices

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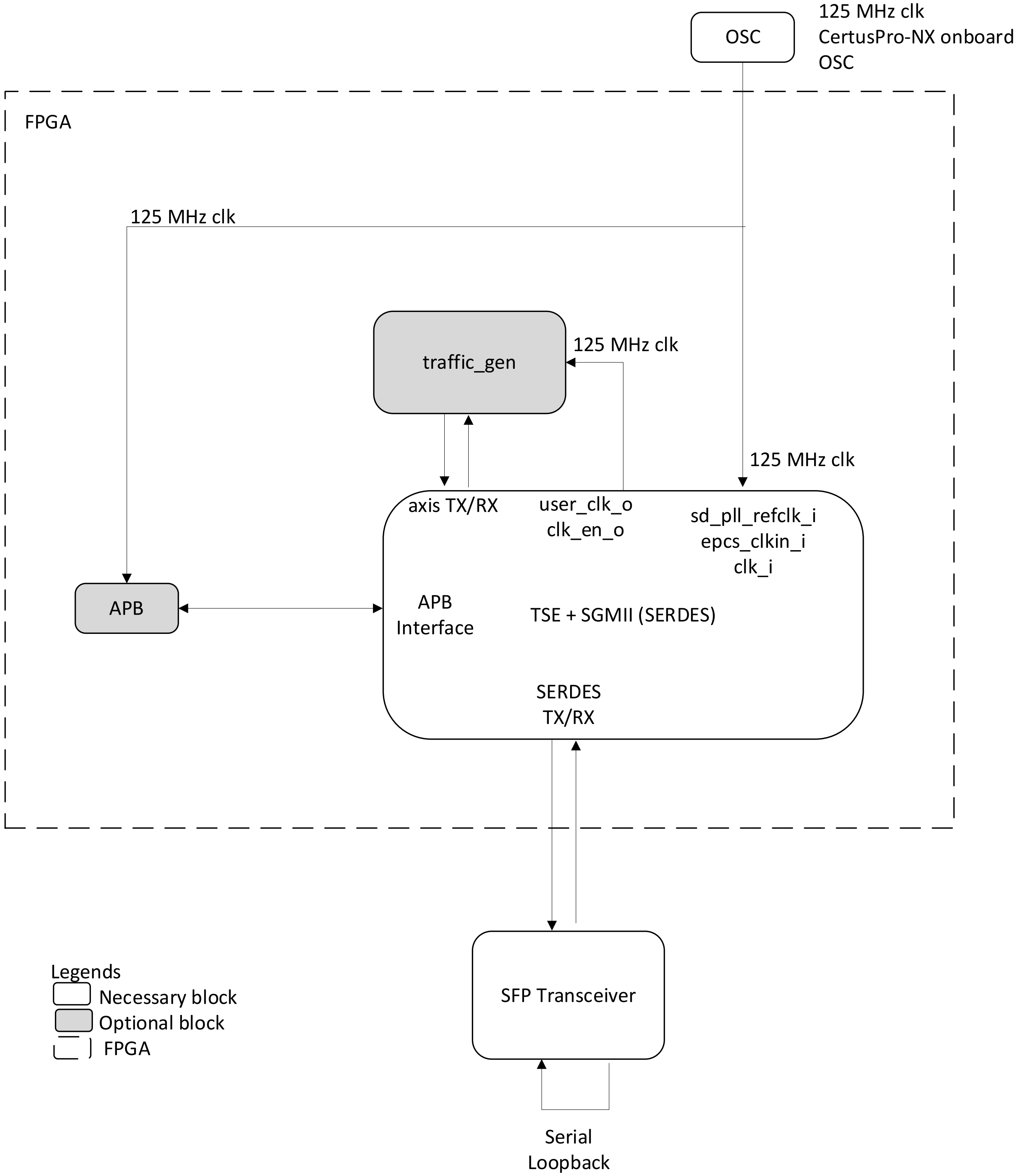

Figure 6.9. SGMII SERDES Example Design Block Diagram for CertusPro-NX Devices

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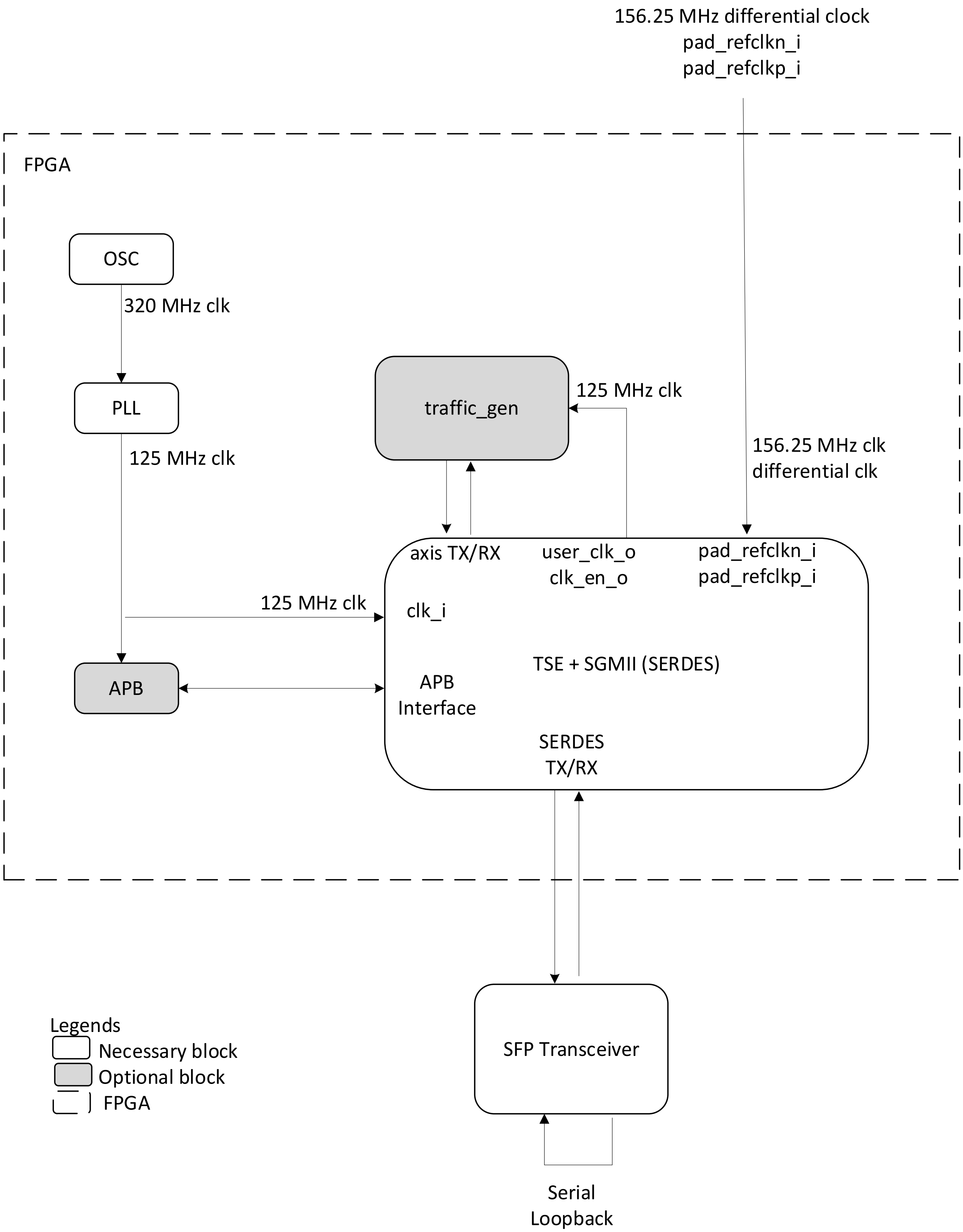

Figure 6.10. SGMII SERDES Example Design Block Diagram for Avant-X Devices

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The SGMII LVDS and SERDES example design includes the following blocks:

- Tri-Speed Ethernet IP
- OSC
- PLL
- APB
- Traffic gen

6.5.2.1. Tri-Speed Ethernet IP

The Tri-Speed Ethernet IP core contains all the necessary logic, interfacing, and clocking infrastructure to integrate an external industry-standard Ethernet PHY with internal processor efficiently. It supports the ability to transmit and receive data between standard interfaces, such as APB, AHB-Lite or AXI4-Lite, and an Ethernet network.

6.5.2.2. OSC

Oscillator module, designed to produce two clock signals that drive the FPGA clock tree.

6.5.2.3. PLL

The phase-locked loop module is capable of frequency synthesis and clock phase management including clock injection delay cancellation. It has flexibility of input and feedback source selections, multiple output selections, and independent phase-shifting features.

6.5.2.4. APB

The Advanced Peripheral Bus is the standard interface that the TSE IP core uses to interface with the host. The example design includes APB wrapper to configure MAC registers.

6.5.2.5. Traffic gen

The Traffic Generator block module is used to generate traffic for transmission using AXI4-Stream Transmit and Receive Interface. This module has data checker included, which performs checking on the data received against the data transmitted.

6.6. Using Hardware Example Design

This section provides information on how to generate an example design for the supported devices. Supported hardware example designs include the following devices:

- Avant SGMII (LVDS)
- Avant SGMII (SERDES)
- Avant RGMII
- CertusPro-NX RGMII
- CertusPro-NX RMII
- CertusPro-NX SGMII (SERDES)

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6.6.1. Creating a New Radiant Project

To create a new project, follow these steps:

1. In the Lattice Radiant software, go to **File -> New -> Project**… or click on the **New Project** icon.

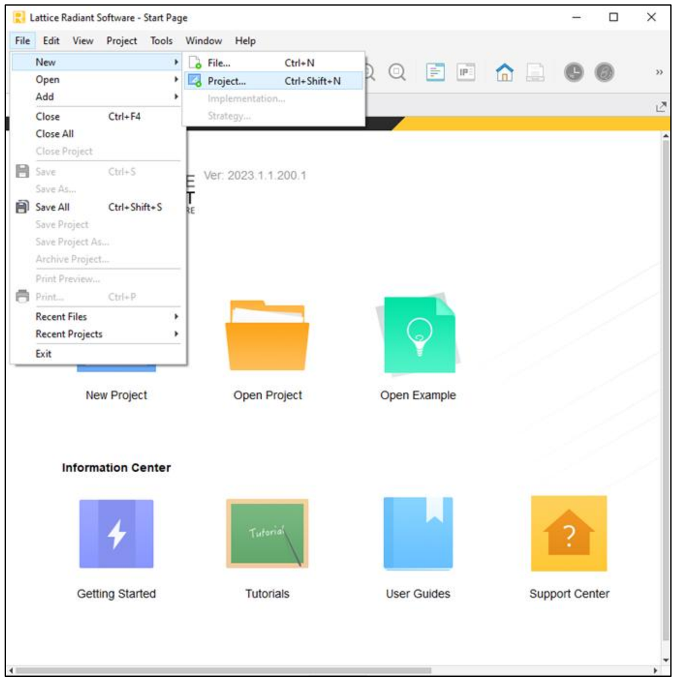

Figure 6.11. Project Creation

2. Specify **Project Name**, **Location**, **Implementation Name**, and click **Next**.

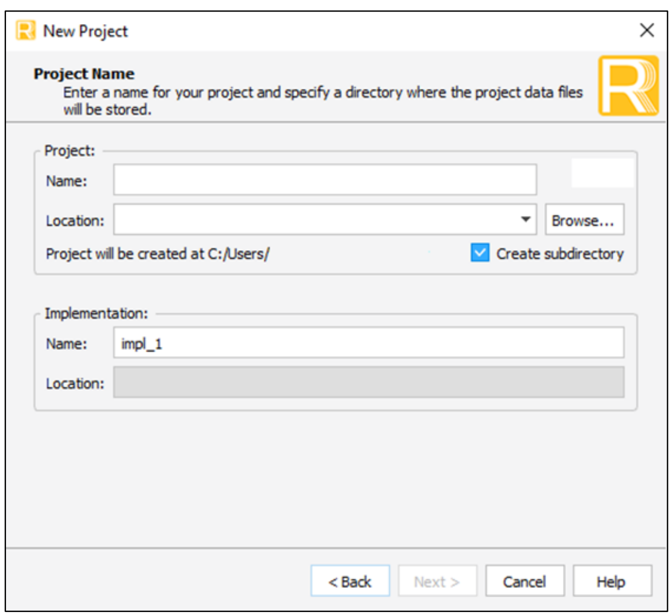

Figure 6.12. Project Name and Location

3. Specify a device for the project by selecting a device family, an operating condition, the package, performance grade, and part number.

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4. Select the device according to the supported hardware example design that corresponds to the actual development kit.
   - LAV-AT Avant-X70-3LFG1156I or Avant-G70-3LFG1156I: SGMII (LVDS), SGMII (SERDES)
   - LAV-AT Avant-E70ES1-3LFG1156I: RGMII
   - LFCPNX-100-9LFG672I: RGMII, RMII, SGMII (SERDES)

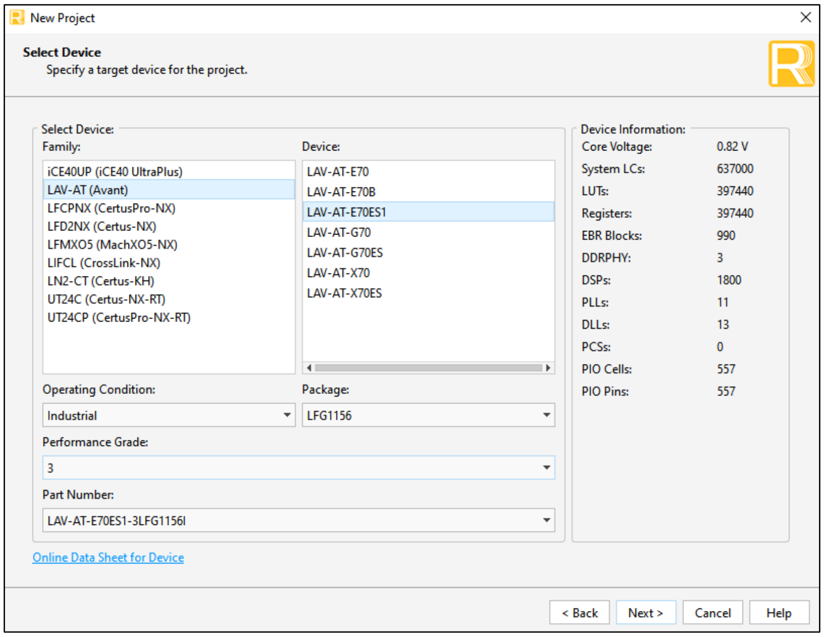

Figure 6.13. Project Device

5. Select a synthesis tool for the project. It is recommended to select Synplify Pro.

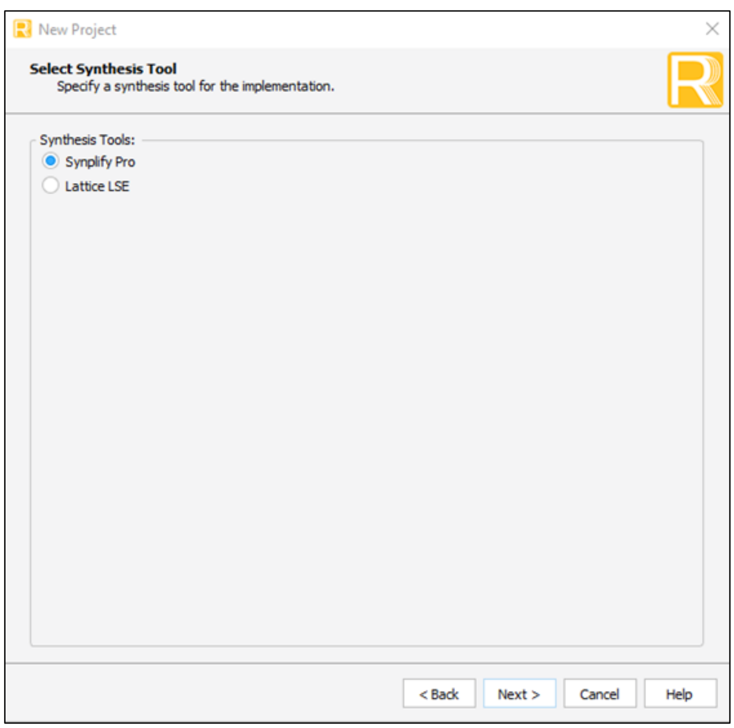

Figure 6.14. Project Synthesis Tool

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6. View and verify the project information for the project creation.

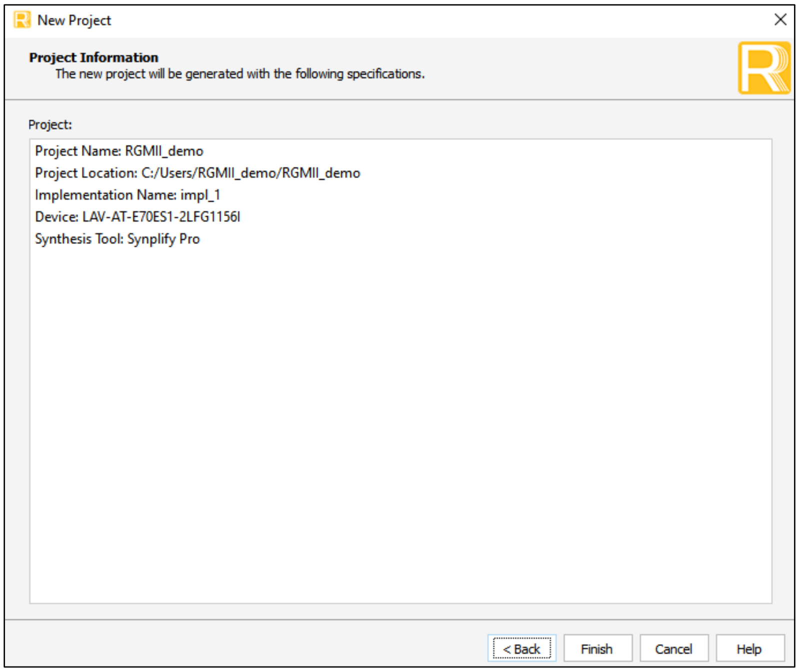

Figure 6.15. Project Information

6.6.2. IP Installation and Generation

To install and generate the IP, follow these steps:

1. Go to **IP Catalog -> IP on Server**, and download **Tri-Speed Ethernet**.
2. After you download and install the IP from the server, go to **IP on Local -> Generate…** to launch the IP generation wizard.

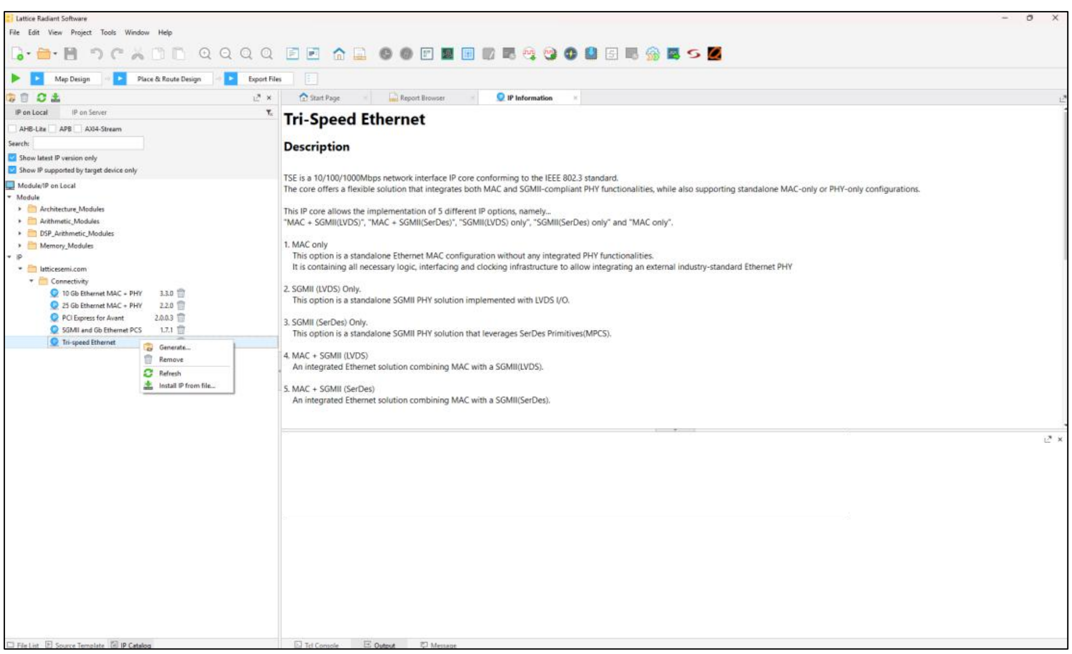

Figure 6.16. Project Information

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3. Enter the Component Name and project directory for IP generation, and click **Next.**

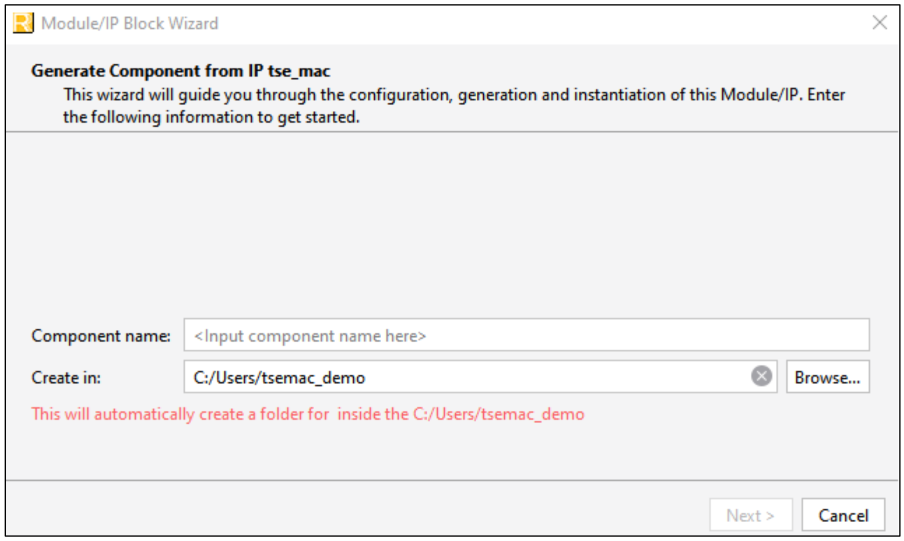

Figure 6.17. IP Component

4. Configure the IP interface, and click **Generate**.

   For RGMII hardware example design, set the following parameters:

   - Select IP Option: **MAC only**
   - Host interface: **APB**
   - Select MAC Operating option: **RGMII**
   - Include MIIM Module: **Unchecked**
   - Statistics Counter Registers: **Unchecked**
   - Enable FPGA delay for TX: **Unchecked**
   - Enable FPGA delay for RX: **Unchecked**

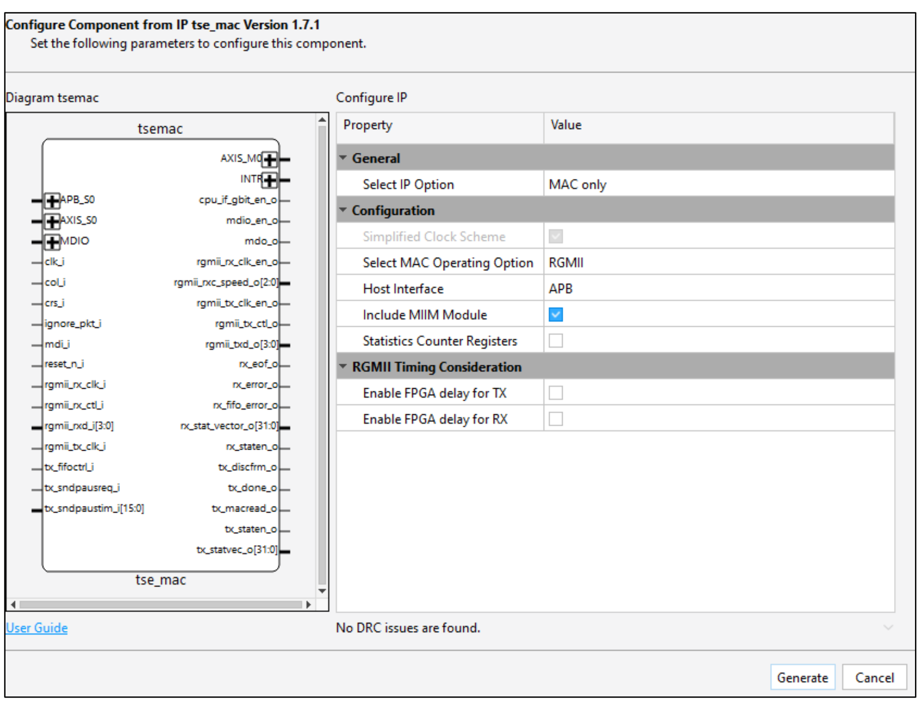

Figure 6.18. IP Component Configuration – RGMII Example Design for Avant and CertusPro-NX Devices

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MIIM module is required for RGMII hardware example. For RGMII timing considerations, refer to the external PHY configuration. Typically only one side delay is required, either from the FPGA or external PHY. Typically PHY performs delay.

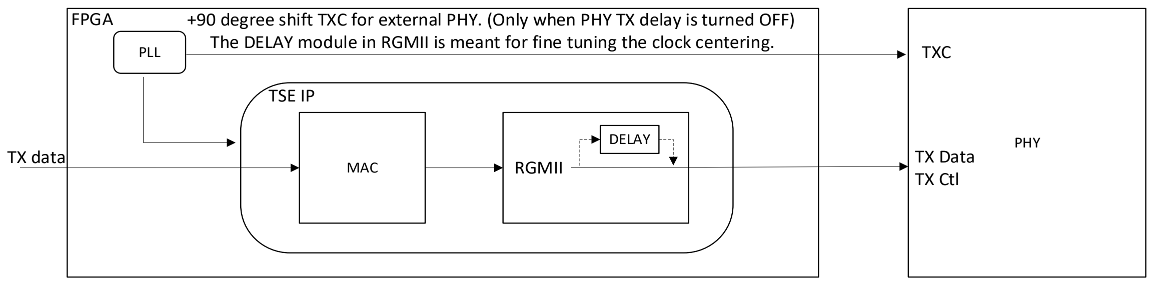

Figure 6.19. TX Path Delay for RGMII

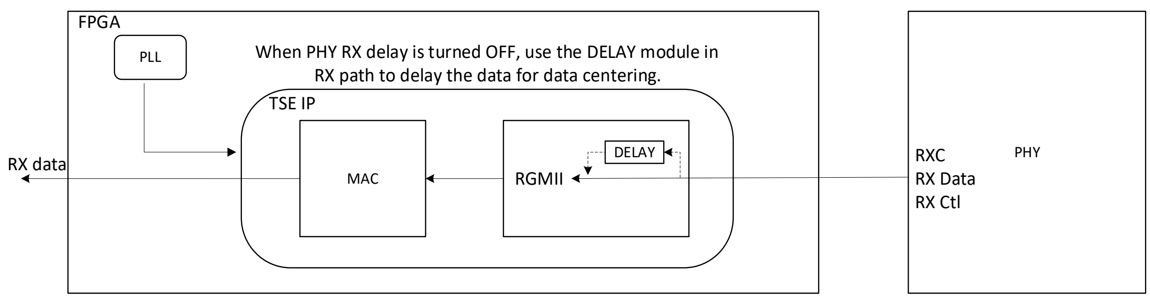

Figure 6.20. RX Path Delay for RGMII

For timing tuning in FPGA, refer to either the Lattice Avant High-Speed I/O and External Memory Interface User Guide (FPGA-TN-02300) or the CertusPro-NX High-Speed I/O Interface (FPGA-TN-02244), depending on the selected device family.

For SGMII (LVDS) hardware example design on Avant-X Versa board, set the following parameters:

- Select IP Option: **MAC + SGMII (LVDS)**
- Select MAC + SGMII Operating Option: **Multi-rate SGMII Ethernet**
- Host Interface: **APB**
- Statistics Counter Registers: **Unchecked**
- RX CTC Mode: **Dynamic**

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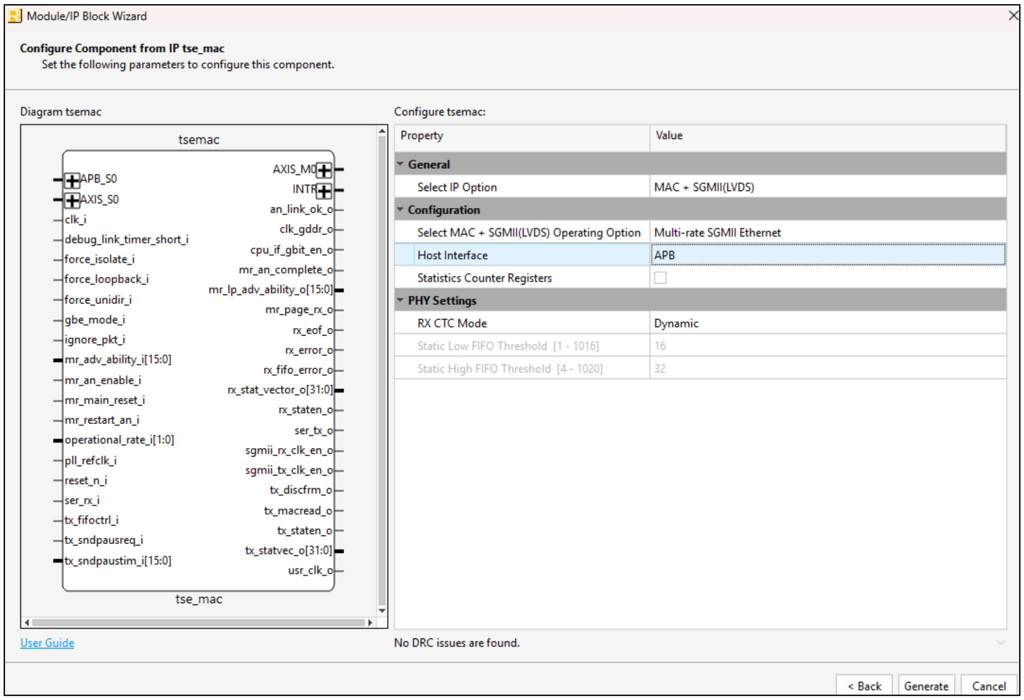

Figure 6.21. IP Component Configuration – SGMII LVDS Example Design for CertusPro-NX Devices

For SGMII (SERDES) hardware example design on Avant-X Versa board, set the following parameters:

- Select IP Option: **MAC + SGMII (SERDES)**
- Host Interface: **APB**
- Statistics Counter Registers: **Unchecked**
- RX CTC Mode: **Dynamic**
- Select MPPHY lane or channel: **Auto**
- Loopback Mode: **Disable**
- RX Coupling Mode: **AC Coupling**
- RX Loss of Sig port Enable: **Unchecked**

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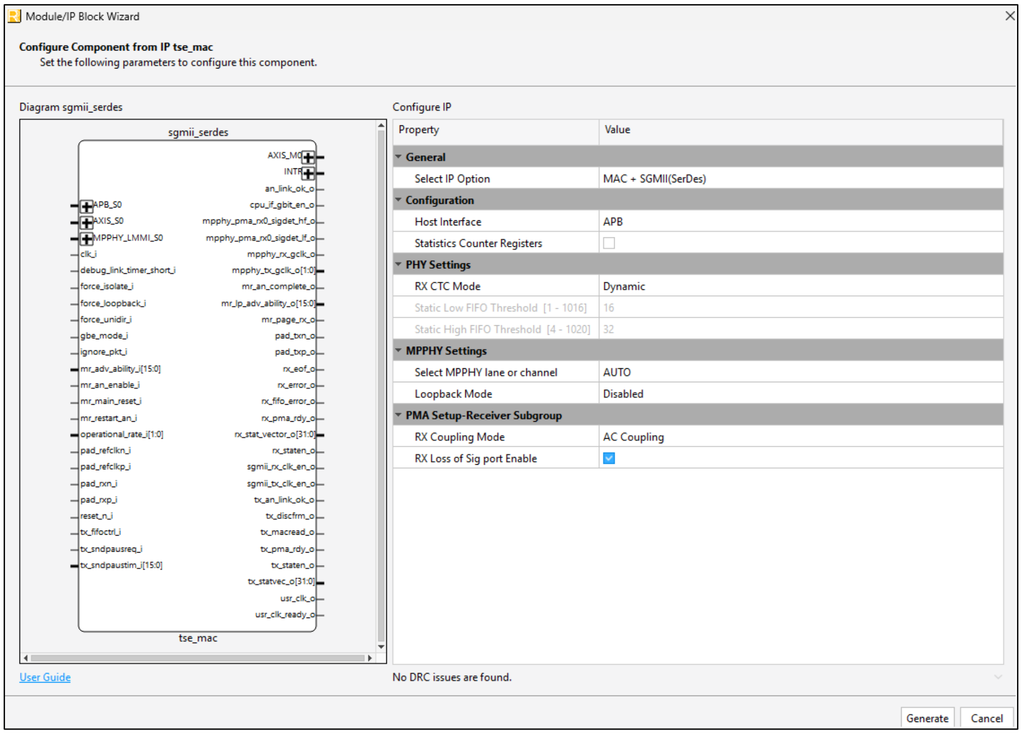

Figure 6.22. IP Component Configuration – SGMII SERDES Example Design for Avant Devices

For SGMII (SERDES) hardware example design on the CertusPro-NX Versa board, set the following parameters:

- Select IP Option: **MAC + SGMII (SERDES)**
- Host Interface: **APB**
- Statistics Counter Registers: **Unchecked**
- RX CTC Mode: **Dynamic**
- Select MPCS lane or channel: **6**
- MPCS PMA loopback: **Unchecked**

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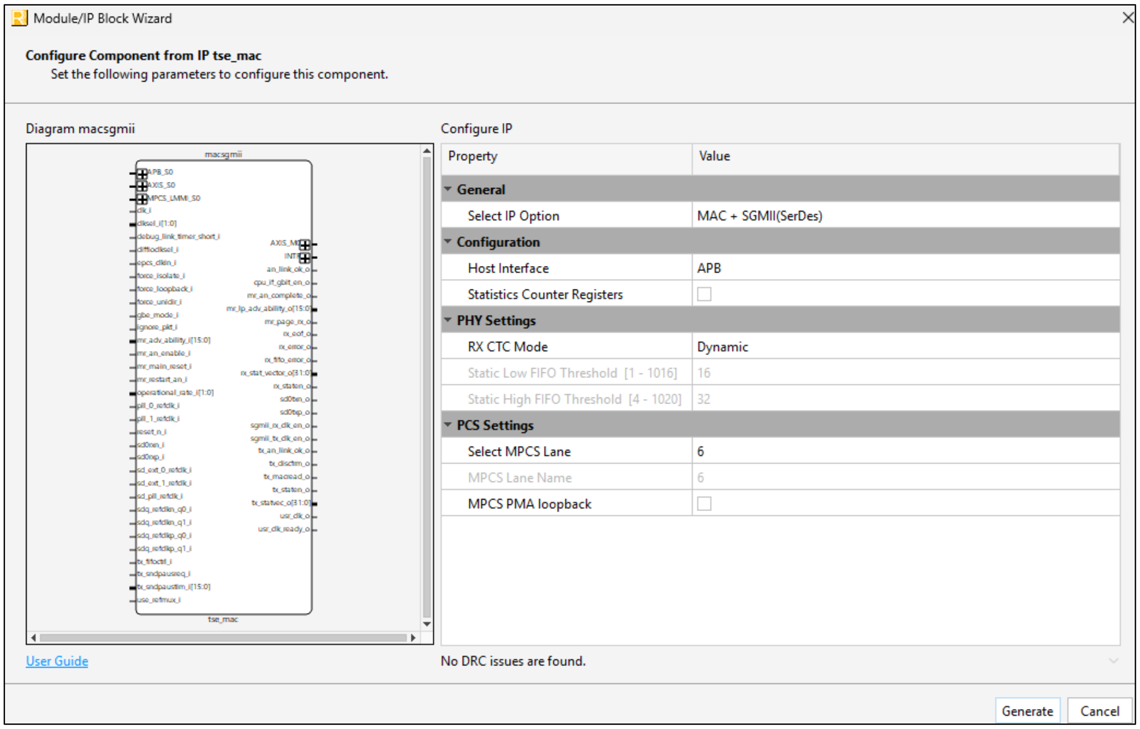

Figure 6.23. IP Component Configuration – SGMII SERDES Example Design for CertusPro-NX Devices

For RMII interfaces, set the following parameters:

- Select IP Option: **MAC only**
- Select MAC Operating Option: **RMII**
- Host Interface: **APB**

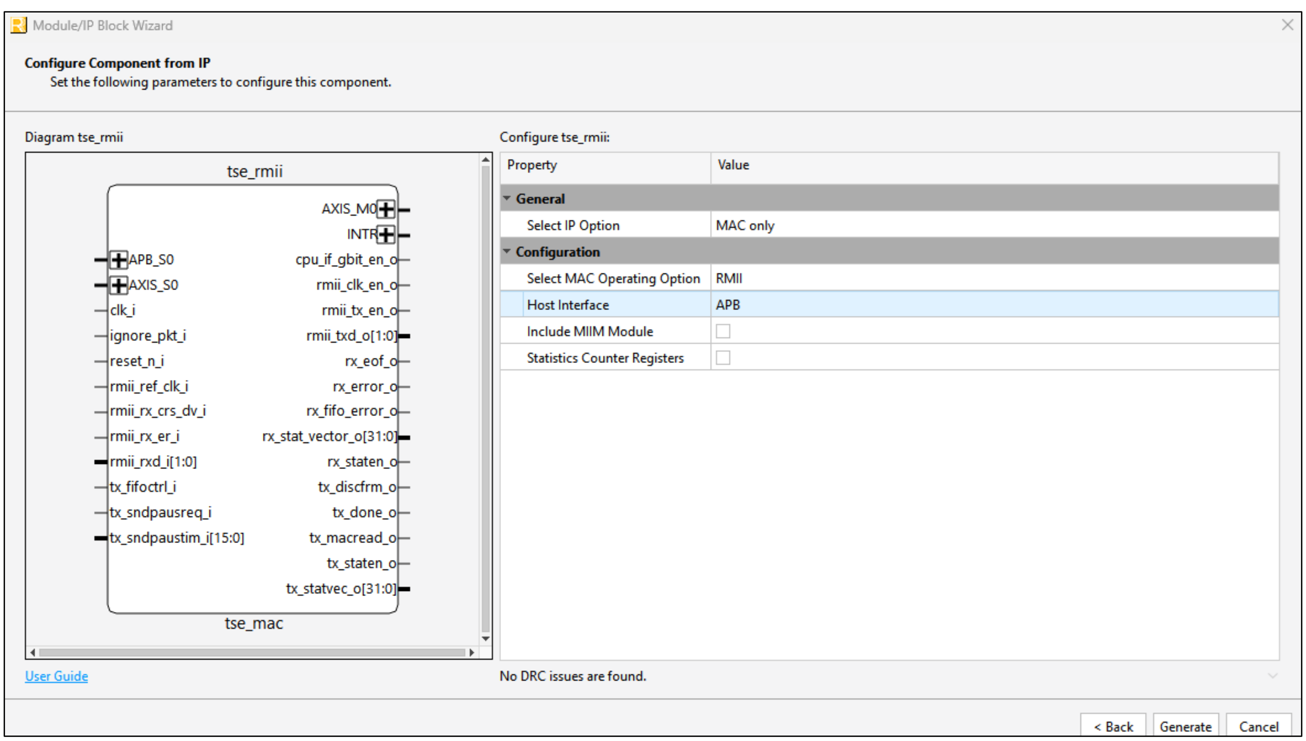

Figure 6.24. IP Components Configuration – RMII Example Design for CertusPro-NX Devices

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5. Verify the generated IP, and click **Finish**.

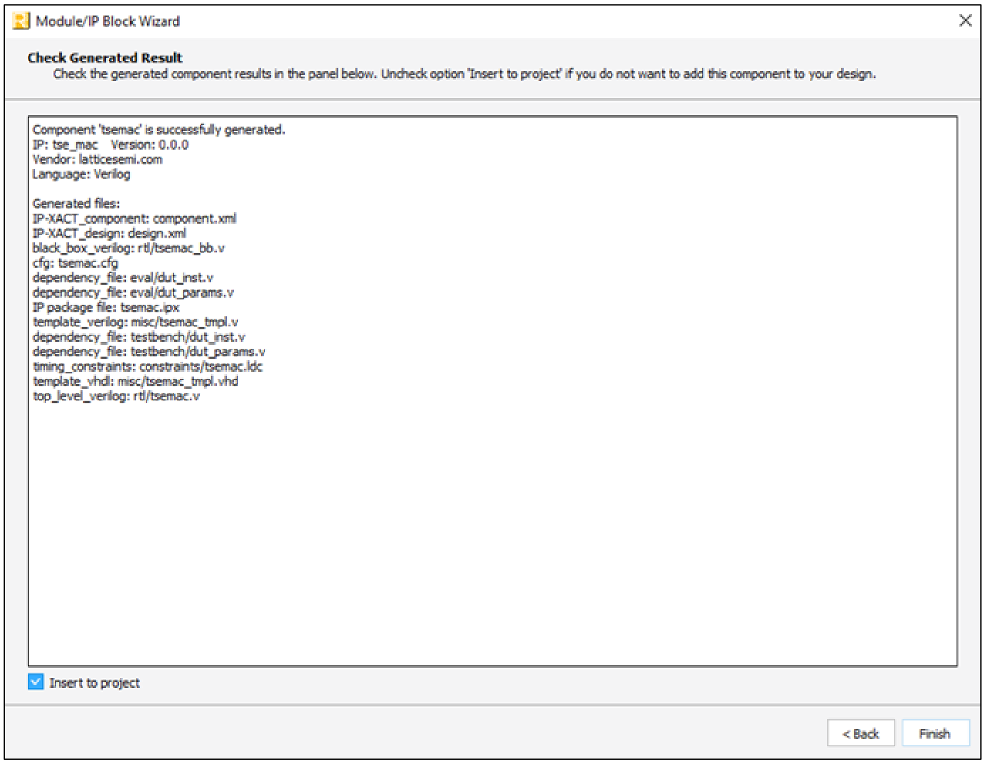

Figure 6.25. IP Generation Result

6.6.3. Importing Versa Files into a Project

To add an existing example design into a project, follow these steps:

1. Go to **Add->Existing File…** and select an existing example design using the Radiant software graphical user interface. Import the top-level file, tb_top (for simulation use) and the *.pdc* file from the *<IP_INSTANCE_NAME>\eval\versa_top\<DEVICE>_<INTERFACE> folder.*

   Alternately, you may set up the example design using TCL scripts by entering the command mentioned for each different device and IP. Replace *<IP_INSTANCE_NAME>* with actual IP instance name created.

   TCL script is an alternate way to set up the example design files, including setting simulation and post-synthesis file. If TCL script is used, you do not have to perform add files using the graphical user interface.

   For Avant X70 SGMII (**LVDS**):

   Top-level file to include in project: *sgmii_avant_x_versa_top.v*

   Simulation for top-level file to include: *tb_sgmii_avant_x_versa_top.v*
   (From the Radiant software, set this file to be included for simulation only)

   Post-synthesis constraint file: *sgmii_avant_x_versa.pdc*

   TCL command: *source {<IP_INSTANCE_NAME>\eval\versa_top\avant_x70_sgmii_lvds\ed_setup.tcl}*

   For Avant X70 SGMII (**SERDES**):

   Top-level file to include in project: *sgmii_top.v*

   Simulation for top-level file to include: *tb_sgmii_top.v*
   (From the Radiant software, set this file to be included for simulation only)

   Post-synthesis constraint file: *sgmii_avant_x_versa.pdc*

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TCL command: *source {<IP_INSTANCE_NAME>\eval\versa_top\avant_x70_sgmii_serdes\ed_setup.tcl}*

For Avant E70 RGMII

Top-level file to include in project: *rgmii_top.v*

Simulation for top-level file to include: *tb_rgmii_top.v*
(From the Radiant software, set this file to be included for simulation only)

Post-synthesis constraint file: *avant_rgmii.pdc*

TCL command: *source {<IP_INSTANCE_NAME>\eval\versa_top\avant_e70_eval_rgmii\ed_setup.tcl}*

For CertusPro-NX RGMII

Top-level file to include in project: *rgmii_top.v*

Simulation for top-level file to include: *tb_rgmii_top.v*
(From the Radiant software, set this file to be included for simulation only)

Post-synthesis constraint file: *cpnx_rgmii.pdc*

TCL command: *source {<IP_INSTANCE_NAME>\eval\versa_top\lfcpnx_eval_rgmii\ed_setup.tcl}*

For CertusPro-NX RMII

Top-level file to include in project: *rmii_top.v*

Simulation for top-level file to include: *tb_rmii_top.v*

(From the Radiant software, set this file to be included for simulation only)

Post-synthesis constraint file: *cpnx_rmii.pdc*

TCL command: *source {<IP_INSTANCE_NAME>\eval\versa_top\lfcpnx_versa_rmii\ed_setup.tcl}*

For CertusPro-NX SGMII (SERDES)

Top-level file to include in project: *sgmii_top.v*

Simulation for top-level file to include: *tb_sgmii_top.v*
(From the Radiant software, set this file to be included for simulation only)

Post-synthesis constraint file: *cpnx_sgmii.pdc*

TCL command: *source {<IP_INSTANCE_NAME>\eval\versa_top\lfcpnx_versa_sgmii\ed_setup.tcl}*

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The figure below shows how to add files using the Radiant software graphical user interface.

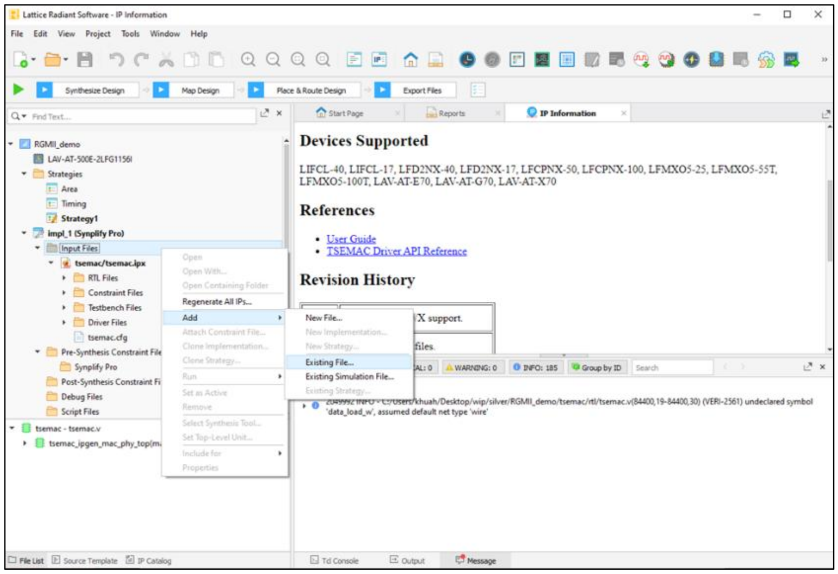

Figure 6.26. Add an Existing File Using Graphical Interface

The figure below shows an example on how to run TCL using the TCL Console in the Radiant software bottom panel with *<IP_INSTANCE_NAME>* of *tse2rgmii.*

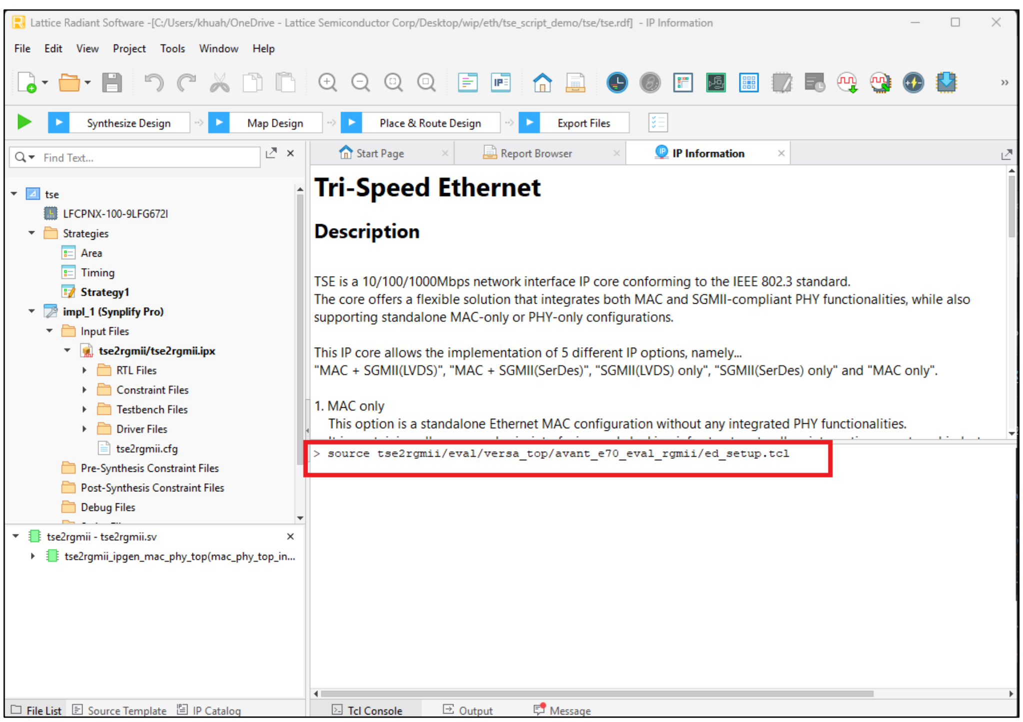

Figure 6.27. Set Up Example Design Using TCL

The following figure shows the localparam that you may change to configure the speed for RGMII. By default, the speed is set at 1G mode. However, you can choose to operate at lower speeds by changing the speed to 10M or 100M mode. However, for RMII interface, the default speed is 100M. Recompilation is required for each selected speed operation, and on-the-fly changes are not allowed.

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This is not applicable for SGMII hardware example design For SGMII (SERDES) and SGMII (LVDS) hardware example design, you may toggle speed change using on board DIP SW. For more details, refer to the Hardware Setup for Avant-X Versa Board with SGMII LVDS Hardware Example Design section and the Hardware Setup for CertusPro-NX with SGMII SERDES Hardware Example Design section.

```
localparam SPEED_MODE = "1G"; //RGMII speed mode: "10M"; "100M"; "1G"
localparam CLK_ALGN = "1";
//clock alignment for data sampling
//"0"= MAC's TX & MAC's RX delay
//"1"= PHY's TX & PHY's RX delay [recommended]
//"2"= MAC's TX & PHY's RX delay
//"3"= PHY's TX & MAC's RX delay
// For MAC's TX delay, this example design will perform PLL phase shift 90degree for TXC.
// The delay performed in IP is meant for fine tuning the delay for signal integrity.
// FPGA Delay setting in IPGUI, for 191 steps can be translated into about 1.91ns (observe from simmulation), which is equalvalent to 90 degree shift.
// User may use this config to further fine tune the signal.
```

Figure 6.28. Speed and Clock Alignment Param in rgmii_avant_e versa_top

2. Update Strategy, Place & Route Design, Command Line Options with *-exp WARNING_ON_PCLKPLC1=1* for external clock routing using RGMII external PHY. This command resolves the error that might occur during Place & Route Design for external clocks.

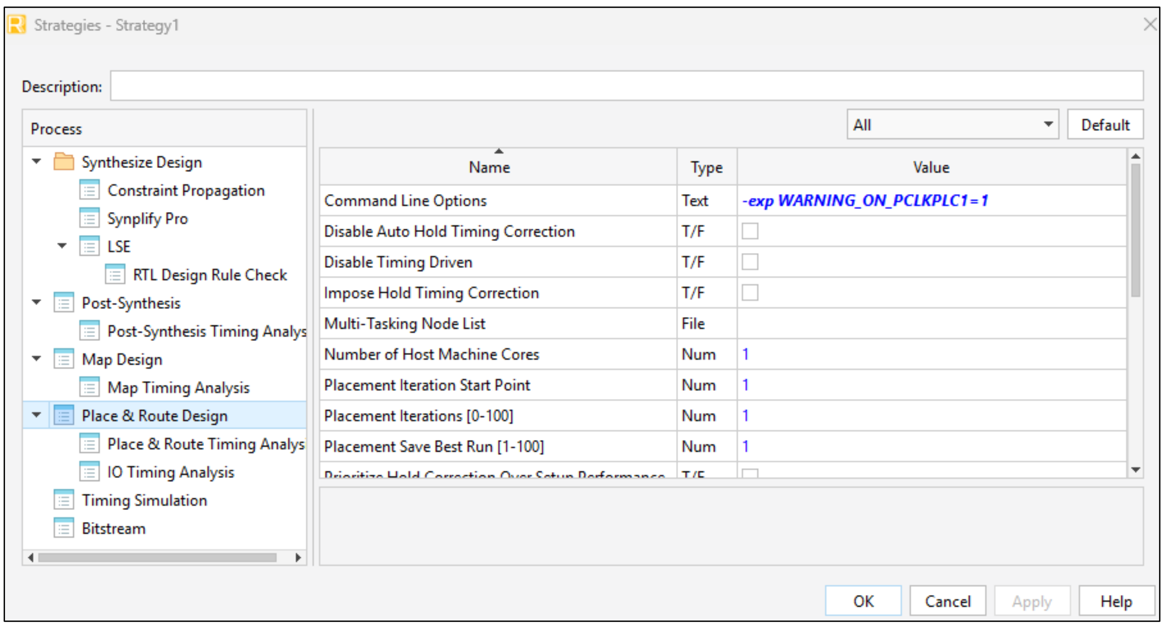

Figure 6.29. Strategy Interface for Command Line Options in Place & Route Design

3. To compile low-speed only RGMII (100M or 10M), update the *.pdc* file by adding false path of low-speed clock to high-speed clock. To compile multiple-speed RGMII on the same device, set clock group accordingly.

```
#FOR 100M and 10M use ONLY, to set false path to 1Gbps clock
#set_false_path -from [get_clocks pllclk_125]
#set_false_path -to [get_clocks pllclk_125 ]
```

Figure 6.30. Set False Path Constraints in the .pdc file for Low-Speed RGMII

4. Click **Run All** to compile the bitstream file from design. Do not include any tb_* files for synthesis.

   For timing considerations and post-synthesis constraints, refer to the Timing Constraints section.

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5. Click **Run All** to compile the bitstream file from design. Do not include any tb_* files for synthesis.

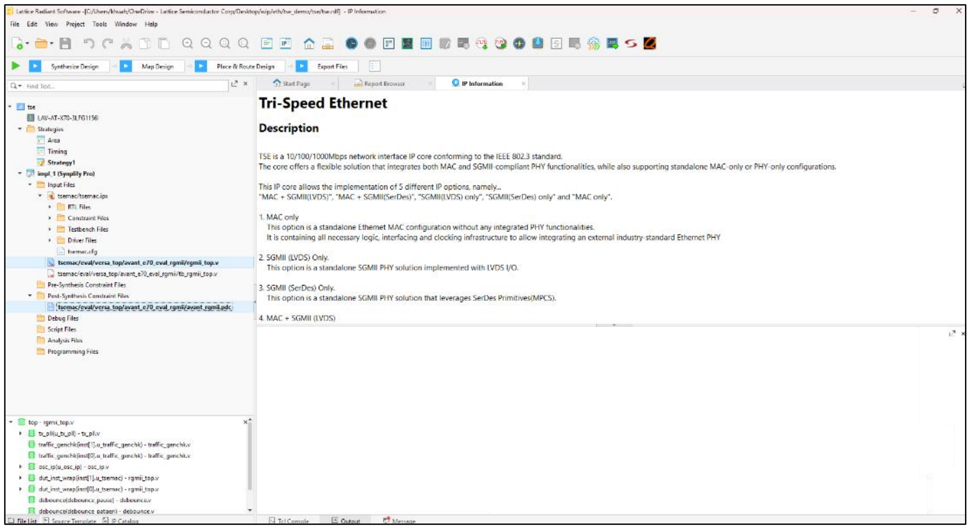

Figure 6.31. Generate Bitstream

6. After the bitstream is compiled successfully, the run button turns green with a checked sign.

Figure 6.32. Bitstream Completion

6.6.4. Program Bitstream

To program the bitstream, follow these steps:

1. Go to **Tools -> Programmer** to launch the Radiant Programmer.

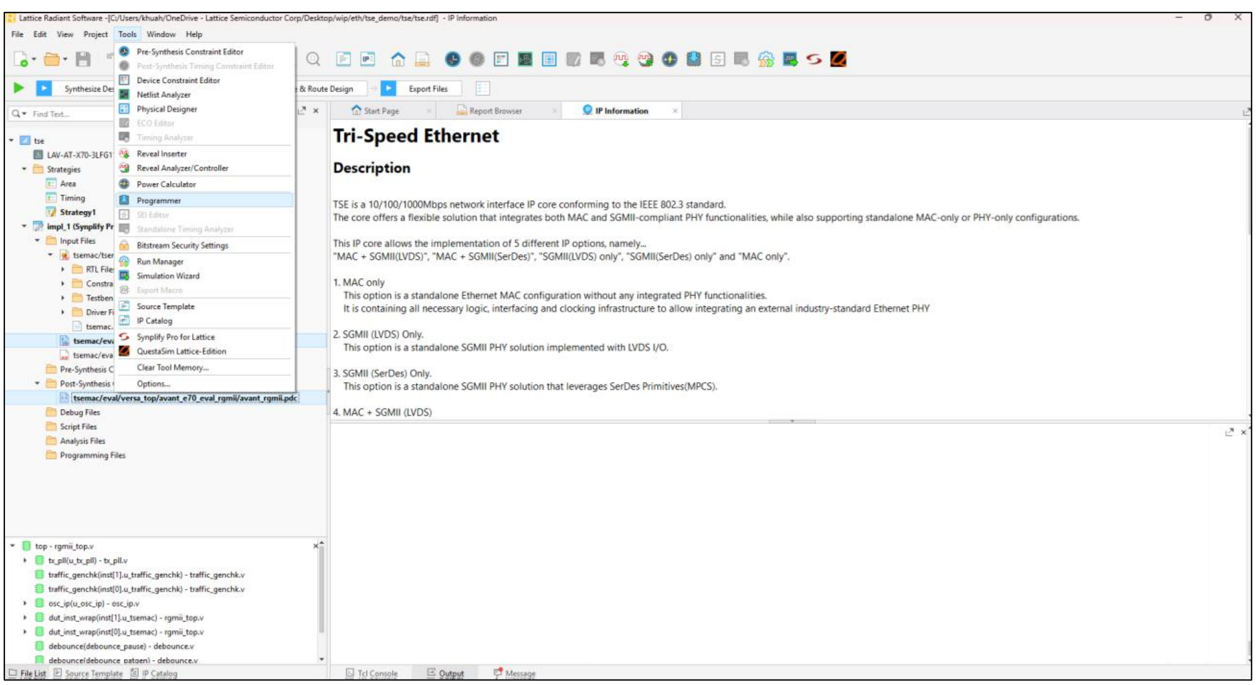

Figure 6.33. Programmer

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For more information on the Radiant Programmer, refer to the *Programming* section of the Avant Evaluation Board User Guide (FPGA-EB-02057), Avant-G/X Versa Board User Guide (FPGA-EB-02063), or CertusPro-NX Versa Board User Guide (FPGA-EB-02053) .

2. Verify the settings under **Cable Setup**, the device family detected from the programmer, and the correct bitstream is selected in the **File Name** column. You may click on the **Detect Cable** button and select **Tools/Scan Device** from the menu bar to automatically detect connected devices.

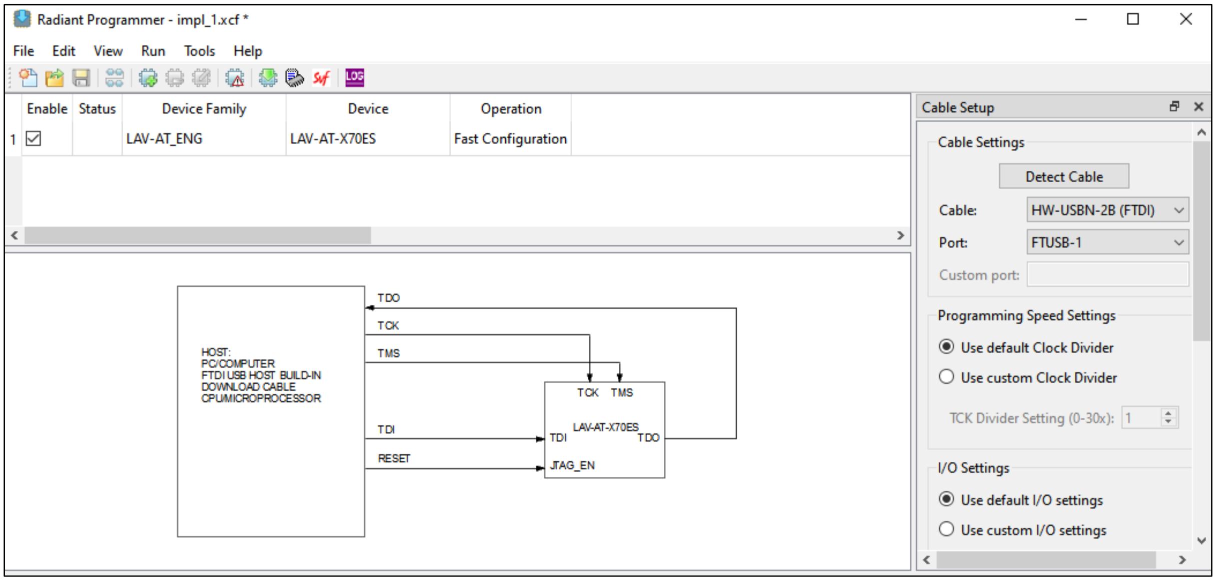

Figure 6.34. Select Bitstream

3. Select **Run -> Program Device** to program bitstream into the target device.

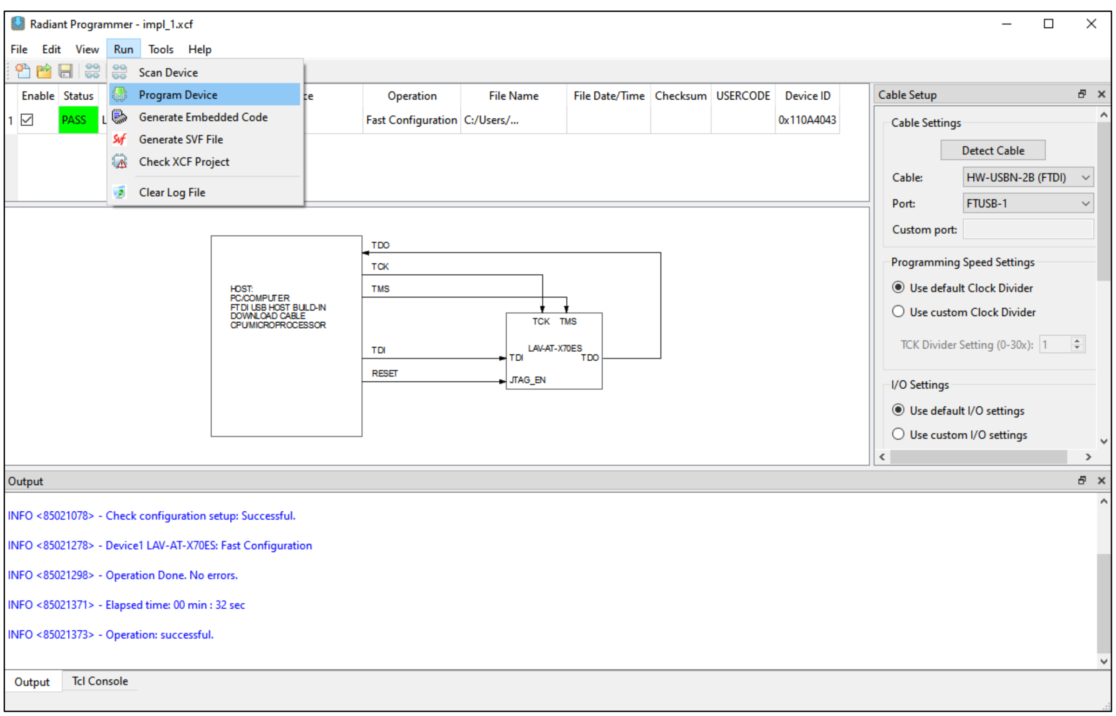

Figure 6.35. Programming Bitstream

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6.6.5. Hardware Setup for Evaluation Board with RGMII Hardware Example Design

Figure 6.36 shows the complete hardware setup for an example design. Refer to the corresponding board user guide for the names of mechanical input signals, including DIP switches and pushbuttons:

- Avant E70 Evaluation Board
- CertusPro-NX Evaluation Board

The evaluation board is powered up with 12 V power supply. The Ethernet FMC is connected to the board FMC connector with an Ethernet cable in loopback between PORT0 and PORT1.

6.6.5.1. DIP Switch Definition

After programing the bitstream into the device, make sure the DIP switch is configured to the right position before triggering the RESET via a pushbutton.
The following lists the DIP switch definitions:

- Avant E70 Evaluation Board:
  DIP_SW1: Start transmission
- CertusPro-NX Evaluation Board:
  DIP_SW1: Start transmission

For more details on DIP switch configuration modes, refer to the following table.

Table 6.2. DIP Switch Configuration Modes—Pre Reset Traffic Generation Trigger

Device	DIP_SW1 / SWITCH0 (Default state before RESET)
Avant E70 Evaluation Board	LOW
CertusPro NX Evaluation Board	LOW

After the link up is successful, toggle DIP_SW1 or SWITCH0 from LOW to HIGH to start the traffic generator, which checks the IP performance. For details on which LED to target and the device status, refer to the following LED indicator table.

Note: Speed configuration is done beforehand during compilation for the RGMII example design. For details, refer to the Importing Versa Files into a Project section.

6.6.5.2. Pushbutton Definition

The following lists the pushbutton definitions for Avant E70 Evaluation Board and CertusPro-NX Evaluation Board:

- SW1: Reset
- SW5: Pause or resume data transmission

6.6.5.3. LED Definition

Each LED indicates the status of Tri-Speed Ethernet. Refer to the table below for details on each LED update, and refer to the device user guide for signal naming conventions.

LED_10 and LED_11 must be ON when TX and RX are actively transmitting (for CONTINUOUS_TRAFFIC enabled mode). LED_10 and LED_11 must be OFF when transmission is paused or completed (for CONTINUOUS_TRAFFIC disabled mode), then LED_12 must be ON.

The following lists the failing scenario:

- LED_8 or LED_9 is OFF after RESET.
- LED_14 and LED_15 are both OFF.
- LED_10 or LED_11 is OFF during transmission (for CONTINUOUS_TRAFFIC enabled mode).
- LED_13 is ON.

Table 6.3. LED Indicator Status

Avant E70 (Red)	CertusPro-NX Eval (Yellow)	Description
D22 / LED_8	D14 / LED_8	PLL locked.
D23 / LED_9	D15 / LED_9	MDIO configuration completed.

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Avant E70 (Red)	CertusPro-NX Eval (Yellow)	Description
D24 / LED_10	D16 / LED_10	TX channel is transmitting.
D25 / LED_11	D17 / LED_11	RX channel is receiving.
D26 / LED_12	D18 / LED_12	PASS traffic generator check.
D27 / LED_13	D19 / LED_13	FAIL traffic generator check.
D28 / LED_14	D20 / LED_14	Link up to 100M or 10M speed.
D29 / LED_15	D21 / LED_15	Link up to 1G speed.

The USB-Mini B is connected to the host for the Reveal tool to check the signal from the hardware, including TX, RX, and data comparison.

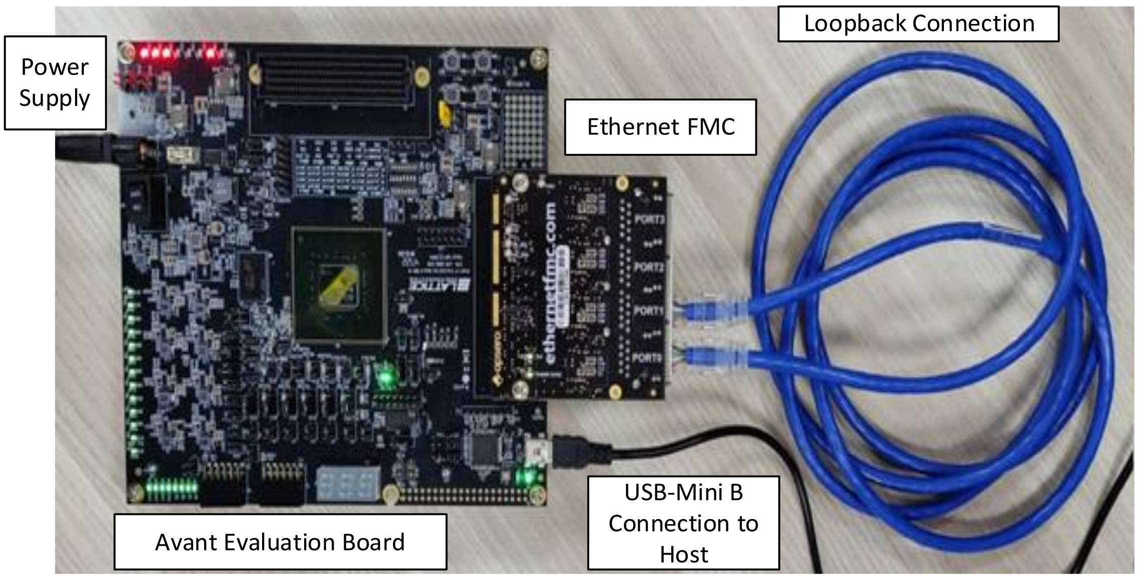

Figure 6.36. Avant Evaluation Board and FMC Setup

The following figure shows the continuous transmission that are sent using the pattern generator, and go through the TX, RX in loopback setup. Each frame is validated. The *compareFail* signal is asserted if the frame checker detected a mismatch, and the done signal is asserted at the end of the transmission. These signals must be added to the Reveal tool manually. For more information, refer to the Reveal User Guide for Radiant Software.

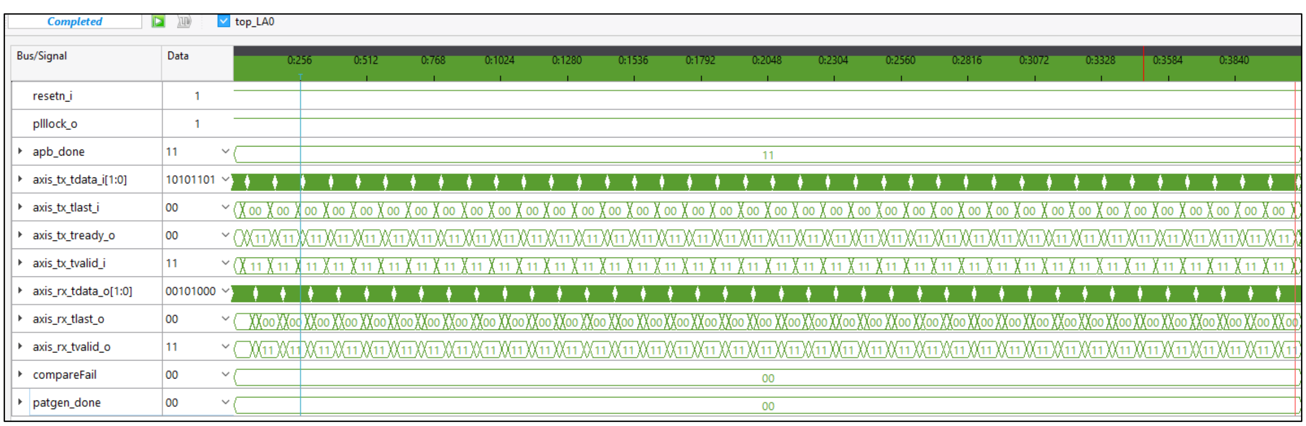

Figure 6.37. Signals Shown on the Reveal Tool

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6.6.6. Hardware Setup for CertusPro-NX Versa Board with RMII Hardware Example Design

Program the bitstream into the device, and make sure DIP switch is set to the right position before triggering the RESET.

6.6.6.1. DIP Switch Definition

The following lists the DIP switch definitions:

- DIP_SW1: Reset
- DIP_SW2: Start or pause transmission

Ensure that DIP_SW2 is set to LOW before reset. Set DIP_SW1 from LOW to HIGH to perform a reset to the hardware design. After configuring the register using APB, LED_1 lights up, and you can start transmission by toggling DIP_SW2 from LOW to HIGH. You can control data transmission by setting DIP_SW2 to LOW to pause or HIGH to resume.

6.6.6.2. HPIO Pin Definition

The following lists the HPIO pin definitions:

- HP_GPIO1 : RMII TX 0
- HP_GPIO2 : RMII TX 1
- HP_GPIO3 : RMII TX EN
- HP_GPIO6 : RMII RX 0
- HP_GPIO7 : RMII RX 1
- HP_GPIO8 : RMII CSR DV

LED_2 and LED_3 must be ON when TX and RX are actively transmitting (for CONTINUOUS_TRAFFIC enabled mode). LED_2 and LED_3 must be OFF when transmission is paused or completed (for CONTINUOUS_TRAFFIC disabled mode), then LED_4 must be ON.

The following lists the failing scenario:

- LED_0 or LED_1 is OFF after RESET.
- LED_6 and LED_7 both are OFF.
- LED_2 or LED_3 is OFF during transmission (for CONTINUOUS_TRAFFIC enabled mode).
- LED_5 is ON.

Table 6.4. LED Indicator Status

CertusPro-NX Evaluation Board (Green)	Description
D63 / LED_0	PLL locked.
D64 / LED_1	Register configuration completed.
D67 / LED_2	TX channel is transmitting.
D65 / LED_3	RX channel is receiving.
D66 / LED_4	PASS traffic generator check.
D104 / LED_5	FAIL traffic generator check.
D105 / LED_6	100M speed.
D68 / LED_7	10M speed.

6.6.7. Hardware Setup for Avant-X Versa Board with SGMII LVDS Hardware Example Design

Program the bitstream into the device, and make sure DIP switch is configured to the right position before triggering the RESET via pushbutton.

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6.6.7.1. DIP Switch Definition

The following lists the available switches:

- DIP_SW1: (LOW) *traffic generator trigger
- DIP_SW2: (LOW)
- DIP_SW3: (HIGH) TSE SPEED bit [0], to configure TSE SPEED, 1G / 100M / 10M
- DIP_SW4: (LOW) TSE SPEED bit [1], to configure TSE SPEED, 1G / 100M / 10M

Speed is configured by concatenating two inputs from DIP_SW3 and DIP_SW4. For all the supported pre-traffic generation speed modes, refer to the following table.

Table 6.5. DIP Switch Configuration Modes and 7-Segment LED—Pre-Reset Traffic Generation Trigger

TSE SPEED	DIP_SW3	DIP_SW4	DIG_2	DIG_3
1G	HIGH	LOW	1	0
100M	LOW	HIGH	0	1
10M	LOW	LOW	0	0
Unsupported	HIGH	HIGH	—	—

6.6.7.2. Pushbutton

The following lists the available pushbuttons:

- SW12 RESET
- SW13 PAUSE transmission

To perform RESET after programming the bitstream or configuring the TSE SPEED from DIP_SW, follow these steps:

1. Confirm that the traffic generator (DIP_SW1) is LOW before triggering the RESET.
2. After the link-up is completed successfully, toggle DIP_SW1 from LOW to HIGH to start the traffic generator, which checks the IP performance.
3. Check the 7-segment LED indicator for device status.
4. You may pause the traffic transmission using SW13 if CONTINUOUS_TRAFFIC is enabled.

6.6.7.3. 7-Segment LED Definition

Each segment in DIG 1 represents the status of the Tri-Speed Ethernet. Refer to the following table for the description of each segment.

Table 6.6. LED 7-Segment Description

Segment	Description
A	Traffic transmission is completed or paused.
B	Reset initiated.
C	Link up is completed successfully.
D	Register configuration is completed successfully.
E	TX transmission is up or transmitting.
F	RX transmission is up or receiving.
G	Data checker detected a mismatch.

DIG 2 and DIG 3 represent the Ethernet SPEED, which can be configured from DIP_SW3 (to DIG 2) and DIP_SW4 (to DIG 3).

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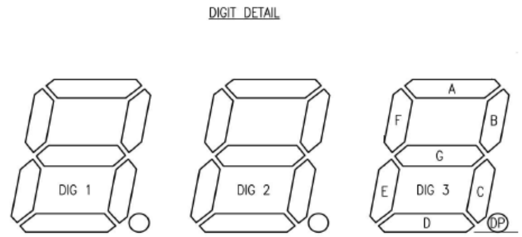

Figure 6.38. 7-Segment LED from Avant-AT-X Devices

You may change the traffic generator mode for sending *n* numbers of frame, or continuous mode in versa_top *CONTINUOUS_TRAFFIC* parameter.

The *SIM* parameter is used for simulation. For hardware example design, keep SIM = 0.

```
module sgmii_avant_x_versa_top # (
    parameter CONTINUOUS_TRAFFIC = 1,
    parameter SIM = 0
) (
```

Figure 6.39. Continuous Traffic Configuration from versa_top

The 7-segment LED shows the following figure when a successful transmission is completed or paused in 1G speed.

Figure 6.40. 7-Segment LED Sample of a Successful Transmission

The USB-Mini B is connected to the host for the Reveal tool to check the signal from hardware, including TX, RX, and data comparison.

The following figure shows the 12 frames that are sent using the pattern generator, and go through the PCS loopback. Each frame is validated. The *compareFail* signal is asserted if the frame checker detected a mismatch, and the *done* signal is asserted at the end of transmission.

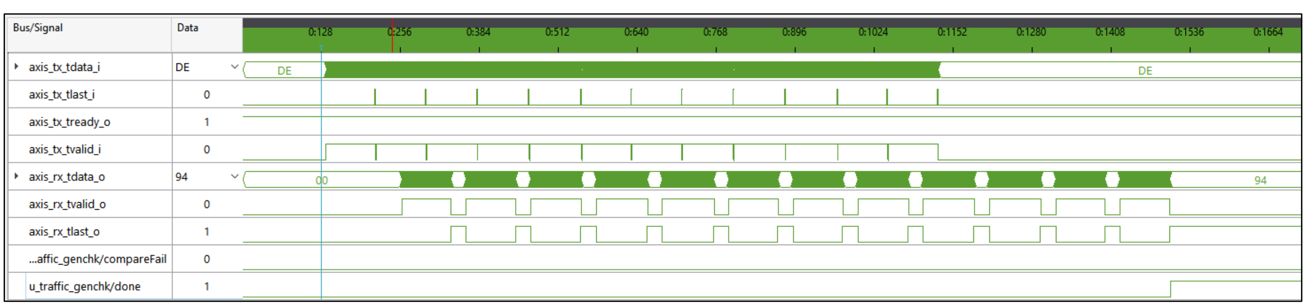

Figure 6.41. 7 Signals Shown on the Reveal Tool

6.6.8. Hardware Setup for Avant-X Versa Board with SGMII SERDES Hardware Example Design

Program the bitstream into the device and make sure the DIP switch is configured to the right position before triggering the RESET via pushbutton.

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6.6.8.1. DIP Switch Definition

The following lists the available switches:

- DIP_SW1: (LOW) *traffic generator trigger
- DIP_SW2: (LOW)
- DIP_SW3: (HIGH) TSE SPEED bit [0], to configure TSE SPEED, 1G / 100M / 10M
- DIP_SW4: (LOW) TSE SPEED bit [1], to configure TSE SPEED, 1G / 100M / 10M

Speed is configured by concatenating two inputs from DIP_SW3 and DIP_SW4. For all the supported pre-traffic generation speed modes, refer to the following table in 7-Segment LED definition.

6.6.8.2. Pushbutton

The following lists the available pushbuttons:

- SW12 RESET
- SW13 PAUSE / RESUME transmission
- SW14 pattern generator mode change (fix frame size, random frame size, or increment frame size)

To perform RESET after programming the bitstream or configuring the TSE SPEED from DIP_SW, follow these steps:

1. Confirm that the traffic generator (DIP_SW1) is LOW before triggering the RESET.
2. After the link-up is completed successfully, toggle DIP_SW1 from LOW to HIGH to start the traffic generator, which checks the IP performance.
3. Check the 7-segment LED indicator for device status, SGMII SERDES operational speed, and pattern generator mode.
4. You may pause the traffic transmission using SW13 if CONTINUOUS_TRAFFIC is enabled.

For DIG 7-segment definitions, refer to Figure 6.42.

DIG 1, Segment B, C, D, E, F must be ON, when TX and RX are actively transmitting (for CONTINUOUS_TRAFFIC enabled mode).

DIG 1, Segment A must be ON when transmission is paused or completed (for CONTINUOUS_TRAFFIC disabled mode).

The following lists the failing scenario:

- DIG 1, any of Segment B, C, D is OFF after reset.
- DIG 1, any of Segment E, F is OFF after the transmission starts.
- DIG 1, Segment G is ON.

6.6.8.3. 7-Segment LED Definition

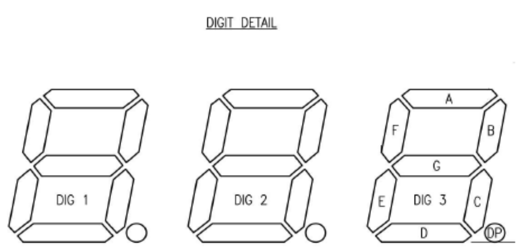

Figure 6.42. 7-Segment LED from Avant-AT-X Devices

Each segment in DIG 1 represents the status of the Tri-Speed Ethernet. Refer to the following table for the description of each segment.

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Table 6.7. LED 7-Segment Description for DIG 1

Segment	Description
A	Traffic transmission is completed or paused.
B	Reset initiated, PLL locked achieved.
C	Link up is completed successfully.
D	Register configuration is completed successfully.
E	TX transmission is up or transmitting.
F	RX transmission is up or receiving.
G	Data checker detected a mismatch.

DIG 2 displays code corresponding to DIP_SW3 and DIP_SW4.

Table 6.8. DIG 2 Code Definition

Code for DIG 2	Code Description	DIP_SW3	DIP_SW4
0	SGMII operational speed 10M	LOW	LOW
1	SGMII operational speed 100M	LOW	HIGH
2	SGMII operational speed 1G	HIGH	LOW

DIG 3 displays code corresponding to different types of frame length, including static frame size, randomize frame size, and incremental frame size. To change the type of frame size, use pushbutton SW14.

Table 6.9. LED 7-Segment Description for DIG 3

Code for DIG 3	Code Description
0	Fix frame size.
1	Randomize frame size.
2	Incremental frame size.

The maximum and minimum boundary for randomized and incremental frame size can be defined in the top file, traffic_genchk module.

FRAME_BOUNDARY_MIN is the minimum value for randomized size, and the starting value for incremental frame size.

FRAME_BOUNDARY_MAX is the maximum value for randomized size, and the largest value for incremental frame size, which starts over again using the minimum value.

STATIC_FRAME_LEN_INIT is used for defining the static frame size.

```
traffic_genchk #(
    .MAX_DATA_WIDTH(8),
    .CONTINUOUS_TRAFFIC (CONTINUOUS_TRAFFIC),
    .FRAME_BOUNDARY_MIN(16'd64),
    .FRAME_BOUNDARY_MAX(16'd9600),
    .STATIC_FRAME_LEN_INIT(16'd1500),
    .NUM_PKT(12)
) u_traffic_genchk (
```

Figure 6.43. Parameters for Frame Size in the Top File

Connect SFP transceiver loopback module to the J27 SFP+ cage. The USB-Mini B is connected to the host for the Reveal tool to check the signal from hardware, including TX, RX, and data comparison.

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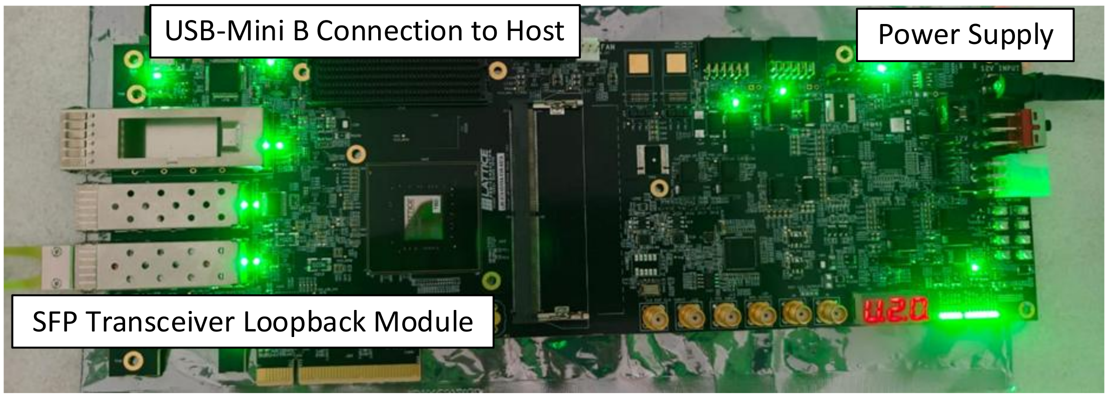

Figure 6.44. Avant-X Versa Board with SFP Transceiver Loopback Module

The following figure shows the continuous transmission using the pattern generator through the SFP loopback. Each frame is validated. The *compareFail* signal is asserted if the frame checker detects a mismatch in the traffic checker.

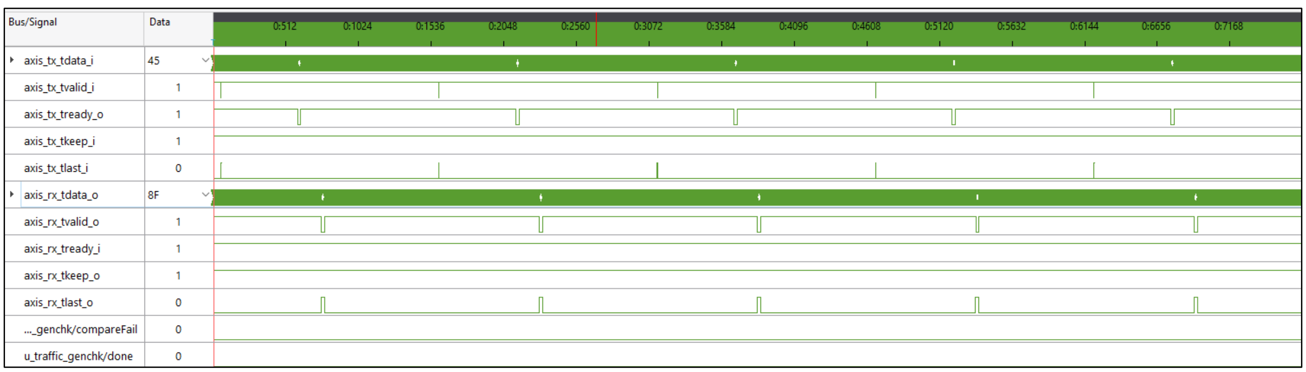

Figure 6.45. Signals shown on the Reveal Tool

6.6.9. Hardware Setup for CertusPro-NX with SGMII SERDES Hardware Example Design

Program the bitstream into the device and make sure DIP switch is configured to the default position before triggering the RESET via DIP switch.

6.6.9.1. DIP Switch Definition

The following lists the available switches:

- DIP_SW1: (LOW) RESET
- DIP_SW2: (LOW) Traffic generator, to start or pause transmission
- DIP_SW3: (HIGH) TSE SPEED bit [0], to configure TSE SPEED, 1G / 100M / 10M
- DIP_SW4: (LOW) TSE SPEED bit [1], to configure TSE SPEED, 1G / 100M / 10M

Speed is configured by concatenating two inputs from DIP_SW3 and DIP_SW4. For all the supported pre-traffic generation speed modes, refer to the following table. Pause transmission when performing speed changes.

Table 6.10. DIP Switch Configuration Modes and LED – Pre-traffic Generation Trigger

TSE SPEED	DIP_SW3	DIP_SW4	LED_6	LED_7
1G	HIGH	LOW	ON	OFF
100M	LOW	HIGH	OFF	ON
10M	LOW	LOW	OFF	OFF
Unsupported	HIGH	HIGH	—	—

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To perform RESET after programming the bitstream or configuring the TSE SPEED change from DIP SW, follow these steps:

1. Confirm that the traffic generator (DIP_SW2) is LOW before asserting RESET (DIP_SW1).
2. After link up complete (LED_0 and LED_1) light up, toggle DIP_SW2 from LOW to HIGH to start traffic generator.
3. You may toggle DIP_SW2 from HIGH to LOW to pause the transmission, and from LOW to HIGH to resume transmission, if CONTINUOUS_TRAFFIC is enabled.

LED_2 and LED_3 must be ON when TX and RX are actively transmitting (for CONTINUOUS_TRAFFIC enabled mode). LED_2 and LED_3 must be OFF when transmission is paused or completed (for CONTINUOUS_TRAFFIC disabled mode), then LED_4 must be ON.

The following lists the failing scenario:

- LED_0 or LED_1 is OFF after RESET.
- LED_2 or LED_3 is OFF during transmission (for CONTINUOUS_TRAFFIC enabled mode).
- LED_5 is ON.

6.6.9.2. LED Definition

Each LED indicates the status of example design. Reger to the table below for details on each LED update, and refer to the device user guide for signal naming conventions.

Table 6.11. General-Purpose LED Signals

CertusPro-NX Evaluation Board (Green)	Description
D63 / LED_0	PLL locked.
D64 / LED_1	APB configuration completed.
D67 / LED_2	TX channel is transmitting.
D65 / LED_3	RX channel is receiving.
D66 / LED_4	Transmission is paused or done.
D104 / LED_5	FAIL traffic checker test.
D105 / LED_6	Tied to DIP_SW3, TSE SPEED bit [0], to identify speed selected.
D68 / LED_7	Tied to DIP_SW4, TSE SPEED bit [1], to identify speed selected.

Connect SFP+ transceiver loopback module to J12 SFP+ cage. The USB-Mini B is connected to the host for Reveal tool to check the signal from hardware, including TX, RX, and data comparison.

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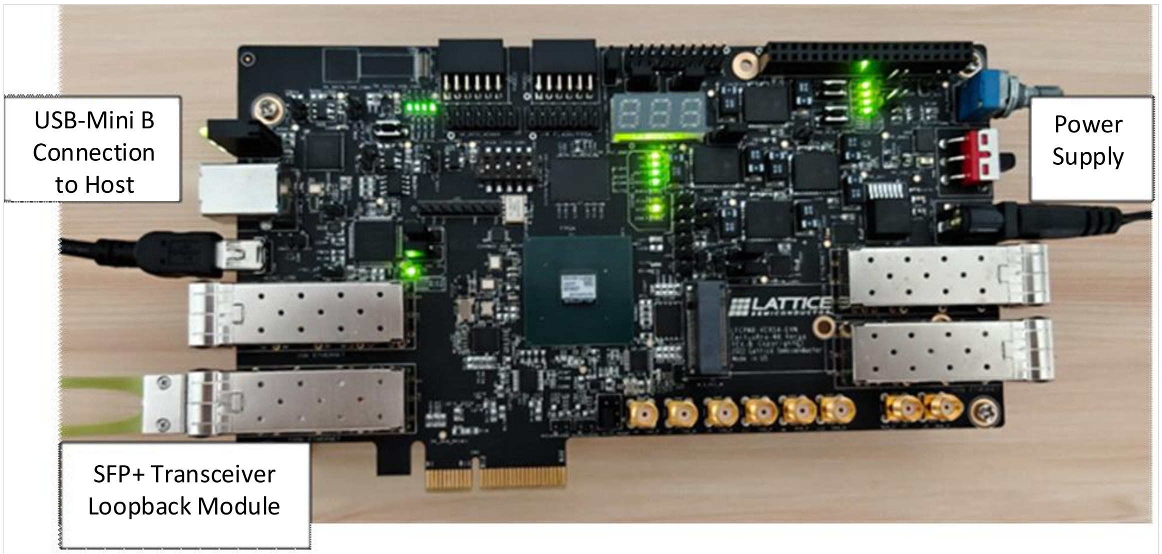

Figure 6.46. CertusPro-NX Versa Board with SFP+ Transceiver Loopback Module

The following figure shows the continuous transmission from TX-AXIS and RX-AXIS using the pattern generator. The compareFail signal is asserted if the checker detects a mismatch.

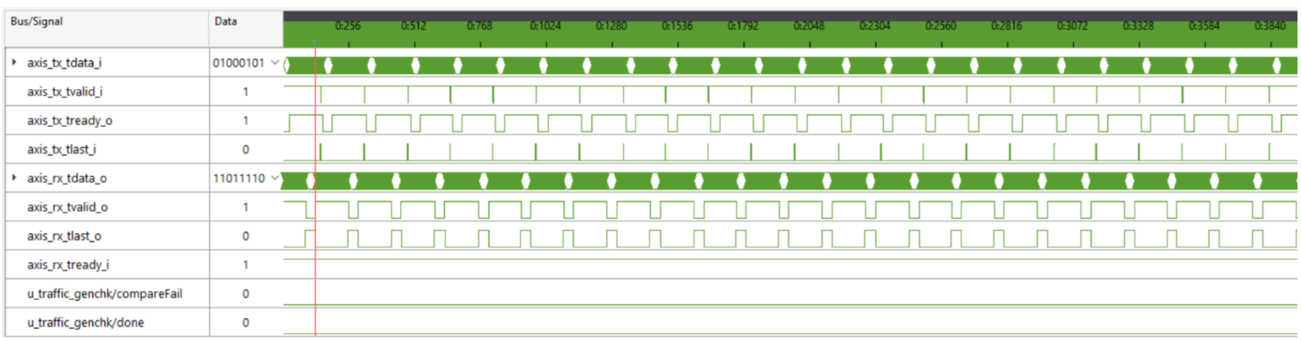

Figure 6.47. Signals shown on the Reveal Tool

6.7. Simulating the Example Design

The hardware example design comes with a testbench for simulating the top file. Supported simulations include the following example designs:

- Avant SGMII (LVDS)
- Avant SGMII (SERDES)
- Avant RGMII
- CertusPro-NX RGMII
- CertusPro-NX RMII
- CertusPro-NX SGMII (SERDES)

6.7.1. Simulating the Top File for Hardware Example Design

The testbench includes initiating the TSE IP and performs continuous traffic transmission and data checking from the traffic generator module.

6.7.1.1. Hardware Example Design Simulation Flow

The following flowchart shows the simulation process from initializing TSE IP and starting the traffic generators to showcasing the IP transmission and receiver performance.

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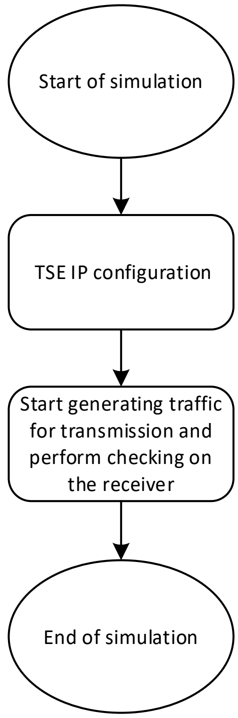

Figure 6.48. SGMII Versa Testbench Example Design Flowchart

Launch the Simulation Wizard from the Radiant software and follow the onscreen instructions. Select **tb*top** as the simulation top module.

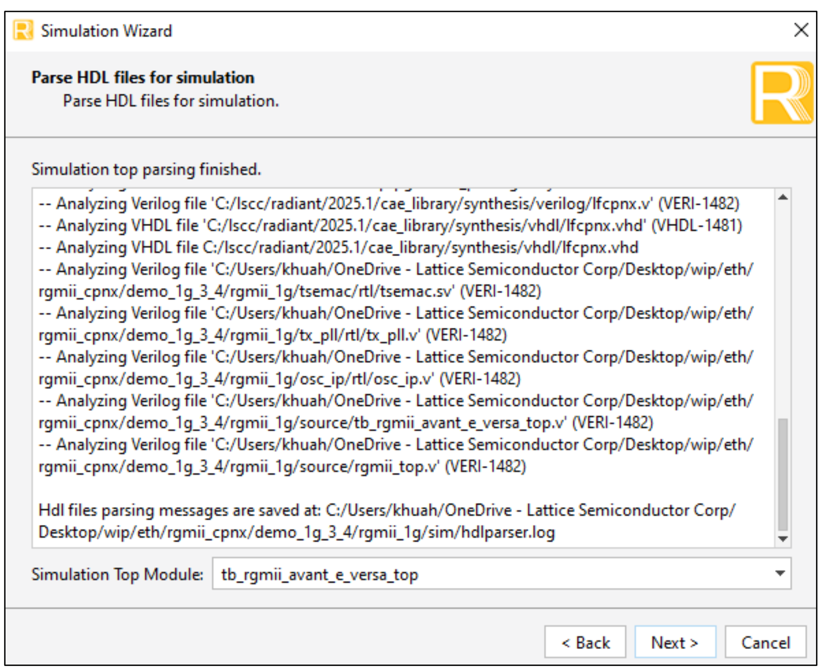

Figure 6.49. Simulation Wizard Top Module Selection

The following figure shows the simulation results for RGMII 1G. Similar simulation results are expected from different available testbenches. The *compareFail* signal indicates whether any data has failed the checker test. The test results in this example show that the data received is error free.

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You may load the *wave.do* macro to group the simulation signals.

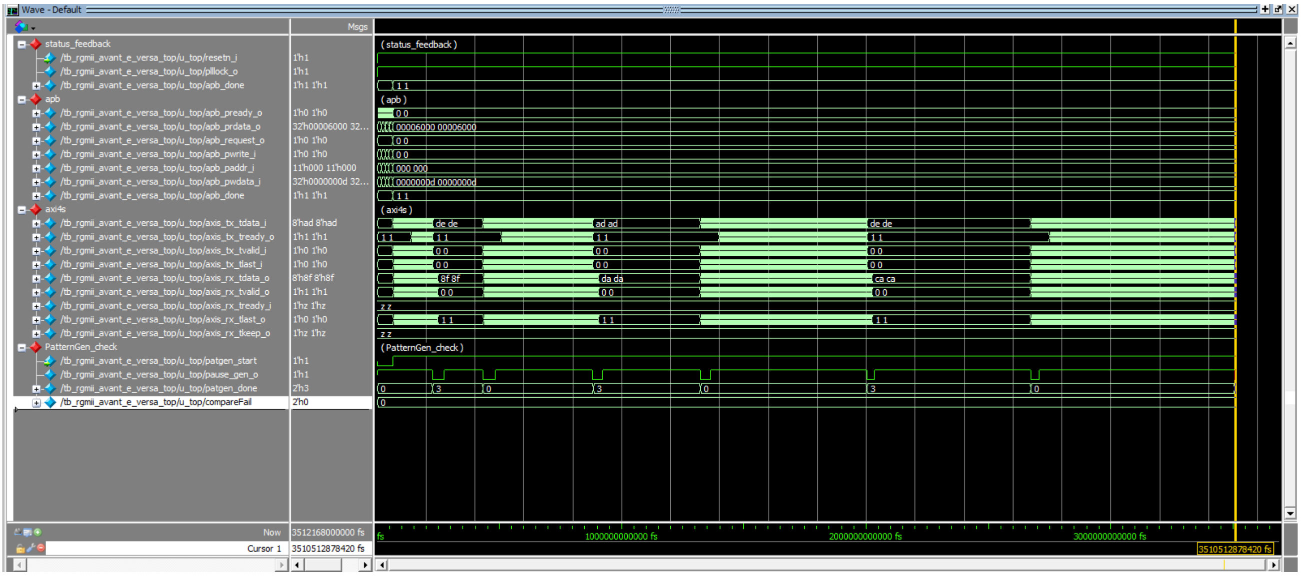

Figure 6.50. Simulation Results for MAC+SGMII (LVDS) Loopback

7. Designing with the IP

This section provides information on how to generate the IP core using the Lattice Radiant software and how to run simulation and synthesis. For more details on the Lattice Radiant software, refer to the Lattice Radiant Software User Guide.

Note: The screenshots provided are for reference only. Details may vary depending on the version of the IP or software being used. If there have been no significant changes to the GUI, a screenshot may reflect an earlier version of the IP.

7.1. Generating and Instantiating the IP

You can use the Lattice Radiant software to generate IP modules and integrate them into the device architecture. The following steps describe how to generate the TSE IP in the Lattice Radiant software.

To generate the TSE IP, follow these steps:

1. Create a new Lattice Radiant software project or open an existing project.
2. In the **IP Catalog** tab, double-click **Tri-Speed Ethernet** under **IP, Connectivity** category. The **Module/IP Block Wizard** opens as shown in Figure 7.1. Enter values in the **Component name** and **Create in** fields and click **Next**.

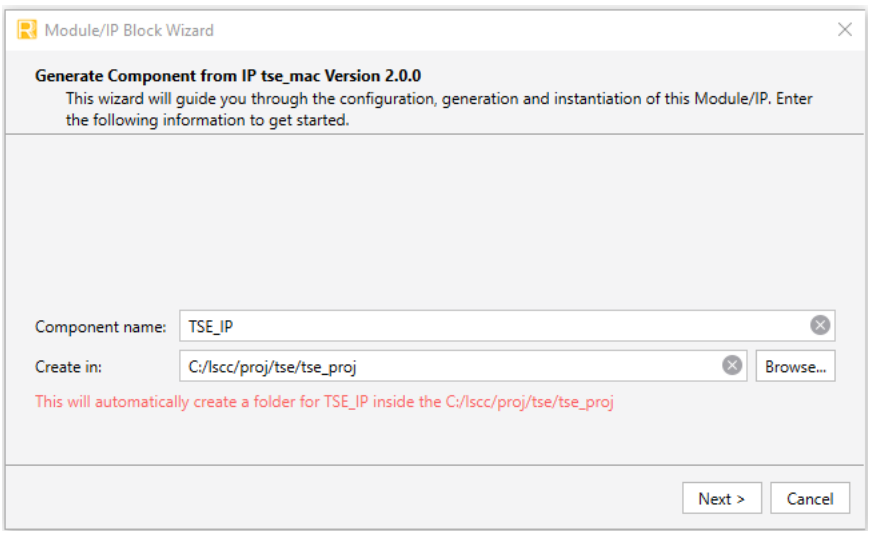

Figure 7.1. Module/IP Block Wizard

3. In the next **Module/IP Block Wizard** window, customize the selected TSE IP using the drop-down list and check boxes. Figure 7.2 shows a configuration example of the TSE IP. For details on the configuration options, refer to the IP Parameter Description section. For RGMII interface configuration, follow the instructions in the Using Hardware Example Design section and use the MII/GMII MAC operating option.

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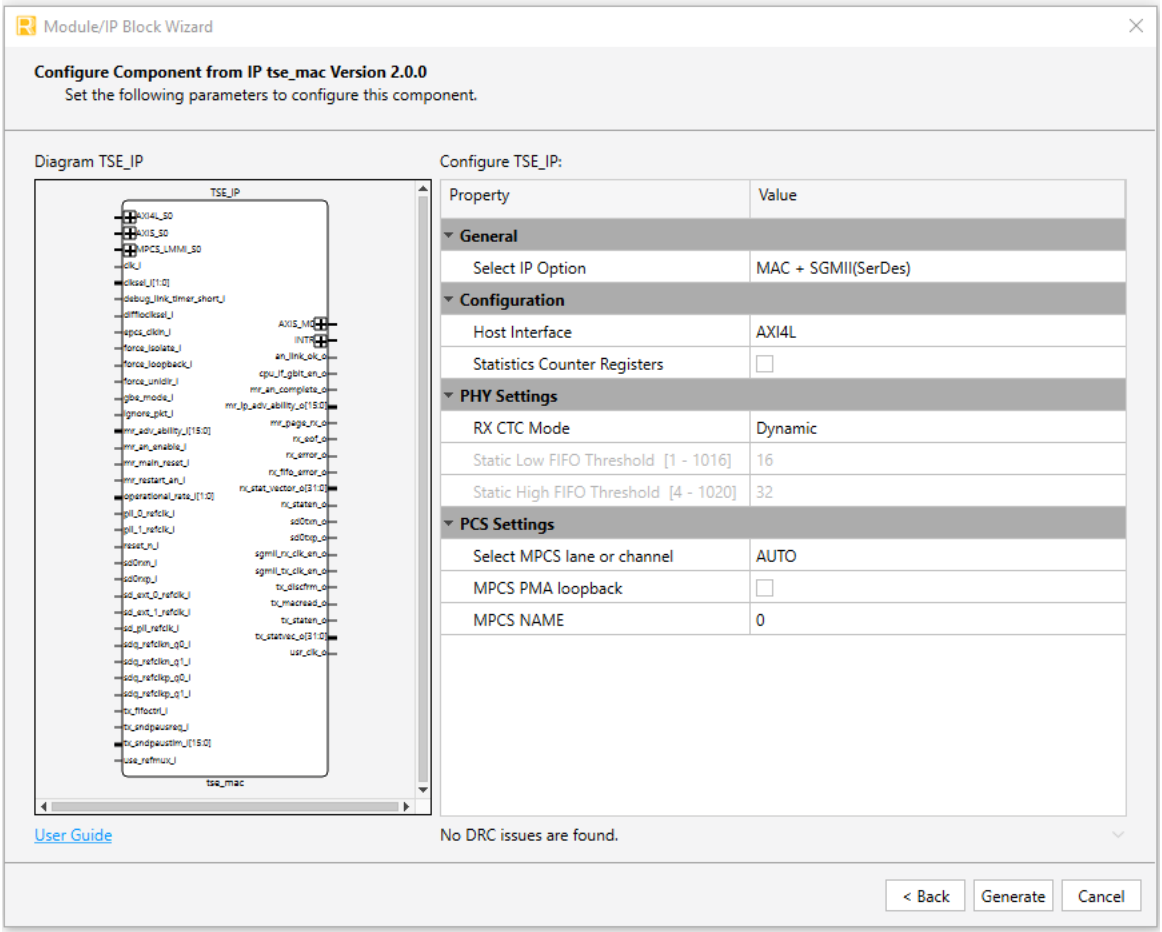

Figure 7.2. IP Configuration

4. Click **Generate**. The **Check Generating Result** dialog box opens and displays the design block messages and results as shown in Figure 7.3.

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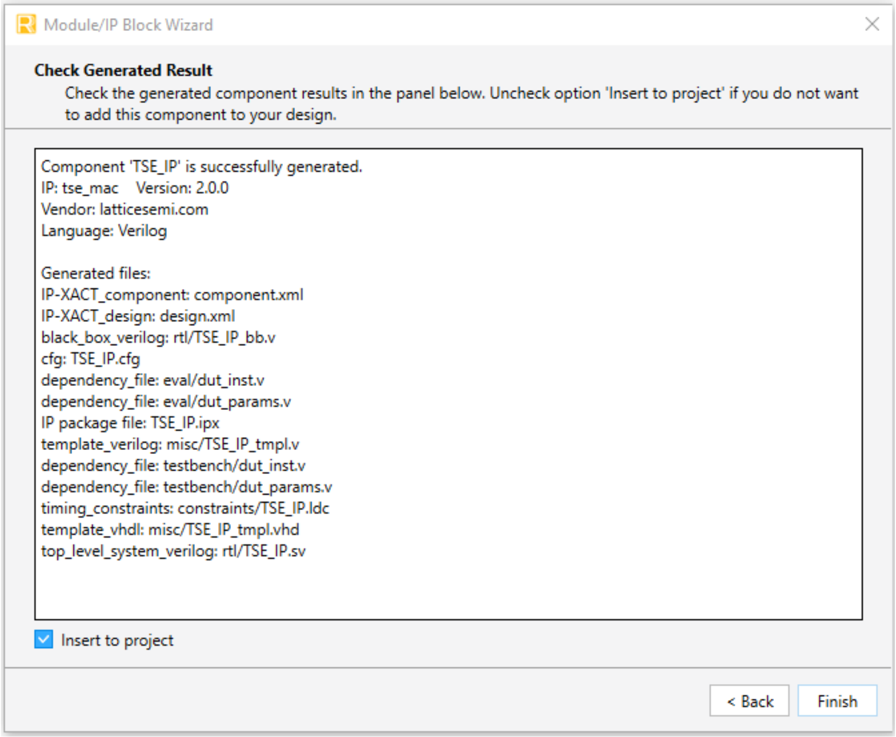

Figure 7.3. Check Generated Result

5. Click **Finish**. All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields shown in Figure 7.1.

7.1.1. Generated Files and File Structure

The generated TSE MAC module package includes the black box (*<Component name>_bb.v*) and instance templates (*<Component name>_tmpl.v/vhd*) that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file (*<Component name>.v*) that can be used as an instantiation template for the module is also provided. You may also use this top-level reference as the starting template for your top-level design. The generated files are listed in Table 7.1.

Table 7.1. Generated File List

Generated File	Description
<Component name>.ipx	This file contains the information on the files associated to the generated IP.
<Component name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Component name>.v	This file provides an example RTL top file that instantiates the module.
rtl/<Component name>_bb.v	This file provides the synthesis closed-box.
misc/<Component name>_tmpl.v *misc /<Component name>_tmpl.vhd*	These files provide instance templates for the module.
testbench/tb_top.v	Top testbench for MAC-only configuration.
constraint/<Component name>.ldc	Pre-synthesis constraint file.
eval/tb_top_eval.v	Top testbench for MAC + PHY configuration.
eval/constraint.pdc	Post-synthesis constraint file.

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7.2. Design Implementation

Completing your design includes additional steps to specify analog properties, pin assignments, and timing and physical constraints. You can add and edit the constraints using the Device Constraint Editor or by manually creating a PDC file.

Post-Synthesis constraint files (*.pdc*) contain both timing and non-timing *constraint.pdc* source files for storing logical timing or physical constraints. Constraints that are added using the Device Constraint Editor are saved to the active *.pdc* file. The active post-synthesis design constraint file is then used as input for post-synthesis processes.

For more information on how to create or edit constraints and how to use the Device Constraint Editor, refer to the relevant sections in the Lattice Radiant Software User Guide.

7.3. Timing Constraints

To ensure proper design coverage and hardware functionality, you must include the following necessary constraints in your design for the IP project. The timing constraints are based on the clock frequency used. The timing constraints for the IP are defined in relevant constraint files. The following example shows the IP timing constraints generated for the TSE IP.

The content of the file should be used as reference to constrain the IP only, you must modify the constraints according to system level implementation. For example, the default clock period of clk_i is 10 ns (100 MHz), if this clock is driven by 125 MHz clock in your project, the clock period of the constraint must be changed to 8 ns.

For more information on timing constraints, refer to the Lattice Radiant Timing Constraints Methodology Application Note (FPGA-AN-02059).

7.3.1. Timing Constraints Files (.sdc)

Timing constraints files (*.sdc*) are generated automatically during IP generation. There is no action required for you to include it in the project. It contains all the constraints for some common clocks of the IP.

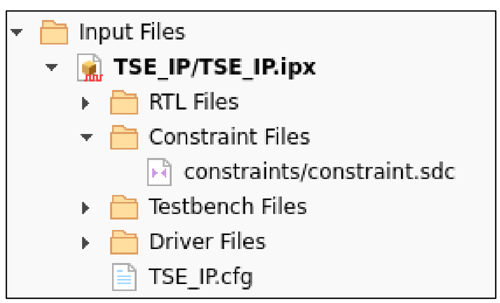

Figure 7.4 Timing Constraint File (.sdc) for the TSE IP

7.3.2. Post-Synthesis Timing Constraint Files (.pdc)

Some internally generated clocks can only be constrained after design synthesis. Those clocks must be constrained for PAR timing closure. For IP level post-synthesis timing constraints, multiple *.pdc* files are provided, refer to Table 7.2.

Table 7.2. Project Constraint Files

File Name	Description
Virtual I/O file: *eval/constraint/virtual_io.pdc*	The *virtual_io.pdc* file provides essential I/O constraints for designs targeting devices with limited physical I/O resources. It enables the IP to be synthesized and implemented successfully by defining virtual I/O assignments that help the design fit within the available capacity.
Nexus SERDES Clocks Constraint file: *eval/constraint/mpcs_clks_eval.pdc*	The *mpcs_clks_eval.pdc* is a constraint file for Nexus SGMII (SERDES). It defines clock-specific constraints required for proper evaluation and implementation of the design. It ensures that certain critical clocks are sourced directly from the expected source, PLL core or CLKDIFFIO core. It is used with the top wrapper, *eval/mpcs_clks_eval/mpcs_clks_eval.v*, refer to Figure 7.5.

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Note: The content of the file must be used as reference to constrain the IP only. You must modify the constraints according to the system-level implementation.

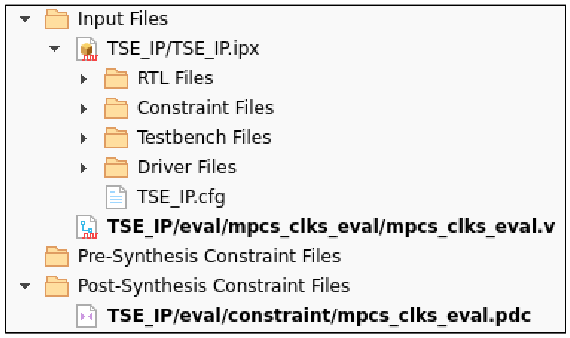

Figure 7.5 Nexus SERDES Clocks Constraint File

7.4. Specifying the Strategy

The Radiant software provides two predefined strategies—Area and Timing. It also enables you to create customized strategies. For details on how to create a new strategy, refer to the *Strategies* section of the Lattice Radiant Software User Guide.

7.5. Running Functional Simulation

You can run functional simulation after the IP is generated.

7.5.1. MAC Only Configuration

To run functional simulation, follow these steps:

1. Click the  button located on the **Toolbar** to initiate the **Simulation Wizard**.

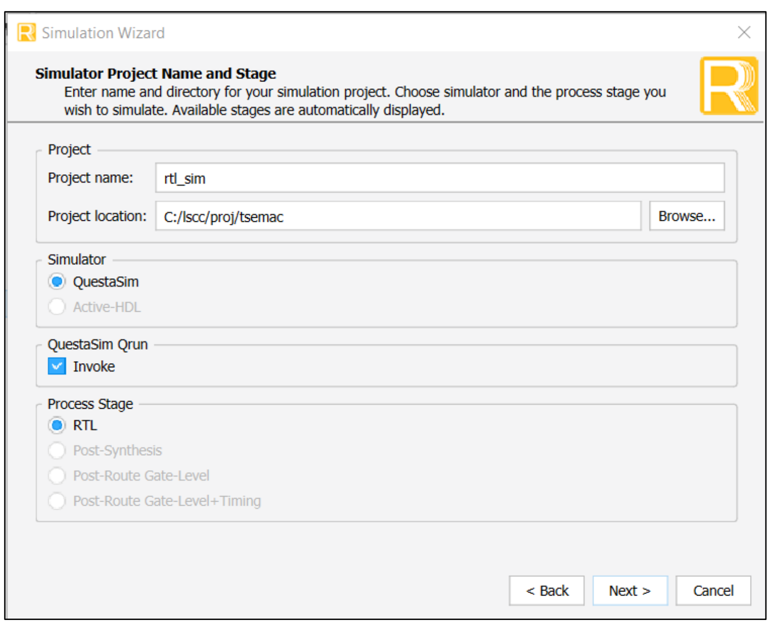

Figure 7.6. Simulation Wizard

2. Click **Next** to open the **Add and Reorder Source** window.

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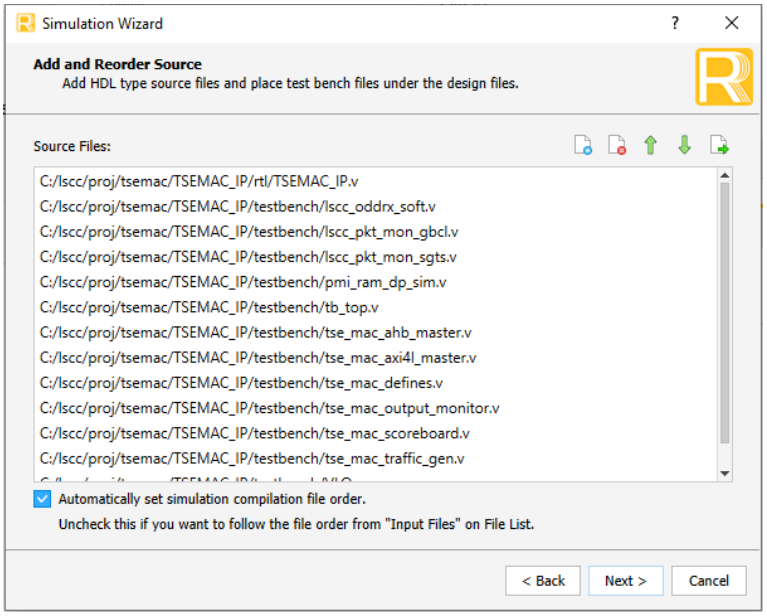

Figure 7.7. Add and Reorder Source

3. Click **Next**. The Parse HDL files for simulation window is shown.

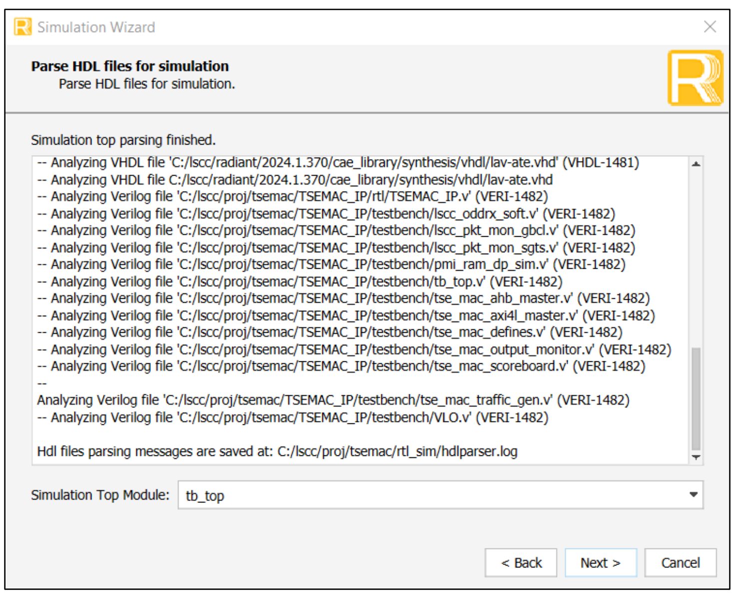

Figure 7.8. Parse HDL Files for Simulation

4. Click **Next**. The **Summary** window is shown.

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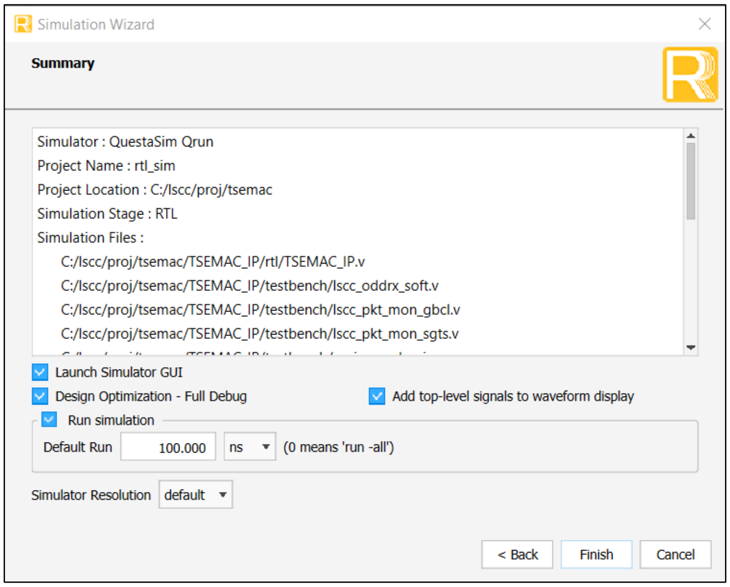

Figure 7.9. Summary

5. Click **Finish** to run the simulation.
6. In the QuestaSim Lattice-Edition transcript window, enter **`run -all`** to run simulation until the end.
7. The following waveform shows an example of the simulation result.

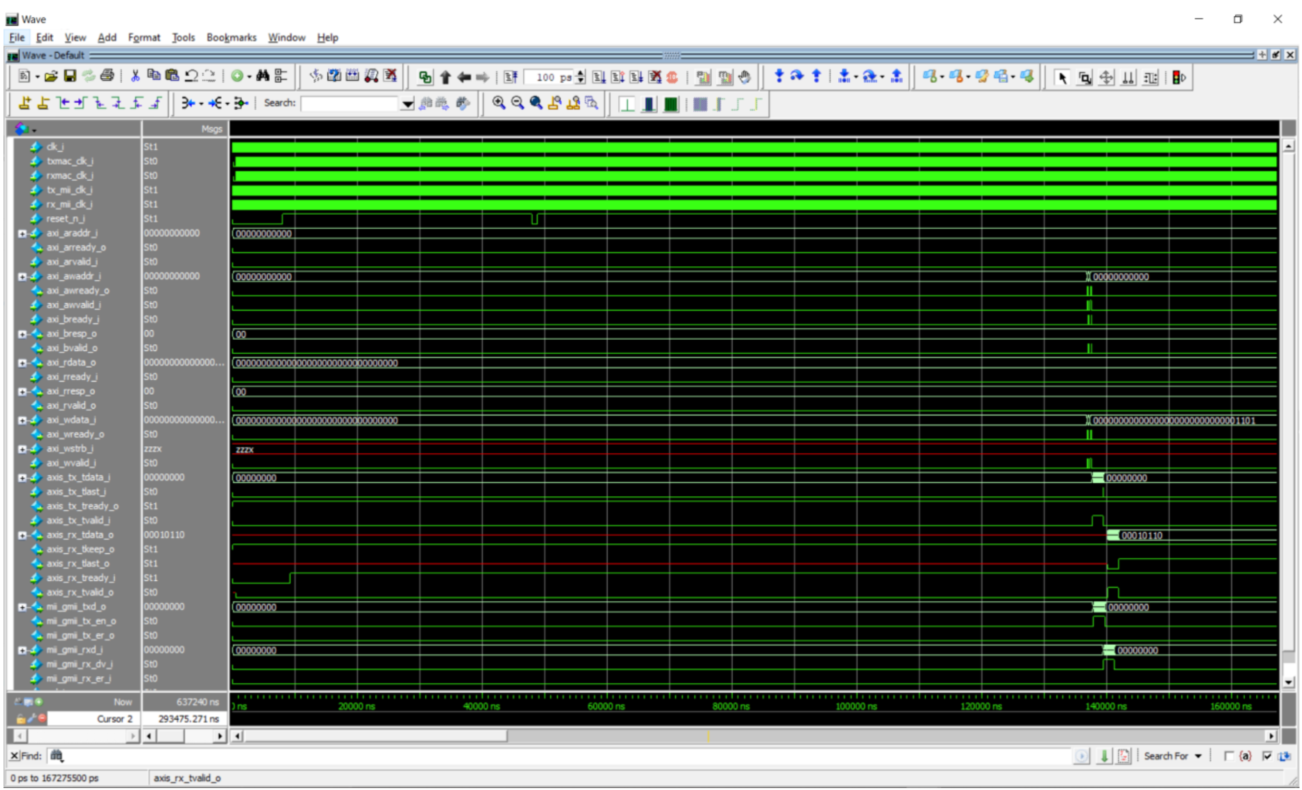

Figure 7.10. Simulation Waveform

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7.5.2. SGMII (LVDS) Only Configuration

To run the Verilog simulation, follow these steps:

1. Add the following files to the Radiant software **Input Files** list:
   - *eval/ sgmii_eval/sgmii_phy_eval.v*—for synthesis and simulation
   - eval/sgmii_eval/tb_top.sv—for simulation only

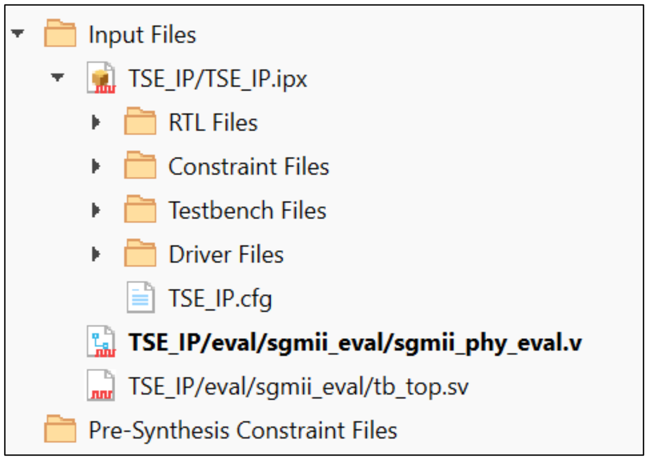

Figure 7.11. Add SGMII Evaluation Top and Testbench in Input Files

2. Repeat steps 1 to 3 in the MAC Only Configuration section to run the simulation.

7.5.3. SGMII (SERDES) Only Configuration

To run the Verilog simulation, follow these steps:

1. Add the following files to the Radiant software **Input Files** list:
   - ***eval/sgmii_eval/tb_top.sv***—for simulation only

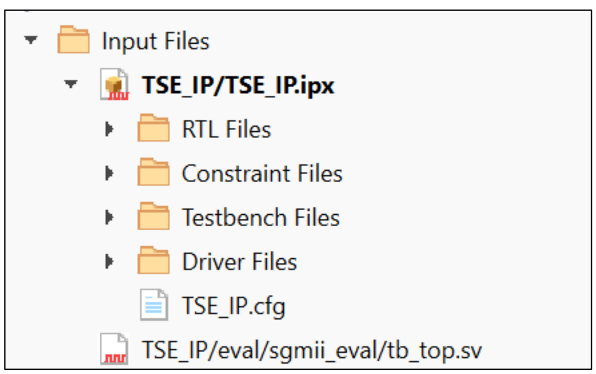

Figure 7.12. Add SGMII Testbench in Input Files

2. Repeat steps 1 to 3 in the MAC Only Configuration section to run the simulation.

7.5.4. MAC + SGMII (LVDS) and MAC + SGMII (SERDES) Configuration

To run the Verilog simulation, follow these steps:

1. Add the **eval/tb_top.sv (**for simulation only) in the Radiant software **Input Files** list.

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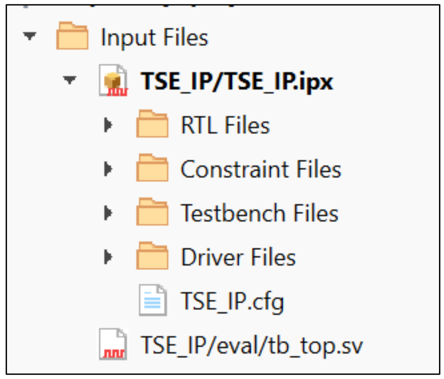

Figure 7.13. Add MAC + SGMII Evaluation Top Testbench in Input Files

2. Repeat steps 1 to 3 in the MAC Only Configuration section to run the simulation.

7.5.5. Simulation Results

The figure below shows an overview of the simulation waveform. The following describes the operations performed by the testbench, which corresponds to the labels in the waveform diagram:

1. Perform TSE IP reset.
2. Configure the TSE IP.
3. Send Ethernet frame in both TX and RX directions.

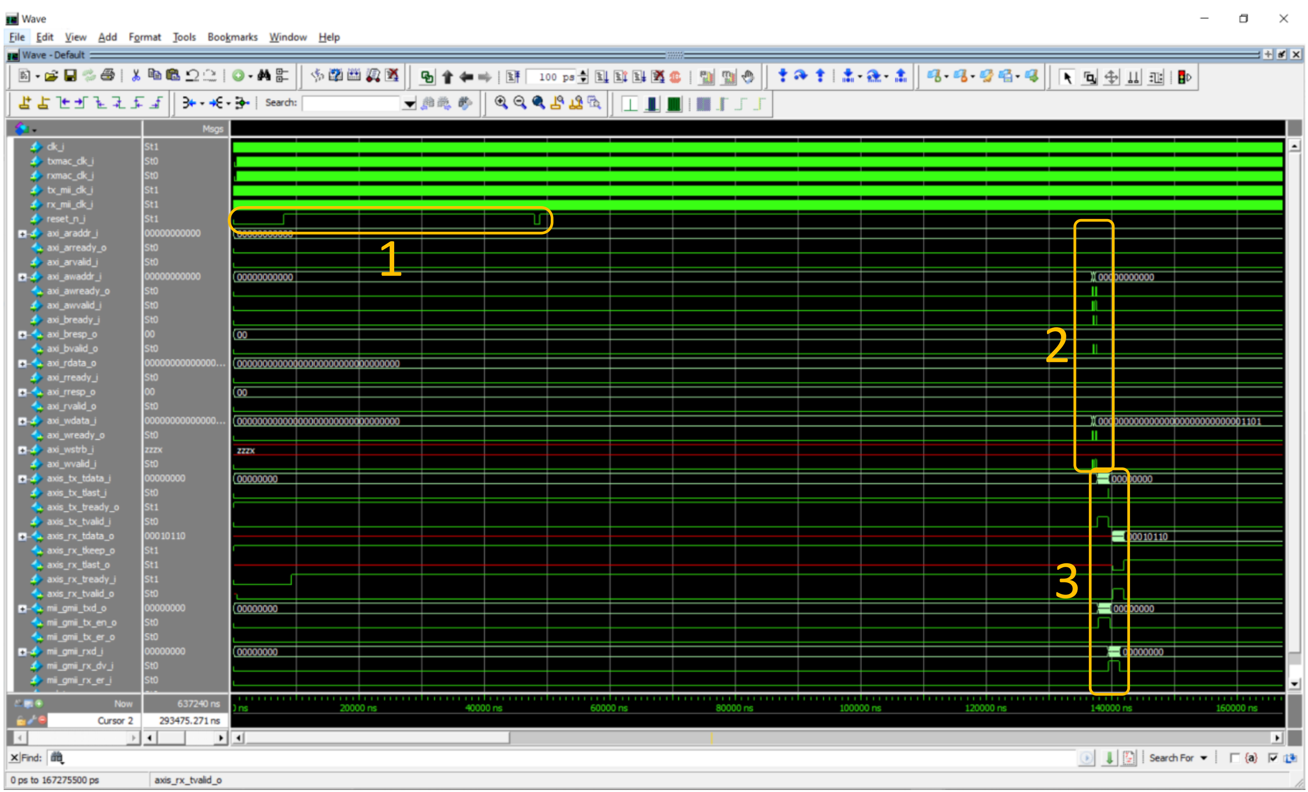

Figure 7.14. Simulation Waveform: Overview

Figure 7.15 shows the details of operation 3 from Figure 7.14. The following describes the labels in the waveform diagram:

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1. Enable Promiscuous Mode of TSE MAC: All loopback frames are received and forwarded to the AXI-4 Stream Receive interface.
   Enable Transmit and Receive datapath: Allows frame transmission and reception.
   Select Gigabit mode: The default Ethernet rate is 1,000 Mbps.
2. The TX clock and RX clock input are changed to 125 MHz for Gigabit mode.
3. The frame is generated for the TX datapath to the TSE MAC AXI-Stream Transmit interface.
4. The transmitted frame output to the TX PHY interface. In this example, the MII/GMII interface is selected as the PHY interface.
5. Frame generated for RX datapath to RX PHY interface. In this example, the MII/GMII interface is selected as the PHY interface.
6. Frame received by the TSE MAC and presented at the AXI-Stream Receive interface.

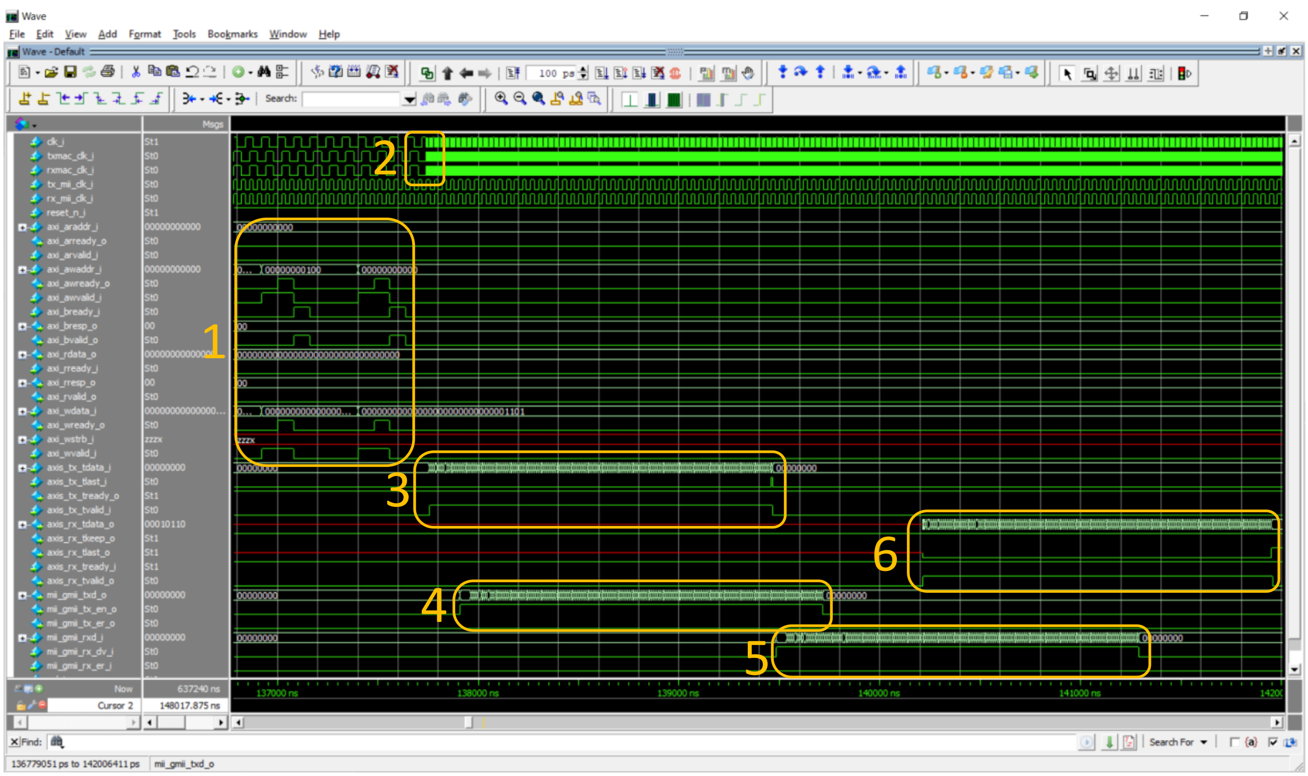

Figure 7.15. Simulation Waveform: Configuring TSE MAC, Frame Transmission and Reception

The figure below shows the simulation output at the beginning of the simulation. The TSE IP configurations are displayed, followed by a reset sequence. After that, the TX and RX traffic generation starts.

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```
# Start collect RX Packet
#
# +---------------------------------------------------------------------------+
# | PARAMETER                                   | VALUE                       |
# +---------------------------------------------------------------------------+
# | INTERFACE                                   | AXI4L                       |
# | SGMII_TSMAC                                 | 0                           |
# | STANDARD MII/GMII                           | 1                           |
# | CLASSIC_TSMAC                               | 0                           |
# | GBE_MAC                                     | 0                           |
# | RGMII                                       | 0                           |
# | MIIM_MODULE                                 | 0                           |
# +---------------------------------------------------------------------------+
# INFO :: @8040ns tb_top.drive_reset() :: Driving reset pin to 1
# INFO :: @48040ns tb_top.drive_reset() :: Driving reset pin to 0
# INFO :: @48840ns tb_top.drive_reset() :: Driving reset pin to 1
# MSG :: @56840ns tb_top.test_runner() :: Setting random seed to default 1
# MSG :: @56840ns tb_top.test_runner() :: Setting num_tran_ui to default 1
# MSG :: @56840ns tb_top.test_runner() :: No testcase name passed with +test option,so calling basic testcase-test_basic..................
VSIM 7> run -all
# MSG :: @137748ns tb_top.U_traffic_gen.tx_fifo_data_write() :: TX Traffic Generation.....
# MSG :: @137916ns tb_top.U_output_monitor() :: Sampling data from the TSE-MAC Transmitter.....
# WRITE TO Data Stream FIFO: Data size: 200 time: 139460
# MSG :: @139476ns tb_top.U_traffic_gen.gen_rx_data() :: RX Traffic Generation.....
```

Figure 7.16. Simulation Output: Beginning of the Simulation

For every transmitted frame, the content of the expected frame and monitored frame are displayed as shown in the following figure.

```
# +---------------------------------------------------------------------------+
# | FIELD                | EXPECTED                  | GOT                       |
# +---------------------------------------------------------------------------+
# | FRAME SIZE           |   214                     |   214                     |
# | DATA                 | 0xdeac80000048deac        | 0xdeac80000048deac        |
# | DATA                 | 0x475cc80080000048        | 0x475cc80080000048        |
# | DATA                 | 0x6a078c2cd0b43986        | 0x6a078c2cd0b43986        |
# | DATA                 | 0xc9a423ec734be811        | 0xc9a423ec734be811        |
# | DATA                 | 0x4982b09d67d4df39        | 0x4982b09d67d4df39        |
# | DATA                 | 0x5dc82ae3931c20d9        | 0x5dc82ae3931c20d9        |
# | DATA                 | 0xd0595212392b843a        | 0xd0595212392b843a        |
# | DATA                 | 0x690f00bba6db976e        | 0x690f00bba6db976e        |
# | DATA                 | 0x77695190cfc5590c        | 0x77695190cfc5590c        |
# | DATA                 | 0x3086b7b8c49bd84a        | 0x3086b7b8c49bd84a        |
# | DATA                 | 0x018be97607d4b577        | 0x018be97607d4b577        |
# | DATA                 | 0xaf66af30c5c280db        | 0xaf66af30c5c280db        |
# | DATA                 | 0x60ee95e1ef06f8e9        | 0x60ee95e1ef06f8e9        |
# | DATA                 | 0x816e77e1296428e5        | 0x816e77e1296428e5        |
# | DATA                 | 0x8e7df10faaf068d5        | 0x8e7df10faaf068d5        |
# | DATA                 | 0xb94aaf5befa93ce2        | 0xb94aaf5befa93ce2        |
# | DATA                 | 0x713a99b751651313        | 0x713a99b751651313        |
# | DATA                 | 0xc9ede5597d2ae462        | 0xc9ede5597d2ae462        |
# | DATA                 | 0xbda20670cddbaf41        | 0xbda20670cddbaf41        |
# | DATA                 | 0x5cf678257b50dc6a        | 0x5cf678257b50dc6a        |
# | DATA                 | 0xce0c730ebbc87923        | 0xce0c730ebbc87923        |
# | DATA                 | 0x390c75f4b3b959d4        | 0x390c75f4b3b959d4        |
# | DATA                 | 0x8d08b8024e051502        | 0x8d08b8024e051502        |
# | DATA                 | 0x25407b4cf590e8af        | 0x25407b4cf590e8af        |
# | DATA                 | 0x50c030bc292d700d        | 0x50c030bc292d700d        |
# | DATA                 | 0xbc6a945df5f54da1        | 0xbc6a945df5f54da1        |
# | DATA                 | 0x0000930746fa9eb8        | 0x0000930746fa9eb8        |
# +---------------------------------------------------------------------------+
```

Figure 7.17. Simulation Output: Transmitted Frame

For every received frame, the content of the expected frame and monitored frame are displayed as shown in the following figure. At the end of the simulation, the number of transactions and the number of detected errors are displayed. The simulation shows a Passed status if no error is detected.

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```
# MSG :: @140220ns tb_top.U_output_monitor.collect_rx_frame() :: Sampling data from the TSE-MAC Receiver.....
#
# +---------------------------------------------------------------------------+
# | FIELD               | EXPECTED                  | GOT                       |
# +---------------------------------------------------------------------------+
# | FRAME SIZE          |   218                     |   218                     |
# | DATA                | 0xdeac80000048deac        | 0xdeac80000048deac        |
# | DATA                | 0x5086c80080000048        | 0x5086c80080000048        |
# | DATA                | 0x734b98c5c12935f5        | 0x734b98c5c12935f5        |
# | DATA                | 0xe60ea1a9a84e8aec        | 0xe60ea1a9a84e8aec        |
# | DATA                | 0xc879389e8d2a2a9f        | 0xc879389e8d2a2a9f        |
# | DATA                | 0xb9c4bab6c76b13ca        | 0xb9c4bab6c76b13ca        |
# | DATA                | 0xbd32f2fa867fb492        | 0xbd32f2fa867fb492        |
# | DATA                | 0x0bfb8ea1a9cae484        | 0x0bfb8ea1a9cae484        |
# | DATA                | 0xae886b8f7536c9ef        | 0xae886b8f7536c9ef        |
# | DATA                | 0x0d1ec24b2d28929b        | 0x0d1ec24b2d28929b        |
# | DATA                | 0x53d83b4186d118ec        | 0x53d83b4186d118ec        |
# | DATA                | 0xb812d87304e25b56        | 0xb812d87304e25b56        |
# | DATA                | 0xa127c8812ba1e539        | 0xa127c8812ba1e539        |
# | DATA                | 0xb19612149658041f        | 0xb19612149658041f        |
# | DATA                | 0xa78427adf52bed55        | 0xa78427adf52bed55        |
# | DATA                | 0x2aa151c9db49b9e7        | 0x2aa151c9db49b9e7        |
# | DATA                | 0x6f68fe727c8345fa        | 0x6f68fe727c8345fa        |
# | DATA                | 0xc0c5f6284038f086        | 0xc0c5f6284038f086        |
# | DATA                | 0xe115622a3cb03974        | 0xe115622a3cb03974        |
# | DATA                | 0x5a8dc12586c94317        | 0x5a8dc12586c94317        |
# | DATA                | 0x9ef7b63b710c2c07        | 0x9ef7b63b710c2c07        |
# | DATA                | 0x0dddb472a020555c        | 0x0dddb472a020555c        |
# | DATA                | 0xe3038f7bfd9e794b        | 0xe3038f7bfd9e794b        |
# | DATA                | 0xf852ede09544b11d        | 0xf852ede09544b11d        |
# | DATA                | 0x6a17908c4684528d        | 0x6a17908c4684528d        |
# | DATA                | 0x25a68bba607caa84        | 0x25a68bba607caa84        |
# | DATA                | 0x13674b3d1449a232        | 0x13674b3d1449a232        |
# | DATA                | 0x0000000000001601        | 0x0000000000001601        |
# +---------------------------------------------------------------------------+
# MSG :: @397240ns tb_top.post_process() :: ######################################################################
# MSG :: @397240ns tb_top.post_process() ::               Errors   detected in CHECKER    0
# MSG :: @397240ns tb_top.post_process() ::               Number of Transactions          2
# MSG :: @397240ns tb_top.post_process() :: ######################################################################
# MSG :: @397240ns tb_top.post_process() ::                         SIMULATION PASSED
# MSG :: @397240ns tb_top.post_process() :: ######################################################################
# ** Note: $finish    : C:/lscc/proj/tsemac/TSEMAC_IP/testbench/tb_top.v(979)
#    Time: 637240 ns  Iteration: 1  Instance: /tb_top
```

Figure 7.18. Simulation Output: Received Frame and End of Simulation

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8. Known Issues

This section provides information on known issues that have a fix planned for future releases.

8.1. RX Stat Vector Limitation for Carrier Event Previously Seen (bit[27]) and Packet Ignored (bit[26])

8.1.1. Devices Affected

All devices.

8.1.2. Designs Affected

This issue affects all IP design options for both *MAC only* and *MAC + SGMII* IP option.

8.1.3. Issue Details

This issue only impacts stat vector logging and does not impact regular transmissions. Error transactions are also unimpacted, whereby crc_error or rx_error_o will be asserted to indicate the erroneous packet that is meant to be dropped.

The RX Stat vector counter related behavior or logging for bits[27:26] have erroneous behavior when error packets are being received. However, for error-related detection, the CRC error (bit[25]), length check error (bit[24], and unsupported opcode error (bit[19]) stat vectors are working as intended.

No issues are seen with good or uncorrupted packets.

8.1.4. Planned Fix

Lattice intends to resolve this issue in a future revision of the Tri-Speed Ethernet IP core.

8.2. Erroneous Length/Type Handling when the L/T is Smaller than 46

8.2.1. Devices Affected

All devices.

8.2.2. Designs Affected

This issue affects all IP design options for both *MAC only* and *MAC + SGMII* IP option.

8.2.3. Issue Details

This issue only impacts packets that are sent with erroneous L/T fields and specifically with a value that is smaller than or equal to 46. For example, a packet that has a size of 73 but wrapped with an L/T value of 46 (erroneous packet) will see this issue. In this case, the packet passes through the MAC without any error flag.

It does not impact valid packets with a valid L/T field of less than or equal to 46, or erroneous packets with an L/T value that is larger than 46.

8.2.4. Planned Fix

Lattice intends to resolve this issue in a future revision of the Tri-Speed Ethernet IP core.

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8.3. Error Handling when rx_fifo_error_o is Asserted

8.3.1. Devices Affected

All devices.

8.3.2. Designs Affected

This issue affects all IP design options for both *MAC only* and *MAC + SGMII* IP option.

8.3.3. Issue Details

This issue occurs when the rx_fifo_error_o signal is asserted (to denote the RX FIFO is full). There may be issues with the packets following the deassertion of this signal. Therefore, you must disregard the next 2,048 bytes of data once the signal is deasserted. After that, wait until a tlast is detected, and upon tlast deassertion, the following packets after that can be consumed as regular error free packets.

8.3.4. Planned Fix

Lattice intends to resolve this issue in a future revision of the Tri-Speed Ethernet IP core.

8.4. SGMII Receiver Sampling Behavior at 100 Mbps and 10 Mbps

8.4.1. Devices Affected

All devices.

8.4.2. Designs Affected

Link partner side receiver. SGMII runs at 10/100 Mbps rate.

8.4.3. Issue Details

SGMII leverages the PCS and serialization mechanisms defined in the IEEE 802.3 1000BASE-X specification.

Using 100 Mbps as an example. When a START_ERROR condition occurs in the 1000BASE-X TX State Machine, the transmitter sends a specific sequence: FB, FE, FE, FE, FE, FE, FE, FE, FE, FE
1 cycle of /S/ (Start of Error, also referred to as FB)
9 cycles of /V/ (Error Propagation, also referred to as FE)

The SGMII specification does not explicitly define where the receiver must sample the data during 100 Mbps and 10 Mbps operation. As a result, the sampling point is implementation-dependent and left to the discretion of the designer.

On the link partner side, the receiver may sample at different points within the 10-cycle sequence:

- Sampling on the first cycle captures the FB
- Sampling on cycles 2 through 10 captures the FB FE

In this implementation, the device under test (DUT) transmits the correct sequence during START_ERROR. Although the DUT behaves correctly, link partner side receivers may implement different sampling logic. If the receiver samples at the first cycle, it captures the FB symbol and correctly decodes the frame as a START_ERROR. However, if sampling occurs at a later cycle (for example, cycle 2 and beyond), the receiver may capture FE instead, which can cause the packets to drop.

8.4.4. Planned Fix

This behavior is not considered a defect and will not be fixed. It serves as a soft reminder that receiver implementations on the link partner side may vary, at lower speeds (100 Mbps and 10 Mbps), and could result in different sampling outcomes.

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References

- Tri-Speed Ethernet IP Release Notes (FPGA-RN-02036)
- Tri-Speed Ethernet Driver API Reference (FPGA-TN-02341)
- SGMII and Gb Ethernet PCS IP Core User Guide (FPGA-IPUG-02077)
- Lattice Memory Mapped Interface (LMMI) and Lattice Interrupt Interface (LINTR) User Guide (FPGA-UG-02039)
- Lattice Radiant Timing Constraints Methodology Application Note (FPGA-AN-02059)
- Avant Evaluation Board User Guide (FPGA-EB-02057)
- Avant-G/X Versa Board User Guide (FPGA-EB-02063)
- TSEMAC & SGMII Reference Design web page
- Tri-Speed Ethernet IP Core web page
- Avant-E web page
- Avant-G web page
- Avant-X web page
- CrossLink-NX web page
- Certus-NX web page
- CertusPro-NX web page
- MachXO5-NX web page
- Lattice Radiant Software web page
- Lattice Solutions IP Cores web page
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Appendix A. Resource Utilization

The following table shows the sample resource utilization of the Tri-Speed Ethernet IP core for the LAV-AT-G70-1LFG676I device using the Synplify Pro tool of the Lattice Radiant software 2025.2. The default configuration is used, and some attributes are changed from the default value to show the effect on the resource utilization.

Table A.1. IP Resource Utilization for an Avant Device

Configuration		Registers	LUTs	EBRs	PLL
Select IP Option: MAC + SGMII (LVDS) (default)	Others= Default	5,293	7,227	5	1
	Select MAC + SGMII (LVDS) Operating Option: Gigabit Ethernet, Others = Default	5,293	7,227	5	1
Select IP Option: SGMII (LVDS) only	Others= Default	2,691	4,817	1	1
Select IP Option: MAC + SGMII (SERDES)	Others= Default	4,337	4,770	5	0
Select IP Option: SGMII (SERDES) only	Others= Default	1,524	2,140	1	0
Select IP Option: MAC only	Others= Default	2,904	2,704	5	0
	Host Interface: AHBL, Others = Default	2,984	2,995	5	0
	Host Interface: APB, Others = Default	2,897	2,635	5	0
	Select MAC Operating Option: Gigabit MAC, Others = Default	2,767	2,388	4	0
	Select MAC Operating Option: SGMII Easy Connect, Others = Default	2,789	2,531	4	0
	Select MAC Operating Option: RGMII, Others = Default	2,847	2,596	4	0
	Select MAC Operating Option: RMII, Others = Default	2,868	2,599	4	0
	Statistics Counter Option: Checked, Others = Default	6,701	6,070	5	0

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Configuration		Registers	LUTs	EBRs	PLL
	Enable Half Duplex Module: Unchecked, *Enable AXIS FIFO Functionality:* Unchecked, Others = Default	2,298	2,070	2	0

The following table shows the sample resource utilization of the Tri-Speed Ethernet IP core for the LFCPNX-50-7ASG256I device using the Synplify Pro tool of the Lattice Radiant software 2025.1. The default configuration is used, and some attributes are changed from the default value to show the effect on the resource utilization.

Table A.2. IP Resource Utilization for a CertusPro-NX Device

Configuration		Registers	LUTs	EBRs	PLLs
Select IP Option: MAC + SGMII (SERDES) (default)	Others = Default	4,170	4,923	5	0
Select IP Option: SGMII (SERDES) only	Others = Default	1,409	2,201	1	0
Select IP Option: MAC only	Others = Default	2,825	2,930	5	0
	Host Interface: AHBL, Others = Default	2,916	3,147	5	0
	Host Interface: APB, Others = Default	2,818	2,882	5	0
	Select MAC Operating Option: Gigabit MAC, Others = Default	2,679	2,628	4	0
	Select MAC Operating Option: SGMII Easy Connect, Others = Default	2,704	2,778	4	0
	Select MAC Operating Option: RGMII, Others = Default	2,762	2,842	4	0
	Select MAC Operating Option: RMII, Others = Default	2,783	2,820	4	0
	Statistics Counter Option: Checked, Others = Default	6,621	6,400	4	0

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Configuration		Registers	LUTs	EBRs	PLLs
	Enable Half Duplex Module: Unchecked, *Enable AXIS FIFO Functionality:* Unchecked, Others = Default	2,311	2,136	2	0

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Revision History

Note: In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

Revision 2.5, IP v2.2.0, December 2025

Section	Change Summary
All	Updated the IP version on the cover page.
Introduction	• Updated Table 1.1. Summary of the TSE IP Core. • Updated the Features section. • Updated the Licensing and Ordering Information section.
Functional Description	• Updated the Clocking for SGMII (LVDS) Only section. • Updated the Clocking for SGMII (SERDES) Only section. • Added the Lane Merging section.
IP Parameter Description	• Updated Table 3.2. MAC Only Mode Attributes. • Updated Table 3.3. SGMII (LVDS) Only Mode Attributes. • Updated Table 3.4. SGMII (SERDES) Only Mode Attributes. • Updated Table 3.5. SGMII (SERDES) Only Mode Attributes. • Updated Table 3.6. MAC + SGMII Mode Attributes. • Updated Table 3.7. MAC + MPCS Mode Attributes.

Signal Description	• Updated the following tables:
	  • Table 4.4. AXI4-Stream Transmit Interface Ports.
	  • Table 4.5. AXI4-Stream Receive Interface Ports.
	  • Table 4.19. SGMII (LVDS) Only Clock and Reset Interface Ports.
	  • Table 4.26. SGMII (SERDES) Only Clock and Reset Interface Ports on Nexus Devices.
	• Removed Table 4.23. SGMII (LVDS) Only MDIO Interface Ports.
	• Removed Table 4.30 SGMII (SERDES) Only MDIO Interface Ports on Nexus Devices.
	• Added pcs_usr_clk_i signal to Table 4.33. SGMII (SERDES) Only Clock and Reset Interface Ports on Avant Devices.
	• Removed Table 4.39 SGMII (SERDES) Only MDIO Interface Ports on Avant Devices.
	• Updated Table 4.43. MAC + SGMII (SERDES) Clock and Reset Interface Ports on Nexus Devices.
	• Added pcs_usr_clk_i signal to Table 4.48. MAC + SGMII (SERDES) Clock and Reset Interface Ports on Avant Devices.

Register Description	Updated the description for the hden register in Table 5.4. Transmit and Receive Control Register.
Example Design	• Updated Table 6.1. TSE IP Configuration Supported by Example Designs. • Updated the Importing Versa Files into a Project section. • Updated the Hardware Setup for Avant-X Versa Board with SGMII SERDES Hardware Example Design section.
Known Issues	Added the SGMII Receiver Sampling Behavior at 100 Mbps and 10 Mbps section.
Appendix A. Resource Utilization	Updated the following tables: • Table A.1. IP Resource Utilization for an Avant Device. • Table A.2. IP Resource Utilization for a CertusPro-NX Device.

Revision 2.4, IP v2.1.0, October 2025

Section	Change Summary
Introduction	• Updated Table 1.2. TSE IP Core Support Readiness. • Updated the Hardware Support section.
Functional Description	• Updated the following tables: • Table 2.1. Operation Options.

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Section	Change Summary

	• Table 2.2. Summary of Implementation Options.
	• Updated the title for Figure 2.12. Detailed Block Diagram of the SGMII (LVDS) Only Mode.
	• Updated the following sections:
	  • SGMII (SERDES) Only Mode section.
	  • MAC + SGMII (SERDES) Mode section.
	  • Clocking for SGMII (LVDS) Only section.
	  • Clocking for SGMII (SERDES) Only section.
	  • Reset Overview section.

IP Parameter Description	• Updated the following sections:
	  • General Attributes section.
	  • SGMII (SERDES) Only Mode Attributes (Nexus Devices) section.
	  • MAC + SGMII (SERDES) Mode Attributes section.
	• Added the SGMII (SERDES) Only Mode Attributes (Avant Devices) section.

Signal Description	Updated the following sections: • AXI4-Stream Transmit Interface section. • AXI4-Stream Receive Interface section. • SGMII (LVDS) Only Interfaces section. • SGMII (SERDES) Only Interfaces section. • MAC + SGMII (LVDS) Interfaces section. • MAC + SGMII (SERDES) Interfaces section.
Register Description	Updated Table 5.1. Register Address Map.
Example Design	Updated the introductory content in this section and the following subsections: • Example Design Supported Configuration section. • RGMII Example Design section. • RMII Example Design section. • SGMII Example Design section. • Simulating the Example Design section. • Using Hardware Example Design section.
Designing with the IP	Updated the following sections: • Timing Constraints Files (.sdc) section. • Post-Synthesis Timing Constraint Files (.pdc)Post-Synthesis Timing Constraint Files (.pdc) section.
Known Issues	Removed the Fail to Handle CTC at RX/TX Rate Adapter Blocks section.
Resource Utilization	Updated the following tables: • Table A.1. IP Resource Utilization for an Avant Device. • Table A.2. IP Resource Utilization for a CertusPro-NX Device.

Revision 2.3, IP v2.0.0, June 2025

Section	Change Summary
All	• Renamed *Tri-Speed Ethernet MAC* to *Tri-Speed Ethernet*. • Updated the IP version on the cover page. • Added the following note on SGMII interface: *Note: The SGMII interface using LVDS I/O in Certus-NX, CertusPro-NX, MachXO5-NX, and CrossLink-NX FPGAs has limitations when operating across the full specified temperature range. Lattice recommends using alternative interfaces, such as SERDES or RGMII, for designs requiring Gigabit Ethernet. Refer to the* Knowledge Base article *for details. Contact your local Lattice sales representative for more information.*
Introduction	• Updated the Overview of the IP section. • Updated the IP Support Summary section. • Updated the following tables:

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Section	Change Summary
	• Table 1.1. Summary of the TSE IP Core. • Table 1.2. TSE IP Core Support Readiness. • Table 1.3. Ordering Part Number. • Updated the Features section. • Updated the Hardware Support section.
Functional Description	• Updated the title for Figure 2.4. TSE IP Connected to External Ethernet PHY with Serial Interface via Embedded SGMII PCS IP. • Updated the Summary of Supported Operation Options section. • Updated the Summary of Implementation section. • Updated the MAC Only Mode section. • Updated the SGMII (LVDS) Only Mode section. • Added the SGMII (SERDES) Only Mode section. • Updated the MAC + SGMII (LVDS) Mode section. • Updated the MAC + SGMII (SERDES) Mode section. • Updated the Clocking section. • Updated the Hardware Requirements (Avant Devices) section.
IP Parameter Description	Updated the following sections: • General Attributes section. • MAC Only Mode Attributes section. • SGMII (LVDS) Only Mode Attributes section. • GMII (SERDES) Only Mode Attributes section. • MAC + SGMII (LVDS) Mode Attributes section. • MAC + SGMII (SERDES) Mode Attributes section.
Signal Description	Updated the following sections: • Clock Interface section. • AXI4-Stream Transmit Interface section. • AXI4-Stream Receive Interface section. • Transmit MAC Control and Status Interface section. • Receive MAC Control and Status Interface section. • PHY Interface section. • Miscellaneous Interface section. • SGMII (LVDS) Only Interfaces section. • SGMII (SERDES) Only Interfaces section. • MAC + SGMII (LVDS) Interfaces section. • MAC + SGMII (SERDES) Interfaces section.
Register Description	• Updated the description for SGMII PHY register in Table 5.1. Register Address Map. • Updated the [0x400 – 0x50C] SGMII and Gb Ethernet PCS Soft IP Register section. • SGMII and Gb Ethernet PCS Soft IP Register section. • Updated Table 5.35. PCS Control Register 0. • Removed the [0x02B] PCS Control Register 11 section.
Example Design	• Updated the list of evaluation boards. • Updated the Example Design Supported Configuration section. • Updated the RGMII Example Design section. • Updated the Hardware Testing with RGMII Example Design section. • Added the RMII Example Design section. • Updated the SGMII Example Design section. • Added the Simulating the Example Design section. • Updated the Using Hardware Example Design section.
Designing with the IP	• Updated the Generating and Instantiating the IP section. • Updated the Timing Constraints sections. • Updated the Running Functional Simulation section.

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Section	Change Summary
Known Issues	• Updated the RX Stat Vector Limitation for Carrier Event Previously Seen (bit[27]) and Packet Ignored (bit[26]) section. • Updated the Erroneous Length/Type Handling when the L/T is Smaller than 46 section. • Added the Fail to Handle CTC at RX/TX Rate Adapter Blocks section.
References	Added a reference link to the *Tri-Speed Ethernet Driver API Reference (FPGA-TN-02341).*
Appendix A. Resource Utilization	• Updated Table A.1. IP Resource Utilization for an Avant Device. • Updated Table A.2. IP Resource Utilization for a CertusPro-NX Device.

Revision 2.2, IP v1.7.1, December 2024

Section	Change Summary
All	Added IP version on the cover page.
Introduction	• Updated Table 1.1. Summary of the TSE MAC IP Core. • Added the IP Support Summary section. • Updated the Features section. • Renamed the section title IP Validation Summary to Hardware Support and updated the content in the Hardware Support section. • Added part numbers for Certus-N2 device family.

Functional Description	• Added Figure 2.6. TSE MAC IP Connected to External Ethernet PHY with Serial Interface via SGMII Only Mode (All Devices).
	• Added the following sections:
	  • Summary of Supported Operation Options section.
	  • Summary of Implementation section.
	• Added Table 2.3. Speed Selection Configuration of the Simplified Clock Scheme Design.
	• Updated the Transmit SGMII Core section.
	• Updated the Receive SGMII Core section.
	• Added the SGMII Only Mode section.
	• Updated the MAC + SGMII Mode (Avant Devices Only) section.
	• Updated the section title MAC + MPS Mode to MAC + MPCS (CertusPro-NX Devices Only).
	• Updated the Clocking section.
	• Added the Clocking for SGMII Only Mode section.
	• Added the Hardware Requirements (Avant Devices) section.

IP Parameter Description	• Updated Table 3.1. General Attributes.
	• Added the following sections:
	  • MAC Only Mode Attributes.
	  • SGMII Only Mode Attributes.
	  • MAC + SGMII Mode Attributes.
	  • MAC + MPCS Mode Attributes.
	• Removed the following sections:
	  • Configuration Attributes.
	  • SGMII PHY Settings.

Signal Description	• Updated the following tables:
	  • Table 4.1. Common Clock Ports.
	  • Table 4.6. AXI4-Stream Transmit Interface Ports.
	  • Table 4.7. AXI4-Stream Receive Interface Ports.
	  • Table 4.8. Transmit MAC Control and Status Interface Ports.
	  • Table 4.9. Receive MAC Control and Status Interface Ports.
	  • Table 4.10. MII/GMII Interface Ports.
	  • Table 4.11. Gigabit MAC Interface Ports.
	  • Table 4.12. SGMII Easy Connect Interface Ports.
	  • Table 4.13. RGMII Interface Ports.

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Section	Change Summary
	• Table 4.14. RMII Interface Ports. • Table 4.20. Miscellaneous Interface Ports. • Table 4.21. SGMII Only Clock and Reset Interface Ports. • Added the following tables: • Table 4.2. Non Simplified Clock Scheme Design Clock Ports. • Table 4.3. Clock Frequencies of txmac_clk_i and rxmac_clk_i. • Table 4.4. Simplified Clock Scheme Design Clock Ports. • Added the SGMII Only Interfaces section. • Removed the following reference from the MAC + SGMII Interfaces section: For more information, refer to the Lattice SGMII and Gb Ethernet PCS IP Core User Guide (FPGA-IPUG-02077). • Added the following reference to the MAC + MPCS Interfaces section: For more information on this register, refer to the NX MPCS Module User Guide (FPGA IPUG-02118).
Register Description	• *Updated the introductory paragraph in this section.* • *Updated Table 5.3. Mode Register.* • *Updated the description for the tx_dis_fcs register in Table 5.4. Transmit and Receive Control Register.* • *Updated the following reference in the [0x400 – 0x50C] SGMII and Gb Ethernet PCS Soft IP Register section:* *For more information on the PCS registers, refer to the SGMII and Gb Ethernet PCS IP Core User Guide (FPGA-IPUG-02077) or refer to section 5.20 for the SGMII-only PHY registers.*
Example Design	• Added a list of evaluation boards that are used to test the IP. • Added the Example Design Supported Configuration section. • Added the RGMII Example Design section. • Added the SGMII Example Design section. • Added the Using the RGMII or SGMII Example Design section.
Designing with the IP	• Updated the Timing Constraints section. • Added the SGMII Only Configuration section.
Known Issues	• Added the following sections: • Erroneous Length/Type Handling when the L/T is Smaller than 46. • Error Handling when rx_fifo_error_o is Asserted.
References	Added the following references: • Tri-Speed Ethernet MAC IP Release Notes (FPGA-RN-02036) • Avant-G/X Versa Board User Guide (FPGA-EB-02063) • TSE MAC IP Core web page • Lattice Radiant Software web page • Lattice Solutions IP Cores web page • Lattice Solutions Reference Designs web page • Lattice Solutions Boards web page • Lattice Solutions Demonstrations web page
Appendix A. Resource Utilization	• Updated the following tables: • Table A.1. IP Resource Utilization for an Avant Device. • Table A.2. IP Resource Utilization for a CertusPro-NX Device.

Revision 2.1, September 2024

Section	Change Summary
Introduction	• Added *LFD2NX-28* device to Table 1.1. Summary of the TSE MAC IP Core. • Updated the following bullet point in the Signal Names section: *_n are active low signals (asserted when value is logic 0)*
Functional Description	• Updated Table 2.2. Summary of Implementation Options.

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Section	Change Summary
	• Updated Table 2.2 Operation Options. • Added the following description to the Implementation Options section and the RGMII Configuration Option section: *For RGMII interface implementation, follow the instructions in the RGMII Hardware Example Design section and use the MII/GMII MAC operating option.* • Updated the description for Gigabit MAC operation in Table 2.2. Operation Options.
IP Parameter Description	Updated Table 3.2. Configuration Attributes.

Signal Description	• Added the following description to the RGMII Interface section:
	For RGMII interface implementation, follow the instructions in the RGMII Hardware Example Design section and use the MII/GMII MAC operating option. For more information on MII/GMII interface ports, refer to the MII/GMII Interface section.
	• Updated the PLL reference clock input value to 250 MHz in Table 4.19. MAC + SGMII Clock Interface Ports.
	• Updated the table title of the following tables:
	  • Table 4.19. MAC + SGMII Clock Interface Ports
	  • Table 4.20. MAC + SGMII Serial Interface Ports
	  • Table 4.21. MAC + SGMII Configuration Interface Ports
	  • Table 4.22. MAC + SGMII Miscellaneous Interface Ports
	  • Table 4.23. MAC + MPCS Clock Interface Ports
	  • Table 4.24. MAC + MPCS Serial Interface Ports
	  • Table 4.25. MAC + MPCS Configuration Interface Ports
	  • Table 4.26. MAC + MPCS Miscellaneous Interface Ports
	  • Table 4.27. MAC + MPCS LMMI Interface Ports

RGMII Hardware Example Design	• Added the following sentence to the Importing Versa Files into a Project section: *For 1G RGMII speed, use CLK_ALGN = "1" or "2".* • Updated Figure 7.22. RGMII_eval_top Block Diagram.

Revision 2.0, July 2024

Section	Change Summary
Abbreviations in This Document	Added the following abbreviations: • CRC • FCS • HIP • MAC • MDIO • MPCS • PCS • PHY • PLL • SERDES • SFD
Introduction	• Updated the IP version in Table 1.1. Summary of the TSE MAC IP Core. • Updated the Selectable MAC operating options in the Features section. • Updated the IP version for all device families in Table 1.3. IP Validation Level.
Functional Description	• Updated the following sentence in the IP Architecture Overview section: *For Avant devices, the TSE MAC IP core also provides an option to include the SGMII/Gb Ethernet PCS IP core that converts MII/GMII interfaces of the MAC to serial interfaces in both transmit and receive directions and performs auto-negotiation with a link partner as described in the Cisco SGMII and IEEE 802.3 specifications.* • Updated the title to include RMII for the Interface to External PHY with MII/GMII/RGMII/RMII Interface section and Figure 2.3. TSE MAC IP Connected to External PHY with MII/GMII/RGMII/RMII.

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Section	Change Summary

	• Updated Table 2.1. Summary of Implementation Options.
	• Updated Table 2.2. Operation Options.
	• Removed the Classic TSMAC Option section.
	• Added the RMII Configuration Option section.
	• Updated the subsections title for Multi-Rate SGMII Ethernet Option section and the Gigabit SGMII Ethernet Option section.
	• Updated the figure title for Figure 2.10. Top-Level Block Diagram for Multi-Rate SGMII Ethernet Option.
	• Updated the content and figures in the MAC + SGMII Mode section.
	• Added the MAC + MPCS Mode section.
	• Added the Clocking of RMII section.
	• Updated the title for the following sections:
	  • Clocking of TSE MAC (Gigabit MAC) and SGMII PCS (TSMAC Easy Connect) section.
	  • Clocking of TSE MAC (SGMII Easy Connect) and SGMII PCS (TSMAC Easy Connect) section.
	• Added the Clocking of TSE MAC (Gigabit MAC) and MPCS section.
	• Updated the following sentence in the Reset section:
	During power-up, the active-low reset must be asserted, and only de-asserted when all input clocks are valid and stable.
	• Updated Table 2.3. User Interfaces and Supported Protocols.
	• Updated the content for the AXI4-Lite Interface section.

IP Parameter Description	• Updated the following sections:
	  • General Attributes section.
	  • Configuration Attributes section.
	  • SGMII PHY Settings section.
	• Added the Statistics Counter Configuration section.

Signal Description	• Updated the following tables to include RMII port and clock frequency option:
	  • Table 4.1. Clock Ports.
	  • Table 4.2. Clock Frequencies of txmac_clk_i and rxmac_clk_i.
	• Updated the following sentence for clk_i port in Table 4.1. Clock Ports:
	• The supported clock frequency is between 20 MHz to 125 MHz.
	• Removed the Classic TSMAC Interface section.
	• Updated the description for the cpu_if_gbit_en_o port in Table 4.19. MAC + SGMII Clock Interface Ports.
	• Removed gbe_mode_i and sgmii_mode_i ports from Table 4.21. MAC + SGMII Configuration Interface Ports.
	• Updated the MAC + SGMII Interfaces section.
	• Added the following sections:
	  • RMII Interface section.
	  • MAC + MPCS Interfaces section.

Register Description	• Updated the Pause Opcode Access value to RO in Table 5.1. Register Address Map. • Added a new register—MPCS PHY in Table 5.1. Register Address Map. • Added a new mode register—rmii_100m_en in Table 5.3. Mode Register. • Updated the description for Gigabit Enable register in Table 5.3. Mode Register. • Updated the description for max_frame register in Table 5.5. Maximum Packet Size Register. • Updated the Pause Opcode Access value to RO in Table 5.15. Pause Opcode Register. • Updated Table 5.22. Summary of Statistics Counters.

Designing with the IP	• Updated the following figures in the Generating and Instantiating the IP section:
	  • Figure 6.1. Module/IP Block Wizard.
	  • Figure 6.2. IP Configuration.
	  • Figure 6.3. Check Generated Result.

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Section	Change Summary
	• Figure 6.4 Timing Constraint File (.ldc) for the TSE MAC IP. • Added the MAC + SGMII Post-Synthesis Timing Constraints section. • Updated the content and figures in the following sections: • MAC Only Configuration. • MAC + PHY Configuration.
RGMII Hardware Example Design	Added this new section.
Known Issues	Added this new section.
References	Added a reference to the Avant Evaluation Board User Guide (FPGA-EB-02057).
Appendix A. Resource Utilization	• Updated Table A.1. IP Resource Utilization for an Avant Device. • Added Table A.2. IP Resource Utilization for a CertusPro-NX Device.

Revision 1.9, March 2024

Section	Change Summary
Introduction	• Removed *Lattice Synthesis Engine (LSE*) from the Quick Facts section. • Removed *Lattice Synthesis Engine* from the IP Validation Summary section.
Register Description	Updated the register description for 5.5 [0x010 – 0x014] MAC Address Register (0,1) section to: *The MAC address is stored in the registers in hexadecimal form. For example, to set the MAC address to: AC-DE-48-00-00-80 would require writing 0xAC_DE_48_00 to address 0x010 (MAC_ADDR_0), 0x00_80 to address 0x014 (MAC_ADDR_1).*

Revision 1.8, December 2023

Section	Change Summary
Introduction	• Added MII/GMII MAC operating option. • Added Avant-G/X device support to Table 1.3. Ordering Part Number with new ordering part number. • Added Table 1.3. IP Validation Level.
Functional Description	• Added chapter 2.1.1 Implementation Options. • Added chapter 2.6.1.4 MII/GMII Configuration Option. • Added clocking diagrams in chapter 2.2 Clocking.
Signal Description	• Added clock frequencies requirements. • Added clock domain for input and output signals. • Grouped all PHY interfaces in chapter 4.7 PHY Interface. • Grouped all host interfaces in chapter 4.8 Host Interface. • Grouped MAC + PHY interface signals in multiple tables in chapter 0 • MAC + SGMII Interfaces.
Register Description	• Added address offset to chapter titles for ease of reference. • Added address offset mapping of SGMII & Gb Ethernet PCS register in chapter 5.19 [0x400 – 0x50C] SGMII and Gb Ethernet PCS Soft IP Register.
Designing with the IP	Added description of simulation waveform and output in chapter 6.5.3 Simulation Results.
All	Updated the document to new IP user guide format.

Revision 1.7, June 2023

Section	Change Summary
Acronyms in This Document	Added Acronym *AXI* in Acronyms in This Document section.
Introduction	• Added LFMXO5-55T and LFMXO5-100T to Targeted Devices in Table 1.1. TSE MAC IP Quick Facts. • Updated the sentence from "*The TSE MAC IP core supports the ability to transmit and receive data between the standard interfaces, such as APB or AHB-Lite, and an Ethernet network.*" to "*The TSE MAC IP core supports the ability to transmit and receive data*

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Section	Change Summary
	between the standard interfaces, such as APB, AHB-Lite or AXI4-Lite, and an Ethernet network." In the Introduction section. • Updated bullet information from *Transmit and receive statistics vector and statistic counter* to *Transmit and receive statistics vector and statistic counter* in the Features section.
Functional Description	• Deleted Transmit MAC (TX MAC) section. • Deleted the sentence *In the 10/100 mode, an external PHY device supplies the 25 MHz clock to the Transmit MAC and the Receive MAC* from Overview section. • Added Statistics Counters, TX FIFO Almost Full Threshold Register, TX FIFO Almost Empty Threshold Register, RX FIFO Almost Full Threshold Register, RX FIFO Almost Empty Threshold Register, Transmit MAC, Clock Network sections. • Updated MAC Address Register (0,1) section. • Updated AXI4-Lite Interface section and Figure 2.10. State Diagram. • Added Statistic Counter Registers attribute information in Table 2.2. Attributes Table. • Added Statistic Counter Registers attribute, RX FIFO and TX FIFO threshold information in Table 2.4. Register Address Map. • Updated the description of gbit_en to "*Gigabit Enable.* *For the Classic Tri-speed MAC option, to operate in GbE mode, this bit must be set to 1. For 10/100 mode, this bit must be set 0.* *For the SGMII Easy Connect MAC, Gigabit MAC, RGMII option, this bit does not control anything (note the MAC operation speed is determined by the clock enables provided by the SGMII IP core). This bit echoes back what is written to it.* *Note: The state of this bit is useful for system use, since the cpu_if_gbit_en_o output signal, from the core, always reflects the state of this register bit"* in Table 2.6. Mode Register. • Updated Bit Field value from 15:9 to 31:9 in Table 2.7. Transmit and Receive Control Register. • Updated Width value for 31:15 Bit Field from *12* to *27* in Table 2.9. Inter-Packet Gap Register. • Updated Default values in Table 2.14. GMII Management Register Access Control Register and Table 2.15. GMII Management Access Data Register. • Updated the description of 28-Bit from *Not Used. This bit always returns a zero* to *PTP 1588 frame. This bit is set when the TSE MAC IP receives a PTP 1588 frame* in Table 2.27. Receive Statistics Vector Description. • Added 31 bit description in Table 2.28. Transmit Statistics Vector Description. • Added *Multicast* to the title of Multicast Table Registers (0,1) section. • Deleted *(RX MAC)* from the title of Receive MAC section. • Updated Figure 2.5. Top-Level Block Diagram for the Classic TSMAC IP Option, Figure 2.6. Top-Level Block Diagram for the One Gigabit and SGMII Options, and Figure 2.7. Top-Level Block Diagram for the RGMII Configuration Option.
IP Generation and Evaluation	Updated Figure 3.2. Configure User Interface of TSE MAC IP Core as per IP tse_mac version 1.4.0.
Appendix A. Resource Utilization	Updated the values in Table A.1. LAV-AT-500E-1LFG1156I Resource Utilization and Table A.2. LAV-AT-500E-3LFG1156I Resource Utilization.
Technical Support Assistance	Added Lattice Answer Database link in Technical Support Assistance section.
References	Added links for MachXO5, Lattice Avant, and TSE MAC IP Core web pages.

Revision 1.6, December 2022

Section	Change Summary

Introduction	• Updated the following in Table 1.1. TSE MAC IP Quick Facts:
	  • Added Lattice Avant to the Supported FPGA Family and LAV-AT-500E to the Targeted Devices.
	  • Updated information for Supported User Interfaces.

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Section	Change Summary
	• Added bullet for MAC support and updated Host control bullet information in the Features section.
Functional Description	• Updated Lattice Gigabit Ethernet PCS IP Core to Functional Description section name. • Changed LMMI to AXI4-Stream references in this section. • Added Block Diagram section. • Updated content of Configuration Options section. • Updated content of Receive MAC (Rx MAC) section. • Updated content of Statistics Vector section. • Updated content of Table 2.2. Attributes Table to Table 2.28. RX FIFO Almost Empty Threshold Register. • Updated Figure 2.5. Top-Level Block Diagram for the Classic TSMAC IP Option, Figure 2.6. Top-Level Block Diagram for the One Gigabit and SGMII Options, and Figure 2.7. Top-Level Block Diagram for the RGMII Configuration Option . • Added MAC + PHY Mode, Media Independent Interface Management, and Host Interface section.
IP Core Generation and Evaluation	Updated entire content including adding MAC Only Configuration, MAC + PHY Configuration, Constraining the IP, and Hardware Validation.
Ordering Part Number	Added OPN for Avant device.
Appendix A. Resource Utilization	Updated Table A.1. LAV-AT-500E-1LFG1156I Resource Utilization and Table A.2. LAV-AT-500E-3LFG1156I Resource Utilization.

Revision 1.5, May 2022

Section	Change Summary
Introduction	Added MachXO5-NX to the Supported FPGA Family, and LFMXO5-25 to the Supported User Interfaces in Table 1.1
IP Core Generation and Evaluation	Updated Figure 3.1, Figure 3.2, and Figure 3.3 to show the latest version 1.2.0.
Ordering Part Number	Added Part Numbers of Tri-speed Ethernet MAC for MachXO5-NX - Site License.
Appendix A. Resource Utilization	• Updated Table A.1 for resource utilization of the Tri-Speed Ethernet MAC IP Core for the LFMXO5-25-9BBG400I. • Added Table A.2 for resource utilization of the Tri-Speed Ethernet MAC IP Core for the LFMXO5-25-7BBG400I.

Revision 1.4, June 2021

Section	Change Summary
Introduction	Updated Table 1.1. TSE MAC IP Quick Facts. • Revised Supported FPGA Families • Revised Targeted Devices • Revised Lattice Implementation
Functional Description	In the Hardware Evaluation section, replaced specific device with *Lattice FPGA devices built on the Lattice Nexus platform*.
Ordering Part Number	Added this section.
References	Added reference to the CertusPro-NX web page.

Revision 1.3, December 2020

Section	Change Summary

Introduction	• Updated Table 1.1.
	  • Added LFD2NX-17 as targeted device.
	  • Updated Resources.
	  • Updated Lattice Implementation to Lattice Radiant 2.1.

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Section	Change Summary
	• Updated reference to Lattice Radiant Software User Guide. • Added RGMII under Features.
Functional Description	• Added RGMII Configuration Option section. • Added RGMII Signals in Table 2.2. TSE MAC IP Core Signal Description. • Added RGMII as selectable value for Select MAC Operating Option in Table 2.3. Attributes Table
Appendix A. Resource Utilization	General update to this section.
References	Updated this section. Added references to product web pages.

Revision 1.2, June 2020

Section	Change Summary
Introduction	Updated Table 1.1: • Added Certus-NX support. • Added LFD2NX-40 as targeted device. • Updated Supported User Interfaces. • Updated Synopsis Synplify Pro version. • Updated Lattice Implementation to Lattice Radiant 2.1.
Functional Description	• Removed the block diagram of the TSE MAC IP Core. • Added Figure 2 1. Un-Tagged Ethernet Frame Format and Figure 2 2. VLAN-Tagged Ethernet Frame Format. • Updated Receive MAC (Rx MAC) information. • Updated Table 2.2. TSE MAC IP Core Signal Description
Ordering Part Number	Added this section.
Appendix A. Resource Utilization	• Updated device to LIFCL-40-9BG400I. • Updated Table A.1. Resource Utilization.
All	Updated references to Lattice Radiant Software 2.1 User Guide.

Revision 1.1, February 2020

Section	Change Summary
Introduction	Updated Table 1.1 to add LIFCL-17 as targeted device.

Revision 1.0, November 2019

Section	Change Summary
All	Initial release.

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